具有内部参考和内部温度传感器的 12 位、1 每秒百万次采样 (MSPS)、8 通道、逐次逼近寄存器 (SAR) 数模转换器 (ADC)

查询样品: ADS8028

特性

- 出色性能：
  - 吞吐量：高达 1MSPS
  - 无丢码：12 位
  - 积分非线性 (INL)：±0.5 LSB
  - 信噪比 (SNR)：72dB
- 高度集成的：
  - 八个模拟输入
  - 高分辨率内部温度传感器
  - 带有通道排序器的九通道复用器
  - 低漂移内部电压基准
- 宽电源范围：
  - 模拟电源 (AVDD)：2.7V 至 5.25V
  - 数字电源 (DVDD)：1.65V 至 5.25V
- 低功率:
  - 1MSPS 时为 17mW
  - 灵活的断电模式
- 串行外设接口 (SPI)™- 兼容串口：20MHz
- 小型封装：4mm x 4mm 薄型四方扁平无引线 (QFN)-20

应用范围

- 可编程逻辑控制 (PLC)
- 工业过程控制 (IPC)
- 电信
- 电源监控
- 印刷电路板 (PCB) 热点分析
- 电池供电型应用

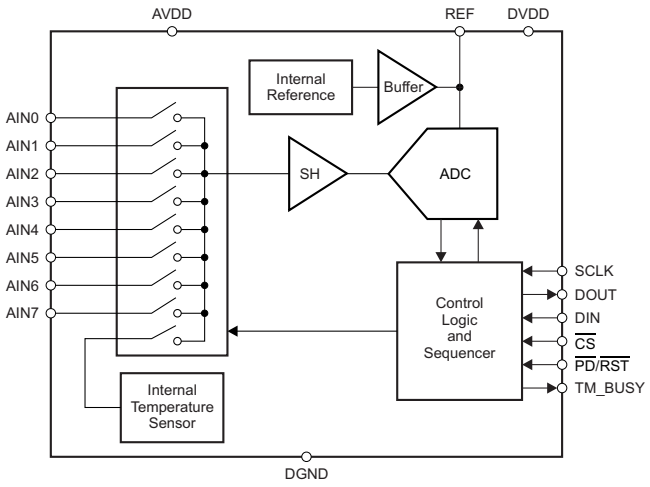
说明

ADS8028 是一款 12 位模数转换器 (ADC)，此转换器采样速度高达 1MSPS。 此器件基于逐次逼近 (SAR) 内核并且提供一个固有的采样保持 (SH) 前端。

除了具有八个模拟输入通道之外，ADS8028 还提供一个分辨率为 0.25°C 且带有一个内部电压基准的内部温度传感器。 一个九通道复用器可选择多重通道（包括内部温度传感器），采用顺序方式对这些通道进行非限定扫描。 一个简单的 SPI 兼容串行接口提供了器件和主控制器之间的简易通信和控制。 数字电源可在 1.65V 至 5.25V 之间运行，从而实现了到宽范围处理器和控制器的接口连接。

在 1MSPS 全速时，ADS8028 功率耗散只有 17mW。此器件提供灵活的断电模式以在不执行转换时节省电能。 ADS8028 性能的额定扩展工业温度范围为 –40°C 至 +125°C。

ADS8028 非常适合于要求严格的测量应用，例如传感器输出监控、电源监控、和印刷电路板 (PCB) 热点分析。此器件采用小外形尺寸 QFN-20 封装。



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING	TRANSPORT MEDIA
ADS8028	QFN-20	RTJ	ADS8028IRTJ	Tape and Reel
				Tape and Reel

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE	UNIT
AVDD to DGND, AGND		–0.3 to +7	V
DVDD to DGND, AGND		–0.3 to AVDD + 0.3	V
DGND to AGND		–0.3 to +0.3	V
Analog input (AIN0 to AIN7) to AGND		–0.3 to AVDD + 0.3	V
Digital input ($\overline{CS}$, DIN, SCLK, $\overline{PD}$/$\overline{RST}$) to DGND		–0.3 to DVDD + 0.3	V
Digital output (DOUT, TM_BUSY) to DGND		–0.3 to DVDD + 0.3	V
REF to AGND		AVDD + 0.3	V
Input current to any pin (except supply), continuous		±10	mA
Operating temperature range		–40 to +125	°C
Storage temperature range		–65 to +150	°C
Maximum junction temperature		+150	°C
Electrostatic discharge (ESD) ratings:	Human body model (HBM)	±2000	V
	Charge device model (CDM)	±500	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = +25°C. All specifications at AVDD = 2.7 V to 5.25 V, DVDD = 1.65 V to 5.25 V, f_{SAMPLE} = 1 MHz, f_{SCLK} = 20 MHz, and V_{REF} = 2.5 V internal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8028			UNIT
			MIN	TYP	MAX	
ANALOG INPUTS						
AINx	Analog input voltage		0		V_{REF}	V
	Input capacitance	In sample mode		40		pF
		In hold mode		8		pF
	Input bias current			±0.01		µA
SAMPLING DYNAMICS						
	Conversion time	SCLK = 20 MHz		660	700	ns
		T_{SENSE} temperature sensor channel			100	µs
	Acquisition time	Full-scale step input	100			ns
	Throughput rate	SCLK = 20 MHz, AINx channel			1	MSPS
		SCLK = 20 MHz, temperature measurement channel			10	kSPS
	Aperture delay				14	ns
	Full-power bandwidth	At 3 dB		30		MHz
		At 0.1 dB		10		MHz
	Step response			100		ns
	Overload recovery			100		ns
DC ACCURACY						
	Resolution		12			Bits
	No missing codes		12			Bits
INL	Integral nonlinearity			±0.5	±1	LSB
DNL	Differential nonlinearity			±0.5	±0.99	LSB
	Offset error			±2	±4.5	LSB
	Offset error matching			±2.5	±4.5	LSB
	Offset temperature drift			4		ppm/°C
	Gain error			±1	±4	LSB
	Gain error matching			±1	±2.5	LSB
	Gain temperature drift			0.5		ppm/°C
DYNAMIC PERFORMANCE						
SNR	Signal-to-noise ratio	50-kHz input, –0.5 dBFS	70	72		dB
SINAD	Signal-to-noise and distortion ratio	50-kHz input, –0.5 dBFS	70	71		dB
THD	Total harmonic distortion	50-kHz input, –0.5 dBFS		–82	–77	dB
SFDR	Spurious-free dynamic range	50-kHz input, –0.5 dBFS	77.5	84		dB
IMD	Intermodulation distortion	f_A = 40.1 kHz, f_B = 41.5 kHz				
		Second-order terms		–84		dB
		Third-order terms		–93		dB
	Channel-to-channel isolation	f_{IN} = 50 kHz, f_{NOISE} = 60 kHz		–100		dB
INTERNAL REFERENCE OUTPUT						
	Reference output voltage	±0.3% maximum at +25°C	2.4925	2.5	2.5075	V
	Long-term stability			150		ppm
	Output voltage hysteresis			50		ppm
	Internal reference output impedance			1		Ω
	Internal reference temperature coefficient			12	35(1)	ppm/°C
	Internal reference noise	10-MHz bandwidth		60		$µV_{RMS}$

(1) Sample tested during initial release to ensure compliance.

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = +25°C. All specifications at AVDD = 2.7 V to 5.25 V, DVDD = 1.65 V to 5.25 V, f_{SAMPLE} = 1 MHz, f_{SCLK} = 20 MHz, and V_{REF} = 2.5 V internal, unless otherwise noted.

PARAMETER			TEST CONDITIONS	ADS8028 MIN	ADS8028 TYP	ADS8028 MAX	UNIT
EXTERNAL REFERENCE INPUT							
	External reference input voltage range			1		AVDD	V
	DC leakage current				±0.01	±1	µA
TEMPERATURE SENSOR							
	Operating range			–40		+125	°C
	Accuracy		T_A = –40°C to +125°C		±1	±3	°C
	Resolution		LSB size		0.25		°C
DIGITAL INPUT AND OUTPUT							
V_{IH}	Logic level			0.7 DVDD			V
V_{IL}						0.3 DVDD	V
V_{OH}			SDO load = 20 pF, I_{SOURCE} = 500 µA	0.8 DVDD			V
V_{OL}			SDO load = 20 pF, I_{SINK} = 500 µA			0.2 DVDD	V
	Input capacitance				5		pF
I_{IN}	Input current		0 V < $V_{DigitalInput}$ < DVDD		±0.01	±1	µA
POWER-SUPPLY REQUIREMENTS							
AVDD	Analog supply		Internal reference mode	2.7	3.0	5.25	V
			External reference mode with V_{EXT_REF} ≤ 2.7 V	2.7	3.0	5.25	
			External reference mode with V_{EXT_REF} > 2.7 V	V_{EXT_REF}		5.25	
DVDD	Digital supply			1.65	3.0	5.25	V
SUPPLY CURRENT							
I_{TOTAL}	Total current(2)						
	Normal mode	Operational	AVDD = 3.6 V, DVDD = 3.6 V		5.8	6.3	mA
			AVDD = 5.25 V, DVDD = 5.25 V		7	7.5	mA
		Static	AVDD = 3.6 V, DVDD = 3.6 V		4.1	4.6	mA
			AVDD = 5.25 V, DVDD = 5.25 V		4.5	5	mA
	STANDBY mode		AVDD = 3.6 V, DVDD = 3.6 V		1.5	2.5	mA
	Power-down mode		AVDD = 3.6 V, DVDD = 3.6 V		1	10	µA

(2) I_{TOTAL} is the total current flowing in AVDD and DVDD.

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = +25°C. All specifications at AVDD = 2.7 V to 5.25 V, DVDD = 1.65 V to 5.25 V, f_{SAMPLE} = 1 MHz, f_{SCLK} = 20 MHz, and V_{REF} = 2.5 V internal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8028			UNIT
			MIN	TYP	MAX	
POWER CONSUMPTION						
Power consumption						
Normal mode	Operational	AVDD = DVDD = 3.0 V		17	18.9	mW
		AVDD = DVDD = 3.6 V		20.9	22.7	mW
		AVDD = DVDD = 5.25 V		36.8	39.4	mW
	Static	AVDD = DVDD = 3.6 V		14.8	16.6	mW
		AVDD = DVDD = 5.25 V		23.6	26.2	mW
STANDBY mode		AVDD = DVDD = 3.6 V		5.4	9	mW
Power-down mode		AVDD = DVDD = 3.6 V		3.6	36	µW
TEMPERATURE						
Operating temperature range			–40		+125	°C

THERMAL INFORMATION

THERMAL METRIC(1)		ADS8028 RTJ (QFN) 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	32.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	27.8	
θ_{JB}	Junction-to-board thermal resistance	9.3	
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	9.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	1.9	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 SPRA953。

PARAMETER MEASUREMENT INFORMATION

TIMING CHARACTERISTICS

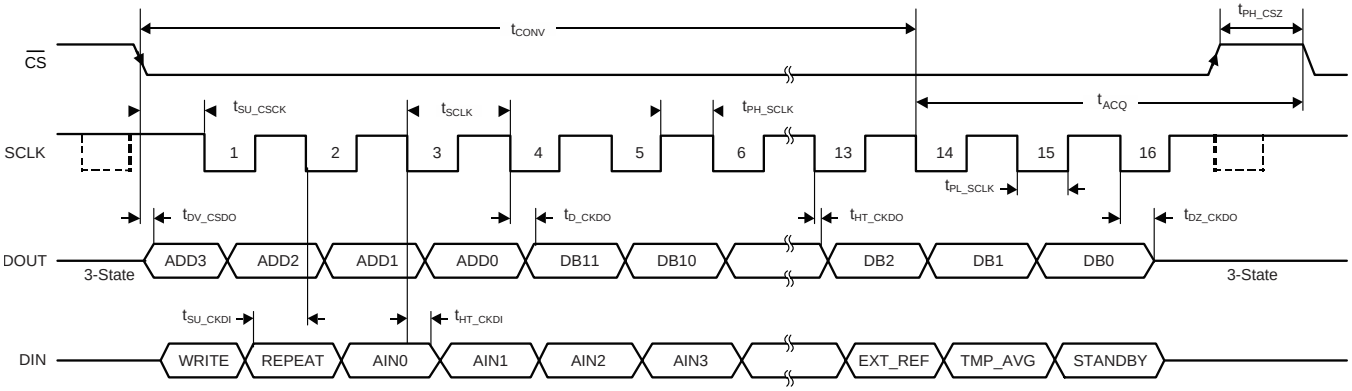


Figure 1. Serial Interface Timing Diagram

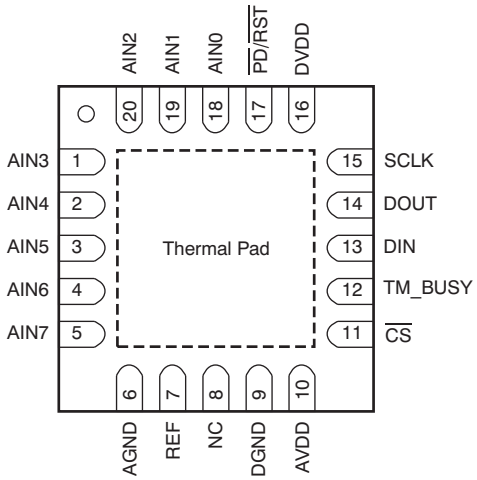
Timing Requirements for Figure 1(1)

PARAMETER	DESCRIPTION	TEST CONDITIONS	ADS8028			UNIT
			MIN	TYP	MAX	
f_{SCLK}	External serial clock frequency				20	MHz
t_{SCLK}	External interface clock time period		50			ns
t_{PH_SCLK}	SCLK high pulse width		0.4 t_{SCLK}		0.6 t_{SCLK}	ns
t_{PL_SCLK}	SCLK low pulse width		0.4 t_{SCLK}		0.6 t_{SCLK}	ns
t_{CONV}	Conversion time:				t_{SU_CSCK} + 13 t_{SCLK}	ns
	For channels AIN0 to AIN7	f_{SCLK} = 20 MHz			700	ns
	For internal temperature sensor measurement				100	µs
t_{PH_CSZ}	$\overline{CS}$ high pulse width		6			ns
t_{ACQ}	Acquisition time (for channel AINx)	f_{SCLK} = 20 MHz	100			ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ to SCLK falling edge		10			ns
t_{DV_CSDO}	Delay time between $\overline{CS}$ falling edge to DOUT enabled				17	ns
t_{D_CKDO}	Delay time between SCLK falling edge to (new) data available on DOUT	DVDD = 1.65 V to 3 V			32	ns
		DVDD = 3 V to 3.6 V			29	ns
		DVDD = 3.6 V to 5.25 V			28	ns
t_{HT_CKDO}	Hold time: SCLK falling edge to (previous) data valid on DOUT		10			ns
t_{DZ_CKDO}	Delay time between 16th SCLK falling edge to DOUT going to high-impedance		12		27	ns
t_{DZ_CSDO}	Delay time between $\overline{CS}$ going high to DOUT going to high-impedance				26	ns
t_{SU_CKDI}	DIN setup time before SCLK falling edge		5			ns
t_{HT_CKDI}	DIN hold time after SCLK falling edge		4			ns
t_{ACQ_TMP}	TM_BUSY falling edge to $\overline{CS}$ falling edge		100			ns
$t_{PU\_STANDBY}$	Power-up time after coming out of STANDBY mode				1	µs
t_{POWER_UP}	Power-up time after coming out of power-down mode	Internal reference mode, 10-µF capacitor on REF pin			6	ms

(1) Specifications apply from T_A = –40°C to +125°C, AVDD = 2.7 V to 3.6 V, DVDD = 1.65 V to 5.25 V, V_{REF} = 2.5 V internal, load on DOUT = 15 pF || 100 kΩ, and t_R = t_F = 5 ns (10% to 90% of DVDD) and timed from a voltage level of 0.5 DVDD, unless otherwise noted.

PIN CONFIGURATIONS

RTJ PACKAGE(1)
QFN-20
(TOP VIEW)



(1) The exposed thermal pad on the bottom of the package must be soldered to the printed circuit board (PCB) ground for proper functionality and heat dissipation.

NOTE: NC = no connection.

PIN ASSIGNMENTS

NAME	PIN	FUNCTION	DESCRIPTION
AGND	6	Supply	Analog ground
AIN0	18	Analog input	Analog input channel 0
AIN1	19	Analog input	Analog input channel 1
AIN2	20	Analog input	Analog input channel 2
AIN3	1	Analog input	Analog input channel 3
AIN4	2	Analog input	Analog input channel 4
AIN5	3	Analog input	Analog input channel 5
AIN6	4	Analog input	Analog input channel 6
AIN7	5	Analog input	Analog input channel 7
AVDD	10	Supply	ADC operation supply voltage
$\overline{CS}$	11	Digital input	Chip select; active low logic input
DGND	9	Supply	Digital ground
DIN	13	Digital input	SPI data input
DOUT	14	Digital output	SPI data output
DVDD	16	Supply	ADC interface supply voltage
NC	8	—	This pin has no internal connection. Any passive component connected to this pin does not affect device functionality.
$\overline{PD}/\overline{RST}$	17	Digital input	Dual function pin for power-down and reset operation; active low logic input
REF	7	Analog input/output	ADC internal reference output or ADC external reference input
SCLK	15	Digital input	SPI clock
Thermal pad	—	Thermal pad	Exposed thermal pad; this pin should be soldered to the PCB ground for proper functionality and heat dissipation
TM_BUSY	12	Digital input	Busy output; this pin transitions high and remains high during conversion for temperature sensor input

TYPICAL CHARACTERISTICS

All plots at T_A = +25°C, AVDD = 3.0 V, DVDD = 3.0 V,
f_{SAMPLE} = 1 MHz, f_{SCLK} = 20 MHz, and V_{REF} = 2.5 V internal, unless otherwise noted.

TYPICAL FFT

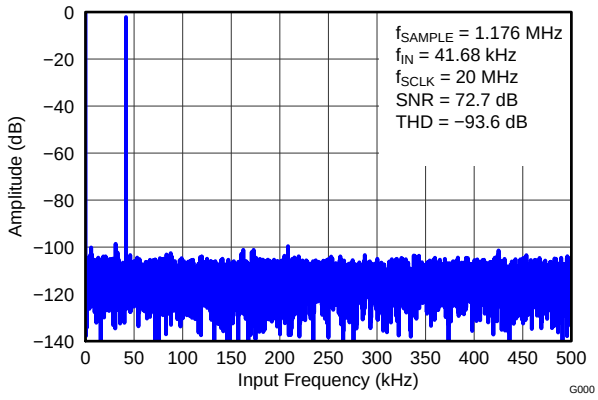


Figure 2.

INL vs V_{REF}

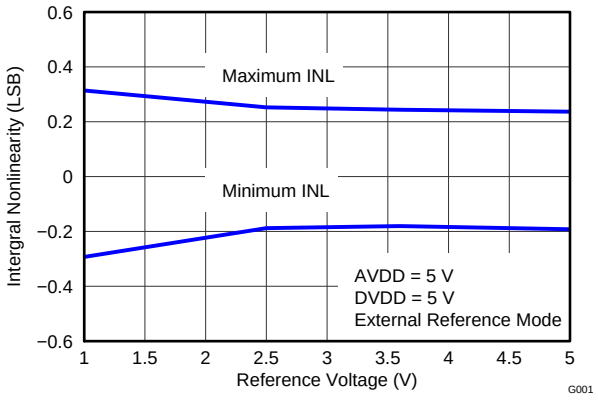


Figure 3.

TYPICAL ADC INL

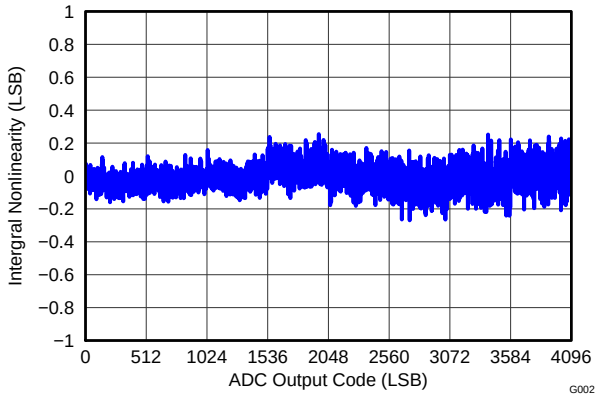


Figure 4.

DNL vs V_{REF}

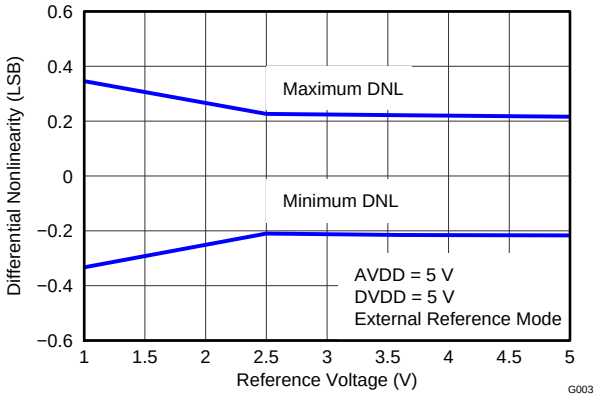


Figure 5.

TYPICAL ADC DNL

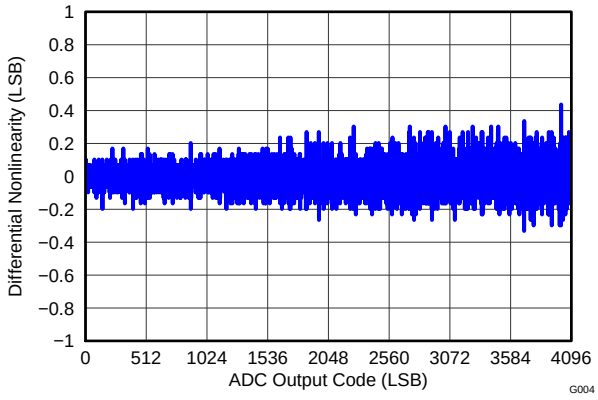


Figure 6.

ENOB vs V_{REF}

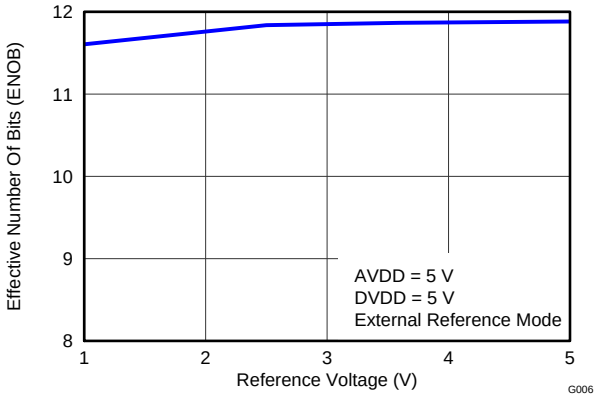


Figure 7.

TYPICAL CHARACTERISTICS (continued)

All plots at T_A = +25°C, AVDD = 3.0 V, DVDD = 3.0 V,

f_{SAMPLE} = 1 MHz, f_{SCLK} = 20 MHz, and V_{REF} = 2.5 V internal, unless otherwise noted.

V_{REF} vs CURRENT LOAD

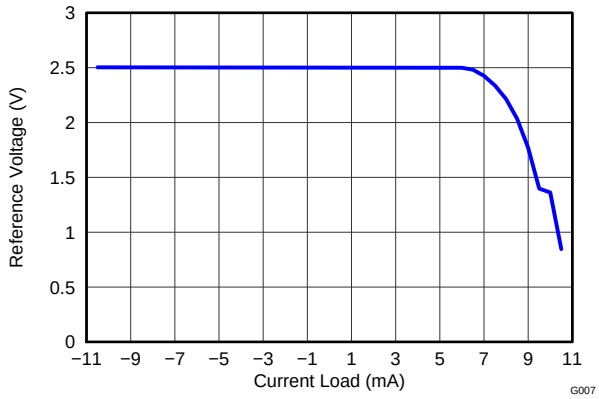


Figure 8.

SINAD vs V_{REF}

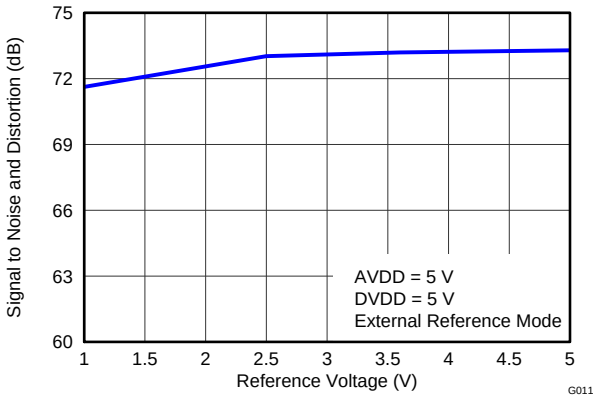


Figure 9.

SINAD vs INPUT FREQUENCY FOR VARIOUS SOURCE IMPEDANCES

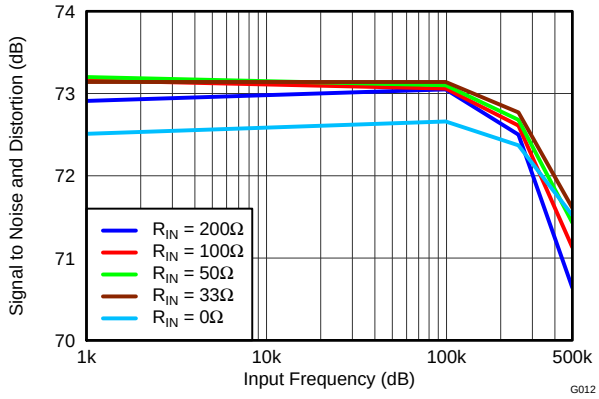


Figure 10.

THD vs INPUT FREQUENCY FOR VARIOUS SOURCE IMPEDANCES

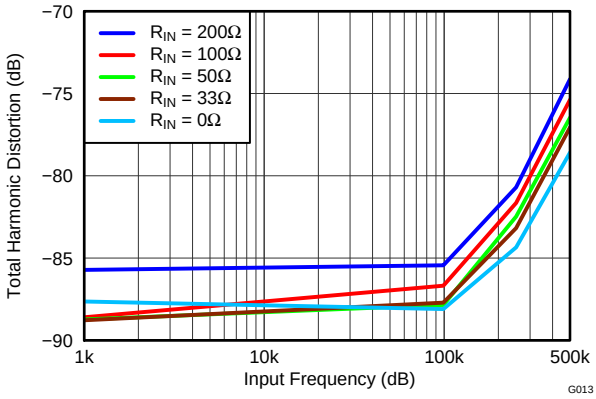


Figure 11.

PSRR vs POWER-SUPPLY RIPPLE FREQUENCY

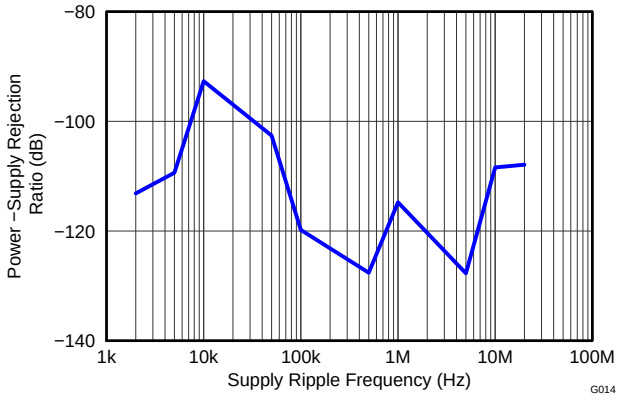


Figure 12.

CROSSTALK vs INPUT REQUENCY

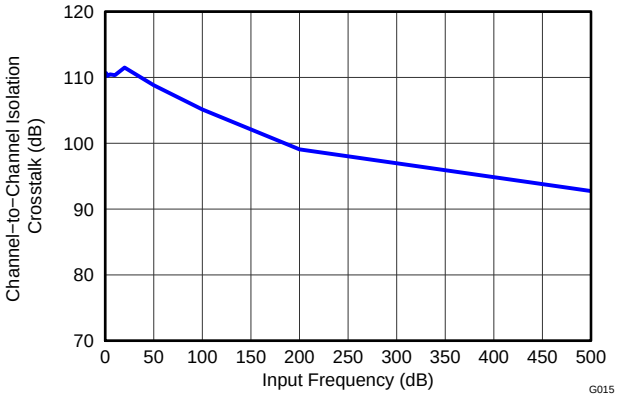


Figure 13.

TYPICAL CHARACTERISTICS (continued)

All plots at T_A = +25°C, AVDD = 3.0 V, DVDD = 3.0 V,

f_{SAMPLE} = 1 MHz, f_{SCLK} = 20 MHz, and V_{REF} = 2.5 V internal, unless otherwise noted.

AVDD POWER vs THROUGHPUT (AVDD = 3 V)

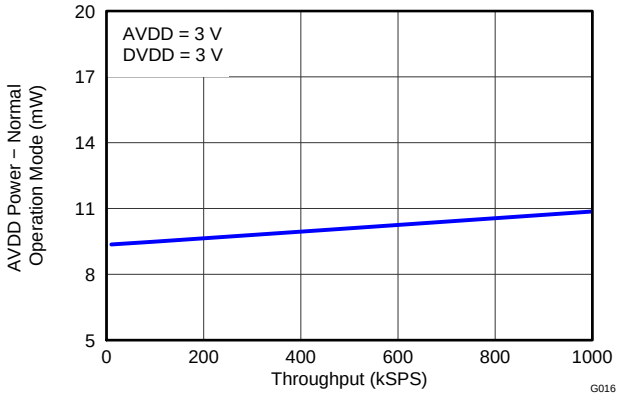


Figure 14.

AVDD POWER vs THROUGHPUT (AVDD = 5 V)

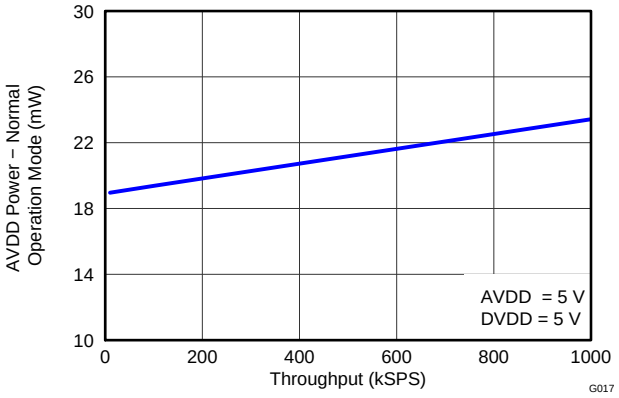


Figure 15.

POWER-DOWN CURRENT vs AVDD AT VARIOUS TEMPERATURES

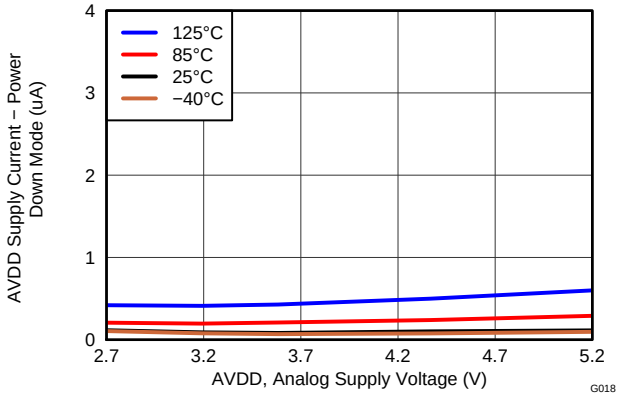


Figure 16.

AVDD CURRENT vs THROUGHPUT (AVDD = 3 V)

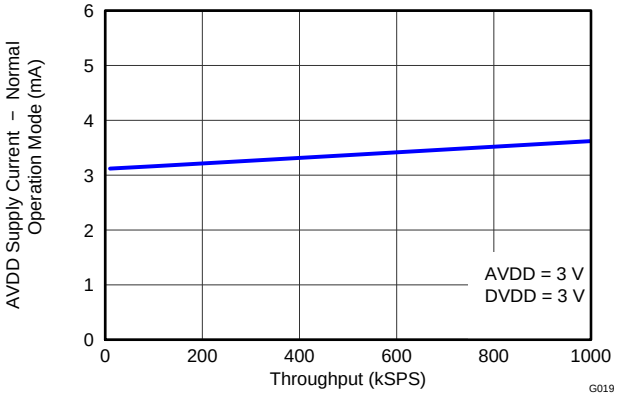


Figure 17.

AVDD CURRENT vs THROUGHPUT (AVDD = 5 V)

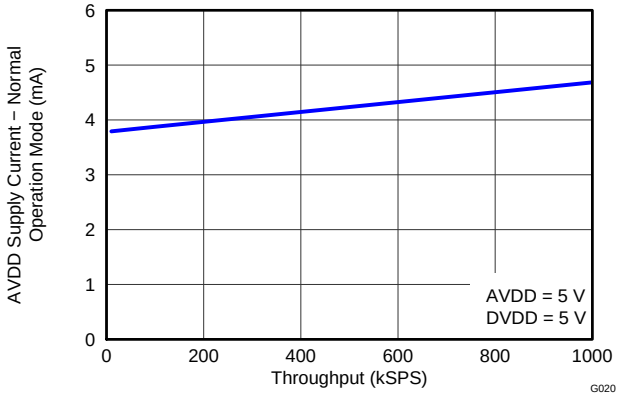


Figure 18.

DNL vs TEMPERATURE

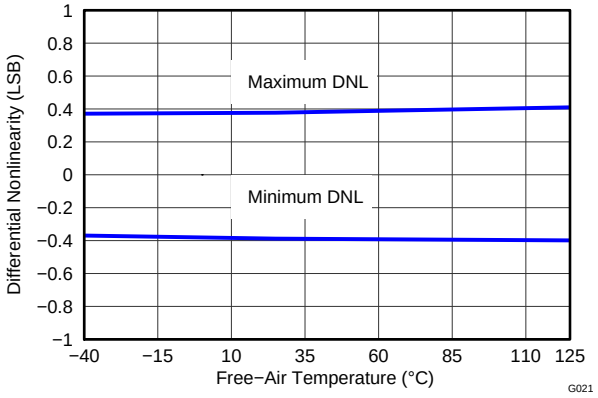


Figure 19.

TYPICAL CHARACTERISTICS (continued)

All plots at T_A = +25°C, AVDD = 3.0 V, DVDD = 3.0 V,

f_{SAMPLE} = 1 MHz, f_{SCLK} = 20 MHz, and V_{REF} = 2.5 V internal, unless otherwise noted.

INL vs TEMPERATURE

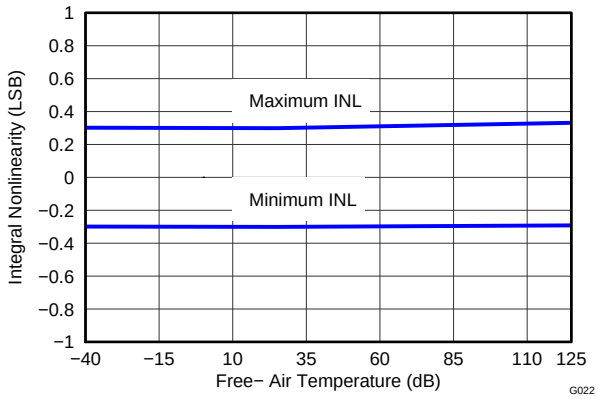


Figure 20.

OFFSET ERROR vs TEMPERATURE

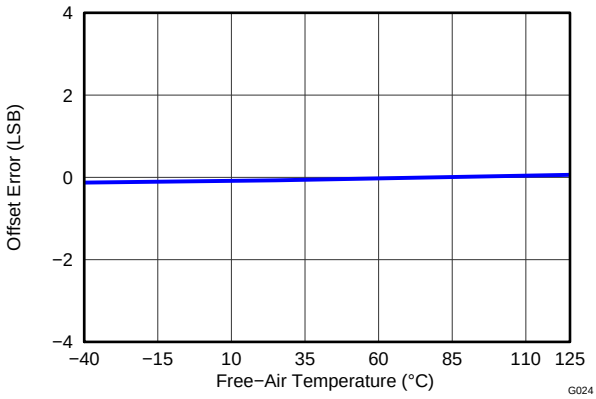


Figure 21.

GAIN ERROR vs TEMPERATURE

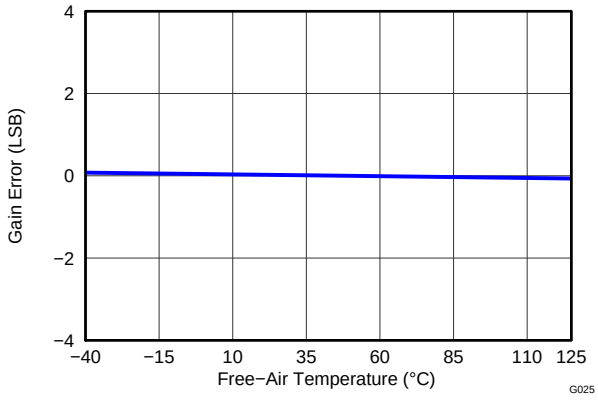


Figure 22.

SINAD vs AVDD

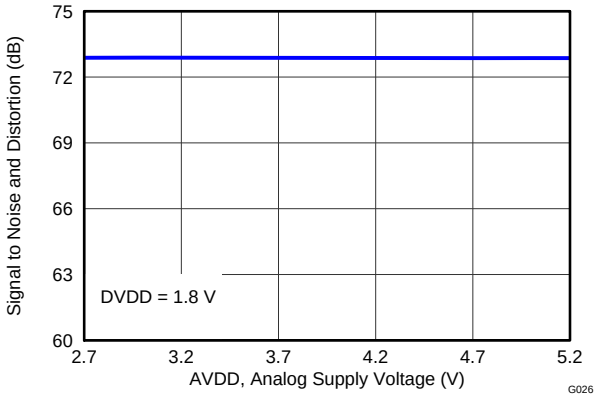


Figure 23.

DNL vs AVDD

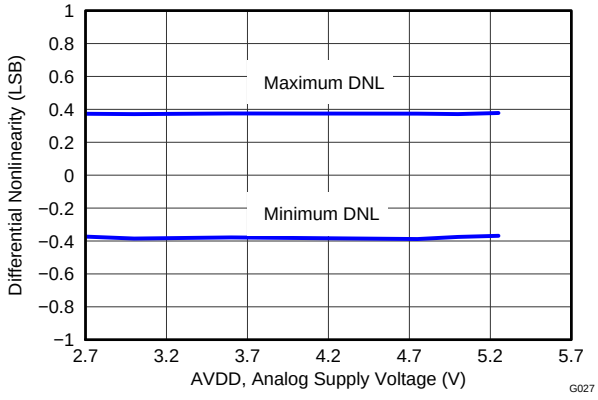


Figure 24.

INL vs AVDD

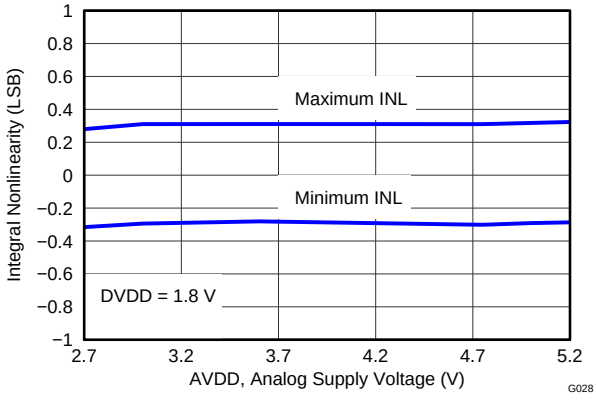


Figure 25.

TYPICAL CHARACTERISTICS (continued)

All plots at T_A = +25°C, AVDD = 3.0 V, DVDD = 3.0 V,

f_{SAMPLE} = 1 MHz, f_{SCLK} = 20 MHz, and V_{REF} = 2.5 V internal, unless otherwise noted.

OFFSET ERROR vs AVDD

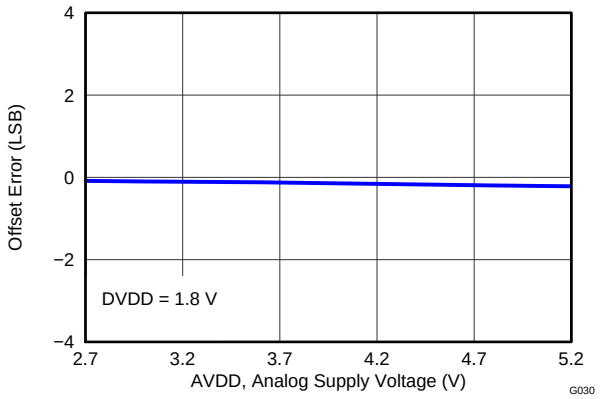


Figure 26.

GAIN ERROR vs AVDD

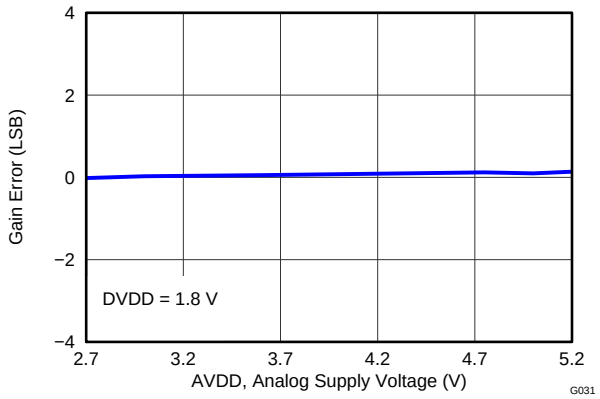


Figure 27.

CROSSTALK vs INPUT FREQUENCY

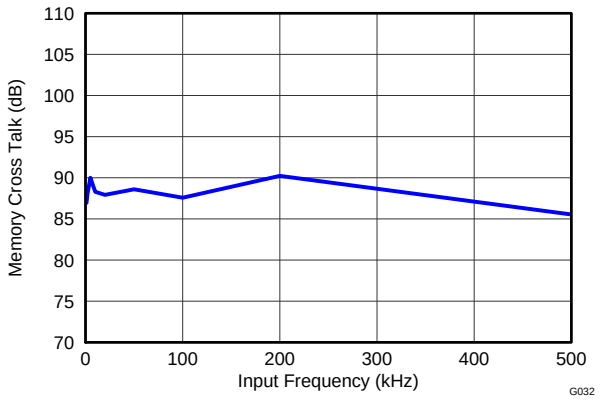


Figure 28.

TEMPERATURE SENSOR ACCURACY

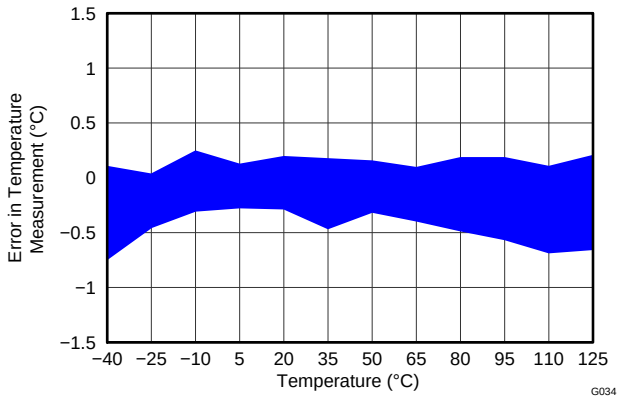


Figure 29.

TEMPERATURE SENSOR RESPONSE TO THERMAL SHOCK – FROM ROOM TEMPERATURE INTO 50°C STIRRED OIL

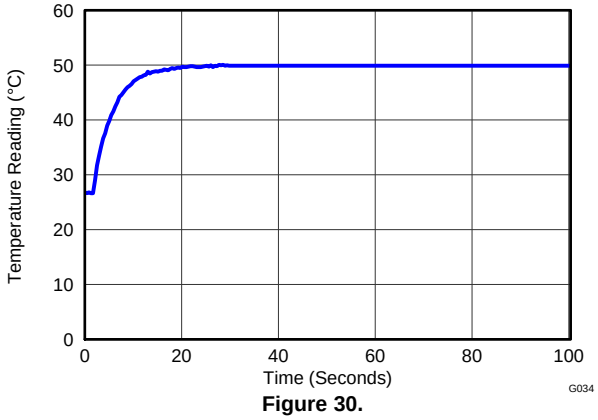


Figure 30.

OVERVIEW

The ADS8028 is a 12-bit successive-approximation register (SAR) analog-to-digital converter (ADC) that can support throughput rates up to 1 MSPS. The device features a 2.5-V internal reference, but can also function with an external reference source. The analog input range is 0 V to V_{REF}. The device supports eight single-ended analog inputs and integrates an internal temperature sensor. A nine-channel (eight analog inputs plus the internal temperature sensor) internal multiplexer allows selection of multiple channels to be scanned sequentially. Additionally, this scan sequence can be repeated indefinitely with minimal intervention.

The internal temperature sensor has a resolution of 0.25°C and measures the ADS8028 die temperature. To measure the temperature of an external heat source, thermal resistance should be minimized between the heat source and the ADS8028 thermal pad (refer to the *Application Information* section for more details).

The ADS8028 consumes only 17 mW of power at 1 MSPS and also provides hardware (PD) and software (STANDBY) selectable low-power modes for optimal power usage.

The device provides an SPI-compatible serial interface that can operate up to 20 MHz over a wide supply range (DVDD = 1.65 V to 5.25 V). The ADS8028 operates with one cycle latency, thus the conversion result performed in one cycle can be read out in the subsequent cycle.

ANALOG INPUTS AND MULTIPLEXER

The ADS8028 has eight single-ended analog input channels (AIN0 to AIN7). Figure 31 shows an equivalent circuit for each analog input pin. The two diodes, D_1 and D_2, provide electrostatic discharge (ESD) protection for the individual analog pins. These diodes can conduct approximately 10 mA of current without causing irreversible damage to the device. Diode D_1 turns on when AINx is greater than AVDD + 0.3 V and diode D_2 turns on when AINx is less than AGND – 0.3 V. Therefore, care must be taken to always ensure that Equation 1 is met.

$$AGND - 0.3\ V < AINx < AVDD + 0.3\ V \quad (1)$$

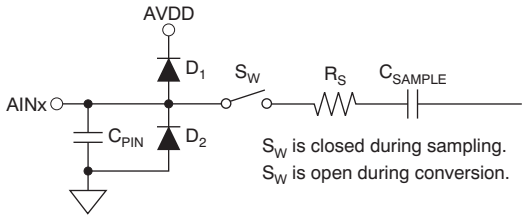


Figure 31. Equivalent Analog Input Circuit

Capacitor C_{PIN} is approximately 8 pF. Resistor R_S represents the sampling switch on-state resistance plus the input multiplexer on-state resistance. The total resistance is approximately 130 Ω. C_{SAMPLE} is the ADC sampling capacitor, typically 40 pF.

The ADS8028 contains a nine-channel input multiplexer that either allows one of the eight analog input channels or the internal temperature sensor to be converted. Multiple channels can be converted in a predetermined sequence; this sequence can be repeated indefinitely with appropriate Control Register settings (refer to the *Modes of Operation* section for more details). On power-up, no channel is selected for conversion and SDO returns all '1's. One write cycle must be executed to select the channels and start the conversion process.

In order to achieve specified signal-to-noise ratio (SNR) and total-harmonic-distortion (THD) performance, especially at higher input frequencies, it is recommended to drive each analog input pin with a low impedance source. An external amplifier can also be used to drive the input pins. A simple RC low-pass filter can be used on the analog input pins to reduce the input signal bandwidth and remove the noise components at higher frequencies (refer to the *Application Information* section for more details).

TEMPERATURE SENSOR

The internal temperature sensor measures the ADS8028 die temperature. The temperature sensor can be selected for conversion by setting the T_{SENSE} bit in the Control Register to '1'. The TM_BUSY pin goes high as soon as the temperature sensor is selected for conversion and remains high until the conversion is completed (100 µs, max).

The operating temperature range for this internal temperature sensor is limited by the operating temperature range of the ADS8028 (–40°C to +125°C).

Modes of Operation

The ADS8028 temperature sensor can operate in two modes: normal mode and averaging mode.

Normal Mode

To operate in normal mode (without the averaging feature), the TMP_AVG bit in the Control Register should be set to '0' and the T_{SENSE} bit in the Control Register should be set to '1'. Output data are the result of a single conversion performed on the temperature sensor. This mode is the default mode of operation for the temperature sensor. A single conversion on the temperature sensor takes 100 µs, max.

Averaging Mode

In this mode, the ADS8028 provides rolling average filtering to increase the accuracy of the temperature sensor measurement. To activate this filter, the TMP_AVG bit in the Control Register should be set to '1'. This bit must be set to '1' in subsequent write operations for the duration of the filter operation. Resetting the TMP_AVG bit to '0' resets and deactivates the filter and places the ADS8028 in a normal mode of operation.

When the TMP_AVG and T_{SENSE} bits are both set to '1', the temperature sensor is selected and the conversion result is sent to the filter block. The filter block output is given by Equation 2:

$$\text{New\_Average\_Result} = \frac{7}{8}\ (\text{Previous\_Average\_Result}) + \frac{1}{8}\ (\text{Current\_Result}) \quad (2)$$

This output can be read during the next conversion cycle. After enabling the averaging feature, the first ADS8028 output data are the same as the temperature sensor conversion result. Averaging starts taking effect from the subsequent conversion performed on the temperature sensor.

Temperature Sensor Data Format

The temperature sensor, along with the ADC, gives 0.25°C resolution over the operating temperature range. The temperature reading from the ADC is in 12-bit twos complement format, as shown in Table 1.

Table 1. Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT
–40	1111 0110 0000
–25	1111 1001 1100
–10	1111 1101 1000
–0.25	1111 1111 1111
0	0000 0000 0000
+0.25	0000 0000 0001
+10	0000 0010 1000
+25	0000 0110 0100
+50	0000 1100 1000
+75	0001 0010 1100
+100	0001 1001 0000
+105	0001 1010 0100
+125	0001 1111 0100

If the output data MSB is '0', the temperature can be calculated with Equation 3:

$$\text{Temperature} = V_{EXT\_REF} \left(\frac{\text{ADC\_Code}}{10} + 109.3 \right) - 273.15$$

where:

V_{EXT_REF} is the value of the external reference voltage (3)

If the output data MSB is '1', the temperature can be calculated with Equation 4:

$$\text{Temperature} = V_{EXT\_REF} \left(\frac{\text{ADC\_Code} - 4096}{10} + 109.3 \right) - 273.15$$

where:

V_{EXT_REF} is the value of the external reference voltage (4)

For a 2.5-V reference (internal or external), Equation 3 and Equation 4 simplify to Equation 5 and Equation 6, respectively.

$$\text{Positive Temperature} = \frac{\text{ADC\_Code}}{4} \quad (5)$$

$$\text{Negative Temperature} = \frac{4096 - \text{ADC\_Code}}{4} \quad (6)$$

REFERENCE

The ADS8028 can operate with either an internal voltage reference or an optional external reference. The type of reference used is set by the EXT_REF bit in the Control Register.

The internal reference is selected when the EXT_REF bit is set to '0'. A 2.5-V output of the internal reference is available on the REF pin. A 10-µF decoupling capacitor is recommended between the REF and AGND pins. The reference circuit requires 5.5 ms to charge the decoupling capacitor. The internal reference is capable of sourcing up to 2 mA of current and is designed to drive the ADS8028. It is recommended to buffer this output for use elsewhere in the system.

The ADS8028 can operate with an external reference when the EXT_REF bit is set to '1'. An external reference can be supplied through the REF pin. By default, the ADS8028 powers up in internal reference mode and must be programmed to function with an external reference. Until such a time, the ADS8028 draws additional current from the external reference source. This current is limited to 20 mA, using internal protection circuitry. Texas Instruments' REF5025 can be used as external reference source for the ADS8028.

ADC TRANSFER FUNCTION

The ADS8028 output is in straight binary format for all analog input channels (AIN0 to AIN7) and is in twos complement format for the temperature sensor conversion result. The transition in output code occurs at every LSB step. For the ADS8028, LSB step size is V_{REF}/4096. The ideal ADS8028 transfer characteristic for straight binary coding is shown in Figure 32.

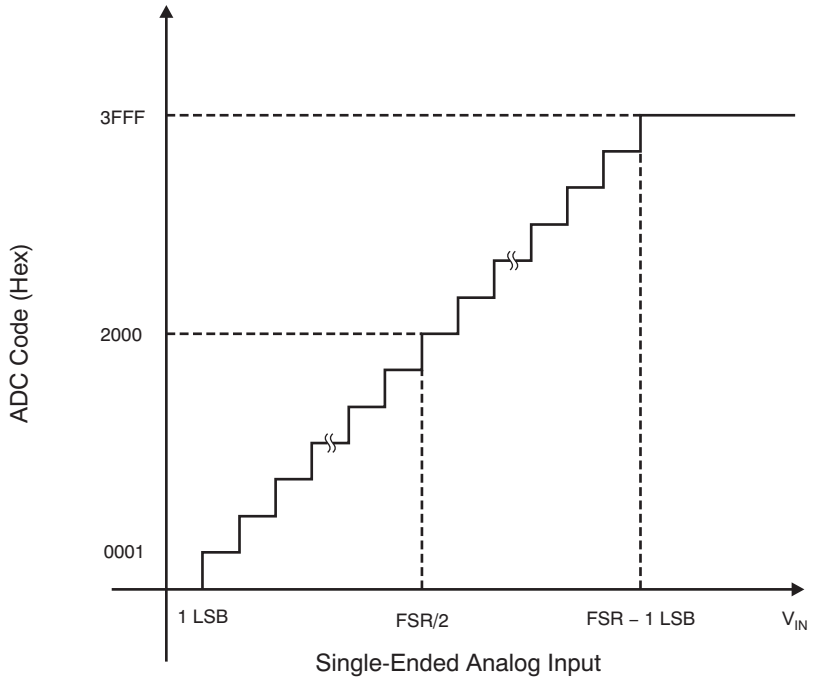


Figure 32. Straight Binary Transfer Characteristic

SERIAL INTERFACE

Figure 33 shows a detailed ADS8028 serial interface timing diagram. The device uses the serial clock (SCLK) for internal conversion and for data transfer into and out of the device.

The $\overline{CS}$ signal defines one frame of conversion and serial transfer. The ADS8028 samples the analog input on the $\overline{CS}$ falling edge. The sample-and-hold circuit enters into hold mode and the serial data bus comes out of 3-state. The subsequent 16 SCLK cycles are used for conversion and data transfer. As shown in Figure 33, the MUX selects the programmed channel and the sample-and-hold circuit enters into hold mode on the 14th SCLK falling edge. The DOUT pin goes back to 3-state on the 16th SCLK falling edge or on the $\overline{CS}$ rising edge (whichever occurs first). For a valid read or write operation to the ADS8028, 16 clocks must be provided on the SCLK pin between the $\overline{CS}$ falling edge to the subsequent $\overline{CS}$ rising edge. If the $\overline{CS}$ rising edge occurs before 16 SCLKs have elapsed, the conversion is terminated, the DOUT line goes back into 3-state, and the Control Register is not updated.

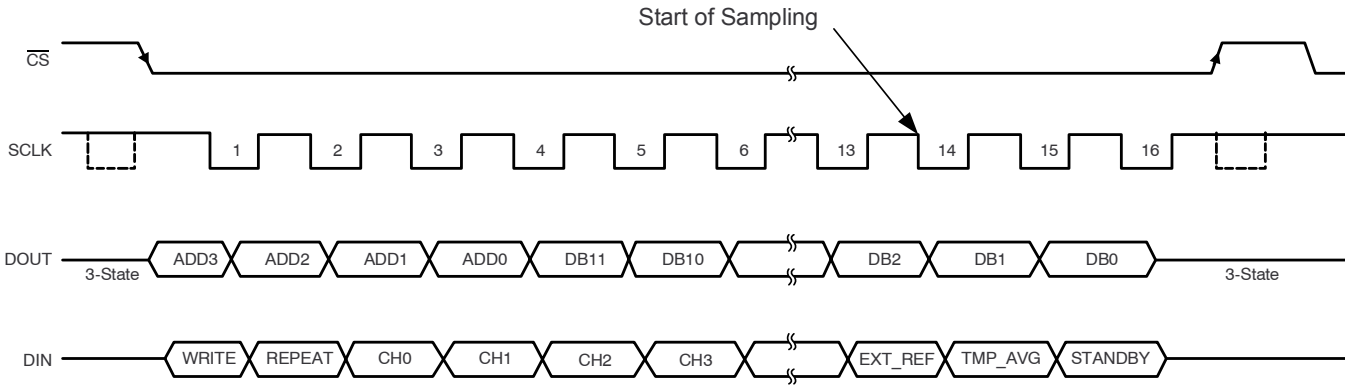


Figure 33. Serial Interface Timing Diagram

Refer to Table 3 for the ADS8028 output data format. Bits ADD[3:0] specify the channel selected for conversion and bits DB[11:0] are the conversion result for the selected channel.

A $\overline{CS}$ falling edge brings the DOUT pin out of 3-state and also outputs the ADD3 bit on the DOUT pin. The next 15 bits of data (ADD2 to DB0) are clocked out on the subsequent SCLK falling edges. Therefore, the first SCLK falling edge outputs the ADD2 bit on DOUT and can also be used by the microcontroller or digital signal processor (DSP) to read the first bit (ADD3). Similarly, bit DB0 is clocked out on the 15th SCLK falling edge and can be read by the microcontroller or DSP on the 16th SCLK falling edge. The 16th SCLK falling edge also puts the DOUT pin into 3-state.

When using a slower SCLK, it may be possible for the microcontroller or DSP to read the data on each SCLK rising edge. The first SCLK rising edge (after the $\overline{CS}$ falling edge) reads ADD3 and the 15th SCLK rising edge reads DB0.

Data provided on the DIN pin are clocked into the ADS8028 on the first 16 SCLK falling edges (after the $\overline{CS}$ falling edge). However, if the WRITE bit is not set to '1', the ADS8028 ignores the subsequent 15 bits of data (refer to the *Data Write Operation* section for more details).

DATA WRITE OPERATION

Control Register Settings

The ADS8028 operation is controlled by the status of the internal Control Register. Data written into the Control Register decide the configuration of the ADS8028 for the next conversion cycle. The Control Register is 16 bits wide, and only supports write operation. The Control Register can be written to with the serial interface. Data on the DIN pin are loaded into the Control Register on the first 16 SCLK falling edges (after a $\overline{CS}$ falling edge). The bit functions are outlined in Table 2. On power-up, the default Control Register content is all '0's.

Table 2. Control Register Bit Functions

MSB							
15	14	13	12	11	10	9	8
WRITE	REPEAT	AIN0	AIN1	AIN2	AIN3	AIN4	AIN5
							LSB
7	6	5	4	3	2	1	0
AIN6	AIN7	T_{SENSE}	X	X	EXT_REF	TMP_AVG	STANDBY

Bit 15 **WRITE: Write to Control Register**

Enable write operation.
0 = Write disabled; Control Register is not updated and the next 15 bits are ignored (default)
1 = Write enabled; the next 15 bits update the Control Register

Bit 14 **REPEAT: Repeat conversion mode**

Enable conversion repeat mode (refer to the *Modes of Operation* section).
0 = Disable repeat conversion mode (default)
1 = Enable repeat conversion mode

Bits[13:6] **AIN[0:7]: Analog input channel selection**

Each AINx bit corresponds to the associated analog input channel, AIN0 to AIN7.
0 = AINx channel is not selected for conversion (default)
1 = AINx channel is selected for conversion

Bit 5 **T_{SENSE}: Internal temperature sensor selection**

Internal temperature sensor selection for conversion in subsequent cycles.
0 = Internal temperature sensor output is not selected for conversion (default)
1 = Internal temperature sensor output is selected for conversion

Bits[4:3] **X: Don't care**

Bit 2 **EXT_REF: Reference source selection**

This bit selects the reference source for the next conversion.
0 = Internal reference is used for the next conversion (default)
1 = External reference is used for the next conversion

Bit 1 **TMP_AVG: Temperature sensor averaging selection**

This bit selects the mode of operation for the temperature sensor channel; this bit is ignored if bit 5 is set to '0'.
0 = Averaging is disabled on the temperature sensor result (default)
1 = Averaging is enabled on the temperature sensor result

Bit 0 **STANDBY: STANDBY mode selection**

This bit sets the mode (normal or standby) for the ADS8028.
0 = The ADS8028 operates in normal mode (default)
1 = The ADS8028 goes to standby mode in the next cycle

DATA READ OPERATION

Table 3 shows the ADS8028 output data format. Bits ADD[3:0] specify the channel selected for conversion and bits DB[11:0] are the conversion result for the selected channel.

Table 3. Channel Address Bits

ADD3	ADD2	ADD1	ADD0	ANALOG INPUT CHANNEL
0	0	0	0	AIN0
0	0	0	1	AIN1
0	0	1	0	AIN2
0	0	1	1	AIN3
0	1	0	0	AIN4
0	1	0	1	AIN5
0	1	1	0	AIN6
0	1	1	1	AIN7
1	0	0	0	T_{SENSE} without averaging
1	0	0	1	T_{SENSE} with averaging

Analog Input Channel

A $\overline{CS}$ falling edge brings the DOUT pin out of 3-state and also outputs the ADD3 bit on the DOUT pin. The next 15 bits of data (ADD2 to DB0) are clocked out on the subsequent SCLK falling edges. Therefore, the first SCLK falling edge outputs the ADD2 bit on DOUT and can also be used by the microcontroller or DSP to read the first bit (ADD3). Similarly, bit DB0 is clocked out on the 15th SCLK falling edge and can be read by the microcontroller or DSP on the 16th SCLK falling edge. The 16th SCLK falling edge also puts the DOUT pin into 3-state.

When using a slower SCLK, it may be possible for the microcontroller or DSP to read the data on each SCLK rising edge. The first SCLK rising edge (after the $\overline{CS}$ falling edge) reads ADD3 and the 15th SCLK rising edge reads DB0.

Internal Temperature Sensor Channel

The internal temperature sensor can be selected for conversion by writing a '1' to the T_{SENSE} bit in the Control Register. On the next $\overline{CS}$ falling edge, the TM_BUSY pin goes high and remains high throughout the temperature sensor conversion process. When the TM_BUSY pin goes high, 16 clocks are required to execute one valid read or write cycle: to read the previous conversion result and to program the next conversion settings. However, any subsequent read or write operations are ignored until TM_BUSY goes low; $\overline{CS}$ is ignored, the Control Register is not updated, and DOUT returns all '1's.

The ADS8028 takes 100 µs (max) to measure and convert the temperature channel. A TM_BUSY signal falling edge can be used to initiate a read operation in order to read the temperature conversion result. However, t_{ACQ} must be allowed to elapse between the TM_BUSY falling edge and the subsequent $\overline{CS}$ falling edge to ensure that the subsequent conversion has sufficient acquisition time. Figure 34 shows the temperature sensor conversion sequence.

After TM_BUSY goes high, the temperature conversion can be aborted by writing a '1' to the STANDBY bit in the first write operation. The device aborts the ongoing conversion and enters STANDBY mode on the 16th SCLK falling edge.

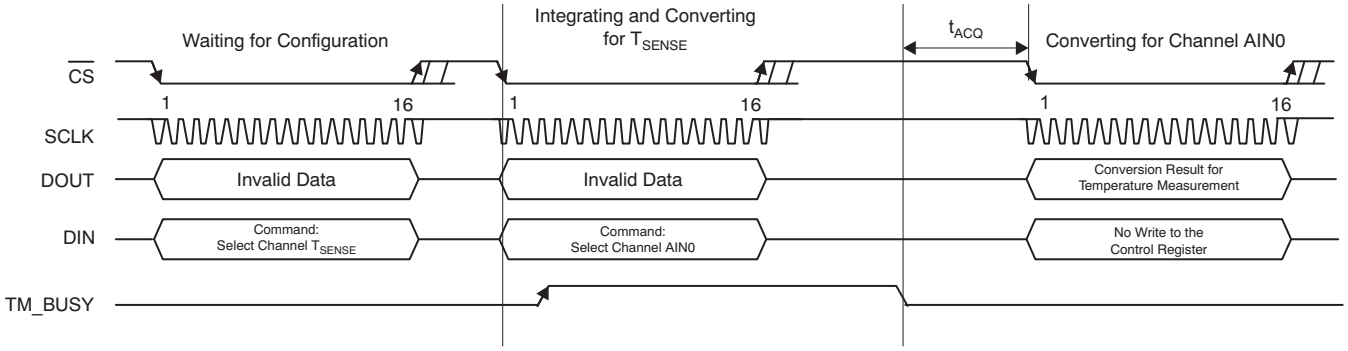


Figure 34. Serial Interface Timing Diagram for the Temperature Sensor Conversion

MODES OF OPERATION

Channel Scanning

The ADS8028 offers different modes of operation that can be selected by programming the Control Register. Channel-scanning modes enable any of the nine channels to be selected for conversion and also allow the selected channels to be repeatedly converted. Low-power modes allow power consumption and throughput rate ratio to be optimized.

Single or Multiple Channels: One Conversion

The ADS8028 can be configured to convert any of the nine channels by writing a '1' to the Control Register bit associated with the desired channel. After power-up, a valid write operation must be executed on the Control Register to select the desired channel. In this mode, the REPEAT bit in the Control Register should be set to '0'. The selected channel is converted in the second frame and the conversion result can be clocked out in the third frame. During the second frame, the Control Register can be written to select the channel to be converted in the third frame. Figure 35 shows a diagram of this configuration.

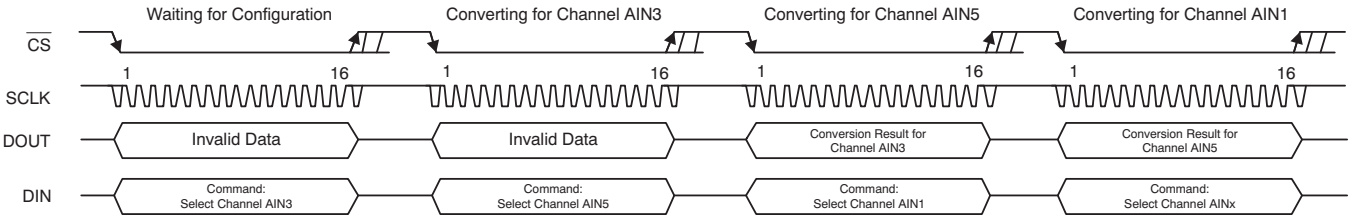


Figure 35. Configuring a Conversion and Read with the ADS8028 (One Channel Selected for Conversion, REPEAT = 0)

If multiple channels are selected by writing a '1' to all associated bits in the Control Register, the ADS8028 converts all selected channels sequentially (in ascending order) in successive frames as defined by the $\overline{CS}$ falling edges. When all selected channels in the Control Register are converted, the ADS8028 stops conversions and waits for a valid write operation to be executed in the Control Register to select the next channel to be converted. This operation is shown in Figure 36. DOUT returns all '1's if the conversion sequence is completed or if no channel is selected. When the ADS8028 begins to convert the first channel in the selected channel sequence, the WRITE bit in the Control Register must be set to '0' in any subsequent frames to avoid interrupting the selected sequence.

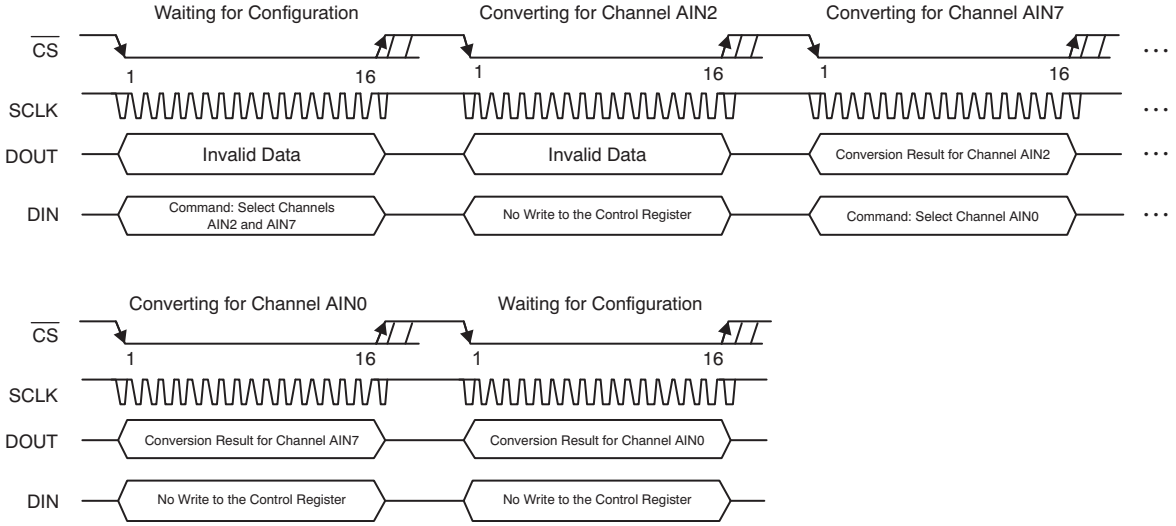


Figure 36. Configuring a Conversion and Read with the ADS8028 (Numerous Channels Selected for Conversion, REPEAT = 0)

Single or Multiple Channels: Repeated Conversions

The ADS8028 can be programmed to repeatedly convert either a single channel or a sequence of channels without having to reprogram the Control Register. To operate in this mode, execute a valid write operation to the Control Register. During this write operation, the REPEAT bit in the Control Register should be set to '1' and the desired channels should be selected by writing a '1' to the associated bits. Thereafter, the ADS8028 continuously cycles through the selected channels in ascending order, beginning with the lowest channel and converting all channels selected in the Control Register. On completion of the sequence, the ADS8028 returns to the first selected channel in the Control Register and repeats the sequence.

The ADS8028 continues to operate in repeat mode until a valid write operation is executed to reprogram the Control Register. When the Control Register is updated, the ADS8028 comes out of repeat mode and begins operating as per the new programmed settings. Therefore, to continue in repeat mode and to avoid accidentally overwriting the Control Register, it is recommended that the WRITE bit in the Control Register be set to '0' while operating in repeat mode. Figure 37 illustrates the repeat mode of operation.

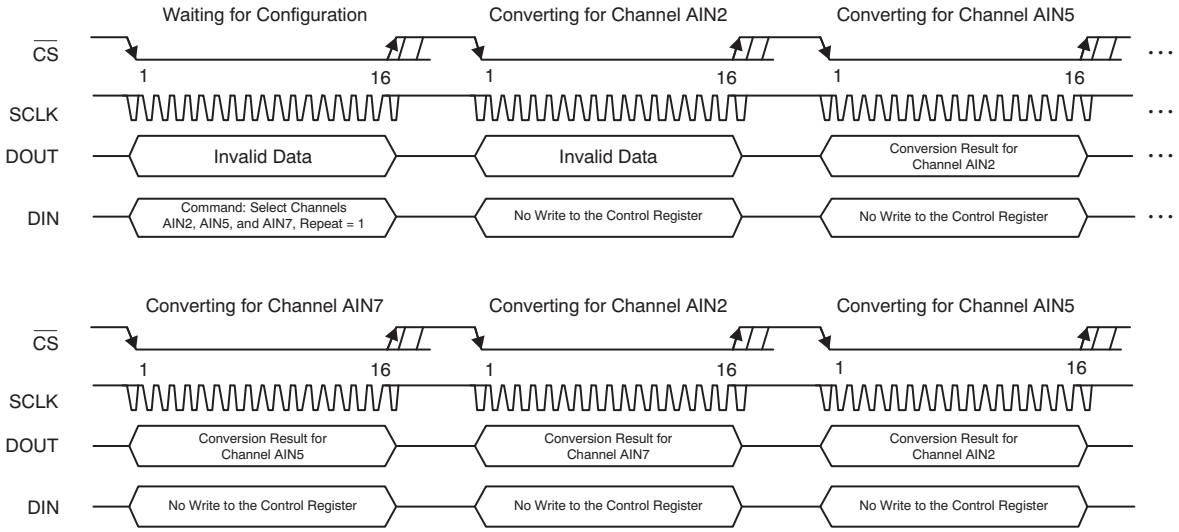


Figure 37. Configuring a Conversion and Read in Repeat Mode

Low-Power Modes

In normal mode of operation, all internal ADS8028 blocks are always powered up and the device is always ready to initiate a new conversion. This architecture enables the ADS8028 to support the 1-MSPS rated throughput rate. However, the ADS8028 also supports two low-power modes that can be used to optimize the power consumption and throughput rate ratio. In these low-power modes, some internal ADS8028 blocks are powered up or down as the operation requires. This flexibility reduces the overall power consumption at lower throughput rates.

STANDBY Mode

In STANDBY mode, only part of the ADS8028 internal circuitry is powered down. The internal reference is not powered down and, therefore, the ADS8028 can be fully powered up within 1 µs. To enter STANDBY mode, a valid write operation should be executed to the Control Register with the STANDBY bit set to '1'. The ADS8028 enters STANDBY mode on the $\overline{CS}$ rising edge following this write operation.

The temperature sensor averaging function is also reset when the device enters STANDBY mode. While in STANDBY mode, any read operation on the ADS8028 returns all '1's on the DOUT pin.

The ADS8028 remains in STANDBY mode until the STANDBY bit in the Control Register is reset to '0' using a valid write operation. Then, the ADS8028 starts powering up on the $\overline{CS}$ rising edge following this write operation. One valid Control Register write cycle must complete in order to update the desired channels for subsequent conversions. After successful completion of these two write cycles, the device enters a normal mode of operation and operates with one cycle latency.

It takes four serial transfer cycles for the ADS8028 to exit STANDBY mode and transmit the first valid conversion data, as shown in Figure 38. The first cycle updates the STANDBY bit to '0'; the second cycle selects the channels and operation mode; the third cycle converts the selected channel; and the result of this conversion can be clocked out in the fourth cycle.

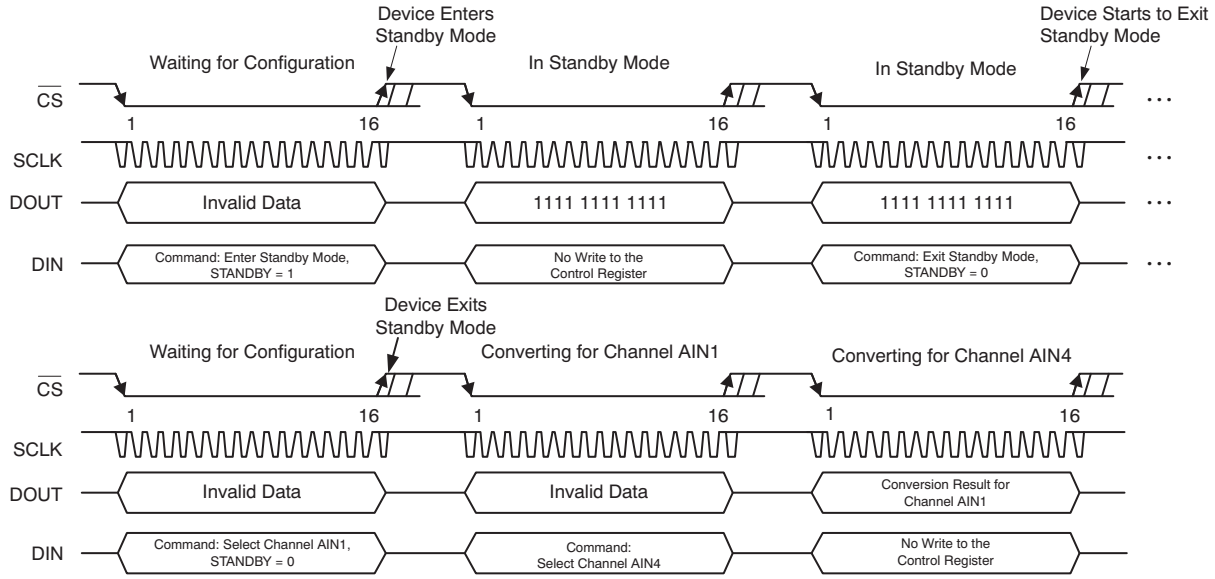


Figure 38. STANDBY Mode of Operation

Power-Down Mode

In power-down mode, all internal ADS8028 circuitry (including the internal reference) is powered down and the Control Register is reset to the default values. The temperature sensor averaging feature is reset and disabled.

The ADS8028 can be placed into power-down mode by pulling the $\overline{PD}/\overline{RST}$ pin to a logic low state for at least 90 ns. The $\overline{PD}/\overline{RST}$ pin is asynchronous to the clock; thus, it can be triggered at any time regardless of the status of other ADS8028 pins (including the analog input channels). When the device is in power-down mode, any activity on the digital input pins (apart from the $\overline{PD}/\overline{RST}$ pin) is ignored and the device does not take input-dependent current from the analog input pins.

The ADS8028 powers up in default condition when the $\overline{PD}/\overline{RST}$ pin is pulled back to a logic high level. Conversions can begin when t_{POWER_UP} has elapsed.

RESET

The ADS8028 can be RESET by pulling the $\overline{PD}/\overline{RST}$ pin to a logic low state for no longer than 60 ns. This input is asynchronous to the clock. On RESET, the Control Register bits are set to the default state and the temperature sensor averaging feature is reset and disabled. When the $\overline{PD}/\overline{RST}$ is pulled back to a logic high state, the ADS8028 is placed in normal mode. One valid write operation must be executed on the Control Register in order to configure the ADS8028 and to select the channels before initiating conversions.

Note that $\overline{PD}/\overline{RST}$ is a dual-function pin. Figure 39 shows the timing of this pin and Table 4 explains the usage of this pin.

Figure 39. $\overline{PD}/\overline{RST}$ Pin Timing

Table 4. $\overline{PD}/\overline{RST}$ Pin Functionality

CONDITION	DEVICE MODE
t_{PL_PDRST} < 60 ns	RESET (device does not enter power-down mode)
60 ns < t_{PL_PDRST} < 90 ns	Device RESET. The ADS8028 may or may not enter power-down mode. **This setting is not recommended.**
t_{PL_PORST} > 90 ns	Device enters power-down mode

POWER SUPPLY

The ADS8028 has two separate power supplies: AVDD and DVDD. The ADC operates on an AVDD power supply; the DVDD supply is used for the interface circuits. AVDD and DVDD can be set independently to any value within the permissible range; however, care must be taken to ensure that Equation 7 is fulfilled.

$$DVDD \le AVDD + 0.3\ V \quad (7)$$

The ADS8028 contains an internal power-on-reset (POR) circuit that resets the Control Register to the default value (all zeros). Therefore, by default, the ADS8028 powers up in internal reference mode. To continue with the internal reference, a 5.5-ms delay must elapse before initiating the first conversion.

To operate with an external reference, there is no required delay for the internal reference to power-up. The ADS8028 digital interface is fully functional 500 µs after power-up. Therefore, after a 500-µs delay, a valid write operation can be executed to the Control Register to program the device in external reference mode and to select the channels for conversion.

APPLICATION INFORMATION

USAGE OF INTERNAL TEMPERATURE SENSOR

The ADS8028 accurately measures and converts the temperature of its own silicon die. Most of the heat transfer between any external heat source and the ADS8028 die occurs via the thermal pad. Therefore, the ADS8028 can be used to measure the temperature of any external heat source by minimizing the thermal resistance between the heat source and the device thermal pad.

APPLICATION CIRCUITS

ADC Driver

The OPA836 is a low-power, 205-MHz bandwidth op amp with 560-V/µs slew rate, and is an excellent driver for the ADS8028 SAR ADC for high ac performance at maximum throughput (1 MSPS). The high bandwidth of the OPA836 is able to correct for fast load transients created by the SAR ADC switching behavior. An RC circuit inserted between the OPA836 and ADS8028 is recommended to further aid the overall circuit performance. This configuration is shown in Figure 40. The RC filter effectively limits the full-power bandwidth of the ADS8028 to reduce the overall noise bandwidth and peak-to-peak noise sampled by the ADS8028. The capacitance is sized to be 10 to 20 times larger than the internal ADS8028 sampling capacitor to provide quick charge sharing to the ADC during switching transients. Furthermore, the resistor provides some isolation between the OPA836 output and the capacitive load to stabilize the amplifier. The RC circuit –3-dB cutoff frequency should be an order of magnitude or larger than the highest input signal frequency to avoid attenuating the desired input signal. A collection of other ADC driving circuits can be found in application note *Buffer Op Amp to ADC Circuit Collection* (SLOA098).

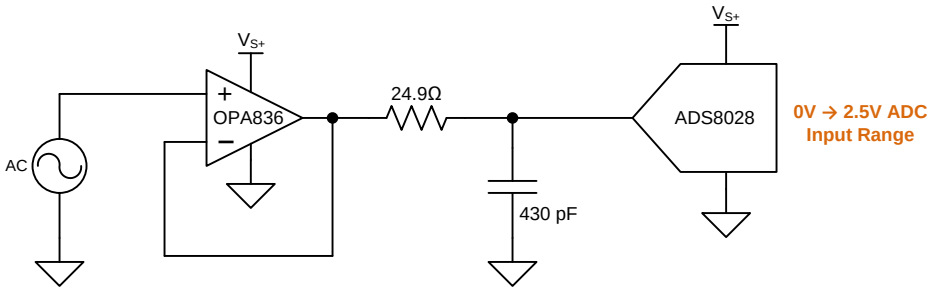


Figure 40. OPA836 Buffer

The TINA-TI simulation file of this circuit can be downloaded by clicking the following link: OPA836 Buffer.

The ac performance of the circuit in Figure 40 was tested with a 2.36-V_{PP} (–0.5 dBFS), 49.911499023-kHz input sine wave. The FFT of the sampled input signal with 8192 samples is shown in Figure 41. The high-precision input signal frequency used to achieve coherent sampling without a windowing function is applied to the data prior to the Fourier Transform. Figure 41 shows that this driver circuit allows the ADS8028 to operate at full throughput within typical characteristic specifications.

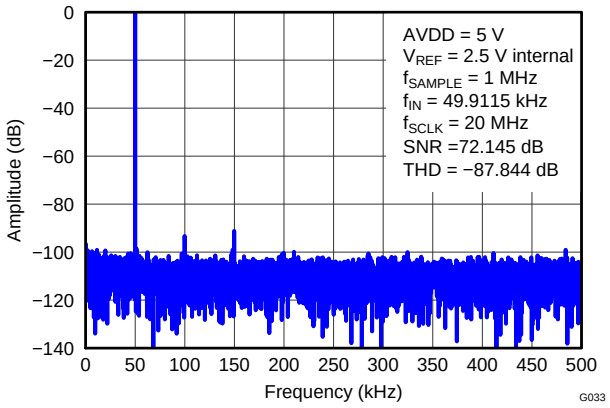


Figure 41. FFT Showing OPA836 Buffer and ADS8028 AC Performance

The ADC drive circuitry may also function to scale output signals from a sensor to the full input voltage range of the ADS8028 to take advantage of the full ADC dynamic range. It is likely that the input signal range will not match the ADS8028 voltage range (0 V to V_{REF}). Input signals to the ADC may need to be amplified, attenuated, or level-shifted. In Figure 42, a resistor network is added in the circuit prior to the OPA836 buffer that can attenuate and level-shift signals. The input signal in Figure 42 is bipolar and is scaled to a unipolar signal for use in the single-supply circuit. The added resistor network does not significantly increase power consumption or load the sensor if large resistor values are chosen. The trade-off to using large resistor values is the added thermal noise injected into the signal path. A shunt capacitor (47 pF shown) is then added between the resistor network and OPA836 buffer such that the desired input signal is minimally attenuated while higher frequency thermal noise is removed.

More ADC analog interface design details and a step-by-step design example are provided in the Applications Journal article, *Sensor to ADC--analog interface design* (SLYT173).

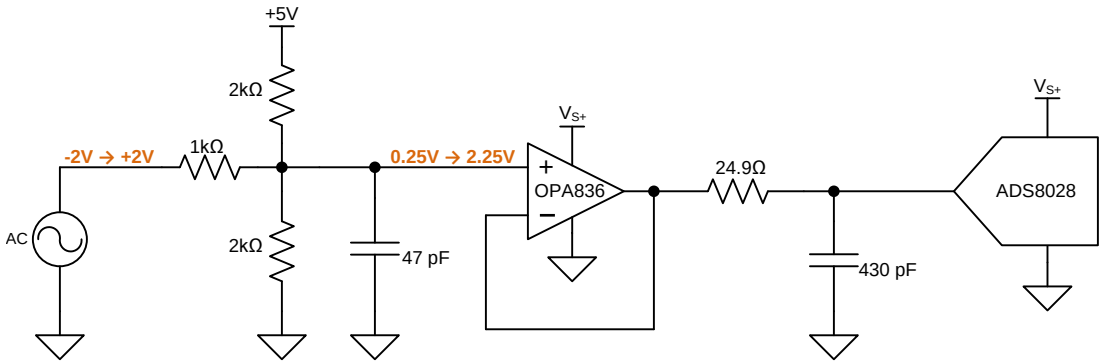


Figure 42. OPA836 Buffer with Voltage Scaling

The TINA-TI simulation file of this circuit can be downloaded by clicking the following link: OPA836 Buffer with Voltage Scaling.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2012) to Revision B	Page
• Changed 产品状态从产品预览改为生产数据	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8028IRTJR	ACTIVE	QFN	RTJ	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS8028	Samples
ADS8028IRTJT	ACTIVE	QFN	RTJ	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ADS8028	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

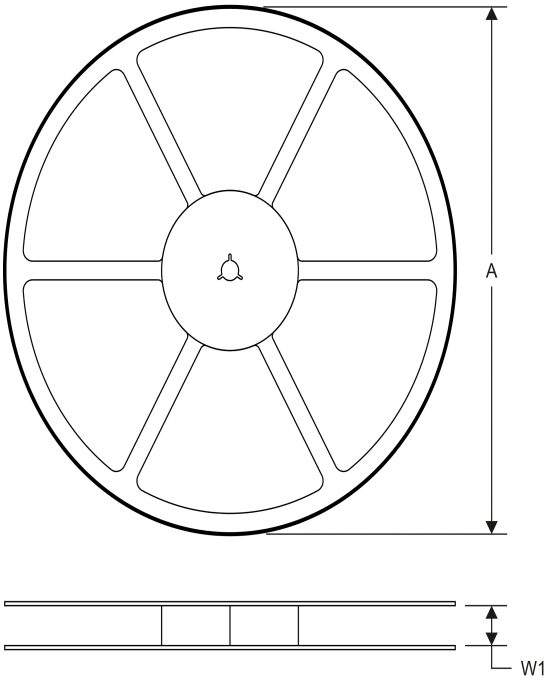
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

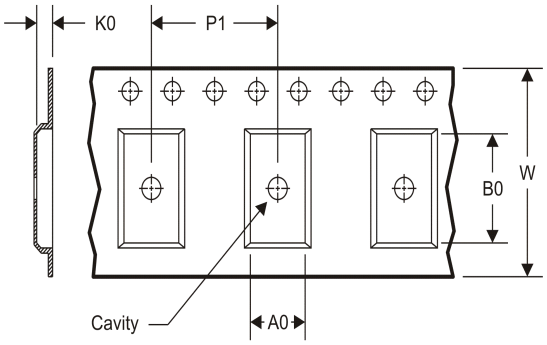
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



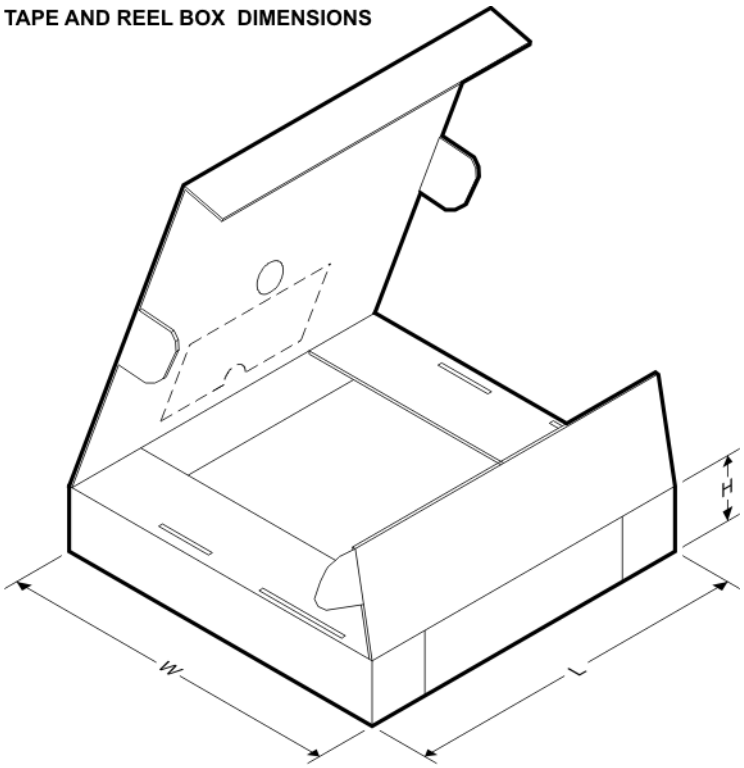
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8028IRTJR	QFN	RTJ	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8028IRTJT	QFN	RTJ	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8028IRTJR	QFN	RTJ	20	3000	367.0	367.0	35.0
ADS8028IRTJT	QFN	RTJ	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

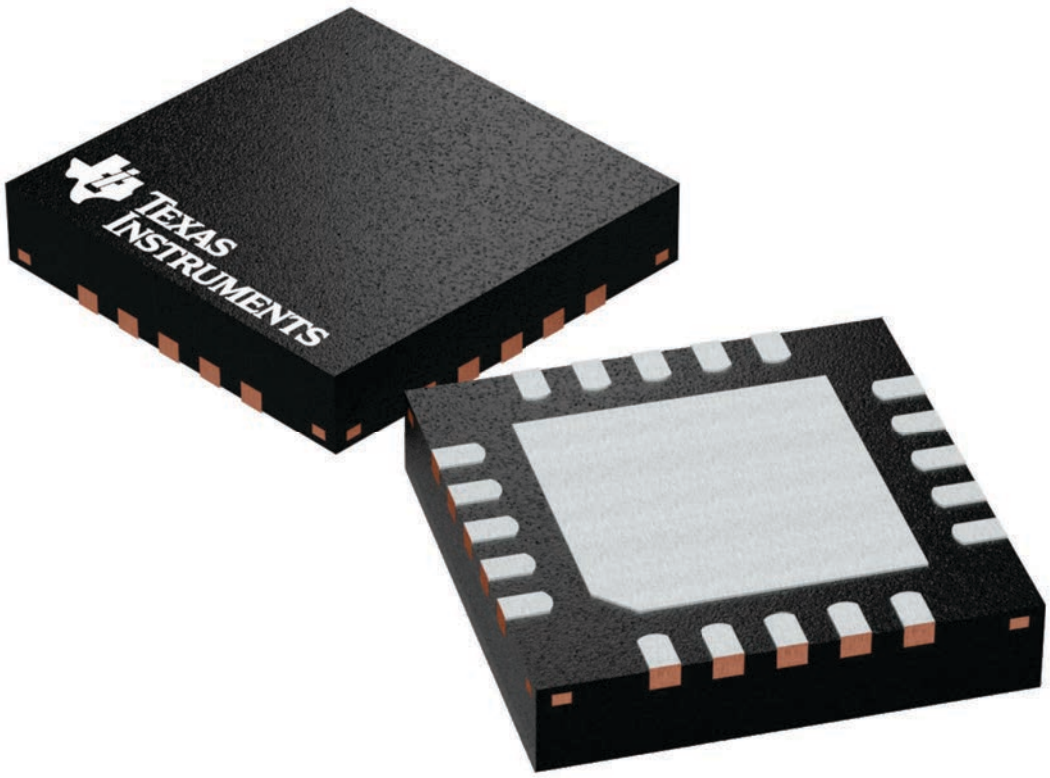
RTJ 20

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



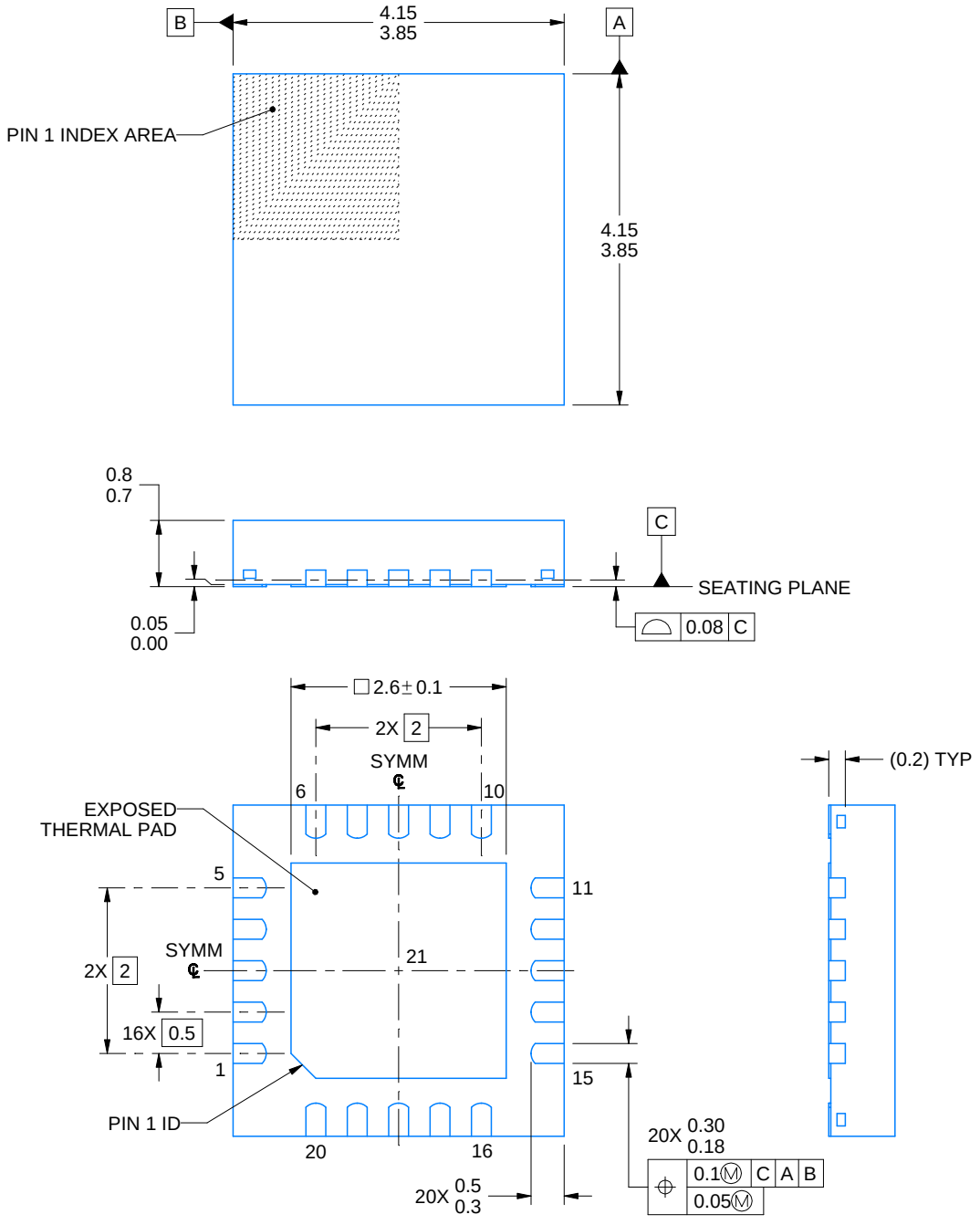
4224842/A

RTJ0020F

PACKAGE OUTLINE

WQFN - 0.8 mm max height

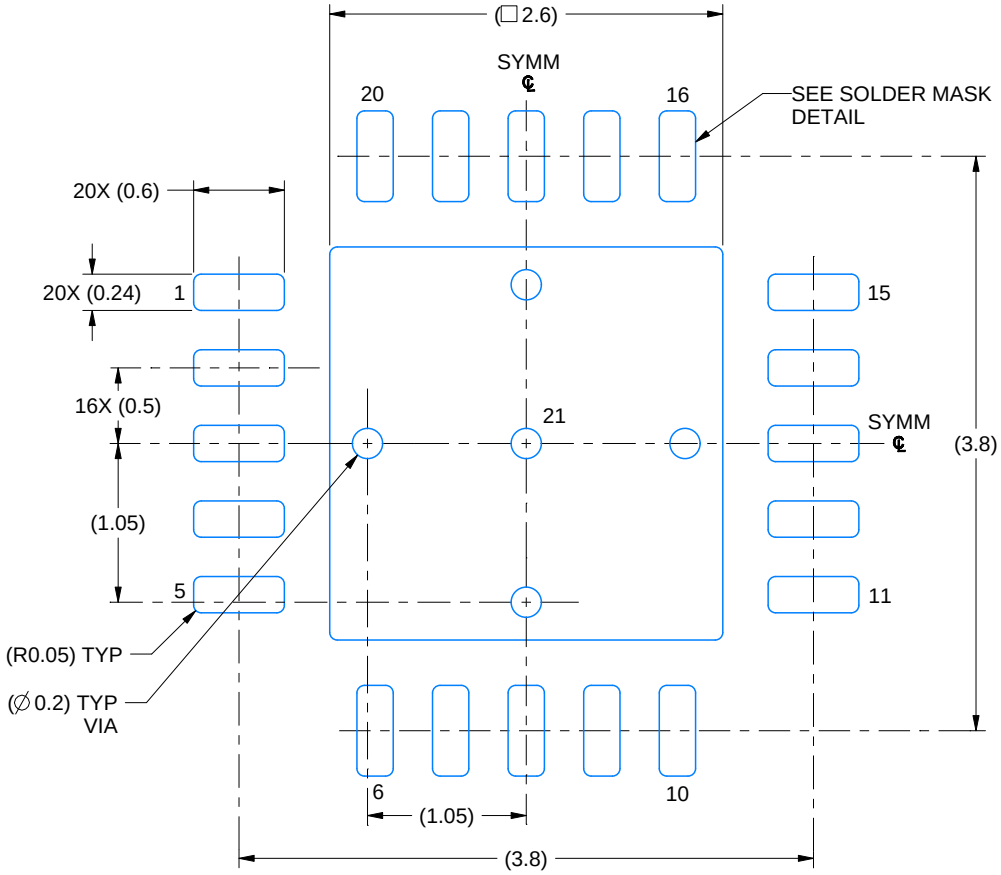
PLASTIC QUAD FLATPACK - NO LEAD



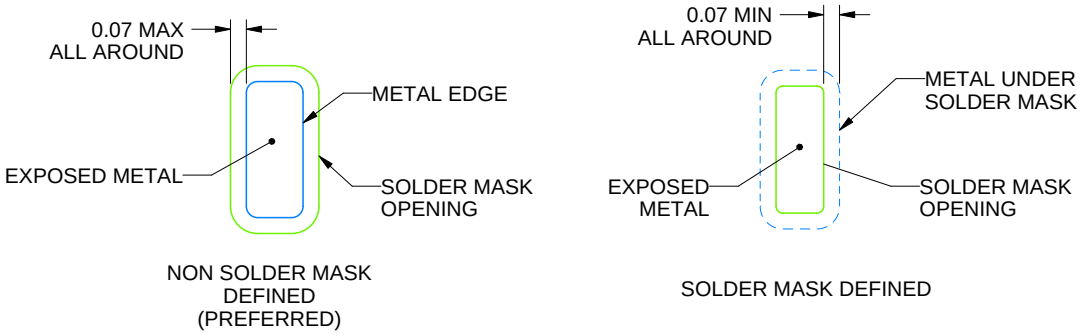
4219126/A 02/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4219126/A 02/2019

NOTES: (continued)

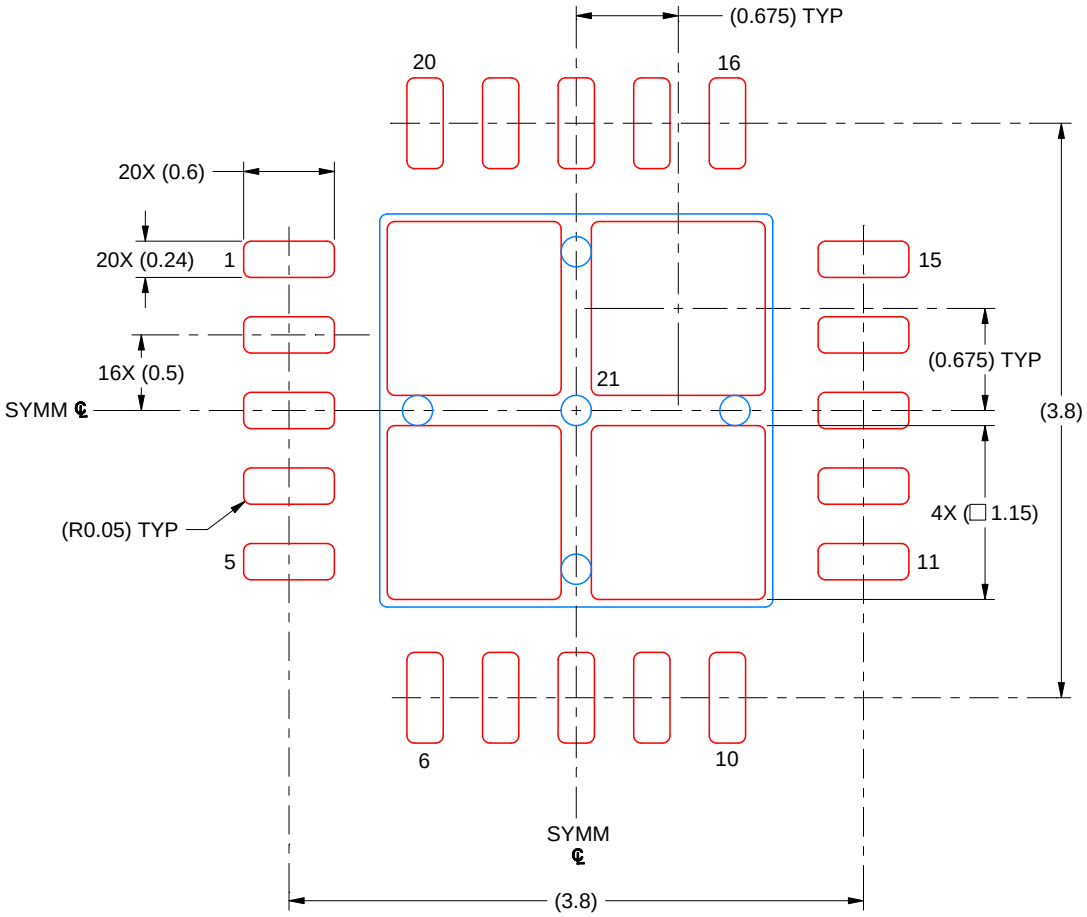
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTJ0020F

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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