TEXAS INSTRUMENTS

ADS1148-Q1

ZHCSFJ3A – JULY 2014 – REVISED SEPTEMBER 2016

ADS1148-Q1 集成有可编程增益放大器 (PGA)、基准和振荡器的汽车用 16 位、2kSPS、模数转换器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 的下列结果：
  - 温度等级 1：-40°C 至 +125°C
  - 人体模型 (HBM) 静电放电 (ESD) 分类等级 2
  - 带电器件模型 (CDM) ESD 分类等级 C5
- 可编程增益：1V/V 至 128V/V
- 可编程数据速率：5SPS 至 2kSPS
- 所有数据速率下均可在单周期内达到稳定
- 带有 8 个独立可选输入的模拟多路选择器
- 双匹配可编程激励电流源：50μA 至 1.5mA
- 2.048V 内部电压基准
- 4.096MHz 内部振荡器
- 内部温度传感器
- 开路状态传感器检测
- 电源和外部基准监控
- 自校准与系统校准
- 8 个通用 I/O
- 兼容 SPI 的串行接口
- 模拟电源：单极（2.7V 到 5.25V）或双极 (±2.5V)
- 数字电源：2.7V 到 5.25V

2 应用

- 基于热电偶、RTD 和热敏电阻的温度测量系统
- 废气感测（煤烟、NO_x、NH_3、O2）
- 电池管理系统 (BMS)
- 多通道电压与电流监控

3 说明

ADS1148-Q1 是一款高度集成的精密 16 位模数转换器 (ADC)，所集成的多种 特性 降低系统成本并减少传感器测量应用中的组件 数量。该器件 具有 一个低噪声的可编程增益放大器 (PGA)、一个具有单周期稳定数字滤波器的精密 Δ-Σ ADC 和一个内部振荡器。ADS1148-Q1 集成了一个低漂移电压基准和两个匹配的可编程激励电流源 (IDAC)。

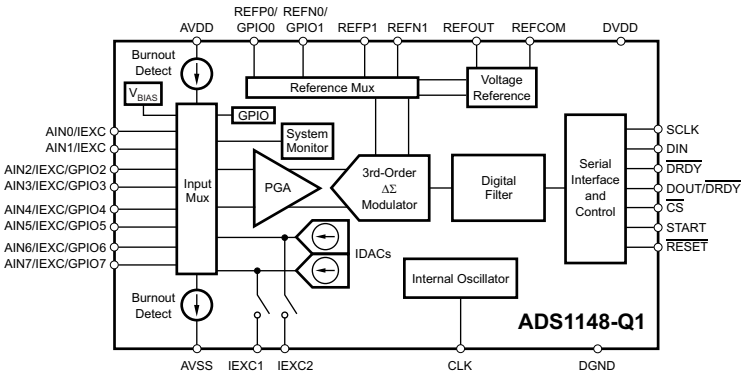
该器件配有一个极其灵活的多路选择器，能够单独选择正负输入。此外，该多路选择器还集成了传感器烧毁检测、热电偶电压偏置和系统监视等功能以及八个通用数字 I/O (GPIO)。PGA 有多种增益可供选择，最高达 128V/V。这些 特性 共同打造了一套面向温度传感器测量应用的完整 前端解决方案，这类应用包括热电偶、热敏电阻和电阻式温度检测器 (RTD) 以及其他小信号测量。数字滤波器可在单周期内达到稳定以在使用输入多路选择器时为快速通道循环提供支持，并且提供高达 2kSPS 的数据速率。数据速率为 20SPS 或更低时，滤波器将滤除 50Hz 和 60Hz 干扰。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS1148-Q1	TSSOP (28)	9.70mm x 4.40mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

功能方框图



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4 修订历史

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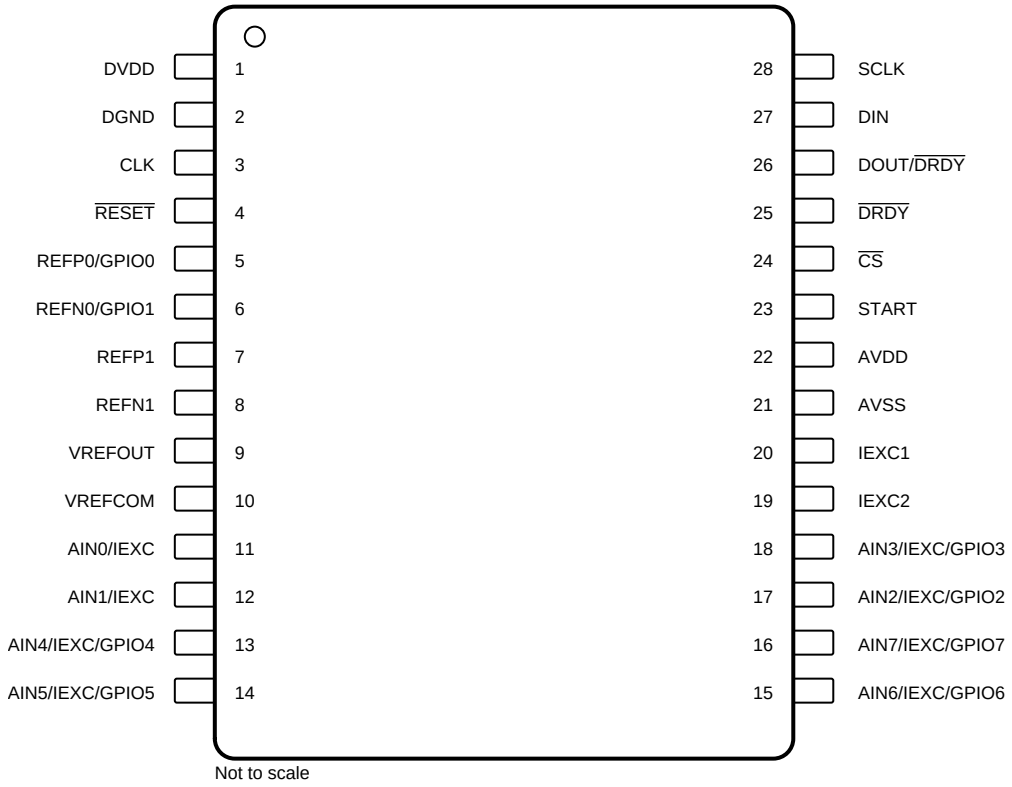
5 Pin Configuration and Functions

PW Package
28-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
AIN0/IEXC	11	I	Analog input 0, optional excitation current output
AIN1/IEXC	12	I	Analog input 1, optional excitation current output
AIN2/IEXC/GPIO2	17	I/O	Analog input 2, optional excitation current output, or general-purpose digital input/output pin 2
AIN3/IEXC/GPIO3	18	I/O	Analog input 3, optional excitation current output, or general-purpose digital input/output pin 3
AIN4/IEXC/GPIO4	13	I/O	Analog input 4, optional excitation current output, or general-purpose digital input/output pin 4
AIN5/IEXC/GPIO5	14	I/O	Analog input 5, optional excitation current output, or general-purpose digital input/output pin 5
AIN6/IEXC/GPIO6	15	I/O	Analog input 6, optional excitation current output, or general-purpose digital input/output pin 6
AIN7/IEXC/GPIO7	16	I/O	Analog input 7, optional excitation current output, or general-purpose digital input/output pin 7
AVDD	22	P	Positive analog power supply, connect a 0.1-µF capacitor to AVSS
AVSS	21	P	Negative analog power supply
CLK	3	I	External clock input, tie to DGND to activate the internal oscillator
$\overline{CS}$	24	I	Chip select (active low)
DGND	2	G	Digital ground
DIN	27	I	Serial data input
DOUT/$\overline{DRDY}$	26	O	Serial data output, or data out combined with data ready
$\overline{DRDY}$	25	O	Data ready (active low)
DVDD	1	P	Digital power supply, connect a 0.1-µF capacitor to DGND
IEXC1	20	O	Excitation current output 1
IEXC2	19	O	Excitation current output 2
REFN0/GPIO1	6	I/O	Negative external reference input 0, or general-purpose digital input/output pin 1
REFN1	8	I	Negative external reference input 1
REFP0/GPIO0	5	I/O	Positive external reference input 0, or general-purpose digital input/output pin 1
REFP1	7	I	Positive external reference input 1
$\overline{RESET}$	4	I	Reset (active low)
SCLK	28	I	Serial clock input
START	23	I	Conversion start
VREFCOM	10	O	Negative internal reference voltage output, connect to AVSS when using a unipolar supply or to the mid-voltage ground when using a bipolar supply
VREFOUT	9	O	Positive internal reference voltage output, connect a capacitor in the range of 1 µF to 47 µF to VREFCOM

(1) G = ground, I = input, O = output, P = and power.
(2) See the *Unused Inputs and Outputs* section for unused pin connections.

6 Specifications

6.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AVSS	–0.3	5.5	V
	AVSS to DGND	–2.8	0.3	
	DVDD to DGND	–0.3	5.5	
Analog input voltage	AINx, REFPx, REFNx, VREFOUT, VREFCOM, IEXC1, IEXC2	AVSS – 0.3	AVDD + 0.3	V
Digital input voltage	SCLK, DIN, DOUT/$\overline{\text{DRDY}}$, $\overline{\text{DRDY}}$, $\overline{\text{CS}}$, START, $\overline{\text{RESET}}$, CLK	DGND – 0.3	DVDD + 0.3	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
	Momentary, any pin except power-supply pins	–100	100	
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AVSS	2.7		5.25	V
		AVSS to DGND	–2.65		0.1	
		AVDD to DGND	2.25		5.25	
	Digital power supply	DVDD to DGND	2.7		5.25	V
ANALOG INPUTS(1)						
V_{IN}	Differential input voltage	$V_{(AINP)} – V_{(AINN)}$(2)	$–V_{REF}$ / Gain		V_{REF} / Gain	V
V_{CM}	Common-mode input voltage	$(V_{(AINP)} + V_{(AINN)}) / 2$	See Equation 3			
VOLTAGE REFERENCE INPUTS(3)						
V_{REF}	Differential reference input voltage	$V_{(REFPx)} – V_{(REFNx)}$	0.5		(AVDD – AVSS) – 1	V
$V_{(REFNx)}$	Absolute negative reference voltage		AVSS – 0.1		$V_{(REFPx)}$ – 0.5	V
$V_{(REFPx)}$	Absolute positive reference voltage		$V_{(REFNx)}$ + 0.5		AVDD + 0.1	V
EXTERNAL CLOCK INPUT(4)						
f_{CLK}	External clock frequency		1		4.5	MHz
	External clock duty cycle		25%		75%	
GENERAL-PURPOSE INPUTS AND OUTPUTS (GPIO)						
	GPIO input voltage		AVSS		AVDD	V
DIGITAL INPUTS						
	Digital input voltage		DGND		DVDD	V
TEMPERATURE RANGE						
T_A	Operating ambient temperature		–40		125	°C

(1) AIN_P and AIN_N denote the positive and negative inputs of the PGA.
(2) For V_{REF} > 2.7 V, the differential input voltage must not exceed 2.7 V / Gain.
(3) REFPx and REFNx denote one of the two available differential reference input pairs.
(4) The external clock is only required if the internal oscillator is not used.

6.4 Thermal Information

THERMAL METRIC(1)		ADS1148-Q1 PW (TSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 5 V, DVDD = 3.3 V, AVSS = 0 V, V_{REF} = 2.048 V, and f_{CLK} = 4.096 MHz (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Differential input current			100		pA
	Absolute input current			See Table 4		
PGA						
	PGA gain settings			1, 2, 4, 8, 16, 32, 64, 128		V/V
SYSTEM PERFORMANCE						
	Resolution	No missing codes		16		Bits
DR	Data rate			5, 10, 20, 40, 80, 160, 320, 640, 1000, 2000		SPS
	ADC conversion time	Single-cycle settling		See Table 10		
INL	Integral nonlinearity	Differential input, end point fit, Gain = 1, V_{CM} = 2.5 V	–1	0.5	1	LSB
	Offset error	After calibration	–1		1	LSB
	Offset drift	Gain = 1		100		nV/°C
		Gain = 128		15		nV/°C
	Gain error	Excluding V_{REF} errors	–0.5%		0.5%	
	Gain drift	Gain = 1, excludes V_{REF} drift		1		ppm°C
		Gain = 128, excludes V_{REF} drift		–3.5		ppm/°C
	Noise			See Table 1 and Table 2		
NMRR	Normal mode rejection			See Table 6		
CMRR	Common-mode rejection ratio	At dc, gain = 1		90		dB
		At dc, gain = 32		100		
PSRR	Power-supply rejection ratio	AVDD, DVDD at dc		100		dB
VOLTAGE REFERENCE INPUTS						
	Reference input current			30		nA
INTERNAL VOLTAGE REFERENCE						
V_{REF}	Internal reference voltage		2.038	2.048	2.058	V
	Reference drift(1)	T_A = –40°C to +125°C		20	50	ppm/°C
	Output current(2)		–10		10	mA
	Load regulation			50		µV/mA
INTERNAL OSCILLATOR						
	Internal oscillator frequency		3.85	4.096	4.3	MHz
EXCITATION CURRENT SOURCES (IDACs)						
	Output current settings			50, 100, 250, 500, 750, 1000, 1500		µA
	Compliance voltage	All currents		See Figure 9 and Figure 10		
	Absolute error	All currents, each IDAC	–6%	±1%	6%	
	Absolute mismatch	All currents, between IDACs		±0.2%		
	Temperature drift	Each IDAC		200		ppm/°C
	Temperature drift matching	Between IDACs		10		ppm/°C
BURN-OUT CURRENT SOURCES						
	Burn-out current source settings			0.5, 2, 10		µA
BIAS VOLTAGE						
	Bias voltage			(AVDD + AVSS) / 2		V
	Bias voltage output impedance			400		Ω
TEMPERATURE SENSOR						
	Output voltage	T_A = 25°C		118		mV
	Temperature coefficient			405		µV/°C

(1) Specified by the combination of design and final production test.
(2) Do not exceed this loading on the internal voltage reference.

Electrical Characteristics (continued)

Minimum and maximum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at AVDD = 5 V, DVDD = 3.3 V, AVSS = 0 V, V_{REF} = 2.048 V, and f_{CLK} = 4.096 MHz (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL-PURPOSE INPUTS AND OUTPUTS (GPIO)						
V_{IL}	Low-level input voltage		AVSS		0.3 × AVDD	V
V_{IH}	High-level input voltage		0.7 × AVDD		AVDD	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	AVSS		0.2 × AVDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × AVDD			V
DIGITAL INPUTS AND OUTPUTS (OTHER THAN GPIO)						
V_{IL}	Low-level input voltage		DGND		0.3 × DVDD	V
V_{IH}	High-level input voltage		0.7 × DVDD		DVDD	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	DGND		0.2 × DVDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 × DVDD			V
	Input leakage	DGND < V_{IN} < DVDD	–10		10	µA
POWER SUPPLY						
I_{AVDD}	Analog supply current	Power-down mode		0.1		µA
		Converting, AVDD = 3.3 V, DR = 20 SPS, external reference		212		
		Converting, AVDD = 5 V, DR = 20 SPS, external reference		225		
		Additional current with internal reference enabled		180		
I_{DVDD}	Digital supply current	Power-down mode		0.2		µA
		Normal operation, DVDD = 3.3 V, DR = 20 SPS, internal oscillator		210		
		Normal operation, DVDD = 5 V, DR = 20 SPS, internal oscillator		230		
P_D	Power dissipation	AVDD = DVDD = 3.3 V, DR = 20 SPS, internal oscillator, external reference		1.4		mW
		AVDD = DVDD = 5 V, DR = 20 SPS, internal oscillator, external reference		2.3		

6.6 Timing Requirements

at T_A = –40°C to +125°C and DVDD = 2.7 V to 5.5 V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SERIAL INTERFACE (See Figure 1 and Figure 2)					
t_{CSSC}	Delay time, first SCLK rising edge after $\overline{CS}$ falling edge	10			ns
t_{SCCS}	Delay time, $\overline{CS}$ rising edge after final SCLK falling edge	7			t_{CLK} (1)
t_{CSPW}	Pulse duration, $\overline{CS}$ high	7			t_{CLK}
t_{SCLK}	SCLK period	488			ns
				64	Conversions
t_{SPWH}	Pulse duration, SCLK high	0.3		0.7	t_{SCLK}
t_{SPWL}	Pulse duration, SCLK low	0.3		0.7	t_{SCLK}
t_{DIST}	Setup time, DIN valid before SCLK falling edge	25			ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	25			ns
t_{STD}	Setup time, SCLK low before $\overline{DRDY}$ rising edge	7			t_{CLK}
t_{DTS}	Delay time, SCLK rising edge after $\overline{DRDY}$ falling edge	1			t_{CLK}
MINIMUM START TIME PULSE DURATION (See Figure 3)					
t_{START}	Pulse duration, START high	3			t_{CLK}
RESET PULSE DURATION, SERIAL INTERFACE COMMUNICATION AFTER RESET (See Figure 4)					
$t_{\overline{RESET}}$	Pulse duration, $\overline{RESET}$ low	4			t_{CLK}
t_{RHSC}	Delay time, SCLK rising edge (start of serial interface communication) after $\overline{RESET}$ rising edge	0.6 (2)			ms

(1) t_{CLK} = 1 / f_{CLK}. The default clock frequency f_{CLK} = 4.096 MHz.
(2) Applicable only when f_{CLK} = 4.096 MHz, scales proportionally with f_{CLK} frequency.

6.7 Switching Characteristics

at T_A = –40°C to +125°C and DVDD = 2.7 V to 5.5 V (unless otherwise noted); see Figure 1 and Figure 2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DOPD}	Propagation delay time, SCLK rising edge to valid new DOUT	DVDD ≤ 3.6 V			50	ns
		DVDD > 3.6 V			180	
t_{DOHD}	DOUT hold time		0			ns
t_{CSDO}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance				25	ns
t_{PWH}	Pulse duration, $\overline{DRDY}$ high		3			t_{CLK}

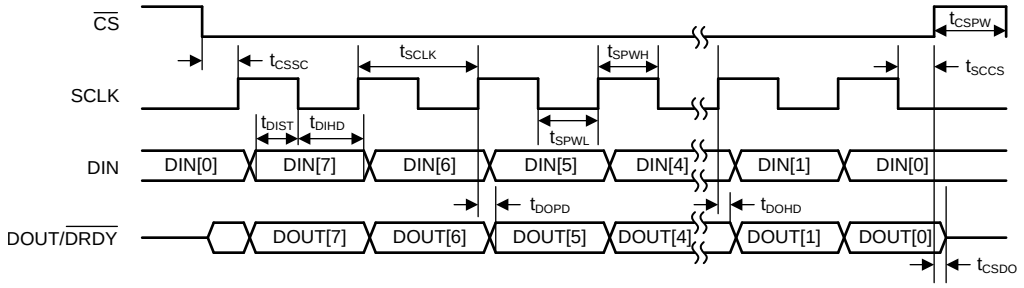
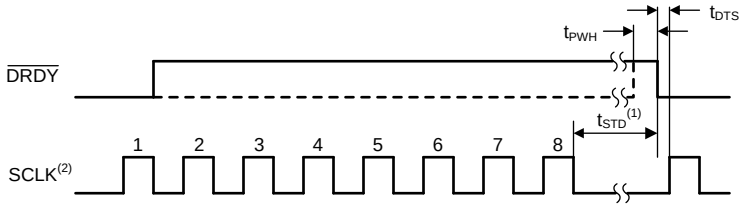


Figure 1. Serial Interface Timing, DRDY MODE Bit = 0



(1) This timing diagram is applicable only when the $\overline{CS}$ pin is low. SCLK does not need to be low during t_{STD} when $\overline{CS}$ is high.

(2) SCLK must only be sent in multiples of eight during partial retrieval of output data.

Figure 2. Serial Interface Timing to Allow Conversion Result Loading

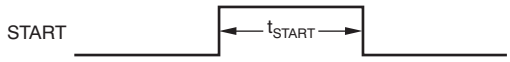


Figure 3. Minimum Start Pulse Duration

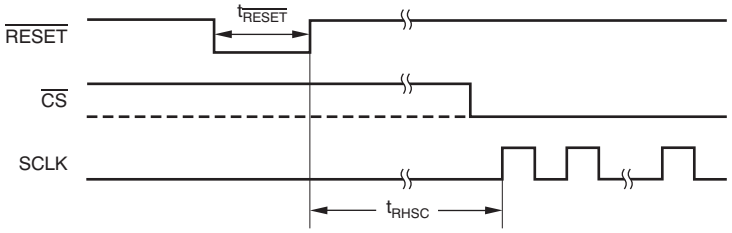


Figure 4. Reset Pulse Duration and Serial Interface Communication After Reset

6.8 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V and V_{REF} = 2.5 V (unless otherwise noted)

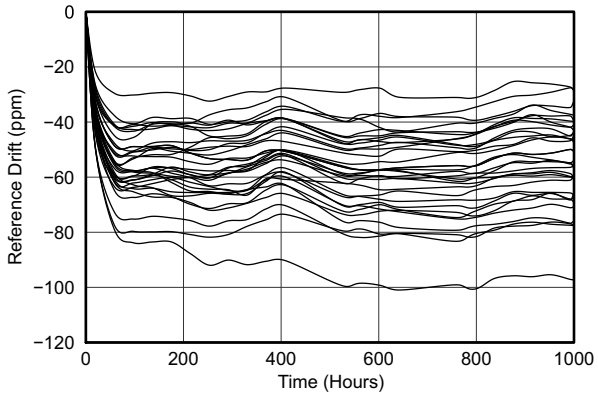


Figure 5. Internal Reference Long-Term Drift

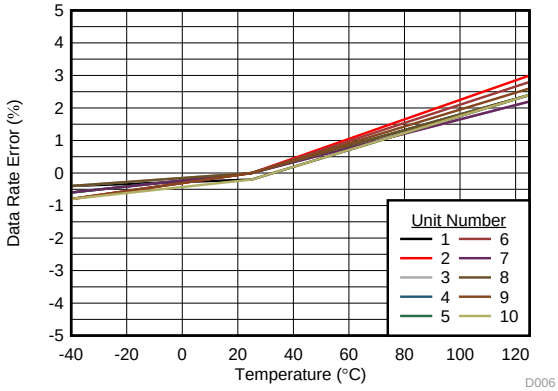


Figure 6. Data Rate Error vs Temperature

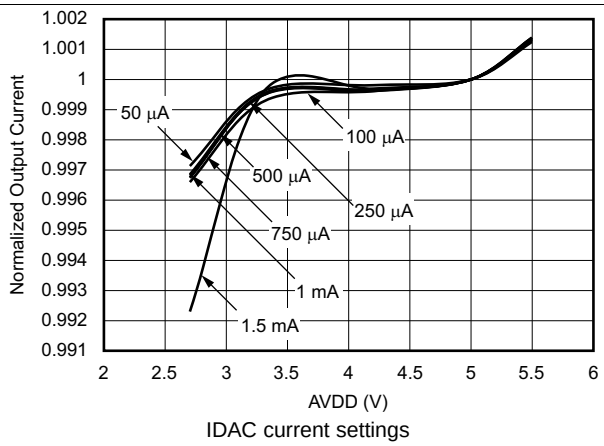


Figure 7. IDAC Line Regulation

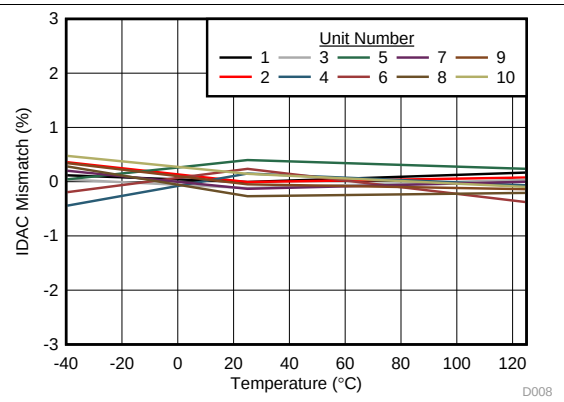


Figure 8. IDAC Drift

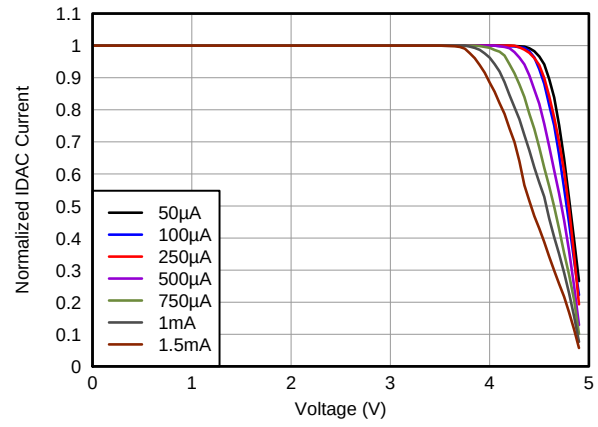


Figure 9. IDAC Voltage Compliance

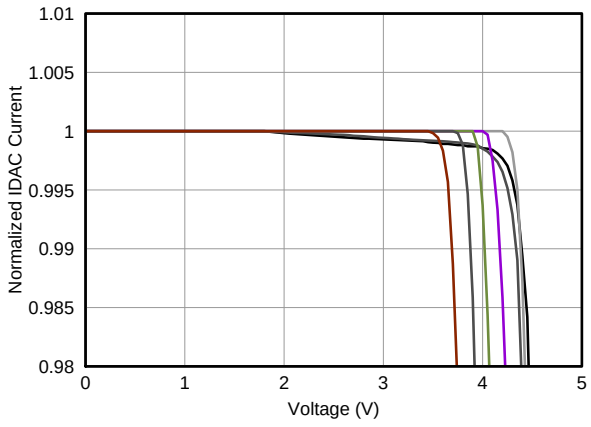


Figure 10. IDAC Voltage Compliance

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V and V_{REF} = 2.5 V (unless otherwise noted)

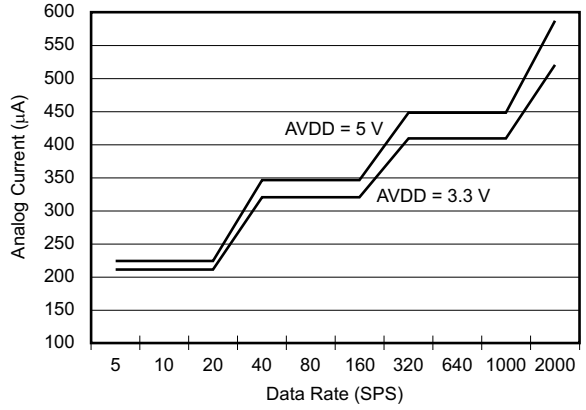


Figure 11. Analog Supply Current vs Data Rate

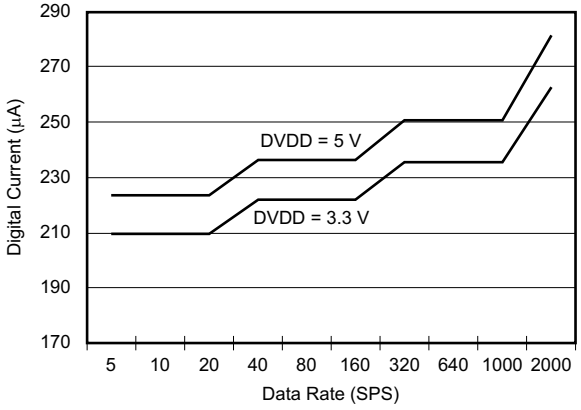


Figure 12. Digital Supply Current vs Data Rate

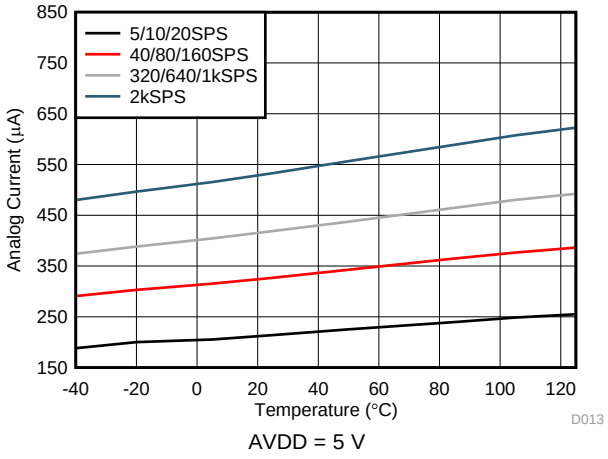


Figure 13. Analog Supply Current vs Temperature

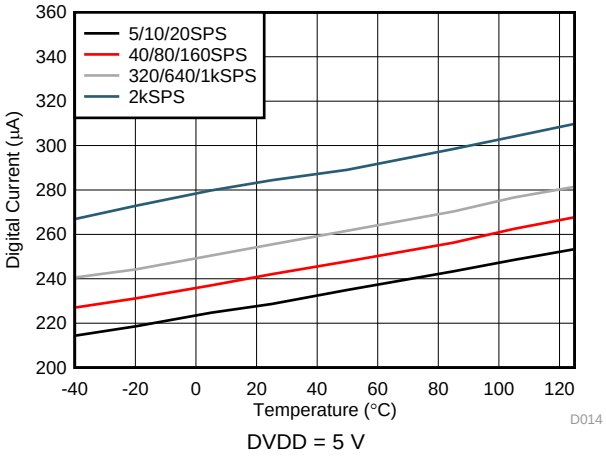


Figure 14. Digital Supply Current vs Temperature

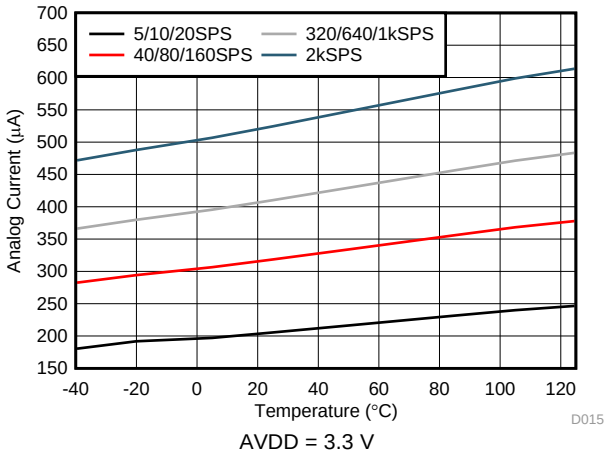


Figure 15. Analog Supply Current vs Temperature

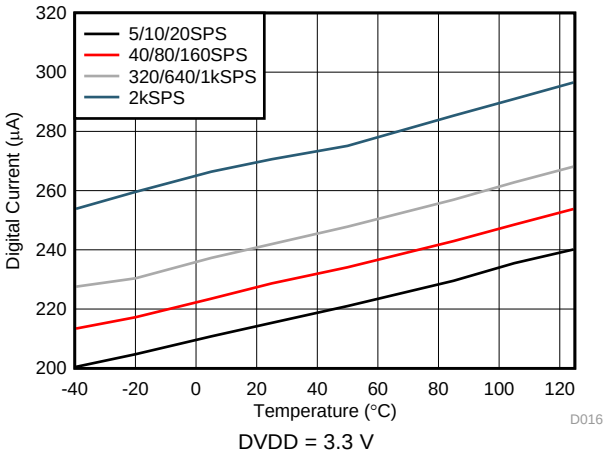


Figure 16. Digital Supply Current vs Temperature

7 Parameter Measurement Information

7.1 Noise Performance

The ADC noise performance is optimized by adjusting the data rate and PGA setting. Generally, the lowest input-referred noise is achieved using the highest gain possible, consistent with the input signal range. Do not set the gain too high or the result is an ADC overrange. Noise also depends on the output data rate. When the data rate reduces, the ADC bandwidth correspondingly reduces. This reduction in total bandwidth results in lower overall noise. Table 1 and Table 2 summarize the noise performance of the device. The data are representative of typical noise performance at T_A = 25°C. The data shown are the result of averaging the readings from multiple devices and were measured with the inputs shorted together.

Table 1 lists the input-referred noise in units of μV_{PP} for the conditions shown. Table 2 lists the corresponding data in units of effective number of bits (ENOB), where ENOB for the peak-to-peak noise is defined in Equation 1.

$$ENOB = \ln((2 \times V_{REF} / Gain) / V_{NPP}) / \ln(2) \quad (1)$$

where

- V_{NPP} is the input-referred peak-to-peak noise voltage

Table 1. Noise in μV_{PP}
At V_{REF} = 2.048 V, AVDD = 5 V, AVSS = 0 V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	0.98(1)	0.49(1)
10	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	0.98(1)	0.49(1)
20	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	0.98(1)	0.55
40	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	0.98(1)	0.75
80	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	1.09	0.98
160	62.5(1)	31.25(1)	15.63(1)	7.81(1)	3.91(1)	1.95(1)	1.88	1.57
320	62.5(1)	35.3	17.52	8.86	4.35	3.03	2.44	2.34
640	93.06	45.2	18.73	12.97	6.51	4.2	3.69	3.5
1000	284.59	129.77	61.3	33.04	16.82	9.08	5.42	4.65
2000	273.39	130.68	67.13	36.16	19.22	9.87	6.93	6.48

(1) Peak-to-peak noise rounded up to 1 LSB.

Table 2. Effective Number of Bits From Peak-to-Peak Noise
At V_{REF} = 2.048 V, AVDD = 5 V, AVSS = 0 V

DATA RATE (SPS)	PGA SETTING							
	1	2	4	8	16	32	64	128
5	16	16	16	16	16	16	16	16
10	16	16	16	16	16	16	16	16
20	16	16	16	16	16	16	16	15.8
40	16	16	16	16	16	16	16	15.4
80	16	16	16	16	16	16	15.8	15
160	16	16	16	16	16	16	15.1	14.3
320	16	15.8	15.8	15.8	15.8	15.4	14.7	13.7
640	15.4	15.5	15.7	15.3	15.3	14.9	14.1	13.2
1000	13.8	13.9	14	13.9	13.9	13.8	13.5	12.7
2000	13.9	13.9	13.9	13.8	13.7	13.7	13.2	12.3

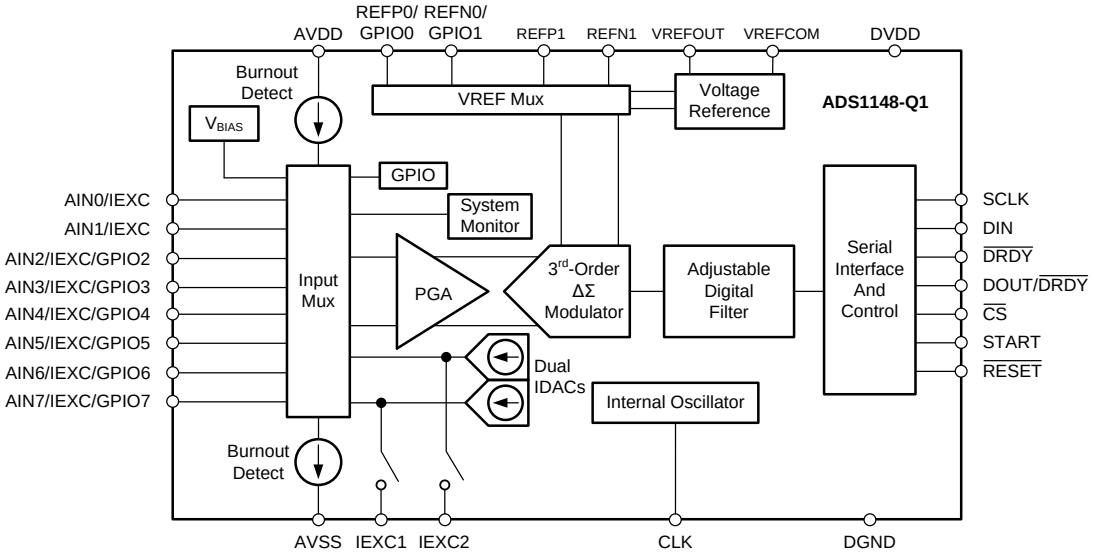
8 Detailed Description

8.1 Overview

The ADS1148-Q1 includes a low-noise, high-input impedance programmable gain amplifier (PGA), a delta-sigma (ΔΣ) analog-to-digital converter (ADC) with an adjustable single-cycle settling digital filter, an internal oscillator, and an SPI-compatible serial interface.

The ADS1148-Q1 also includes a flexible input multiplexer with system monitoring capability and general-purpose I/O settings, a low-drift voltage reference, and two matched current sources for sensor excitation. The *Functional Block Diagram* section shows the various functions incorporated into ADS1148-Q1.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ADC Input and Multiplexer

The ADC measures the input signal through the onboard PGA. All analog inputs are connected to the internal AIN_P or AIN_N analog inputs through the analog multiplexer. Figure 17 shows a block diagram of the analog input multiplexer.

The input multiplexer connects to eight analog inputs. Any analog input pin can be selected as the positive input or negative input through the MUX0 register. The multiplexer also allows the on-chip excitation current and bias voltage to be selected to a specific channel.

Through the input multiplexer, the ambient temperature (internal temperature sensor), AVDD, DVDD, and the external reference can all be selected for measurement. See the *System Monitor* section for more details.

The analog inputs can also be configured as general-purpose inputs and outputs (GPIOs). See the *General-Purpose Digital I/O* section for more details.

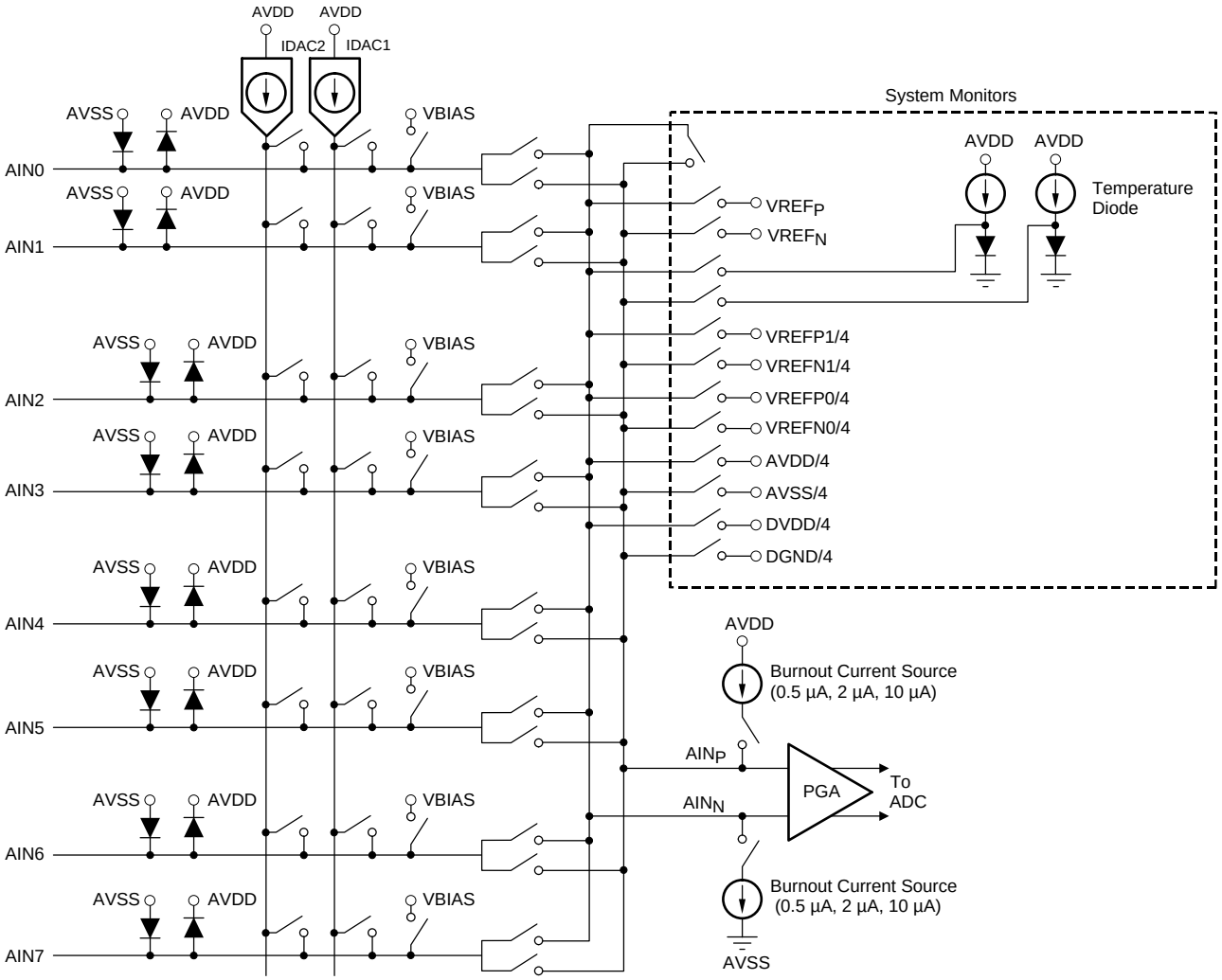


Figure 17. Analog Input Multiplexer Circuit

Feature Description (continued)

ESD diodes protect the ADC inputs. To prevent these diodes from turning on, make sure the voltages on the input pins do not go below AVSS by more than 100 mV, and do not exceed AVDD by more than 100 mV, as shown in Equation 2. Note that the same caution is true if the inputs are configured to be GPIOs.

$$AVSS - 100\ mV < V_{(AINX)} < AVDD + 100\ mV \quad (2)$$

8.3.2 Low-Noise PGA

The ADS1148-Q1 features a low-drift, low-noise, high input impedance programmable gain amplifier (PGA). The PGA can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128 by the SYS0register. Figure 18 shows a simplified diagram of the PGA.

The PGA consists of two chopper-stabilized amplifiers (A1 and A2) and a resistor feedback network that sets the gain of the PGA. The PGA input is equipped with an electromagnetic interference (EMI) filter, as shown in Figure 18. As with any PGA, ensure that the input voltage stays within the specified common-mode input range. The common-mode input (V_{CM}) must be within the range shown in Equation 3.

$$\left(AVSS + 0.1\,V + \frac{V_{IN(MAX)} \cdot Gain}{2}\right) \le V_{CM} \le \left(AVDD - 0.1\,V - \frac{V_{IN(MAX)} \cdot Gain}{2}\right) \quad (3)$$

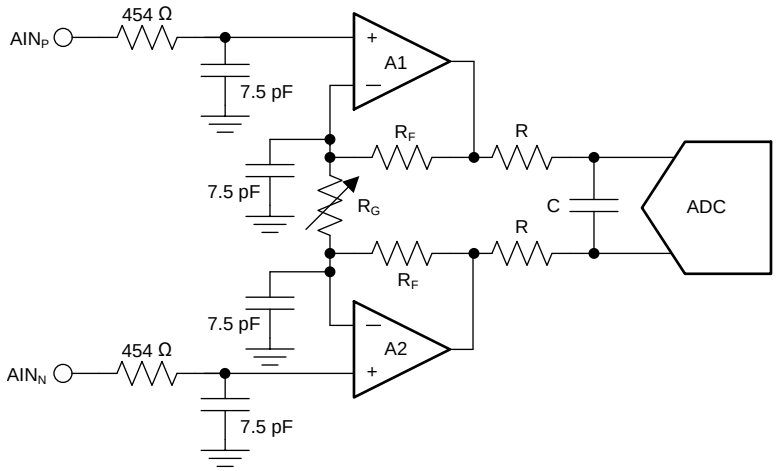


Figure 18. Simplified Diagram of the PGA

Gain is changed inside the device using a variable resistor, R_G. The differential full-scale input voltage range (FSR) of the PGA is defined by the gain setting and the reference voltage used, as shown in Equation 4.

$$FSR = \pm V_{REF} / Gain \quad (4)$$

Table 3 shows the corresponding full-scale input ranges when using the internal 2.048-V reference.

Table 3. PGA Full-Scale Range

PGA GAIN SETTING	FSR
1	±2.048 V
2	±1.024 V
4	±0.512 V
8	±0.256 V
16	±0.128 V
32	±0.064 V
64	±0.032 V
128	±0.016 V

8.3.2.1 PGA Common-Mode Voltage Requirements

To stay within the linear operating range of the PGA, the input signals must meet certain requirements that are discussed in this section.

The outputs of both amplifiers (A1 and A2) in Figure 18 cannot swing closer to the supplies (AVSS and AVDD) than 100 mV. If the outputs OUT_P and OUT_N are driven to within 100 mV of the supply rails, the amplifiers saturate and consequently become nonlinear. To prevent this nonlinear operating condition, the output voltages must meet Equation 5.

$$AVSS + 0.1\ V \le V_{(OUTN)},\ V_{(OUTP)} \le AVDD - 0.1\ V \quad (5)$$

Translating the requirements of Equation 5 into requirements referred to the PGA inputs (AIN_P and AIN_N) is beneficial because there is no direct access to the outputs of the PGA. The PGA employs a symmetrical design; therefore, the common-mode voltage at the output of the PGA can be assumed to be the same as the common-mode voltage of the input signal, as shown in Figure 19.

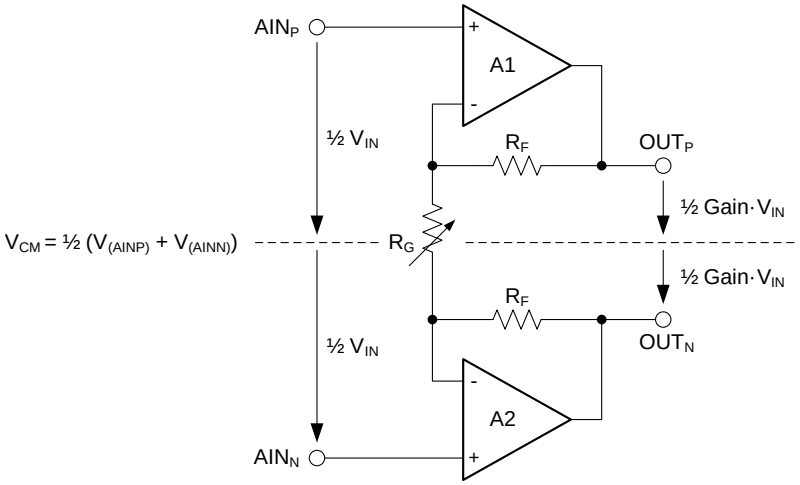


Figure 19. PGA Common-Mode Voltage

The common-mode voltage is calculated using Equation 6.

$$V_{CM} = ½\ (V_{(AINP)} + V_{(AINN)}) = ½\ (V_{(OUTP)} + V_{(OUTN)}) \quad (6)$$

The voltages at the PGA inputs (AIN_P and AIN_N) can be expressed as Equation 7 and Equation 8.

$$V_{(AINP)} = V_{CM} + ½\ V_{IN} \quad (7)$$

$$V_{(AINN)} = V_{CM} - ½\ V_{IN} \quad (8)$$

The output voltages ($V_{(OUTP)}$ and $V_{(OUTN)}$) can then be calculated as Equation 9 and Equation 10.

$$V_{(OUTP)} = V_{CM} + ½\ Gain \times V_{IN} \quad (9)$$

$$V_{(OUTN)} = V_{CM} - ½\ Gain \times V_{IN} \quad (10)$$

The requirements for the output voltages of amplifiers A1 and A2 (Equation 5) can now be translated into requirements for the input common-mode voltage range using Equation 9 and Equation 10, which are given in Equation 11 and Equation 12.

$$V_{CM\ (MIN)} \ge AVSS + 0.1\ V + ½\ Gain \times V_{IN\ (MAX)} \quad (11)$$

$$V_{CM\ (MAX)} \le AVDD - 0.1\ V - ½\ Gain \times V_{IN\ (MAX)} \quad (12)$$

To calculate the minimum and maximum common-mode voltage limits, the maximum differential input voltage ($V_{IN\ (MAX)}$) that occurs in the application must be used. $V_{IN\ (MAX)}$ can be less than the maximum possible full-scale value.

8.3.2.2 PGA Common-Mode Voltage Calculation Example

The following paragraphs explain how to apply Equation 11 and Equation 12 to a hypothetical application. The setup for this example is AVDD = 3.3 V, AVSS = 0 V, and gain = 16, using an external reference of V_{REF} = 2.5 V. The maximum possible differential input voltage $V_{IN} = (V_{(AINP)} – V_{(AINN)})$ that can be applied is then limited to the full-scale range of FSR = ±2.5 V / 16 = ±0.156 V. Consequently, Equation 11 and Equation 12 yield an allowed V_{CM} range of 1.35 V ≤ V_{CM} ≤ 1.95 V.

If the sensor signal connected to the inputs in this hypothetical application does not make use of the entire full-scale range but is limited to $V_{IN\ (MAX)}$ = ±0.1 V, for example, then this reduced input signal amplitude relaxes the V_{CM} restriction to 0.9 V ≤ V_{CM} ≤ 2.4 V.

In the case of a fully differential sensor signal, each input (AIN_P, AIN_N) can swing up to ±50 mV around the common-mode voltage ($V_{(AINP)}$ + $V_{(AINN)}$) / 2, which must remain between the limits of 0.9 V and 2.4 V. The output of a symmetrical wheatstone bridge is an example of a fully differential signal. Figure 20 shows a situation where the common-mode voltage of the input signal is at the lowest limit. $V_{(OUTN)}$ is exactly at 0.1 V in this case. Any further decrease in common-mode voltage (V_{CM}) or increase in differential input voltage (V_{IN}) drives $V_{(OUTN)}$ below 0.1 V and saturates amplifier A2.

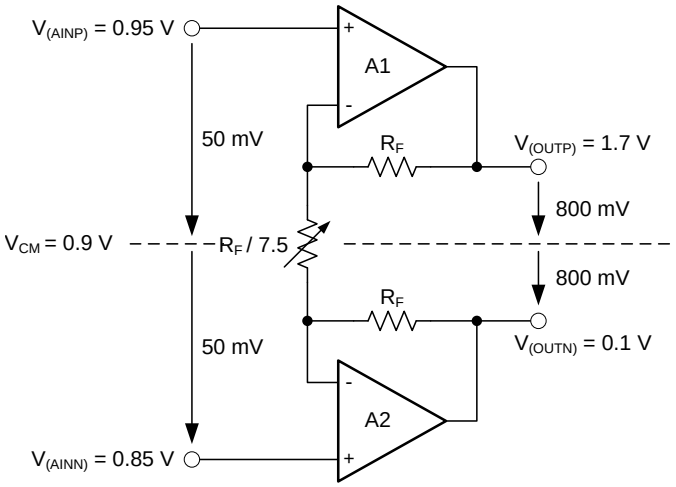


Figure 20. Example Where V_{CM} is at the Lowest Limit

In contrast, the signal of a resistance temperature detector (RTD) is of a pseudo-differential nature (if implemented as in the *3-Wire RTD Measurement System* section), where the negative input is held at a constant voltage other than 0 V and only the voltage on the positive input changes. When a pseudo-differential signal must be measured, the negative input in this example must be biased at a voltage from 0.85 V to 2.35 V. The positive input can then swing up to $V_{IN\ (MAX)}$ = 100 mV above the negative input. In this case, the common-mode voltage changes at the same time that the voltage on the positive input changes. That is, when the input signal swings between 0 V ≤ V_{IN} ≤ $V_{IN\ (MAX)}$, the common-mode voltage swings between $V_{(AINN)}$ ≤ V_{CM} ≤ $V_{(AINN)}$ + ½ $V_{IN\ (MAX)}$. Satisfying the common-mode voltage requirements for the maximum input voltage $V_{IN\ (MAX)}$ ensures the requirements are met throughout the entire signal range.

Figure 21 and Figure 22 show examples of both fully differential and pseudo-differential signals, respectively.

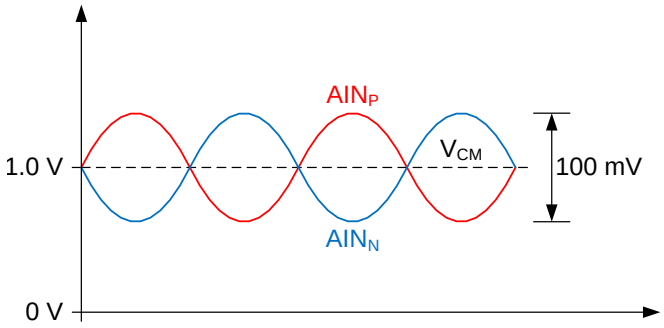


Figure 21. Fully Differential Input Signal

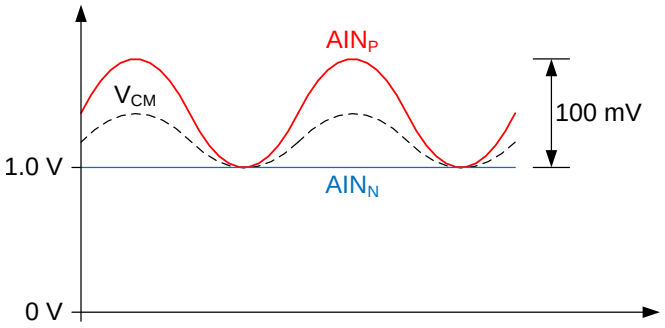


Figure 22. Pseudo-Differential Input Signal

NOTE

With a unipolar power supply, the input range does not extend to the ground. Equation 11 and Equation 12 show the common-mode voltage requirements.

- $V_{CM\ (MIN)} \geq AVSS + 0.1\ V + ½\ Gain \times V_{IN\ (MAX)}$
- $V_{CM\ (MAX)} \leq AVDD - 0.1\ V - ½\ Gain \times V_{IN\ (MAX)}$

8.3.2.3 Analog Input Impedance

The device inputs are buffered through a high-input impedance PGA before reaching the ΔΣ modulator. For the majority of applications, the input current is minimal and can be neglected. However, because the PGA is chopper-stabilized for noise and offset performance, the input impedance is best described as a small absolute input current. The absolute input current for selected channels is approximately proportional to the selected modulator clock. Table 4 shows the typical values for these currents with a differential voltage coefficient and the corresponding input impedances over data rate.

Table 4. Typical Values for Analog Input Current Over Data Rate(1)

CONDITION	ABSOLUTE INPUT CURRENT	EFFECTIVE INPUT IMPEDANCE
DR = 5 SPS, 10 SPS, 20 SPS	± (0.5 nA + 0.1 nA/V)	5000 MΩ
DR = 40 SPS, 80 SPS, 160 SPS	± (2 nA + 0.5 nA/V)	1200 MΩ
DR = 320 SPS, 640 SPS, 1 kSPS	± (4 nA + 1 nA/V)	600 MΩ
DR = 2 kSPS	± (8 nA + 2 nA/V)	300 MΩ

(1) Input current with V_{CM} = 2.5 V, T_A = 25°C, AVDD = 5 V, and AVSS = 0 V.

8.3.3 Clock Source

The device can use either the internal oscillator or an external clock. Connect the CLK pin to DGND before power-on or reset to activate the internal oscillator. Connecting an external clock to the CLK pin at any time deactivates the internal oscillator, with the device then operating on the external clock. After switching to the external clock, the device cannot be switched back to the internal oscillator without cycling the power supplies or resetting the device.

8.3.4 Modulator

A third-order, delta-sigma modulator is used in the ADS1148-Q1. The modulator converts the analog input voltage into a pulse code modulated (PCM) data stream. To save power, the modulator clock runs from 32 kHz up to 512 kHz for different data rates, as shown in Table 5.

Table 5. Modulator Clock Frequency for Different Data Rates

DATA RATE (SPS)	MODULATOR RATE (f_{MOD})(1) (kHz)	f_{CLK} / f_{MOD}
5, 10, 20	32	128
40, 80, 160	128	32
320, 640, 1000	256	16
2000	512	8

(1) When using the internal oscillator or an external 4.096-MHz clock.

8.3.5 Digital Filter

The ADC uses linear-phase finite impulse response (FIR) digital filters that can be adjusted for different output data rates. The digital filter always settles in a single cycle.

Table 6 shows the exact data rates when an external clock equal to 4.096 MHz is used. Also shown is the signal –3-dB bandwidth, and the 50-Hz and 60-Hz attenuation. For good 50-Hz or 60-Hz rejection, use a data rate of 20 SPS or slower.

The frequency responses of the digital filter are illustrated in Figure 23 to Figure 33. Figure 26 illustrates a detailed view of the filter frequency response from 48 Hz to 62 Hz for a 20-SPS data rate. All filter plots are generated with a 4.096-MHz external clock.

Data rates and digital filter frequency responses scale proportionally with changes in the system clock frequency. The internal oscillator frequency has a variation, as specified in the *Electrical Characteristics* section, that also affects data rates and the digital filter frequency response.

Table 6. Digital Filter Specifications(1)

NOMINAL DATA RATE	ACTUAL DATA RATE	–3-dB BANDWIDTH	ATTENUATION			
			f_{IN} = 50 Hz ±0.3 Hz	f_{IN} = 60 Hz ±0.3 Hz	f_{IN} = 50 Hz ±1 Hz	f_{IN} = 60 Hz ±1 Hz
5 SPS	5.018 SPS	2.26 Hz	–106 dB	–74 dB	–81 dB	–69 dB
10 SPS	10.037 SPS	4.76 Hz	–106 dB	–74 dB	–80 dB	–69 dB
20 SPS	20.075 SPS	14.8 Hz	–71 dB	–74 dB	–66 dB	–68 dB
40 SPS	40.15 SPS	9.03 Hz	—	—	—	—
80 SPS	80.301 SPS	19.8 Hz	—	—	—	—
160 SPS	160.6 SPS	118 Hz	—	—	—	—
320 SPS	321.608 SPS	154 Hz	—	—	—	—
640 SPS	643.21 SPS	495 Hz	—	—	—	—
1000 SPS	1000 SPS	732 Hz	—	—	—	—
2000 SPS	2000 SPS	1465 Hz	—	—	—	—

(1) Values shown are for f_{CLK} = 4.096 MHz.

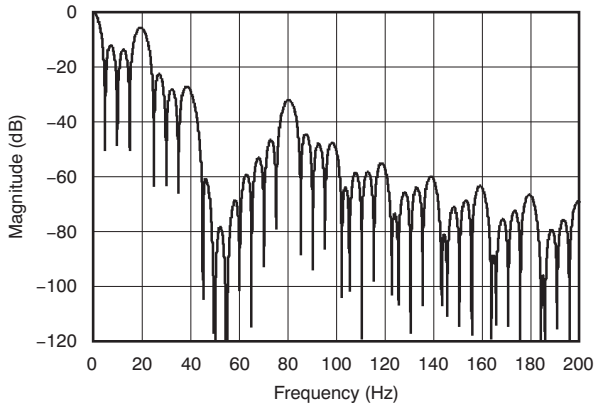


Figure 23. Filter Profile With Data Rate = 5 SPS

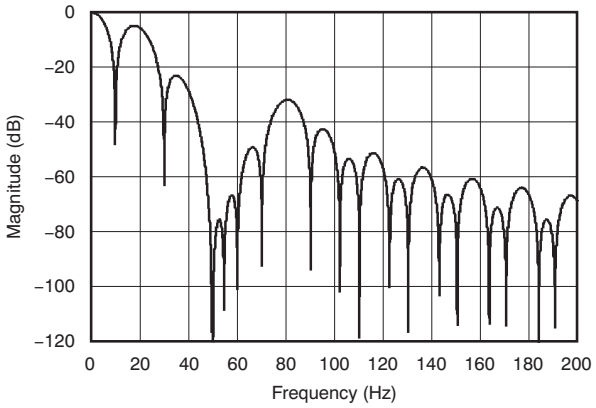


Figure 24. Filter Profile With Data Rate = 10 SPS

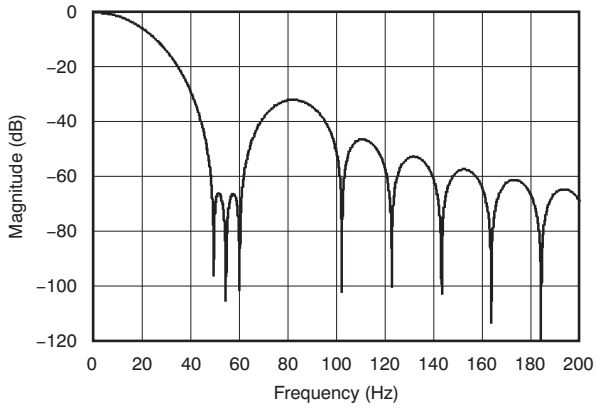


Figure 25. Filter Profile With Data Rate = 20 SPS

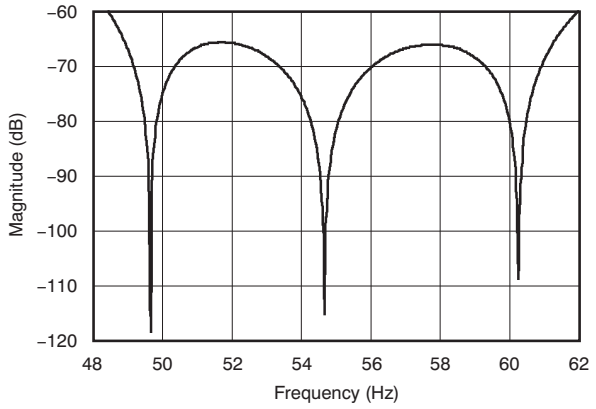


Figure 26. Detailed View of Filter Profile With Data Rate = 20 SPS Between 48 Hz and 62 Hz

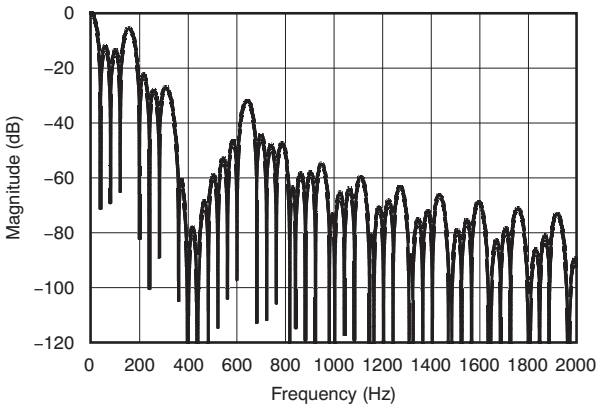


Figure 27. Filter Profile With Data Rate = 40 SPS

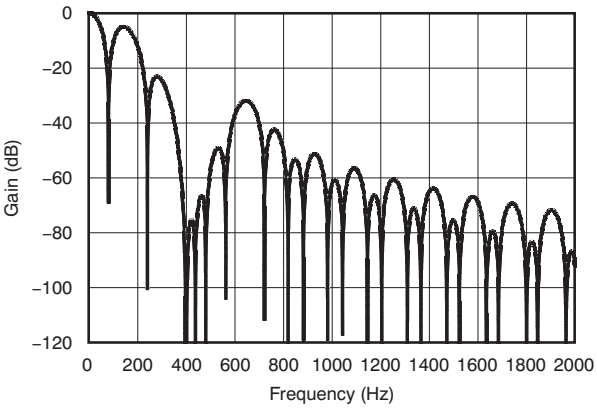


Figure 28. Filter Profile With Data Rate = 80 SPS

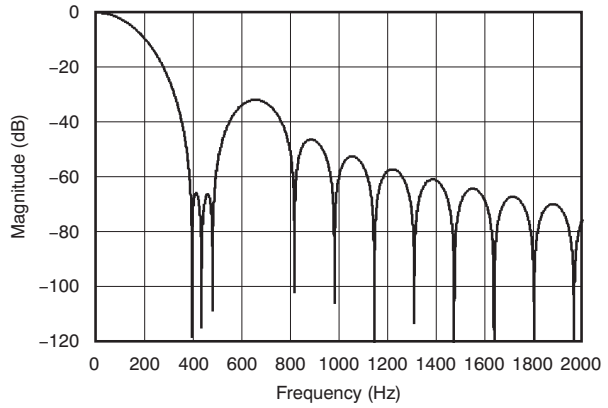


Figure 29. Filter Profile With Data Rate = 160 SPS

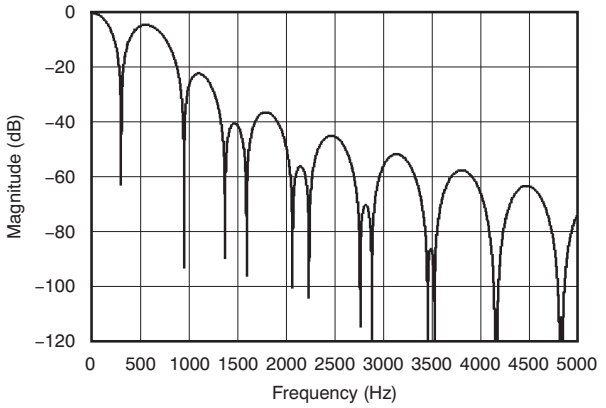


Figure 30. Filter Profile With Data Rate = 320 SPS

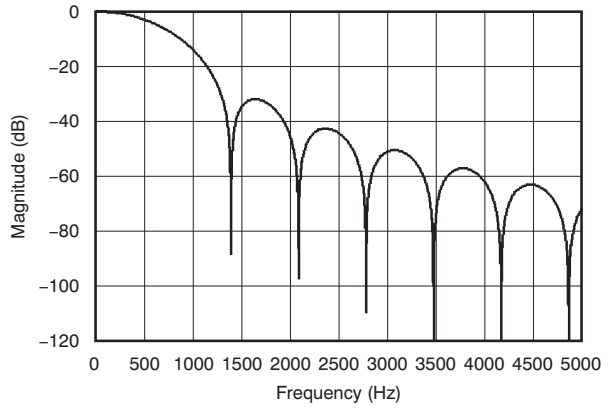


Figure 31. Filter Profile With Data Rate = 640 SPS

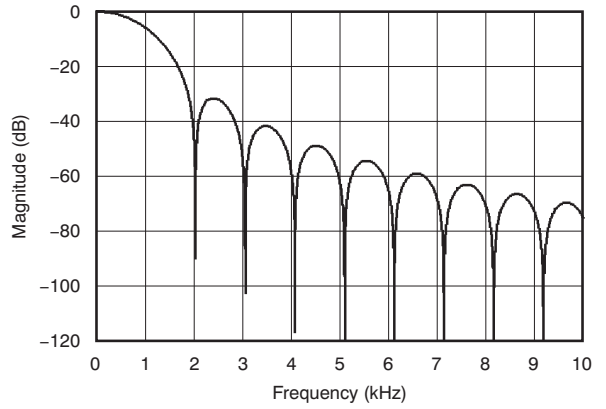


Figure 32. Filter Profile With Data Rate = 1 kSPS

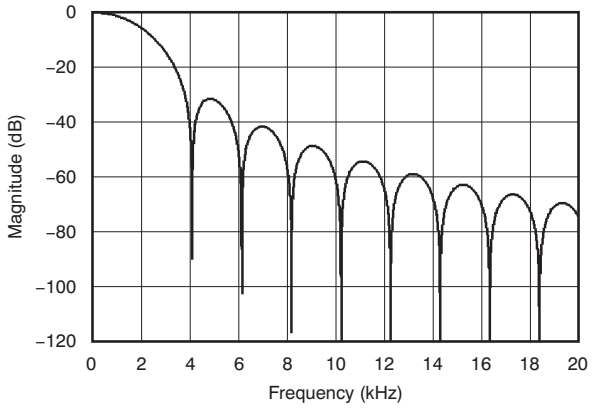


Figure 33. Filter Profile With Data Rate = 2 kSPS

8.3.6 Voltage Reference Input

The voltage reference for the device is the differential voltage between REFP and REFN, given by Equation 13.

$$V_{REF} = V_{(REFP)} - V_{(REFN)} \quad (13)$$

The ADS1148-Q1 has a multiplexer that selects the reference inputs, as shown in Figure 34. The reference inputs use buffers to increase the input impedance.

As with the analog inputs, REFP0 and REFN0 can also be configured as digital I/Os.

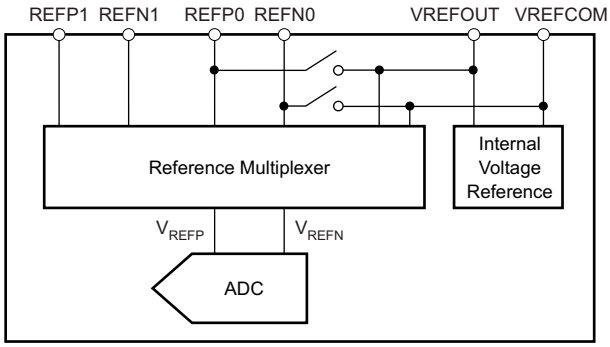


Figure 34. Reference Input Multiplexer

The reference input circuit has ESD diodes to protect the inputs. To prevent the diodes from turning on, make sure the voltage on the reference input pin is not less than AVSS – 100 mV, and does not exceed AVDD + 100 mV, as shown in Equation 14.

$$AVSS - 100\ mV < (V_{(REFP)} \text{ or } V_{(REFN)}) < AVDD + 100\ mV \quad (14)$$

8.3.7 Internal Voltage Reference

The ADS1148-Q1 has an internal voltage reference with a low temperature coefficient. The output of the voltage reference is 2.048 V (nominal) with the capability of both sourcing and sinking up to 10 mA of current.

The voltage reference must have a capacitor connected between VREFOUT and VREFCOM. The value of the capacitance must be in the range of 1 µF to 47 µF. Large values provide more filtering of the reference; however, the turn-on time increases with capacitance, as shown in Table 7. For stability reasons, VREFCOM must have a low-impedance path to an ac ground node. VREFCOM can be connected to AVSS (for a ±2.5-V analog power supply) as long as AVSS has a low-impedance path less than 10 Ω to an ac ground. In case this impedance is higher than 10 Ω, connect a capacitor of at least 0.1 µF between VREFCOM and the ac ground node.

NOTE

Take care when the device is turned off between conversions because time is required for the voltage reference to settle to the final voltage. Allow adequate time for the internal reference to fully settle before starting a new conversion.

Table 7. Internal Reference Settling Time

VREFOUT CAPACITOR	SETTLING ERROR	TIME TO REACH THE SETTLING ERROR
1 µF	±0.5%	70 µs
	±0.1%	110 µs
4.7 µF	±0.5%	290 µs
	±0.1%	375 µs
47 µF	±0.5%	2.2 ms
	±0.1%	2.4 ms

The internal reference is controlled by the MUX1 register; by default, the internal reference is off after power up (see the *Detailed Register Definitions* section for more details). Therefore, the internal reference must first be turned on and then connected through the internal reference multiplexer. The internal reference is used to generate the current reference for the excitation current sources and hence must be turned on before the excitation currents become available.

8.3.8 Excitation Current Sources

The ADS1148-Q1 provides two matched excitation current sources (IDACs) for RTD applications. For three-wire RTD applications, the matched current sources can be used to cancel the errors caused by sensor lead resistance. The output current of the IDACs can be programmed to 50 µA, 100 µA, 250 µA, 500 µA, 750 µA, 1000 µA, or 1500 µA.

The two matched current sources can be connected to the dedicated current output pins, IEXC1 and IEXC2; see the *Detailed Register Definitions* section for more information. Both current sources can be connected to the same pin. The internal reference must be turned on and the proper amount of capacitance applied to VREFOUT when using the excitation current sources.

8.3.9 Sensor Detection

To help detect a possible sensor malfunction, the device provides selectable current sources (0.5 µA, 2 µA, or 10 µA) to function as burn-out current sources. When enabled, one current source sources current to the selected positive analog input (AIN_P) and the other current source sinks current from the selected negative analog input (AIN_N).

In case of an open circuit in the sensor, these burn-out current sources pull the positive input towards AVDD and the negative input towards AVSS, resulting in a full-scale reading. A full-scale reading can also indicate that the sensor is overloaded or that the reference voltage is absent. A near-zero reading can indicate a shorted sensor. The absolute value of the burn-out current sources typically varies by ±10% and the internal multiplexer adds a small series resistance. Therefore, distinguishing a shorted sensor condition from a normal reading can be difficult, especially if an RC filter is used at the inputs. In other words, even if the sensor is shorted, the voltage drop across the external filter resistance and the residual resistance of the multiplexer causes the output to read a value higher than zero.

The ADC readings of a functional sensor can be corrupted when the burn-out current sources are enabled. The burn-out current sources are recommended to be disabled when performing a precision measurement, and are recommended to be enabled only to test for sensor fault conditions.

8.3.10 Bias Voltage Generation

A selectable bias voltage is provided for use with unbiased thermocouples. The bias voltage is (AVDD + AVSS) / 2 and can be applied to any analog input channel through the internal input multiplexer. Table 8 lists the bias voltage turn-on times for different sensor capacitances.

The internal bias voltage generator, when selected on multiple channels, causes the channels to be internally shorted. As a result, take care to limit the amount of current that can flow through the device. No more than 5 mA must be allowed to flow through this path, even if the device is in operation or powered down.

Table 8. Bias Voltage Settling Time

SENSOR CAPACITANCE	SETTLING TIME
0.1 µF	220 µs
1 µF	2.2 ms
10 µF	22 ms
200 µF	450 ms

8.3.11 General-Purpose Digital I/O

The ADS1148-Q1 has eight pins that serve a dual purpose as either analog inputs or GPIOs.

Three registers control the function of the GPIO pins. Use the GPIO configuration register (IOCFG) to enable a pin as a GPIO pin. The GPIO direction register (IODIR) configures the GPIO pin as either an input or an output. Finally, the GPIO data register (IODAT) contains the GPIO data. If a GPIO pin is configured as an input, the respective IODAT[x] bit reads the status of the pin; if a GPIO pin is configured as an output, write the output status to the respective IODAT[x] bit. For more information about the use of GPIO pins, see the *Detailed Register Definitions* section.

Figure 35 shows a diagram of how these functions are combined onto a single pin. Note that when the pin is configured as a GPIO, the corresponding logic is powered from AVDD and AVSS. When the ADS1148-Q1 is operated with bipolar analog supplies, the GPIO outputs bipolar voltages. Care must be taken during loading the GPIO pins when these pins are used as outputs because large currents can cause droop or noise on the analog supplies.

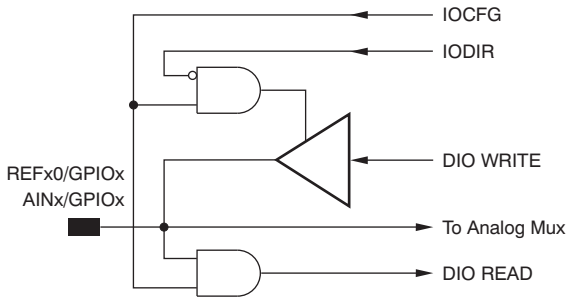


Figure 35. Analog and Data Interface Pin

8.3.12 System Monitor

The ADS1148-Q1 provides a system monitor function. This function can measure the analog power supply, digital power supply, external voltage reference, or ambient temperature. Note that the system monitor function provides a coarse result. When the system monitor is enabled, the analog inputs are disconnected.

8.3.12.1 Power-Supply Monitor

The system monitor can measure the analog or digital power supply. When measuring the power supply (V_{SP}), the resulting conversion is approximately 1/4 of the actual power supply voltage, as shown in Equation 15.

$$\text{Conversion Result} = (V_{SP} / 4) / V_{REF} \quad (15)$$

8.3.12.2 External Voltage Reference Monitor

The ADC can measure the external voltage reference. In this configuration, the monitored external voltage reference (V_{REX}) is connected to the analog input. The result (conversion code) is approximately 1/4 of the actual reference voltage, as shown in Equation 16.

$$\text{Conversion Result} = (V_{REX} / 4) / V_{REF} \quad (16)$$

NOTE

The internal reference voltage must be enabled when measuring an external voltage reference using the system monitor.

8.3.12.3 Ambient Temperature Monitor

On-chip diodes provide temperature-sensing capability. When selecting the temperature monitor function, the anodes of two diodes are connected to the ADC. Typically, the difference in diode voltage is 118 mV at T_A = 25°C with a temperature coefficient of 405 µV/°C.

8.4 Device Functional Modes

8.4.1 Power Up

When DVDD is powered up, the internal power-on reset module generates a pulse that resets all digital circuitry. All digital circuits are held in a reset state for 2^{16} system clocks to allow the analog circuits and the internal digital power supply to settle. SPI communication cannot occur until the internal reset is released.

8.4.2 Reset

When the $\overline{\text{RESET}}$ pin goes low, the device is immediately reset. All registers are restored to default values. The device stays in reset mode as long as the $\overline{\text{RESET}}$ pin stays low. When the $\overline{\text{RESET}}$ pin goes high, the ADC comes out of reset mode and is able to convert data. After the $\overline{\text{RESET}}$ pin goes high, the digital filter and the registers are held in a reset state for 0.6 ms when f_{CLK} = 4.096 MHz. Therefore, valid SPI communication can only be resumed 0.6 ms after the $\overline{\text{RESET}}$ pin goes high; see Figure 4. When the $\overline{\text{RESET}}$ pin goes low, the clock selection is reset to the internal oscillator.

A reset can also be performed by the RESET command through the serial interface and is functionally the same as using the $\overline{\text{RESET}}$ pin. For information about using the RESET command, see the *RESET* section.

8.4.3 Power-Down Mode

Power consumption is reduced to a minimum by placing the device into power-down mode. There are two ways to put the device into power-down mode: using the SLEEP command and taking the START pin low.

During power-down mode, the internal reference status depends on the setting of the VREFCON bits in the MUX1 register; see the *Register Maps* section for details.

8.4.4 Conversion Control

The START pin provides precise control of conversions. Pulse the START pin high to begin a conversion, as described in Figure 36 and Table 9. The conversion completion is indicated by the $\overline{\text{DRDY}}$ pin going low and with the DOUT/$\overline{\text{DRDY}}$ pin when the DRDY MODE bit is 1 in the IDAC0 register. When the conversion completes, the device automatically powers down. During power down, the conversion result can be retrieved; however, START must be taken high before communicating with the configuration registers. The device stays powered down until the START pin is returned high to begin a new conversion. When the START pin returns high, the decimation filter is held in a reset state for 32 modulator clock cycles internally to allow the analog circuits to settle.

Holding the START pin high configures the device to continuously convert; see Figure 37.

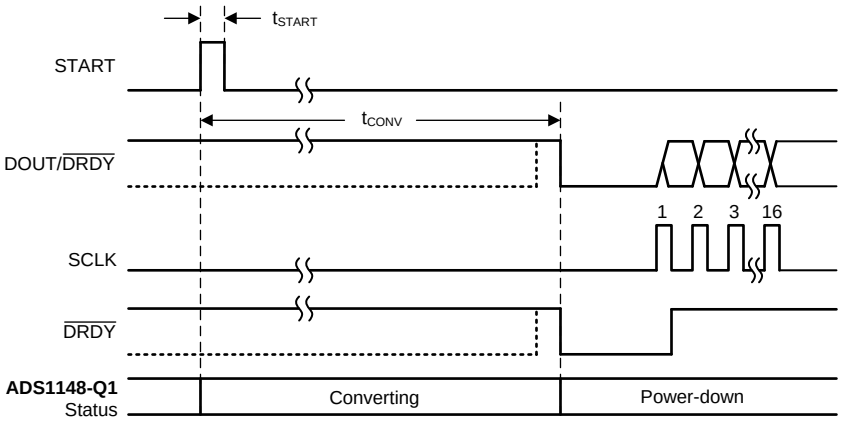
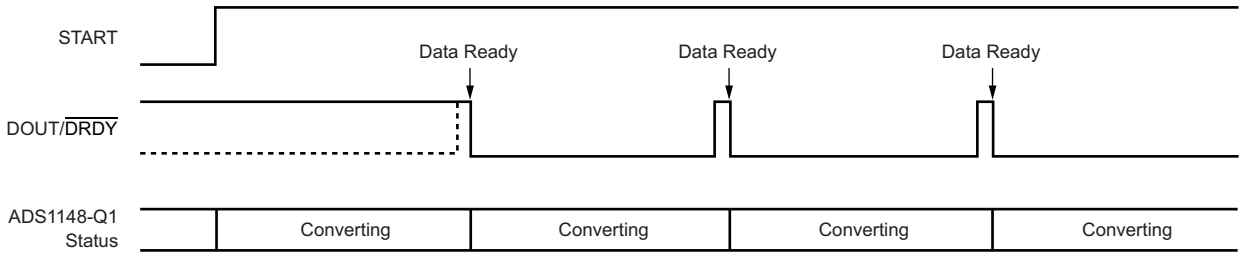


Figure 36. Timing for a Single Conversion Using the START Pin

Table 9. START Pin Conversion Times for Figure 36 (1)

PARAMETER		DATA RATE (SPS)	VALUE	UNIT
t_{CONV}	Time from START pulse to $\overline{DRDY}$ and DOUT/$\overline{DRDY}$ going low	5	200.295	ms
		10	100.644	ms
		20	50.825	ms
		40	25.169	ms
		80	12.716	ms
		160	6.489	ms
		320	3.247	ms
		640	1.692	ms
		1000	1.138	ms
		2000	0.575	ms

(1) For f_{CLK} = 4.096 MHz.



NOTE: SCLK is held low in this example.

Figure 37. Timing for Conversion with the START Pin High

With the START pin held high, the ADC converts the selected input channels continuously. This configuration continues until the START pin is taken low. The START pin can also be used to perform synchronized measurements for multichannel applications by pulsing the START pin. With multiple devices, if each device receives the START pin pulse at the same time, all devices start a conversion when the START pin rises. If all devices are operating with the same data rate, all devices complete the conversion at the same time.

Conversions can also be initiated through SPI commands. Similar to using the START pin, the device can be put into a power-down mode using the SLEEP command. Functionally, this mode is similar to taking the START pin low. To initiate a conversion, the WAKEUP command powers up the ADC and starts a conversion, similar to returning the START pin high. Note that the START pin must be held high to use commands to control conversions. Do not combine using the START pin and using commands to control conversions.

Furthermore, sending a SYNC command immediately starts a new ADC conversion. For the SYNC command, the digital filter is reset, starting a new conversion without completing the previous conversion. This process is useful in synchronizing conversions from multiple devices or for maintaining periodic timing from multiple channels.

Similarly, writing to any of the first four registers (MUX0, VBIAS, MUX1, or SYS0; addresses 00h to 04h) automatically resets the digital filter. A change in any of these registers makes the appropriate setup change in the device, but also restarts the conversion similar to a SYNC command.

8.4.4.1 Settling Time for Channel Multiplexing

The device is a true single-cycle settling $\Delta\Sigma$ converter. The first data available after the start of a conversion are fully settled and valid for use, provided that the input signal has settled to the final result. The time required to settle is roughly equal to the inverse of the data rate. The exact time depends on the specific data rate and the operation that resulted in the start of a conversion; see Table 10 for specific values.

8.4.4.2 Channel Cycling and Overload Recovery

When cycling through channels, take care when configuring the device to ensure that settling occurs within one cycle. For setups that cycle through MUX channels, but do not change PGA and data rate settings, changing the MUX0 register is sufficient. However, when changing PGA and data rate settings, ensure that an overload condition cannot occur during the data transmission. When configuration register data are transferred to the device, new settings become active at the end of each byte sent. Therefore, a brief overload condition can occur during the transmission of configuration data after the completion of the MUX0 byte and before the completion of the SYS0 byte. This temporary overload can result in intermittent incorrect readings. To ensure that an overload does not occur, the communication may need to be split into two separate communications, thus allowing the SYS0 register to before the change of the MUX0 register.

In the event of an overloaded state, take care to ensure single-cycle settling into the next cycle. Changing data rates during an overload state can cause the chopper to become unstable because the device implements a chopper-stabilized PGA. This instability results in slow settling time. To prevent this slow settling, always change the PGA setting or MUX setting to a non-overloaded state before changing the data rate.

8.4.4.3 Single-Cycle Settling

The ADS1148-Q1 is capable of single-cycle settling across all gains and data rates. However, to achieve single-cycle settling at 2 kSPS, special care must be taken with respect to the interface using WREG to change a configuration register. When operating at 2 kSPS, the SCLK period must not exceed 520 ns, and the time between beginning to write a register byte data and the beginning of a subsequent register byte data must not exceed 4.2 µs. Additionally, when performing multiple individual write commands to the first four registers, wait at least 64 oscillator clocks before initiating another write command.

8.4.4.4 Digital Filter Reset Operation

Apart from the RESET command and the $\overline{\text{RESET}}$ pin, the digital filter is reset automatically when either a write operation to the MUX0, VBIAS, MUX1, or SYS0 registers is performed, when a SYNC command is issued, or when the START pin is taken high.

The filter is reset four system clocks (t_{CLK}) after the falling edge of the seventh SCLK of the SYNC command. Similarly, if any write operation takes place in the MUX0 register, regardless of whether the register value changed or not, the filter is reset after the completion of the MUX0 write.

If any write activity takes place in the VBIAS, MUX1, or SYS0 registers, regardless of whether the register value changed or not, the filter is reset. The reset pulse lasts for 32 modulator clocks after the completion of the write operation. If there are multiple write operations, the resulting reset pulse may be viewed as the ANDed result of the different active low pulses created individually by each action.

Table 10 lists the conversion time after a filter reset. Note that this time depends on the operation initiating the reset. Also, the first conversion after a filter reset has a slightly different time than the second and subsequent conversions.

Table 10. Data Conversion Time

NOMINAL DATA RATE (SPS)	EXACT DATA RATE (SPS)	FIRST DATA CONVERSION TIME AFTER FILTER RESET				SECOND AND SUBSEQUENT CONVERSION TIME AFTER FILTER RESET	
		SYNC COMMAND, MUX0 REGISTER WRITE		HARDWARE RESET, RESET COMMAND, START PIN HIGH, WAKEUP COMMAND, VBIAS, MUX1, OR SYS0 REGISTER WRITE			
		VALUE (ms)(1)	NO. OF SYSTEM CLOCK CYCLES	VALUE (ms)(1)	NO. OF SYSTEM CLOCK CYCLES	VALUE (ms)(1)	NO. OF SYSTEM CLOCK CYCLES
5	5.019	199.258	816160	200.26	820265	199.250	816128
10	10.038	99.633	408096	100.635	412201	99.625	408064
20	20.075	49.820	204064	50.822	208169	49.812	204032
40	40.151	24.920	102072	25.172	103106	24.906	102016
80	80.301	12.467	51064	12.719	52098	12.453	51008
160	160.602	6.241	25560	6.492	26594	6.226	25504
320	321.608	3.124	12796	3.250	13314	3.109	12736
640	643.216	1.569	6428	1.695	6946	1.554	6368
1000	1000.000	1.014	4156	1.141	4674	1.000	4096
2000	2000.000	0.514	2108	0.578	2370	0.500	2048

(1) For f_{CLK} = 4.096 MHz.

8.4.5 Calibration

The conversion data are scaled by offset and gain registers before yielding the final output code. As shown in Figure 38, the output of the digital filter is first subtracted by the offset register (OFC) and then multiplied by the full-scale register (FSC) to digitally scale the gain. A digital clipping circuit ensures that the output code does not exceed 16 bits. Equation 17 shows the scaling.

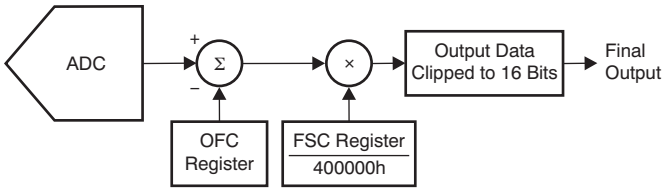


Figure 38. Calibration Block Diagram

$$\text{Final Output Data} = (\text{Input} - \text{OFC}[2:1]) \times \frac{\text{FSC}[2:0]}{400000\text{h}} \quad (17)$$

The values of the offset and full-scale registers are set either by writing to them directly, or are set automatically by calibration commands.

The offset and gain calibration features are intended for the correction of minor system-level offset and gain errors. When entering manual values into the calibration registers, take care to avoid scaling down the gain register to values far below a scaling factor of 1.0. Under extreme situations, overranging the ADC is possible. Avoid encountering situations where analog inputs are connected to voltages greater than V_{REF} / Gain.

Take care when increasing digital gain with the FSC register. When implementing custom digital gains less than 20% higher than nominal and offsets less than 40% of full scale, no special care is required. When operating at digital gains greater than 20% higher than nominal and offsets greater than 40% of full-scale, make sure that the offset and gain registers follow the conditions of Equation 18.

$$\frac{2\text{ V}}{\text{Gain Scaling}} - 1.251\text{ V} > \left|\text{Offset Scaling}\right| \quad (18)$$

8.4.5.1 Offset Calibration Register: OFC[2:0]

The offset calibration is a 24-bit word, composed of three 8-bit registers. The offset is in twos complement format with a maximum positive value of 7FFFFFh and a maximum negative value of 800000h. The upper 16 bits, OFC[2:1], are the most important bits of the offset calibration register for calibration and can correct offsets ranging from –FS to +FS, as shown in Table 11. The lower eight bits, OFC[0], provide sub-LSB correction and are used by the calibration commands. If a calibration command is issued and the offset register is then read for storage and re-use later, all 24 bits of the OFC are recommended to be used. When the calibration commands are not used and the offset is corrected by writing a user-calculated value to the OFC register, only OFC[2:1] are recommended to be used and OFC[0] is recommended to be left as all zeros. A register value of 000000h provides no offset correction.

Note that although the offset calibration register value can correct offsets ranging from –FS to +FS (as shown in Table 11), avoid overloading the analog inputs.

Table 11. Final Output Code vs Offset Calibration Register Setting

OFFSET REGISTER	FINAL OUTPUT CODE WITH V_{IN} = 0 (1)
7FFFFFh	8000h
000100h	FFFFh
000000h	0000h
FFFF00h	0001h
800000h	7FFFh

(1) Excludes effects of noise and inherent offset errors.

8.4.5.2 Full-Scale Calibration Register: FSC[2:0]

The full-scale or gain calibration is a 24-bit word composed of three 8-bit registers. The full-scale calibration value is 24 bits, straight binary, and normalized to 1.0 at code 400000h. Table 12 summarizes the scaling of the full-scale register. Note that although the full-scale calibration register can correct gain errors greater than 1 (with gain scaling less than 1), make sure to avoid overloading the analog inputs.

Table 12. Gain Correction Factor vs Full-Scale Calibration Register Setting

FULL-SCALE REGISTER	GAIN SCALING
800000h	2
400000h	1
200000h	0.5
000000h	0

8.4.5.3 Calibration Commands

The device provides commands for three types of calibration: system gain calibration, system offset calibration, and self offset calibration. Where absolute accuracy is required, a calibration is recommended to be performed after power up, a change in temperature, a change of gain, and in some cases a change in channel. At the completion of calibration the $\overline{\text{DRDY}}$ signal goes low, indicating that the calibration is complete. The first data after calibration are always valid. If the START pin is taken low or a SLEEP command is issued after any calibration command, the device powers down after completing calibration.

After a calibration starts, allow the calibration to complete before issuing any other commands (other than the SLEEP command). Issuing commands during a calibration can result in corrupted data. If this scenario occurs, either resend the calibration command that was aborted or issue a device reset.

8.4.5.3.1 System Offset and Self Offset Calibration

System offset calibration corrects both internal and external offset errors. The system offset calibration is initiated by sending the SYSOCAL command when applying a zero differential input voltage (V_{IN} = 0 V) to the selected analog inputs with the inputs set within the specified input common-mode range, ideally at mid-supply.

The self offset calibration is initiated by sending the SELFOCAL command. During self offset calibration, the selected inputs are disconnected from the internal circuitry and a zero differential signal is applied internally, thus connecting the inputs to mid-supply. With both offset calibrations, the offset calibration register (OFC) is updated afterwards. When either offset calibration command is issued, the device stops the current conversion and starts the calibration procedure immediately. An offset calibration must be performed before a gain calibration.

8.4.5.3.2 System Gain Calibration

System gain calibration corrects for gain error in the signal path. The system gain calibration is initiated by sending the SYSGCAL command when applying a full-scale input to the selected analog inputs. Afterwards, the full-scale calibration register (FSC) is updated. When a system gain calibration command is issued, the device stops the current conversion and starts the calibration procedure immediately.

8.4.5.4 Calibration Timing

When calibration is initiated, the device performs 16 consecutive data conversions and averages the results to calculate the calibration value. This process provides a more accurate calibration value. The time required for calibration is shown in Table 13 and can be calculated using Equation 19.

$$\text{Calibration Time} = t_{CAL} = \frac{50}{f_{CLK}} + \frac{32}{f_{MOD}} + \frac{16}{f_{DATA}} \quad (19)$$

Table 13. Calibration Time versus Data Rate

DATA RATE (SPS)	CALIBRATION TIME (t_{CAL}) (ms)(1)
5	3201.01
10	1601.01
20	801.012
40	400.26
80	200.26
160	100.14
320	50.14
640	25.14
1000	16.14
2000	8.07

(1) For f_{CLK} = 4.096 MHz.

8.5 Programming

8.5.1 Digital Interface

The device provides an SPI-compatible serial communication interface plus a data ready signal ($\overline{DRDY}$). Communication is full-duplex with the exception of a few limitations in regards to the RREG command and the RDATA command. These limitations are explained in detail in the *Commands* section. For the basic serial interface timing characteristics, see Figure 1 and Figure 2.

8.5.1.1 Chip Select ($\overline{CS}$)

The $\overline{CS}$ pin activates SPI communication. $\overline{CS}$ must be low before data transactions and must stay low for the entire SPI communication period. When $\overline{CS}$ is high, the DOUT/$\overline{DRDY}$ pin enters a high-impedance state. Therefore, reads and writes to the serial interface are ignored and the serial interface is reset. The $\overline{DRDY}$ pin operation is independent of $\overline{CS}$. $\overline{DRDY}$ still indicates when a new conversion completes and is forced high in response to SCLK, even if $\overline{CS}$ is high.

Taking $\overline{CS}$ high only deactivates the SPI communication with the device. Data conversion continues and the $\overline{DRDY}$ signal can be monitored to check if a new conversion result is ready. A master device monitoring the $\overline{DRDY}$ signal can select the appropriate slave device by pulling the $\overline{CS}$ pin low.

Programming (continued)

8.5.1.2 Serial Clock (SCLK)

SCLK provides the clock for serial communication. SCLK is a Schmitt-trigger input, but SCLK is recommended to be kept as free from noise as possible to prevent glitches from inadvertently shifting the data. Data are shifted into DIN on the falling edge of SCLK and are shifted out of DOUT on the SCLK rising edge.

8.5.1.3 Data Input (DIN)

DIN is used along with SCLK to send data to the device. Data on DIN are shifted into the device on the SCLK falling edge.

The communication of this device is full-duplex in nature. The device monitors commands shifted in even when data are being shifted out. Data that are present in the output shift register are shifted out when sending in a command. Therefore, make sure that whatever is being sent on the DIN pin is valid when shifting out data. When no command is sent to the device when reading out data, send the no operation command (NOP) command on DIN.

8.5.1.4 Data Ready ($\overline{DRDY}$)

The $\overline{DRDY}$ pin goes low to indicate that a new conversion is complete, and the conversion result is stored in the conversion result buffer. SCLK must be held low for t_{DTS} after the $\overline{DRDY}$ low transition (see Figure 2) so that the conversion result is loaded into both the result buffer and the output shift register. Therefore, do not issue commands during this time frame if the conversion result is to be read out later. This constraint applies only when $\overline{CS}$ is asserted and the device is in RDATAC mode. When $\overline{CS}$ is not asserted, SPI communication with other devices on the SPI bus does not affect loading of the conversion result. After the $\overline{DRDY}$ pin goes low, $\overline{DRDY}$ is forced high on the first falling edge of SCLK (so that the $\overline{DRDY}$ pin can be polled for 0 instead of waiting for a falling edge). If the $\overline{DRDY}$ pin is not taken high by clocking in SCLKs after $\overline{DRDY}$ falls low, a short high pulse for a duration of t_{PWH} indicates that new data are ready.

8.5.1.5 Data Output and Data Ready (DOUT/$\overline{DRDY}$)

The DOUT/$\overline{DRDY}$ pin has two modes: data out (DOUT) only, or DOUT combined with data ready ($\overline{DRDY}$). The DRDY MODE bit determines the function of this pin and can be found in the IDAC0 register. In either mode, the DOUT/$\overline{DRDY}$ pin goes to a high-impedance state when $\overline{CS}$ is taken high.

When the DRDY MODE bit is set to 0, this pin functions as DOUT only. Data are clocked out on the SCLK rising edge, MSB first (as shown in Figure 39).

When the DRDY MODE bit is set to 1, this pin functions as both DOUT and $\overline{DRDY}$. Data are shifted out as with DOUT, but the pin adds the $\overline{DRDY}$ function. Note that this mode is not operational when the device is in stop read data continuous mode when the SDATAC command is given.

The DRDY MODE bit modifies only the DOUT/$\overline{DRDY}$ pin functionality. The $\overline{DRDY}$ pin functionality remains unaffected.

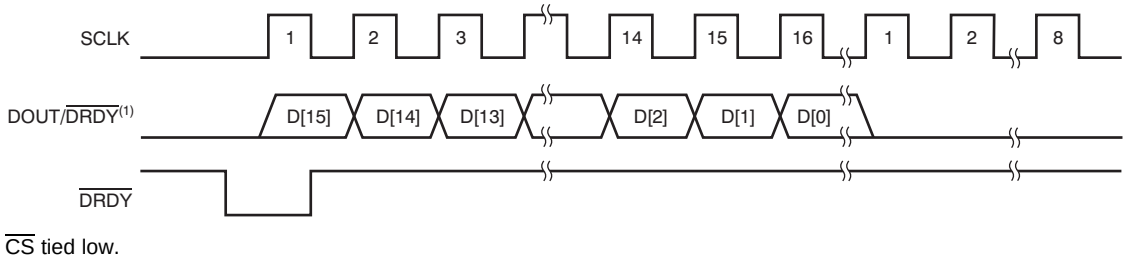
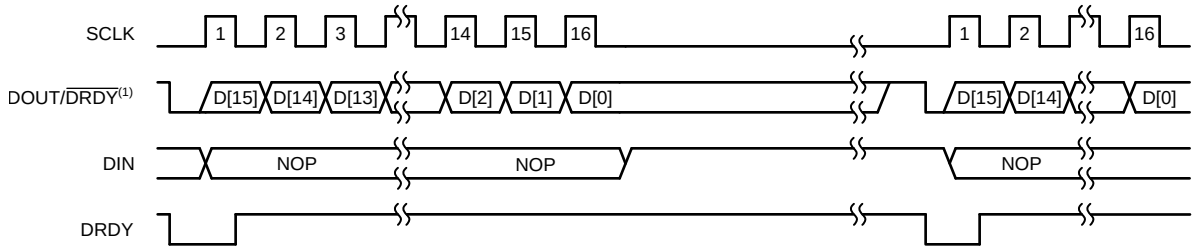


Figure 39. Data Retrieval With the DRDY MODE Bit = 0 (Disabled)

When the DRDY MODE bit is enabled and a new conversion is complete, DOUT/$\overline{DRDY}$ goes low. If DOUT/$\overline{DRDY}$ is already low, then this pin goes high and then goes low (as shown in Figure 40). Similar to the $\overline{DRDY}$ pin, a falling edge on the DOUT/$\overline{DRDY}$ pin signals that a new conversion result is ready. After DOUT/$\overline{DRDY}$ goes low, the data can be clocked out by providing 16 SCLKs if the device is in read data continuous mode. To force DOUT/$\overline{DRDY}$ high (so that DOUT/$\overline{DRDY}$ can be polled for a 0 instead of waiting for a

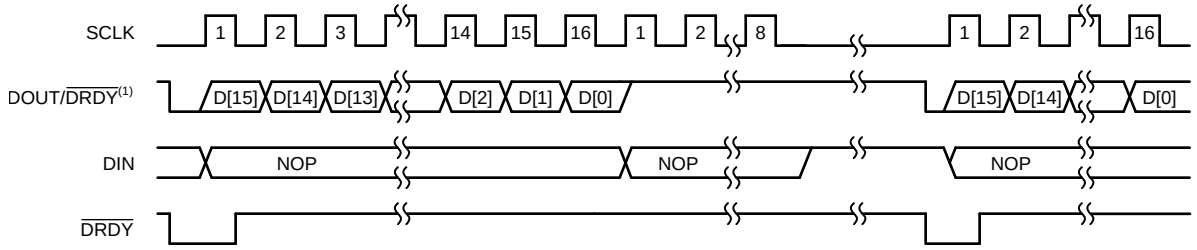
Programming (continued)

falling edge), a NOP command or any other command that does not load the data output register can be sent after reading out the data. Because SCLKs can only be sent in multiples of eight, NOP can be sent to force DOUT/DRDY high if no other command is pending. The DOUT/DRDY pin goes high after the first SCLK rising edge after reading the conversion result completely (as shown in Figure 41). The same condition also applies after an RREG command. After all register bits are read out, the first SCLK rising edge forces DOUT/DRDY high. Figure 42 shows an example where sending an extra NOP command after reading out a register with an RREG command forces the DOUT/DRDY pin high.



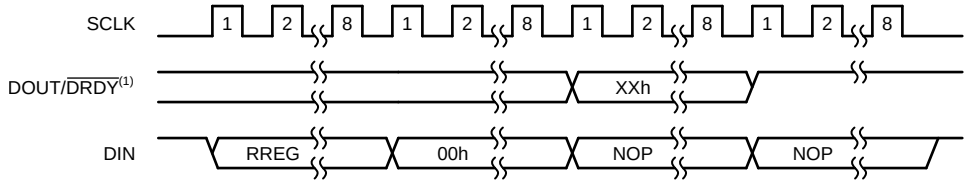
CS tied low.

Figure 40. Data Retrieval With the DRDY MODE Bit = 1 (Enabled)



DRDY MODE bit enabled, CS tied low.

Figure 41. DOUT/DRDY Forced High After Retrieving the Conversion Result



DRDY MODE bit enabled, CS tied low.

Figure 42. DOUT/DRDY Forced High After Reading Register Data

8.5.1.6 SPI Reset

SPI communication is reset in several ways. To reset the serial interface (without resetting the registers or the digital filter), the CS pin can be pulled high. Taking the RESET pin low resets the serial interface along with all the other digital functions. This process also returns all registers to the default values and starts a new conversion.

In systems where CS is tied low permanently, register writes must always be fully completed in 8-bit increments. If a glitch on SCLK disrupts SPI communications, commands are not recognized by the device. The device implements a timeout function for all listed commands in the *Commands* section in the event that data are corrupted and the CS pin is permanently tied low. The SPI timeout resets the interface if idle for 64 conversion cycles.

Programming (continued)

8.5.1.7 SPI Communication During Power-Down Mode

When the START pin is low or the device is in power-down mode, only the RDATA, RDATAC, SDATAC, WAKEUP, and NOP commands can be issued. The RDATA command can be used to repeatedly read the last conversion result during power-down mode. Other commands do not function because the internal clock is shut down to save power during power-down mode.

8.5.2 Data Format

The device provides 16 bits of data in binary twos complement format. The size of one code (LSB) is calculated using Equation 20.

$$1\ \text{LSB} = (2 \times V_{REF} / \text{Gain}) / 2^{16} = +\text{FS} / 2^{15} \quad (20)$$

A positive full-scale (FS) input [$V_{IN} \geq (+\text{FS} - 1\ \text{LSB}) = (V_{REF} / \text{Gain} - 1\ \text{LSB})$] produces an output code of 7FFFh and a negative full-scale input ($V_{IN} \leq -\text{FS} = -V_{REF} / \text{Gain}$) produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 14 summarizes the ideal output codes for different input signals.

Table 14. Ideal Output Code vs Input Signal

INPUT SIGNAL, V_{IN} ($AIN_P - AIN_N$)	IDEAL OUTPUT CODE(1)
≥ FS ($2^{15} - 1$) / 2^{15}	7FFFh
FS / 2^{15}	0001h
0	0000h
–FS / 2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes effects of noise, linearity, offset, and gain errors.

Figure 43 shows the mapping of the analog input signal to the output codes.

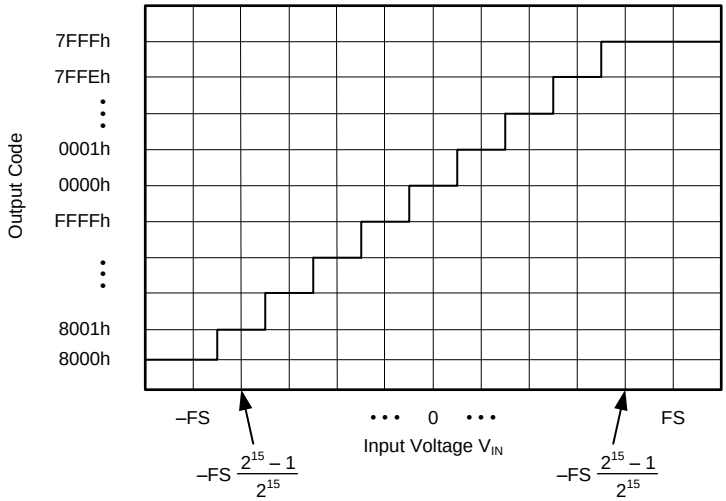


Figure 43. Code Transition Diagram

8.5.3 Commands

The device offers 13 commands to control device operation, as shown in Table 15. Some of the commands are stand-alone commands (WAKEUP, SLEEP, SYNC, RESET, SYSOCAL, SYSGCAL, and SELFOCAL). There are three additional commands used to control reading of data from the device (RDATA, RDATAC, and SDATAC). The commands to read (RREG) and write (WREG) configuration register data from and to the device require additional information as part of the instruction. A NOP command can be used to clock out data from the device without clocking in a command.

Operands:

- n = number of registers to be read or written (number of bytes – 1)
- r = register (0 to 15)
- x = don't care

Table 15. SPI Commands

COMMAND(1)	DESCRIPTION	1st COMMAND BYTE	2nd COMMAND BYTE
WAKEUP	Exit power down mode	0000 000x (00h, 01h)	
SLEEP	Enter power down mode	0000 001x (02h, 03h)	
SYNC	Synchronize ADC conversions	0000 010x (04h, 05h)	0000 010x (04,05h)
RESET	Reset to default values	0000 011x (06h, 07h)	
NOP	No operation	1111 1111 (FFh)	
RDATA	Read data once	0001 001x (12h, 13h)	
RDATAC	Read data continuous mode	0001 010x (14h, 15h)	
SDATAC	Stop read data continuous mode	0001 011x (16h, 17h)	
RREG	Read from register *rrrr*	0010 rrrr (2xh)	0000 nnnn
WREG	Write to register *rrrr*	0100 rrrr (4xh)	0000 nnnn
SYSOCAL	System offset calibration	0110 0000 (60h)	
SYSGCAL	System gain calibration	0110 0001 (61h)	
SELFOCAL	Self offset calibration	0110 0010 (62h)	
Restricted	Restricted command. Never send to the device.	1111 0001 (F1h)	

(1) Only the RDATA, RDATAC, SDATAC, WAKEUP, and NOP commands can be issued when the START pin is low or when the device is in power-down mode.

8.5.3.1 WAKEUP (0000 000x)

Use the WAKEUP command to power up the device after a SLEEP command. After execution of the WAKEUP command, the device powers up on the falling edge of the eighth SCLK.

8.5.3.2 SLEEP (0000 001x)

The SLEEP command places the device into power-down mode. When the SLEEP command is issued, the device completes the current conversion and then goes into power-down mode. Note that this command does not automatically power down the internal voltage reference; see the VREFCON bits in the *MUX1* section for each device for further details.

To exit power-down mode, issue the WAKEUP command. Single conversions can be performed by issuing a WAKEUP command followed by a SLEEP command.

Both WAKEUP and SLEEP are the software command equivalents of using the START pin to control the device; see Figure 44.

NOTE

If the START pin is held low, a WAKEUP command does not power up the device. When using the SLEEP command, $\overline{CS}$ must be held low for the duration of the power-down mode.

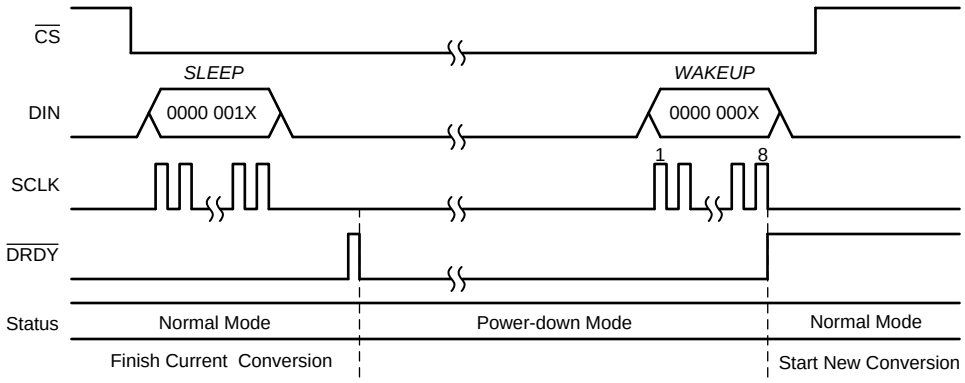


Figure 44. SLEEP and WAKEUP Commands Operation

8.5.3.3 SYNC (0000 010x)

The SYNC command resets the ADC digital filter and starts a new conversion. The $\overline{\text{DRDY}}$ pin from multiple devices connected to the same SPI bus can be synchronized by issuing a SYNC command to all devices simultaneously.

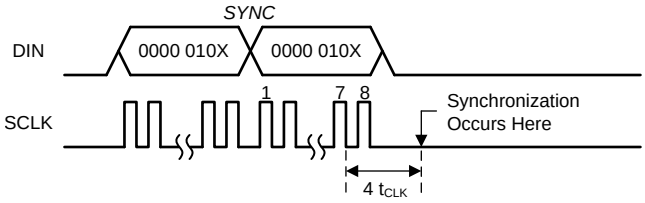


Figure 45. SYNC Command Operation

8.5.3.4 RESET (0000 011x)

The RESET command restores the registers to the respective default values. This command also resets the digital filter. RESET is the command equivalent of using the $\overline{\text{RESET}}$ pin to reset the device. However, the RESET command does not reset the serial interface. If the RESET command is issued when the serial interface is out of synchronization because of a glitch on SCLK, the device does not reset. The $\overline{\text{CS}}$ pin can be used to reset the serial interface first, and then a RESET command can be issued to reset the device. The RESET command holds the registers and the decimation filter in a reset state for 0.6 ms when the system clock frequency is 4.096 MHz, similar to the hardware reset. Therefore, SPI communication can only be started 0.6 ms after the RESET command is issued, as shown in Figure 46.

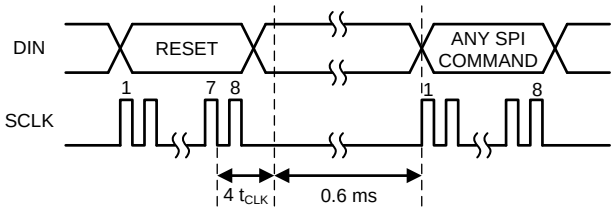


Figure 46. SPI Communication after an SPI Reset

8.5.3.5 RDATA (0001 001x)

The RDATA command loads the most recent conversion result into the output register. After issuing this command, the conversion result is read out by sending 16 SCLKs, as shown in Figure 47. This command also works in RDATAC mode.

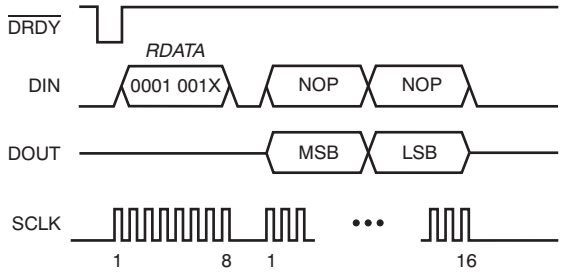


Figure 47. RDATA: Reading Data Once Command

When performing multiple reads of the conversion result, the RDATA command can be sent when the last eight bits of the conversion result are shifted out during the course of the first read operation by taking advantage of the duplex communication nature of the serial interface, as shown in Figure 48.

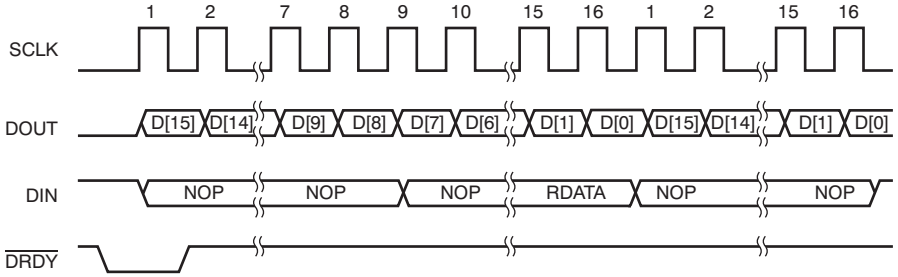


Figure 48. Using RDATA in Full-Duplex Mode

8.5.3.6 RDATAC (0001 010x)

The RDATAC command enables the read data continuous mode. This mode is the default mode after power-up or reset. In read data continuous mode, new conversion results are automatically loaded onto DOUT. The conversion result can be received from the device after the $\overline{\text{DRDY}}$ signal goes low by sending 16 SCLKs. Reading back all the bits is not necessary, as long as the number of bits read out is a multiple of eight. The RDATAC command must be issued after $\overline{\text{DRDY}}$ goes low and the command takes effect on the next $\overline{\text{DRDY}}$, as shown in Figure 49.

Be sure to complete data retrieval (conversion result or register read back) before $\overline{\text{DRDY}}$ returns low, otherwise the resulting data are corrupted. Successful register read operations in RDATAC mode require the knowledge of when the next $\overline{\text{DRDY}}$ falling edge occurs.

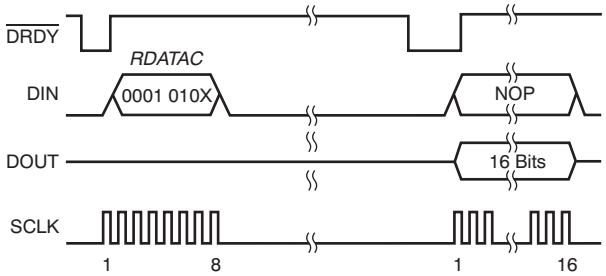


Figure 49. RDATAC: Read Data Continuously Command

8.5.3.7 SDATAC (0001 011x)

The SDATAC command terminates read data continuous mode. In stop read data continuous mode, the conversion result is not automatically loaded onto DOUT when $\overline{\text{DRDY}}$ goes low, and register read operations can be performed without interruption from new conversion results being loaded into the output shift register. Use the RDATA command to retrieve conversion data. The SDATAC command takes effect after the next $\overline{\text{DRDY}}$.

If $\overline{\text{DRDY}}$ is not actively monitored for data conversions, the stop read data continuous mode is the preferred method of reading data. In this mode, a read of ADC data is not interrupted by the completion of a new ADC conversion.

8.5.3.8 RREG (0010 rrrr, 0000 nnnn)

The RREG command outputs the data from up to 15 registers, starting with the register address specified as part of the instruction. The number of registers read is one plus the value of the second byte. If the count exceeds the remaining registers, the addresses wrap back to the beginning. The 2-byte command structure for RREG is listed below.

- First Command Byte: 0010 rrrr, where rrrr is the address of the first register to read.
- Second Command Byte: 0000 nnnn, where nnnn is the number of bytes to read –1.
- Byte: data read from the registers are clocked out with NOPs.

The full-duplex nature of the serial interface cannot be used when reading out register data. For example, a SYNC command cannot be issued when reading out the VBIAS and MUX1 data, as shown in Figure 50. Any command sent during the readout of the register data is ignored. Thus, NOPs are recommended to be sent through DIN when reading out register data.

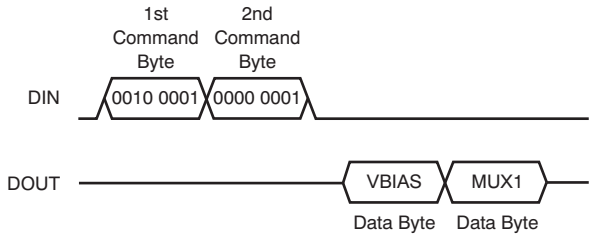


Figure 50. RREG: Read from Register Command

8.5.3.9 WREG (0100 rrrr, 0000 nnnn)

The WREG command writes to the registers, starting with the register specified as part of the instruction. The number of registers that are written is one plus the value of the second byte. The command structure for WREG is:

- First Command Byte: 0100 rrrr, where rrrr is the address of the first register to be written.
- Second Command Byte: 0000 nnnn, where nnnn is the number of bytes to be written – 1.
- Byte: data to be written to the registers.

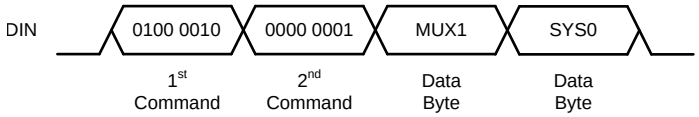


Figure 51. WREG: Write to Register Command

8.5.3.10 SYSOCAL (0110 0000)

The SYSOCAL command initiates a system offset calibration. For a system offset calibration, the inputs must be externally shorted to a voltage within the input common-mode range. The inputs must be near the mid-supply voltage of (AVDD + AVSS) / 2. The OFC register is updated when the command completes. Timing for the calibration commands is shown in Figure 52.

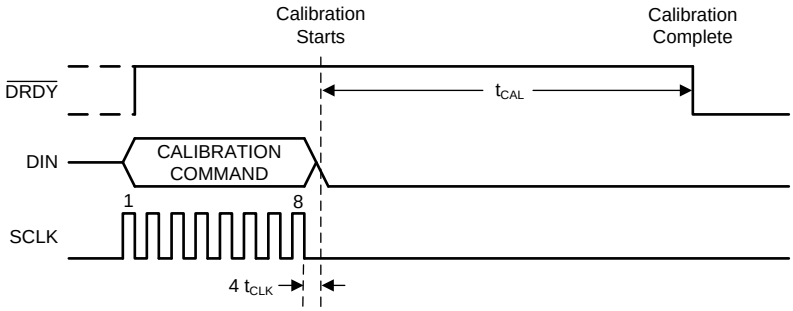


Figure 52. Calibration Command

8.5.3.11 SYSGCAL (0110 0001)

The SYSGCAL command initiates the system gain calibration. For a system gain calibration, the input must be set to full-scale. The FSC register is updated after this operation. Timing for the calibration commands is shown in Figure 52.

8.5.3.12 SELFOCAL (0110 0010)

The SELFOCAL command initiates a self offset calibration. The device internally shorts the inputs to mid-supply and performs the calibration. The OFC register is updated after this operation. Timing for the calibration commands is shown in Figure 52.

8.5.3.13 NOP (1111 1111)

This command is a no-operation command. NOP is used to clock out data without clocking in a command.

8.5.3.14 Restricted Command (1111 0001)

This command is a restricted command. This command must never be issued to the device.

8.6 Register Maps

8.6.1 Register Map

Table 16. Register Map

REGISTER ADDRESS (HEX)	REGISTER NAME	REGISTER DATA							
		7	6	5	4	3	2	1	0
00h	MUX0	BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]		
01h	VBIAS	VBIAS[7:0]							
02h	MUX1	CLKSTAT	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		
03h	SYS0	0	PGA[2:0]			DR[3:0]			
04h	OFC0	OFC[7:0]							
05h	OFC1	OFC[15:8]							
06h	OFC2	OFC[23:16]							
07h	FSC0	FSC[7:0]							
08h	FSC1	FSC[15:8]							
09h	FSC2	FSC[23:16]							
0Ah	IDAC0	ID[3:0]				DRDY MODE	IMAG[2:0]		
0Bh	IDAC1	I1DIR[3:0]				I2DIR[3:0]			
0Ch	GPIOCFG	IOCFG[7:0]							
0Dh	GPIODIR	IODIR[7:0]							
0Eh	GPIODAT	IODAT[7:0]							

8.6.2 Detailed Register Definitions

8.6.2.1 MUX0—Multiplexer Control Register 0 (address = 00h) [reset = 01h]

This register allows any combination of differential inputs to be selected on any of the input channels. Note that this setting can be superceded by the MUXCAL and VBIAS bits.

Figure 53. Multiplexer Control Register 0

7	6	5	4	3	2	1	0
BCS[1:0]		MUX_SP[2:0]			MUX_SN[2:0]		
R/W-0h		R/W-0h			R/W-1h		

LEGEND: R/W = Read/Write; -n = value after reset

Table 17. Multiplexer Control Register 0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-6	BCS[1:0]	R/W	0h	**Burn-out detect current source register.** These bits control the setting of the sensor burnout detect current source. 00: Burn-out current source off (default) 01: Burn-out current source on, 0.5 µA 10: Burn-out current source on, 2 µA 11: Burn-out current source on, 10 µA
5-3	MUX_SP[2:0]	R/W	0h	**Multiplexer selection, adc positive input.** These bits are the positive input channel selection bits. 000: AIN0 (default) 001: AIN1 010: AIN2 011: AIN3 100: AIN4 101: AIN5 110: AIN6 111: AIN7
2-0	MUX_SN[2:0]	R/W	1h	**Multiplexer selection, adc negative input.** These bits are the negative input channel selection bits. 000: AIN0 001: AIN1 (default) 010: AIN2 011: AIN3 100: AIN4 101: AIN5 110: AIN6 111: AIN7

8.6.2.2 VBIAS—Bias Voltage Register (address = 01h) [reset = 00h]

Figure 54. Bias Voltage Register

7	6	5	4	3	2	1	0
VBIAS[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 18. Bias Voltage Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	VBIAS[7]	R/W	0h	**VBIAS[7] voltage enable.** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN7. 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN7
6	VBIAS[6]	R/W	0h	**VBIAS[6] voltage enable.** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN6. 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN6
5	VBIAS[5]	R/W	0h	**VBIAS[5] voltage enable.** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN5. 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN5
4	VBIAS[4]	R/W	0h	**VBIAS[4] voltage enable.** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN4. 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN4
3	VBIAS[3]	R/W	0h	**VBIAS[3] voltage enable.** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN3. 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN3
2	VBIAS[2]	R/W	0h	**VBIAS[2] voltage enable.** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN2. 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN2
1	VBIAS[1]	R/W	0h	**VBIAS[1] voltage enable.** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN1. 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN1
0	VBIAS[0]	R/W	0h	**VBIAS[0] voltage enable.** A bias voltage of mid-supply (AVDD + AVSS) / 2 is applied to AIN0. 0: Bias voltage is not enabled (default) 1: Bias voltage is applied to AIN0

8.6.2.3 MUX1—Multiplexer Control Register 1 (address = 02h) [reset = x0h]

Figure 55. Multiplexer Control Register 1

7	6	5	4	3	2	1	0
CLKSTAT	VREFCON[1:0]		REFSELT[1:0]		MUXCAL[2:0]		
R-xh	R/W-0h		R/W-0h		R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Multiplexer Control Register 0 Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	CLKSTAT	R	xh	**Clock status.** This bit is read-only and indicates whether the internal oscillator or external clock is being used. 0: Internal oscillator in use 1: External clock in use
6-5	VREFCON[1:0]	R/W	0h	**Internal reference control.** These bits control the internal voltage reference. These bits allow the reference to be turned on or off completely, or allow the reference state to follow the state of the device. Note that the internal reference is required for operation of the IDAC functions. 00: Internal reference is always off (default) 01: Internal reference is always on 10, 11: Internal reference is on when a conversion is in progress and powers down when the device receives a SLEEP command or the START pin is taken low
4-3	REFSELT[1:0]	R/W	0h	**Reference select control.** These bits select the reference input for the ADC. 00: REFP0 and REFN0 reference inputs selected (default) 01: REFP1 and REFN1 reference inputs selected 10: Internal reference selected 11: Internal reference selected and internally connected to REFP0 and REFN0 input pins
2-0	MUXCAL[2:0](1)	R/W	0h	**System monitor control.** These bits are used to select a system monitor. The MUXCAL selection supercedes selections from the MUX0, MUX1, and VBIAS registers (includes MUX_SP, MUX_SN, VBIAS, and reference input selections). 000: Normal operation (default) 001: Offset calibration. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to mid-supply (AVDD + AVSS) / 2. 010: Gain calibration. The analog inputs are connected to the voltage reference. 011: Temperature measurement. The inputs are connected to a diode circuit that produces a voltage proportional to the ambient temperature of the device. 100: REF1 monitor. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to $(V_{(REFP1)} – V_{(REFN1)}) / 4$. 101: REF0 monitor. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to $(V_{(REFP0)} – V_{(REFN0)}) / 4$. 110: Analog supply monitor. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to (AVDD – AVSS) / 4. 111: Digital supply monitor. The analog inputs are disconnected and AIN_P and AIN_N are internally connected to (DVDD – DGND) / 4.

(1) When using either reference monitor, the internal reference must be enabled.

Table 20 provides the ADC input connection and PGA settings for each MUXCAL setting. The PGA setting reverts to the original SYS0 register setting when MUXCAL is taken back to normal operation or offset measurement.

Table 20. MUXCAL Settings

MUXCAL[2:0]	PGA GAIN SETTING	ADC INPUT
000	Set by the SYS0 register	Normal operation
001	Set by the SYS0 register	Inputs shorted to mid-supply (AVDD + AVSS) / 2
010	Forced to 1	$V_{(REFP)} – V_{(REFN)}$ (full-scale)
011	Forced to 1	Temperature measurement diode
100	Forced to 1	$(V_{(REFP1)} – V_{(REFN1)}) / 4$
101	Forced to 1	$(V_{(REFP0)} – V_{(REFN0)}) / 4$
110	Forced to 1	(AVDD – AVSS) / 4
111	Forced to 1	(DVDD – DGND) / 4

8.6.2.4 SYS0—System Control Register 0 (address = 03h) [reset = 00h]

Figure 56. System Control Register 0

7	6	5	4	3	2	1	0
0	PGA[2:0]			DR[3:0]			
R-0h	R/W-0h			R/W-0h			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 21. System Control Register 0 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	RESERVED	R	0h	**Reserved.** Always write 0
6-4	PGA[2:0]	R/W	0h	**Gain setting for the PGA.** These bits determine the gain of the PGA. 000: PGA = 1 (default) 001: PGA = 2 010: PGA = 4 011: PGA = 8 100: PGA = 16 101: PGA = 32 110: PGA = 64 111: PGA = 128
3-0	DR[3:0]	R/W	0h	**Data output rate setting.** These bits determine the data output rate of the ADC. 0000: DR = 5 SPS (default) 0001: DR = 10 SPS 0010: DR = 20 SPS 0011: DR = 40 SPS 0100: DR = 80 SPS 0101: DR = 160 SPS 0110: DR = 320 SPS 0111: DR = 640 SPS 1000: DR = 1000 SPS 1001 to 1111: DR = 2000 SPS

8.6.2.5 OFC—Offset Calibration Coefficient Register (address = 04h, 05h, 06h) [reset = 00h, 00h, 00h]

These bits make up the offset calibration coefficient register. Note that address 04h = 7-0, 05h = 15-8, and 06h = 23-16.

Figure 57. Offset Calibration Coefficient Register

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
OFC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
OFC[23:16]							
R/W-00h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 22. Offset Calibration Coefficient Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
23-0	OFC[23:0]	R/W	000000h	**Offset calibration register.** Three registers compose the ADC 24-bit offset calibration word and are in twos complement format. The upper 16 bits (OFC[23:8]) can correct offsets ranging from –FS to +FS, and the lower eight bits (OFC[7:0]) provide sub-LSB correction. The ADC subtracts the register value from the conversion result before full-scale operation.

8.6.2.6 FSC—Full-Scale Calibration Coefficient Register (address = 07h, 08h, 09h) [reset = 00h, 00h, 40h]

These bits make up the full-scale calibration coefficient register. Note that address 07h = 7-0, 08h = 15-8, and 09h = 23-16.

Figure 58. Full-Scale Calibration Coefficient Register

7	6	5	4	3	2	4	0
FSC[7:0]							
R/W-00h							
15	14	13	12	11	10	9	8
FSC[15:8]							
R/W-00h							
23	22	21	20	19	18	17	16
FSC[23:16]							
R/W-40h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 23. Full-Scale Calibration Coefficient Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
23-0	FSC[23:0]	R/W	400000h	**Full-scale calibration register.** Three registers compose the ADC 24-bit, full-scale calibration word. The 24-bit word is straight binary. The ADC divides the register value of the FSC register by 400000h to derive the scale factor for calibration. After the offset calibration, the ADC multiplies the scale factor by the conversion result.

8.6.2.7 IDAC0—IDAC Control Register 0 (address = 0Ah) [reset = x0h]

Figure 59. IDAC Control Register 0

7	6	5	4	3	2	1	0
ID[3:0]				DRDY MODE	IMAG[2:0]		
R-xh				R/W-0h	R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. IDAC Control Register 0 Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-4	ID[3:0]	R	xh	**Revision identification.** Read-only, factory-programmed bits used for revision identification. *Note: The revision ID may change without notification*
3	DRDY MODE	R/W	0h	**Data ready mode setting.** This bit sets the DOUT/$\overline{\text{DRDY}}$ pin functionality. In either setting of the DRDY MODE bit, the dedicated $\overline{\text{DRDY}}$ pin continues to indicate data ready, active low. 0: DOUT/$\overline{\text{DRDY}}$ pin functions only as data out (default) 1: DOUT/$\overline{\text{DRDY}}$ pin functions both as data out and data ready, active low(1)
2-0	IMAG[2:0]	R/W	0h	**IDAC excitation current magnitude.** The device has two excitation current sources (IDACs) that can be used for sensor excitation. The IMAG bits control the magnitude of the excitation current. The IDACs require the internal reference to be on. 000: off (default) 001: 50 µA 010: 100 µA 011: 250 µA 100: 500 µA 101: 750 µA 110: 1000 µA 111: 1500 µA

(1) Cannot be used in SDATAC mode.

8.6.2.8 IDAC1—IDAC Control Register 1 (address = 0Bh) [reset = FFh]

Figure 60. IDAC Control Register 1

7	6	5	4	3	2	1	0
I1DIR[3:0]				I2DIR[3:0]			
R/W-Fh				R/W-Fh			

LEGEND: R/W = Read/Write; -n = value after reset

The two IDACs can be routed to either the IEXC1 and IEXC2 output pins or directly to the analog inputs.

Table 25. IDAC Control Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7-4	I1DIR[3:0]	R/W	Fh	**IDAC excitation current output 1.** These bits select the output pin for the first excitation current source. 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 10x0: IEXC1 10x1: IEXC2 11xx: Disconnected (default)
3-0	I2DIR[3:0]	R/W	Fh	**IDAC excitation current output 2.** These bits select the output pin for the second excitation current source. 0000: AIN0 0001: AIN1 0010: AIN2 0011: AIN3 0100: AIN4 0101: AIN5 0110: AIN6 0111: AIN7 10x0: IEXC1 10x1: IEXC2 11xx: Disconnected (default)

8.6.2.9 GPIOCFG—GPIO Configuration Register (address = 0Ch) [reset = 00h]

Figure 61. GPIO Configuration Register

7	6	5	4	3	2	1	0
IOCFG[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 26. GPIO Configuration Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	IOCFG[7]	R/W	0h	**GPIO[7] (AIN7) pin configuration.** 0: GPIO[7] is not enabled (default) 1: GPIO[7] is applied to AIN7
6	IOCFG[6]	R/W	0h	**GPIO[6] (AIN6) pin configuration.** 0: GPIO[6] is not enabled (default) 1: GPIO[6] is applied to AIN6
5	IOCFG[5]	R/W	0h	**GPIO[5] (AIN5) pin configuration.** 0: GPIO[5] is not enabled (default) 1: GPIO[5] is applied to AIN5
4	IOCFG[4]	R/W	0h	**GPIO[4] (AIN4) pin configuration.** 0: GPIO[4] is not enabled (default) 1: GPIO[4] is applied to AIN4
3	IOCFG[3]	R/W	0h	**GPIO[3] (AIN3) pin configuration.** 0: GPIO[3] is not enabled (default) 1: GPIO[3] is applied to AIN3
2	IOCFG[2]	R/W	0h	**GPIO[2] (AIN2) pin configuration.** 0: GPIO[2] is not enabled (default) 1: GPIO[2] is applied to AIN2
1	IOCFG[1]	R/W	0h	**GPIO[1] (REFN0) pin configuration.** 0: GPIO[1] is not enabled (default) 1: GPIO[1] is applied to REFN0
0	IOCFG[0]	R/W	0h	**GPIO[0] (REFP0) pin configuration.** 0: GPIO[0] is not enabled (default) 1: GPIO[0] is applied to REFP0

8.6.2.10 GPIODIR—GPIO Direction Register (address = 0Dh) [reset = 00h]

Figure 62. GPIO Direction Register

7	6	5	4	3	2	1	0
IODIR[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 27. GPIO Direction Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	IODIR[7]	R/W	0h	**GPIO[7] (AIN7) pin direction.** This bit configures GPIO[7] as a GPIO input or GPIO output. 0: GPIO[7] is an output (default) 1: GPIO[7] is an input
6	IODIR[6]	R/W	0h	**GPIO[6] (AIN6) pin direction.** This bit configures GPIO[6] as a GPIO input or GPIO output. 0: GPIO[6] is an output (default) 1: GPIO[6] is an input
5	IODIR[5]	R/W	0h	**GPIO[5] (AIN5) pin direction.** This bit configures GPIO[5] as a GPIO input or GPIO output. 0: GPIO[5] is an output (default) 1: GPIO[5] is an input
4	IODIR[4]	R/W	0h	**GPIO[4] (AIN4) pin direction.** This bit configures GPIO[4] as a GPIO input or GPIO output. 0: GPIO[4] is an output (default) 1: GPIO[4] is an input
3	IODIR[3]	R/W	0h	**GPIO[3] (AIN3) pin direction.** This bit configures GPIO[3] as a GPIO input or GPIO output. 0: GPIO[3] is an output (default) 1: GPIO[3] is an input
2	IODIR[2]	R/W	0h	**GPIO[2] (AIN2) pin direction.** This bit configures GPIO[2] as a GPIO input or GPIO output. 0: GPIO[2] is an output (default) 1: GPIO[2] is an input
1	IODIR[1]	R/W	0h	**GPIO[1] (REFN0) pin direction.** This bit configures GPIO[1] as a GPIO input or GPIO output. 0: GPIO[1] is an output (default) 1: GPIO[1] is an input
0	IODIR[0]	R/W	0h	**GPIO[0] (REFP0) pin direction.** This bit configures GPIO[0] as a GPIO input or GPIO output. 0: GPIO[0] is an output (default) 1: GPIO[0] is an input

8.6.2.11 GPIODAT—GPIO Data Register (address = 0Eh) [reset = 00h]

Figure 63. GPIO Data Register

7	6	5	4	3	2	1	0
IODAT[7:0]							
R/W-00h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 28. GPIO Data Register Field Descriptions

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	IODAT[7]	R/W	0h	**GPIO[7] (AIN7) pin data.** When configured as an output, a read to this bit returns the register value. When configured as an input, a write to this bit only sets the register value. 0: GPIO[7] is low (default) 1: GPIO[7] is high
6	IODAT[6]	R/W	0h	**GPIO[6] (AIN6) pin data.** When configured as an output, a read to this bit returns the register value. When configured as an input, a write to this bit only sets the register value. 0: GPIO[6] is low (default) 1: GPIO[6] is high
5	IODAT[5]	R/W	0h	**GPIO[5] (AIN5) pin data.** When configured as an output, a read to this bit returns the register value. When configured as an input, a write to this bit only sets the register value. 0: GPIO[5] is low (default) 1: GPIO[5] is high
4	IODAT[4]	R/W	0h	**GPIO[4] (AIN4) pin data.** When configured as an output, a read to this bit returns the register value. When configured as an input, a write to this bit only sets the register value. 0: GPIO[4] is low (default) 1: GPIO[4] is high
3	IODAT[3]	R/W	0h	**GPIO[3] (AIN3) pin data.** When configured as an output, a read to this bit returns the register value. When configured as an input, a write to this bit only sets the register value. 0: GPIO[3] is low (default) 1: GPIO[3] is high
2	IODAT[2]	R/W	0h	**GPIO[2] (AIN2) pin data.** When configured as an output, a read to this bit returns the register value. When configured as an input, a write to this bit only sets the register value. 0: GPIO[2] is low (default) 1: GPIO[2] is high
1	IODAT[1]	R/W	0h	**GPIO[1] (REFN0) pin data.** When configured as an output, a read to this bit returns the register value. When configured as an input, a write to this bit only sets the register value. 0: GPIO[1] is low (default) 1: GPIO[1] is high
0	IODAT[0]	R/W	0h	**GPIO[0] (REFP0) pin data.** When configured as an output, a read to this bit returns the register value. When configured as an input, a write to this bit only sets the register value. 0: GPIO[0] is low (default) 1: GPIO[0] is high

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ADS1148-Q1 offers many integrated features to ease the measurement of the most common sensor types, including various types of temperature and bridge sensors. Primary considerations when designing an application with this device include connecting and configuring the serial interface, designing the analog input filtering, establishing an appropriate external reference for ratiometric measurements, and setting the common-mode input voltage for the internal PGA. These considerations are discussed in this section.

9.1.1 Serial Interface Connections

Figure 64 shows the principle serial interface connections for the ADS1148-Q1.

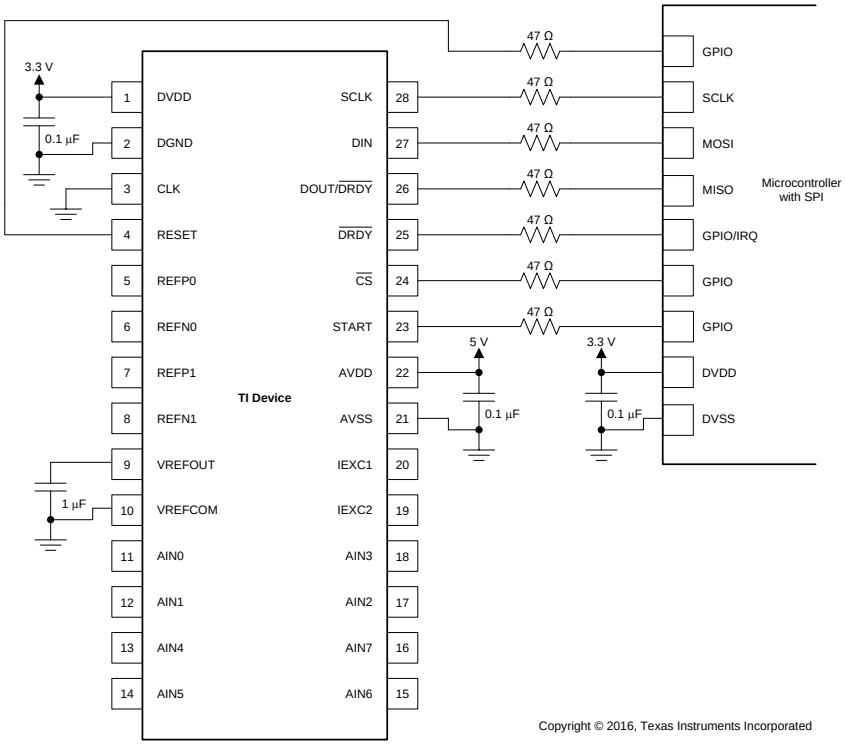


Figure 64. Serial Interface Connections

Most microcontroller SPI peripherals can operate with the ADS1148-Q1. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the device can be found in the *Timing Requirements* section.

47-Ω resistors are recommended to be placed in series with all digital input and output pins ($\overline{CS}$, SCLK, DIN, DOUT/$\overline{DRDY}$, $\overline{DRDY}$, $\overline{RESET}$, and START). This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

Application Information (continued)

9.1.2 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the Nyquist frequency). These frequency components are folded back and show up in the actual frequency band of interest below half the sampling frequency. Note that inside a ΔΣ ADC, the input signal is sampled at the modulator frequency, f_{MOD} and not at the output data rate. The filter response of the digital filter repeats at multiples of the f_{MOD}, as shown in Figure 65. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter, depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

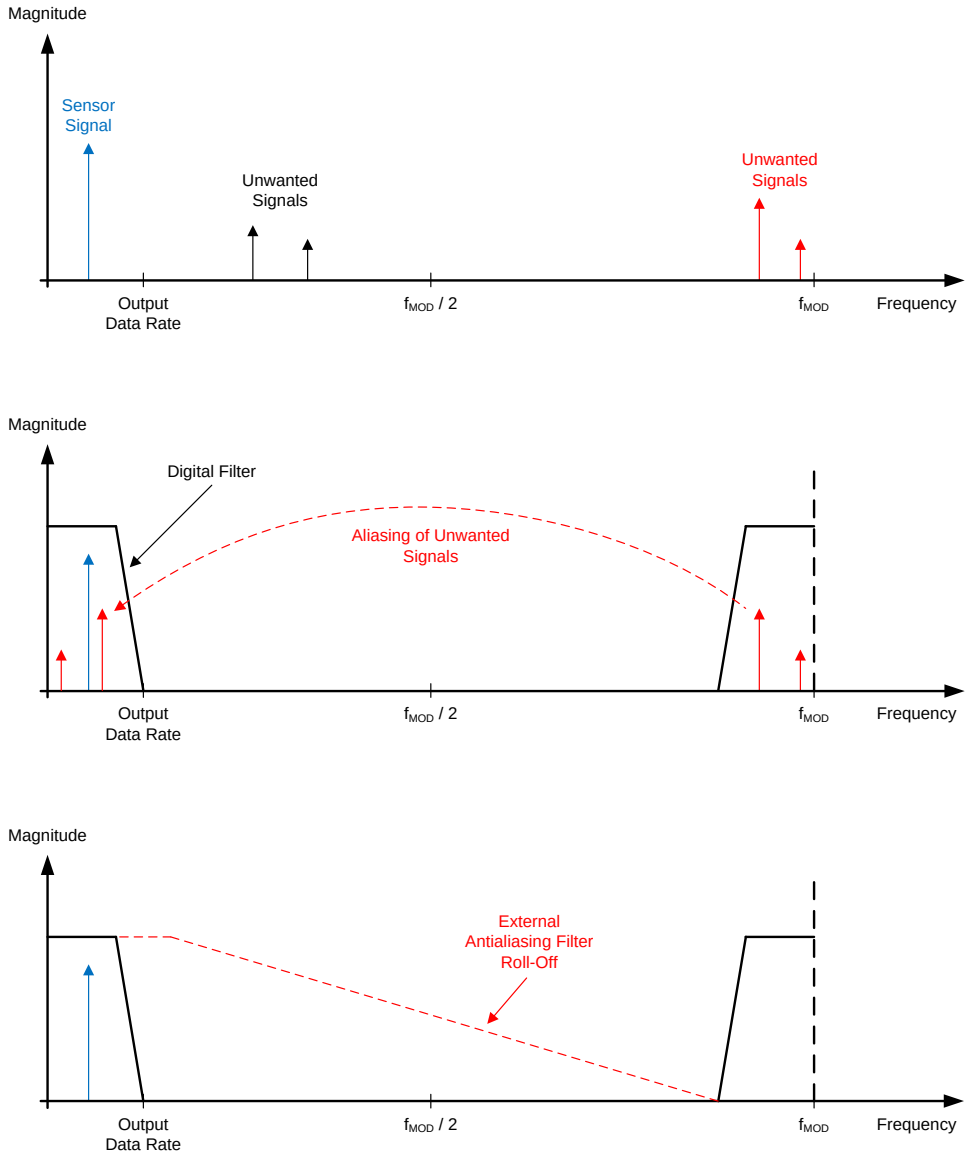


Figure 65. Effect of Aliasing

Application Information (continued)

Many sensor signals are inherently band-limited; for example, the output of a thermocouple has a limited rate of change. In this case, the sensor signal does not alias back into the pass band when using a ΔΣ ADC. However, any noise pickup along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed circuit board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order resistor-capacitor (RC) filter is (in most cases) sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond f_{MOD} / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1148-Q1 attenuates signals to a certain degree, as illustrated in the filter response plots in the *Digital Filter* section. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or 10 times higher is generally a good starting point for a system design.

Internal to the device, prior to the PGA inputs, is an EMI filter; see Figure 18. The cutoff frequency of this filter is approximately 47 MHz, which helps reject high-frequency interferences.

9.1.3 External Reference and Ratiometric Measurements

The full-scale range of the ADS1148-Q1 is defined by the reference voltage and the PGA gain (FSR = $\pm V_{REF}$ / Gain). An external reference can be used instead of the integrated 2.048-V reference to adapt the FSR to the specific system requirements. An external reference must be used if V_{IN} is greater than 2.048 V. For example, an external 2.5-V reference is required to measure signals as large as 2.5 V. Note that the input signal must be within the common-mode input range to be valid, and that the reference input voltage must be between 0.5 V and (AVDD – AVSS – 1 V).

The buffered reference inputs of the device also allow the implementation of ratiometric measurements. In a ratiometric measurement, the same excitation source that is used to excite the sensor is also used to establish the reference for the ADC. As an example, a simple form of a ratiometric measurement uses the same current source to excite both the resistive sensor element (such as an RTD) and another resistive reference element that is in series with the element being measured. The voltage that develops across the reference element is used as the reference source for the ADC. In this configuration, current noise and drift are common to both the sensor measurement and the reference; therefore, these components cancel out in the ADC transfer function. The output code is only a ratio of the sensor element value and the reference resistor value, and is not affected by the absolute value of the excitation current.

9.1.4 Establishing a Proper Common-Mode Input Voltage

The ADS1148-Q1 is used to measure various types of signal configurations. However, configuring the input of the device properly for the respective signal type is important.

The ADS1148-Q1 features an 8-input multiplexer. Each input can be independently selected as the positive input or the negative input to be measured by the ADC. With an 8-input multiplexer, four independent differential-input channels can be measured. Seven channels can also be chosen to be measured, using one input as a fixed common input. Regardless of the analog input configuration, make sure that all inputs, including the common input are within the common-mode input voltage range.

If the supply is unipolar (for example, AVSS = 0 V and AVDD = 5 V), then $V_{(AINN)}$ = 0 V is not within the common-mode input range as given by Equation 3. Therefore, a single-ended measurement with the common input connected to ground is not possible. The common input is recommended to be connected to mid-supply, or alternatively to VREFOUT. Note that the common-mode range becomes further restricted with increasing PGA gain.

If the supply is bipolar (AVSS = –2.5 V and AVDD = 2.5 V), then ground is within the common-mode input range. Single-ended measurements with the common input connected to 0 V are possible in this case.

For a detailed explanation of the common-mode input range in relation to the PGA, see the *PGA Common-Mode Voltage Requirements* section.

Application Information (continued)

9.1.5 Isolated (or Floating) Sensor Inputs

Isolated sensors (sensors that are not referenced to the ADC ground) must have a common-mode voltage established within the specified ADC input range. Level shift the common-mode voltage by external resistor biasing, by connecting the negative lead to ground (bipolar analog supply), or by connecting to a dc voltage (unipolar analog supply). The 2.048-V reference output voltage can also be used to provide level shifting to floating sensor inputs.

9.1.6 Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave unused analog inputs floating, or connect these inputs to mid-supply or to AVDD. Connecting unused analog inputs to AVSS is possible as well, but can yield higher leakage currents than the options mentioned previously.

Do not float unused digital inputs or excessive power-supply leakage current may result. Tie all unused digital inputs to the appropriate levels, DVDD or DGND, even when in power-down mode. If the $\overline{\text{DRDY}}$ output is not used, leave the pin unconnected or tied to DVDD using a weak pullup resistor.

9.1.7 Pseudo Code Example

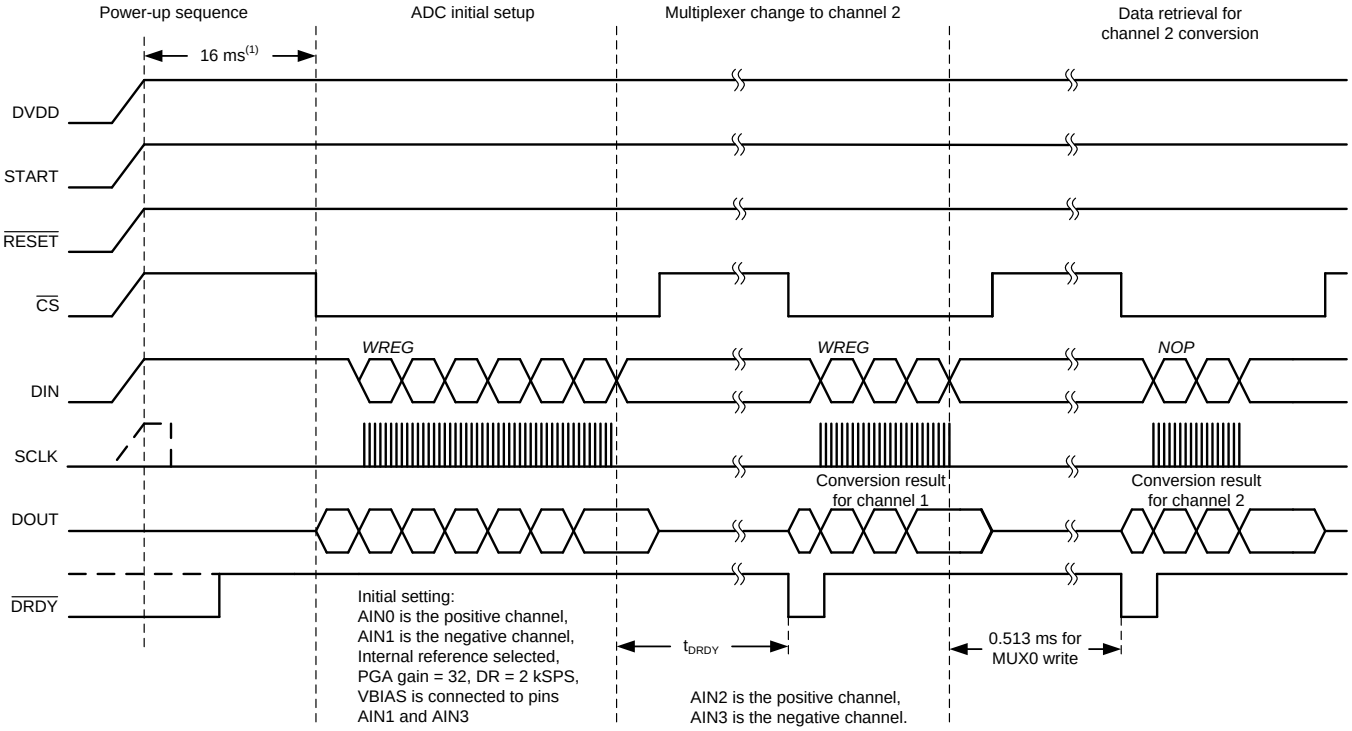
The following list shows a pseudo code sequence with the required steps to set up the device and the microcontroller that interfaces to the ADC to take subsequent readings from the ADS1148-Q1 in stop read data continuous (SDATAC) mode. In SDATAC mode, waiting for a time period longer than the data rate to retrieve the conversion result is sufficient. New conversion data does not interrupt the reading of registers or data on DOUT. However in this example, the dedicated $\overline{\text{DRDY}}$ pin is used to indicate the availability of new conversion data instead of waiting a set time period for a readout. The default configuration register settings are changed to PGA gain = 16, using the internal reference and a data rate of 20 SPS.

```
Power up;
Delay for a minimum of 16 ms to allow power supplies to settle and power-on reset to complete;
Enable the device by setting the START pin high;
Configure the serial interface of the microcontroller to SPI mode 1 (CPOL = 0, CPHA =1);
If the CS pin is not tied low permanently, configure the microcontroller GPIO connected to CS as an
output;
Configure the microcontroller GPIO connected to the DRDY pin as a falling edge triggered interrupt
input;
Set CS to the device low;
Delay for a minimum of tCSSC;
Send the RESET command (06h) to make sure the device is properly reset after power up;
Delay for a minimum of 0.6 ms;
Send the SDATAC command (16h) to prevent the new data from interrupting data or register transactions;
Write the respective register configuration with the WREG command (40h, 03h, 01h, 00h, 03h and 42h);
As an optional sanity check, read back all configuration registers with the RREG command (four bytes
from 20h, 03h);
Send the SYNC command (04h) to start the ADC conversion;
Delay for a minimum of tSCCS;
Clear CS to high (resets the serial interface);
Loop
{
    Wait for DRDY to transition low;
    Take CS low;
    Delay for a minimum of tCSSC;
    Send the RDATA command (12h);
    Send 16 SCLKs to read out conversion data on DOUT/DRDY;
    Delay for a minimum of tSCCS;
    Clear CS to high;
}
Take CS low;
Delay for a minimum of tCSSC;
Send the SLEEP command (02h) to stop conversions and put the device in power-down mode;
```

Application Information (continued)

9.1.8 Channel Multiplexing Example

This example explains a method to use the device with two sensors connected to two different analog channels. Figure 66 shows the sequence of SPI operations performed on the device. After power-up, 2^{16} t_{CLK} cycles are required before communication can be started. During the first 2^{16} t_{CLK} cycles, the device is internally held in a reset state. In this example, one of the sensors is connected to channels AIN0 and AIN1 and the other sensor is connected to channels AIN2 and AIN3. The ADC is operated at a data rate of 2 kSPS. The PGA gain is set to 32 for both sensors. VBIAS is connected to the negative terminal of both sensors (that is, channels AIN1 and AIN3). All these settings can be changed by performing a block write operation on the first four registers of the device. After the DRDY pin goes low, the conversion result can be immediately retrieved by sending in 16 SCLK pulses because the device defaults to RDATAC mode. When the conversion result is being retrieved, the active input channels can be switched to AIN2 and AIN3 by writing into the MUX0 register in a full-duplex manner, as shown in Figure 66. The write operation is completed with an additional eight SCLK pulses. The time from the write operation into the MUX0 register to the next DRDY low transition is shown in Figure 66 and is 0.513 ms in this case. After DRDY goes low, the conversion result can be retrieved and the active channel can be switched as before.



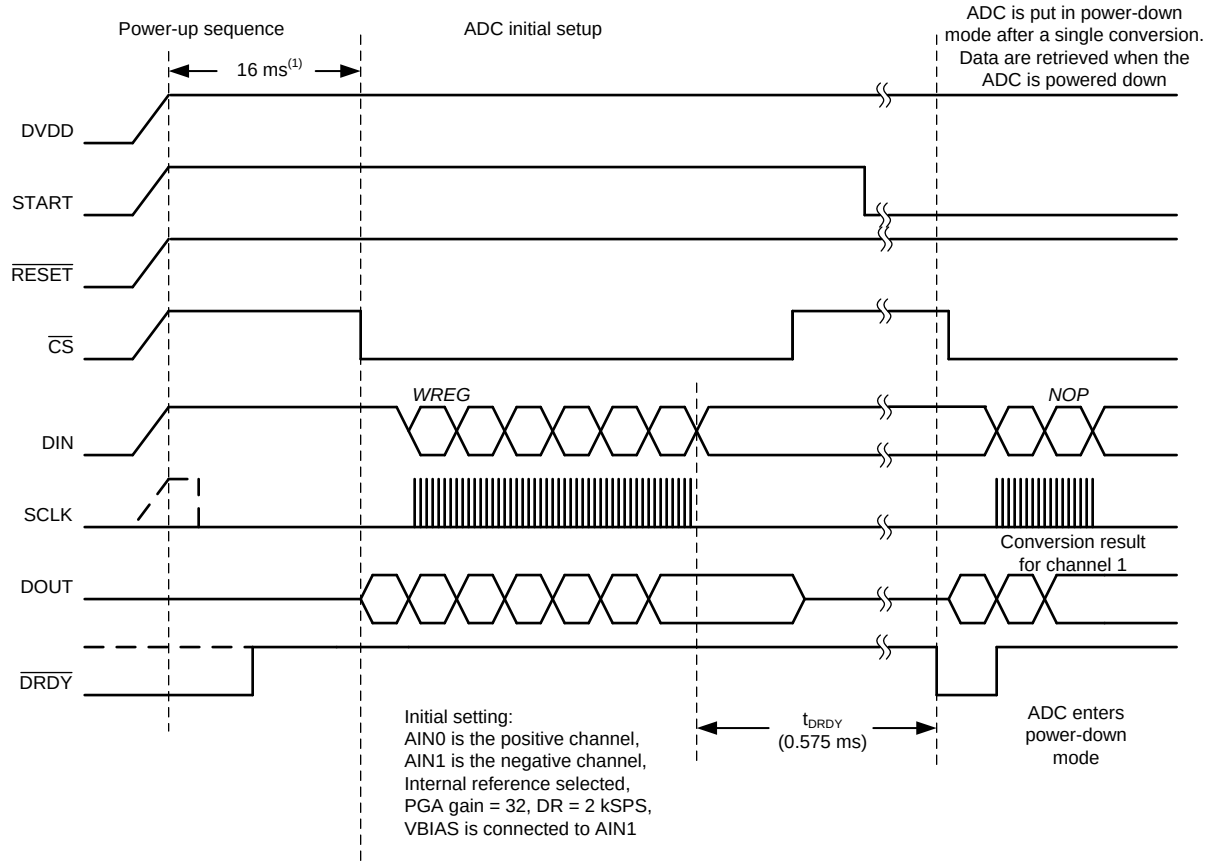
(1) For f_{CLK} = 4.096 MHz.

Figure 66. SPI Communication Sequence for Channel Multiplexing

Application Information (continued)

9.1.9 Power-Down Mode Example

This second example deals with performing one conversion after power-up and then entering power-down mode. In this example, a sensor is connected to input channels AIN0 and AIN1. Commands to set up the device must occur at least 2^{16} system clock cycles after powering up the device. The ADC operates at a data rate of 2 kSPS. The PGA gain is set to 32. VBIAS is connected to the negative terminal of the sensor (that is, channel AIN1). All these settings can be changed by performing a block write operation on the first four registers of the device. After performing the block write operation, the START pin can be taken low. The device enters the power-down mode as soon as $\overline{\text{DRDY}}$ goes low 0.575 ms after writing to the SYS0 register. The conversion result can be retrieved even after the device enters power-down mode by sending 16 SCLK pulses. Figure 67 shows the SPI communication sequence for entering power-down mode after a conversion.



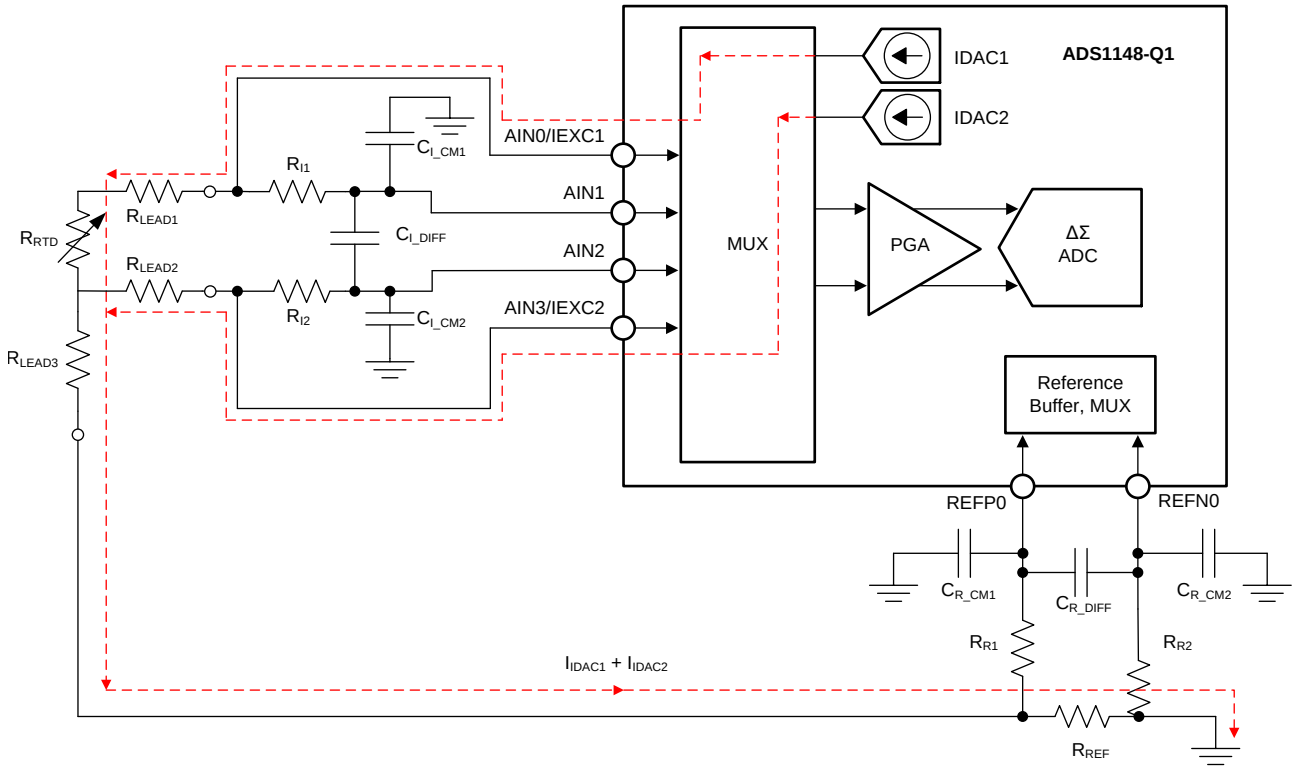
(1) For f_{CLK} = 4.096 MHz.

Figure 67. SPI Communication Sequence for Entering Power-Down Mode After a Conversion

9.2 Typical Applications

9.2.1 Ratiometric 3-Wire RTD Measurement System

Figure 68 shows a 3-wire RTD application circuit with lead-wire compensation using the ADS1148-Q1. The two IDAC current sources integrated in the ADS1148-Q1 are used to implement the lead-wire compensation. One IDAC current source (IDAC1) provides excitation to the RTD element. The other current source (IDAC2) has the same current setting, providing cancellation of lead-wire resistance by generating a voltage drop across the lead-wire resistance R_{LEAD2} equal to the voltage drop across R_{LEAD1}. The voltages across the lead-wire resistances cancel because the voltage across the RTD is measured differentially at ADC pins AIN1 and AIN2. The ADC reference voltage (pins REFP0 and REFN0) is derived from the voltage across R_{REF} with the currents from IDAC1 and IDAC2, providing ratiometric cancellation of the current-source drift. R_{REF} also level shifts the RTD signal to within the ADC specified common-mode input range.



(1) Not all analog inputs are shown.

Figure 68. Ratiometric 3-Wire RTD Measurement System Featuring the ADS1148-Q1

Typical Applications (continued)

9.2.1.1 Design Requirements

Table 29 shows the design requirements of the 3-wire RTD application.

Table 29. 3-Wire RTD Application Requirements

PARAMETER	VALUE
Supply voltage	3.3 V
Data rate	20 SPS
RTD type	3-wire PT100
RTD excitation current	1 mA
Temperature	–200°C to +850°C
Calibrated temperature measurement accuracy at T_A = 25°C (1)	±0.2°C

(1) Not accounting for error of RTD; a two-point gain and offset calibration are performed, as well as chopping of the excitation currents to remove IDAC mismatch errors.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Topology

Figure 69 shows the basic topology of a ratiometric measurement using an RTD. Shown are the ADC with the RTD and a reference resistor R_{REF}. A single current source, labeled IDAC1, is used to excite the RTD as well as to establish a reference voltage for the ADC across R_{REF}.

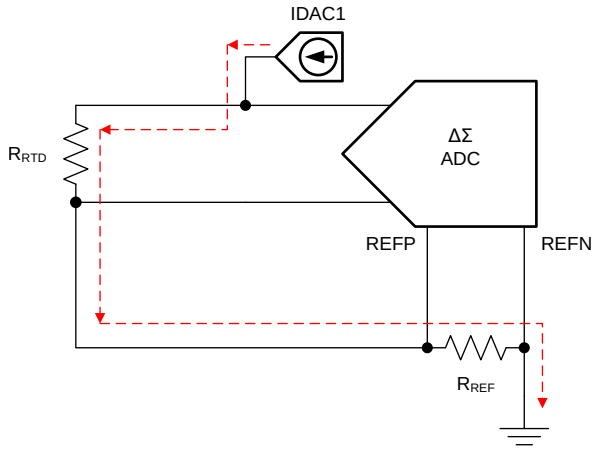


Figure 69. Example of a Ratiometric RTD Measurement

With IDAC1, the ADC measures the RTD voltage using the voltage across R_{REF} as the reference. This process gives a measurement such that the output code is proportional to the ratio of the RTD voltage and the reference voltage, as shown in Equation 21 and Equation 22.

$$\text{Code} \propto V_{RTD} / V_{REF} \quad (21)$$

$$\text{Code} \propto (R_{RTD} \times I_{IDAC1}) / (R_{REF} \times I_{IDAC1}) \quad (22)$$

The currents cancel so that Equation 22 reduces to Equation 23:

$$\text{Code} \propto R_{RTD} / R_{REF} \quad (23)$$

As shown in Equation 23, the measurement depends on the resistive value of the RTD and the reference resistor R_{REF}, but not on the IDAC1 current value. Therefore, the absolute accuracy and temperature drift of the excitation current does not matter. This measurement is ratiometric. As long as there is no current leakage from IDAC1 outside of this circuit, the measurement depends only on R_{RTD} and R_{REF}.

In Figure 70, the lead resistances of a 3-wire RTD are shown and another excitation current source is added, labeled IDAC2.

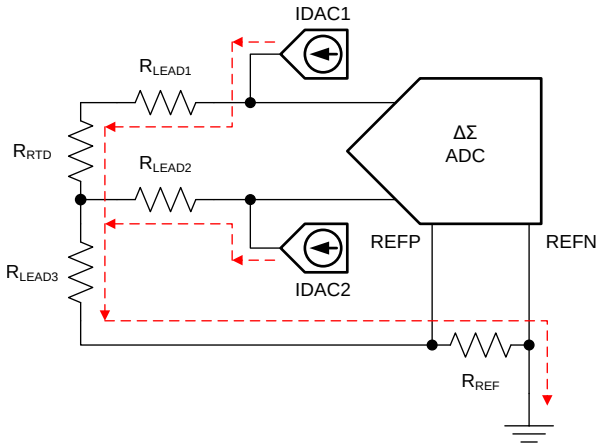


Figure 70. Example of a Lead Wire Compensation

With a single excitation current source, R_{LEAD1} adds an error to the measurement. By adding IDAC2, the second excitation current source is used to cancel out the error in the lead wire resistance. When adding the lead resistances and the second current source, Equation 22 becomes:

$$\text{Code} \propto [V_{RTD} + (R_{LEAD1} \times I_{IDAC1}) - (R_{LEAD2} \times I_{IDAC2})] / [V_{REF} \times (I_{IDAC1} + I_{IDAC2})] \quad (24)$$

If the lead resistances match and the excitation currents match, then $R_{LEAD1} = R_{LEAD2}$ and $I_{IDAC1} = I_{IDAC2}$. The lead wire resistances cancel out so that Equation 24 reduces to the result in Equation 25, thus maintaining a ratiometric measurement.

$$\text{Code} \propto R_{RTD} / (2 \times R_{REF}) \quad (25)$$

R_{LEAD3} is not part of the measurement because this lead resistance is not in the input measurement path or in the reference input path.

As Equation 24 shows, the two current sources must be matched to cancel the lead resistances of the RTD wires. Any mismatch in the two current sources is minimized by using the multiplexer to swap or *chop* the two current sources between the two inputs. Taking measurements in both configurations and averaging the readings reduces the effects of mismatched current sources. The design uses the multiplexer in the ADS1148-Q1 to implement this chopping technique to remove the mismatch error between IDAC1 and IDAC2.

9.2.1.2.2 RTD Selection

The RTD is first chosen to be a PT100 element. The RTD resistance is defined by the Callendar-Van Dusen (CVD) equations and the resistance of the RTD is known depending on the temperature. The PT100 RTD has an impedance of 100 Ω at 0°C and roughly 0.385 Ω of resistance change per 1°C in temperature change. With a desired temperature measurement accuracy of 0.2°C, this value translates to a resistive measurement accuracy of approximately 0.077 Ω. The RTD resistance at the low end of the temperature range of –200°C is 18.59 Ω and the resistance at the high end of the temperature range of 850°C is 390.48 Ω.

9.2.1.2.3 Excitation Current

For the best possible resolution, the voltage across the RTD must be made as large as possible compared to the noise floor in the measurement. In general, measurement resolution improves with increasing excitation current. However, a larger excitation current creates self-heating in the RTD that causes drift and error in the measurement. The selection of excitation currents trades off resolution against sensor self-heating.

The excitation current sources in this design are selected to be 1 mA. This selection maximizes the value of the RTD voltage and keeps the self-heating low. The typical range of RTD self-heating coefficients is 2.5 mW/°C for small, thin-film elements and 65 mW/°C for larger, wire-wound elements. With a 1-mA excitation at the maximum RTD resistance value, the power dissipation in the RTD is less than 0.4 mW and keeps the measurement errors resulting from self-heating to less than 0.01°C.

As mentioned in the *Topology* section, chopping of the excitation current sources cancels mismatches between the IDACs. This technique is necessary for obtaining the best possible accuracy from the system. Mismatch between the excitation current sources is a large source of error if chopping is not implemented.

The internal reference voltage must be enabled when using the IDACs, even if an external ratiometric measurement is used for ADC conversions.

Table 30 shows the ADS1148-Q1 register settings for setting up the internal reference and the excitation current sources.

Table 30. Register Bit Settings for Excitation Current Sources

REGISTER	ADDRESS	BIT NAME	BIT VALUES	COMMENT
MUX1(1)	02h	VREFCON[1:0]	01	Internal reference enabled
MUX1	02h	REFSELT[1:0]	00	REFP0 and REFN0 reference inputs selected
IDAC0	0Ah	IMAG[2:0]	110	IDAC magnitude = 1 mA
IDAC1	0Bh	I1DIR[3:0](2)	0000	IDAC1 = AIN0
IDAC1	0Bh	I2DIR[3:0](2)	0011	IDAC2 = AIN3

(1) The internal reference is required to be enabled to use the IDAC current sources.
(2) To implement chopping, swap the IDAC1 direction for the IDAC2 direction. Set I1DIR[3:0] = 0011 and I2DIR[3:0] = 0000.

9.2.1.2.4 Reference Resistor (R_{REF})

The common-mode voltage of the measurement is recommended to be set near mid-supply, which helps keep the input within the common-mode input range of the PGA.

The reference resistor is selected to be 820 Ω. The voltage across R_{REF} is calculated from Equation 26.

$$V_{REF} = R_{REF} \times (I_{IDAC1} + I_{IDAC2}) = 820\ \Omega \times 2\ mA = 1.64\ V \quad (26)$$

With AVDD = 3.3 V, Equation 26 shows that the input voltage is just below mid-supply.

The excitation current sources operate properly to a maximum IDAC compliance voltage. The current sources lose current regulation above this compliance voltage. In this example, the output voltage of the excitation current source is calculated from the sum of the voltages across the RTD and R_{REF}, as shown in Equation 27.

$$V_{IDAC1\ MAX} = R_{RTD\ MAX} \times I_{IDAC1} + [R_{REF} \times (I_{IDAC1} + I_{IDAC2})] = 0.4\ V + 1.64\ V = 2.04\ V \quad (27)$$

A compliance voltage of 3.3 V – 2.04 V = 1.26 V is sufficient for proper IDAC operation. See Figure 9 and Figure 10 in the *Typical Characteristics* section for details.

Because the voltage across R_{REF} sets the reference voltage for the ADC, the tolerance and temperature drift of R_{REF} directly affects the measurement gain. A resistor with a 0.01% maximum tolerance is selected for this measurement.

9.2.1.2.5 PGA Setting

Because the excitation current is small to reduce self-heating, the PGA in the ADS1148-Q1 is used to amplify the signal across the RTD to use the full-scale range of the ADC. Starting with the reference voltage, the ADC is able to measure a differential input signal range of ±1.64 V. The maximum allowable PGA gain setting is based on the reference voltage, the maximum RTD resistance, and the excitation current.

As mentioned previously, the resistance of the RTD is a maximum of 850°C. The voltage measured at this temperature is at maximum and is given by:

$$V_{RTD\ MAX} = R_{RTD@850°C} \times I_{IDAC1} = 390.48\ \Omega \times 1\ mA = 390.48\ mV$$

where

- $R_{RTD@850°C}$ is 390.48 Ω (28)

With a reference voltage of 1.64 V, the maximum gain for the PGA, without overranging the ADC, is shown in Equation 29.

$$Gain_{MAX} = V_{REF} / V_{RTD\ MAX} = 1.64\ V / 390.48\ mV = 4.2\ V/V \quad (29)$$

Selecting a PGA gain of 4 gives a maximum measurement of 95% of the positive full-scale range. Table 31 shows the register settings to set the PGA gain as well as the inputs for the ADC.

Table 31. Register Bit Settings for the Input Multiplexer and PGA

REGISTER	ADDRESS	BIT NAME	BIT VALUES	COMMENT
MUX0	01h	MUX_SP[2:0]	001	AIN_P = AIN1
MUX0	01h	MUX_SN[2:0]	010	AIN_N = AIN2
SYS0	03h	PGA[2:0]	010	PGA Gain = 4

9.2.1.2.6 Common-Mode Input Range

Now that the component values are selected, the common-mode input range must be verified to ensure that the ADC and PGA are not limited in operation. Start with the maximum input voltage, which gives the most restriction in the common-mode input range. At the maximum input voltage, the common-mode input voltage detected by the ADC is shown in Equation 30.

$$V_{CM} = V_{REF} + (V_{RTD\_MAX} / 2) = 1.64\ V + (390.48\ mV / 2) = 1.835\ V \quad (30)$$

As mentioned in the *Low-Noise PGA* section, the common-mode input range is shown in Equation 3 and is applied to Equation 31.

$$AVSS + 0.1\ V + (V_{RTD\_MAX} \times Gain) / 2 \le V_{CM} \le AVDD - 0.1\ V - (V_{RTD\_MAX} \times Gain) / 2 \quad (31)$$

After substituting in the appropriate values, the common-mode input range can be found in Equation 32 and Equation 33.

$$0\ V + 0.1\ V + (390.48\ mV \times 4) / 2 \le V_{CM} \le 3.3\ V - 0.1\ V - (390.48\ mV \times 4) / 2 \quad (32)$$

$$881\ mV \le V_{CM} \le 2.42\ V \quad (33)$$

Because V_{CM} = 1.835 V is within the limits of Equation 33, the RTD measurement is within the input common-mode range of the ADC and PGA. At the RTD voltage minimum ($V_{RTD\ MIN}$ = 18.59 mV), a similar calculation can be made to show that the input common-mode voltage is within the range as well.

9.2.1.2.7 Input and Reference Low-Pass Filters

The differential filters chosen for this application are designed to have a –3-dB corner frequency at least 10 times larger than the bandwidth of the ADC. The selected ADS1148-Q1 sampling rate of 20 SPS results in a –3-dB bandwidth of 14.8 Hz. The –3-dB filter corner frequency is set to be roughly 250 Hz at a mid-scale measurement resistance. For proper operation, the differential cutoff frequencies of the reference and input low-pass filters must be well matched. This matching can be difficult because when the resistance of the RTD changes over the span of the measurement, the filter cutoff frequency changes as well. To mitigate this effect, the two resistors used in the input filter (R_{I1} and R_{I2}) are chosen to be two orders of magnitude larger than the RTD. Input bias currents of the ADC causes a voltage drop across the filter resistors that shows up as a differential offset error if the bias currents or filter resistors are not equal. The resistors are recommended to be limited to at most 10 kΩ to reduce dc offset errors resulting from the input bias current. R_{I1} and R_{I2} are chosen to be 4.7 kΩ.

The input filter differential capacitor (C_{I_DIFF}) is calculated starting from the cutoff frequency, as shown in Equation 34 and Equation 35.

$$f_{-3dB\_DIFF} = 1 / (2\ \pi \times C_{I\_DIFF} \times (R_{I1} + R_{RTD} + R_{I2})) \quad (34)$$

$$f_{-3dB\_DIFF} = 1 / (2\ \pi \times C_{I\_DIFF} \times (4.7\ k\Omega + 150\ \Omega + 4.7\ k\Omega)) \quad (35)$$

After solving for C_{I_DIFF}, the capacitor is chosen to be a standard value of 68 nF.

To ensure that mismatch of the common-mode filter capacitors does not translate to a differential voltage, the common-mode capacitors (C_{I_CM1} and C_{I_CM2}) are chosen to be 10 times smaller than the differential capacitor, making each capacitor 6.8 nF. These capacitor values result in a common-mode cutoff frequency that is roughly 20 times larger than the differential filter, making the matching of the common-mode cutoff frequencies less critical.

After substituting values into Equation 36 and Equation 37, the common-mode cutoff frequencies are found to be f_{-3dB_CM+} = 4.13 kHz and f_{-3dB_CM-} = 4.24 kHz, respectively.

$$f_{-3dB\_CM+} = 1 / [2\ \pi \times C_{I\_CM1} \times (R_{I1} + R_{RTD} + R_{REF})] \quad (36)$$

$$f_{-3dB\_CM-} = 1 / (2\ \pi \times C_{I\_CM1} \times (R_{I2} + R_{REF})) \quad (37)$$

Often, filtering the reference input is not necessary and adding bulk capacitance at the reference input is sufficient. However, equations showing a design procedure calculating filter values for the reference inputs are shown in Equation 38 and Equation 39.

The differential reference filter is designed to have a –3-dB corner frequency of 250 Hz to match the differential input filter. The two reference filter resistors are selected to be 9.09 kΩ, which is several times larger than the value of R_{REF}. The reference filter resistors must not be sized larger than 10 kΩ or dc bias errors become significant. The differential capacitor for the reference filter is calculated as shown in Equation 38.

$$f_{-3dB\_DIFF} = 1 / [2 \pi \times C_{R\_DIFF} \times (R_{R1} + R_{RTD} + R_{R2})] \quad (38)$$

$$C_{R\_DIFF} \approx 33 \text{ nF} \quad (39)$$

After solving for C_{R_DIFF}, the capacitor is chosen to be a standard value of 33 nF.

To ensure that mismatch of the common-mode filter capacitors does not translate to a differential voltage, the reference common-mode capacitors (C_{R_CM1} and C_{R_CM2}) are chosen to be 10 times smaller than the reference differential capacitor, making these capacitors each 3.3 nF. Again, the resulting cutoff frequency for the common-mode filters is roughly 20 times larger than the differential filter, making the matching of the cutoff frequencies less critical.

After substituting values into Equation 40 and Equation 41, common-mode cutoff frequencies for the reference filter are found to be f_{-3dB_CM+} = 4.87 kHz and f_{-3dB_CM+} = 5.31 kHz, respectively.

$$f_{-3dB\_CM+} = 1 / [2 \pi \times C_{R\_CM1} \times (R_{R1} + R_{REF})] \quad (40)$$

$$f_{-3dB\_CM-} = 1 / (2 \pi \times C_{R\_CM2} \times R_{R2}) \quad (41)$$

9.2.1.2.8 Register Settings

The register settings for this design are shown in Table 32.

Table 32. Register Settings

REGISTER ADDRESS	REGISTER NAME	SETTING	DESCRIPTION
00h	MUX0	0Ah	Select AIN_P = AIN1 and AIN_N = AIN2
01h	VBIAS	00h	—
02h	MUX1	20h	Internal reference enabled, REFP0 and REFN0 reference inputs selected
03h	SYS0	22h	PGA gain = 4, DR = 20 SPS
04h	OFC0 (1)	xxh	—
05h	OFC1	xxh	—
06h	OFC2	xxh	—
07h	FSC0 (1)	xxh	—
08h	FSC1	xxh	—
09h	FSC2	xxh	—
0Ah	IDAC0	x6h	ID bits can be version dependent, IDAC magnitude set to 1 mA
0Bh	IDAC1	03h (2)	IDAC1 set to AIN0; IDAC2 set to AIN3
0Ch	GPIOCFG	00h	—
0Dh	GPIOCDIR	00h	—
0Eh	GPIODAT	00h	—

(1) A two-point gain calibration and offset calibration removes errors from the R_{REF} tolerance, offset voltage, and gain error. The results are used for the OFC and FSC registers.
(2) To chop the excitation current sources, swap the output pins with the IDAC1 register and set to 30h.

9.2.1.3 Application Curves

To test the accuracy of the acquisition circuit, a series of calibrated, high-precision discrete resistors are used as the input to the system. Measurements are taken at T_A = 25°C. Figure 71 displays the uncalibrated resistance measurement accuracy of the system over an input span from 20 Ω to 400 Ω. For each resistor value, 512 measurements are taken. With each measurement, IDAC1 and IDAC2 are chopped to remove the excitation current mismatch.

The uncalibrated measurement error is displayed in Figure 72. The offset and gain error can be primarily attributed to the offset and gain error of the ADC. However, the accuracy of R_{REF} contributes directly to the accuracy of the measurement. To keep the gain error low, R_{REF} must be a low-drift precision resistor.

Precision temperature measurement applications are typically calibrated to remove the effects of gain and offset errors, which generally dominate the total system error. The simplest calibration method is a linear, or two-point, calibration that applies an equal and opposite gain and offset term to cancel the measured system gain and offset errors. Using the results of Figure 72, the uncalibrated gain and offset error are then used to modify the offset calibration and the full-scale calibration registers in the device. The results of this calibrated system measurement are shown in Figure 73.

The results in Figure 73 are converted to temperature accuracy by dividing the results by the RTD sensitivity (α) at the measured resistance. Over the full resistance input range, the maximum total measured error is ±0.011 Ω. Equation 42 uses the measured resistance error and the nominal RTD sensitivity to calculate the measured temperature accuracy.

$$Error\ (^{\circ}C) = \frac{Error\ (\Omega)}{\alpha_{@0^{\circ}C}} = \frac{0.011\,\Omega}{0.385\,\frac{\Omega}{^{\circ}C}} = \pm 0.0286^{\circ}C \tag{42}$$

Figure 74 displays the calculated temperature measurement accuracy of the circuit assuming a linear RTD resistance to temperature response. Figure 74 does not include any linearity compensation of the RTD.

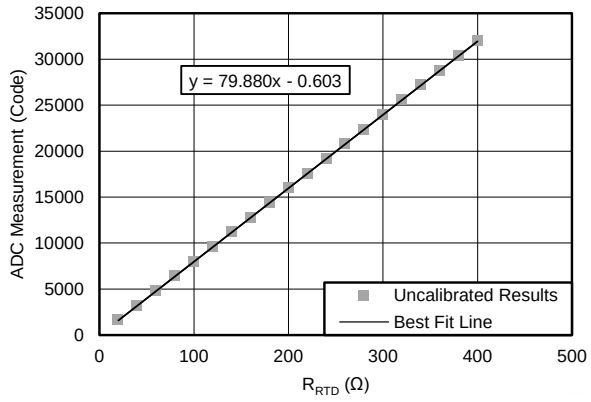


Figure 71. Resistance Measurement Results With Precision Resistors Before Calibration

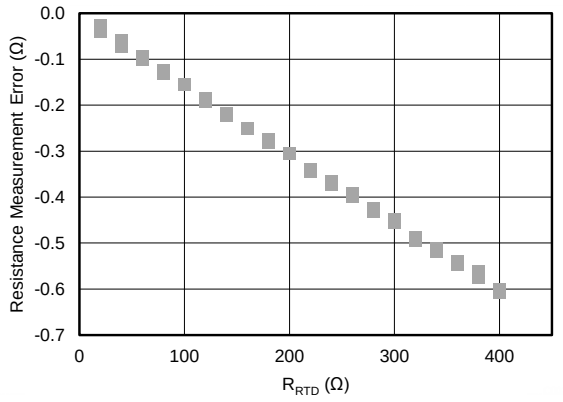


Figure 72. Resistance Measurement Error With Precision Resistors Before Calibration

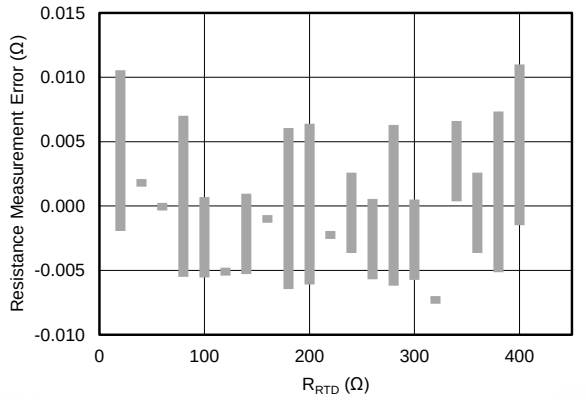


Figure 73. Resistance Measurement Error With Precision Resistors After Calibration

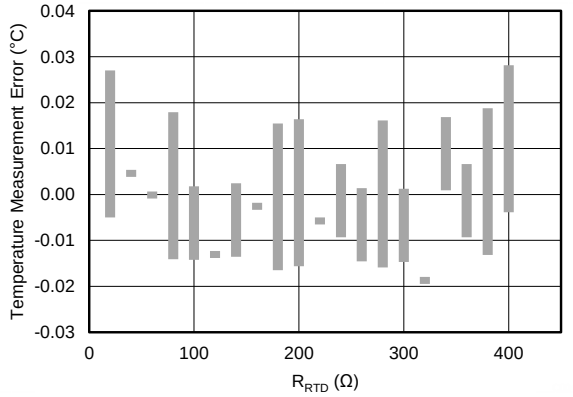


Figure 74. Calculated Temperature Measurement Error from Resistance Measurement Error

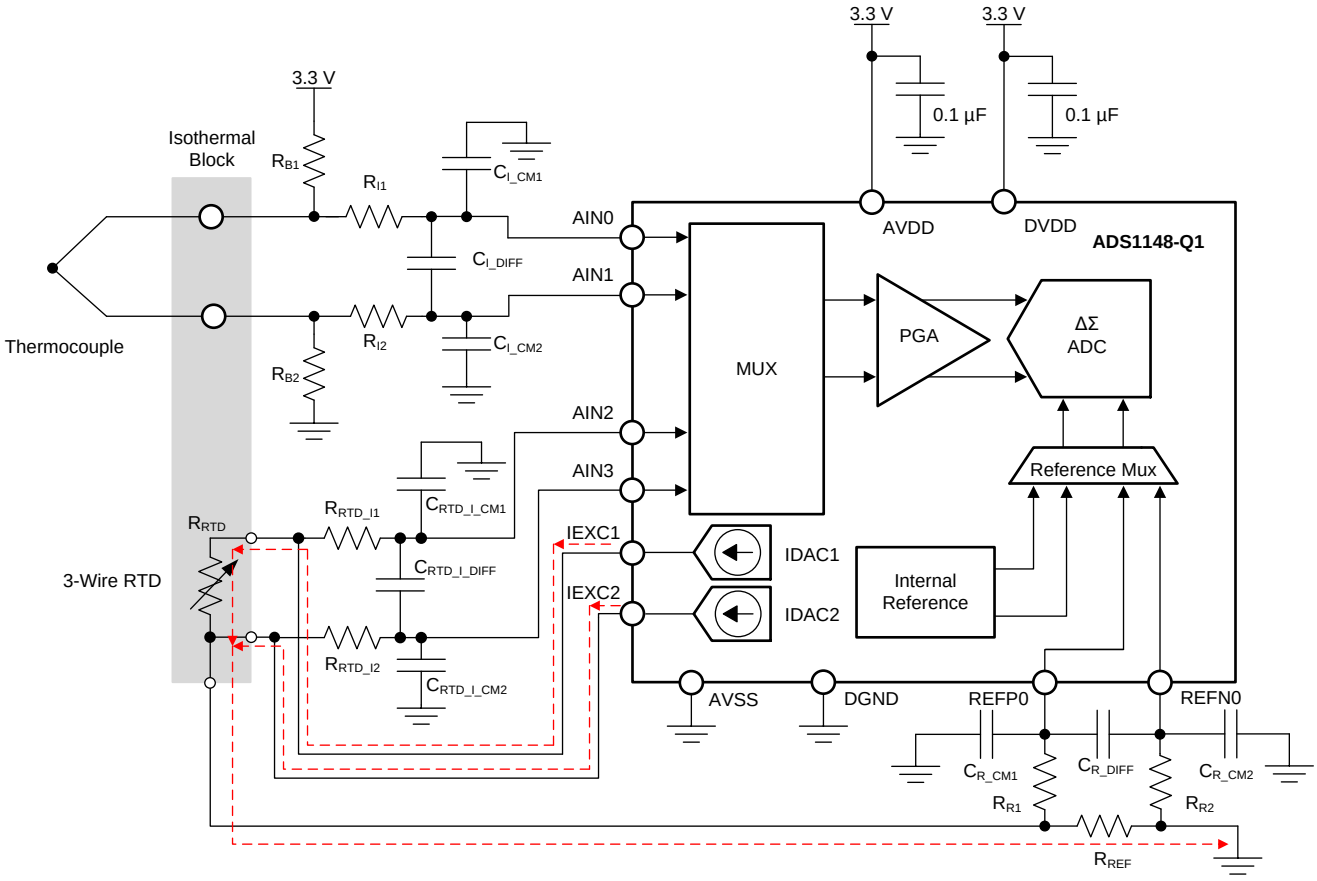
Table 33 compares the measurement accuracy with the design goal from Table 29.

Table 33. Comparison of Design Goals and Measured Performance

PARAMETER	GOAL	MEASURED
Calibrated resistance measurement accuracy at T_A = 25ºC	±0.077 Ω	±0.011 Ω
Calibrated temperature measurement accuracy at T_A = 25ºC	±0.2°C	±0.029°C

9.2.2 K-Type Thermocouple Measurement (–200°C to +1250°C) With Cold-Junction Compensation

Figure 75 shows the basic connections of a thermocouple measurement system. This circuit uses a cold-junction compensation measurement based on the *Ratiometric 3-Wire RTD Measurement System* topology described in the *Ratiometric 3-Wire RTD Measurement System* example. Using the IEXC1 and IEXC2 pins allows for routing of the IDAC currents without using any other analog pins. Along with the thermocouple and cold-junction measurements, four other analog inputs (AIN4 to AIN7, not shown in the schematic) are available for alternate measurements or use as GPIO pins.



(1) Not all analog inputs are shown.

Figure 75. Thermocouple Measurement System Using the ADS1148-Q1

9.2.2.1 Design Requirements

Table 34 shows the design requirements of the thermocouple application.

Table 34. Example Thermocouple Application Requirements

PARAMETER	VALUE
Supply voltage	3.3 V
Reference voltage	Internal 2.048-V reference
Update rate	≥ 10 readings per second
Thermocouple type	K
Temperature measurement	–200ºC to +1250ºC
Measurement accuracy at T_A = 25ºC (1)	±0.5ºC

(1) Not accounting for error of thermocouple and the cold-junction measurement; offset calibration is performed at $T_{(TC)} = T_{(CJ)} = 25°C$; no gain calibration.

9.2.2.2 Detailed Design Procedure

9.2.2.2.1 Biasing Resistors

The biasing resistors R_{B1} and R_{B2} are used to set the common-mode voltage of the thermocouple to within the specified common-mode voltage range of the PGA (in this example, to mid-supply AVDD / 2). If the application requires the thermocouple to be biased to GND, a bipolar supply (for example, AVDD = 2.5 V and AVSS = –2.5 V) must be used for the device to meet the common-mode voltage requirement of the PGA. When choosing the values of the biasing resistors, care must be taken so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 MΩ to 50 MΩ.

In addition to biasing the thermocouple, R_{B1} and R_{B2} are also useful for detecting an open thermocouple lead. When one of the thermocouple leads fails open, the biasing resistors pull the analog inputs (AIN0 and AIN1) to AVDD and AVSS, respectively. The ADC consequently reads a full-scale value, which is outside the normal measurement range of the thermocouple voltage, to indicate this failure condition.

9.2.2.2.2 Input Filtering

Although the digital filter attenuates high-frequency components of noise, a first-order, passive RC filter is recommended to be provided at the inputs to further improve performance. The differential RC filter formed by R_{I1}, R_{I2}, and the differential capacitor C_{I_DIFF} offers a cutoff frequency that is calculated using Equation 43.

$$f_C = 1 / [2 \pi \times (R_{I1} + R_{I2}) \times C_{I\_DIFF})] \quad (43)$$

Two common-mode filter capacitors (C_{I_CM1} and C_{I_CM2}) are also added to offer attenuation of high-frequency, common-mode noise components. The differential capacitor C_{I_DIFF} is recommended to be at least an order of magnitude (10 times) larger than the common-mode capacitors (C_{I_CM1} and C_{I_CM2}) because mismatches in the common-mode capacitors can convert common-mode noise into differential noise.

The filter resistors R_{F1} and R_{F2} also serve as current-limiting resistors. These resistors limit the current into the analog inputs (AIN0 and AIN1) of the device to safe levels if an overvoltage on the inputs occurs. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. For thermocouple measurements, limit the filter resistor values to below 10 kΩ.

The filter component values used in this design are: $R_{I1} = R_{I2} = 1$ kΩ, $C_{I\_DIFF} = 100$ nF, and $C_{I\_CM1} = C_{I\_CM2} = 10$ nF.

9.2.2.2.3 PGA Setting

The highest measurement resolution is achieved when matching the largest potential input signal to the FSR of the ADC by choosing the highest possible gain. From the design requirement, the maximum thermocouple voltage occurs at $T_{TC} = 1250$°C and is $V_{TC} = 50.644$ mV, as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature of $T_{CJ} = 0$°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to –40°C. A K-type thermocouple at $T_{TC} = 1250$°C produces an output voltage of $V_{TC} = 50.644$ mV – (–1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of $T_{CJ} = –40$°C. The maximum gain that can be applied when using the internal 2.048-V reference is then calculated as 39.3 from Equation 44. The next smaller PGA gain setting the device offers is 32.

$$Gain_{MAX} = V_{REF} / V_{TC\ MAX} = 2.048\ V / 52.171\ mV = 39.3 \quad (44)$$

9.2.2.2.4 Cold-Junction Measurement

AIN2 and AIN3 are attached to a 3-wire RTD that is used to measure the cold-junction temperature. Similar to the example in the *Ratiometric 3-Wire RTD Measurement System* section, the 3-wire RTD design is the same except the inputs and excitation current sources have been changed. Note that R_{REF} and PGA Gain can be optimized for a reduced temperature range.

The device does not perform an automatic cold-junction compensation of the thermocouple. This compensation must be done in the microcontroller that interfaces to the device. The microcontroller requests one or multiple readings of the thermocouple voltage from the device and then sets the device to measure the cold junction with the RTD to compensate for the cold-junction temperature.

An algorithm similar to the following must be implemented on the microcontroller to compensate for the cold-junction temperature:

1. Measure the thermocouple voltage, $V_{(TC)}$, between AIN0 and AIN1.
2. Measure the temperature of the cold junction, $T_{(CJ)}$, using a ratiometric measurement with the 3-wire RTD across AIN2 and AIN3.
3. Convert the cold-junction temperature into an equivalent thermoelectric voltage, $V_{(CJ)}$, using the tables or equations provided by NIST.
4. Add $V_{(TC)}$ and $V_{(CJ)}$ and translate the summation back into a thermocouple temperature using the NIST tables or equations again.

There are alternate methods of measuring the cold-junction temperature. The additional analog input channels of the device can be used in this case to measure the cold-junction temperature with a thermistor or an alternate analog temperature sensor.

9.2.2.2.5 Calculated Resolution

To get an approximation of the achievable temperature resolution, the peak-to-peak noise of the ADS1148-Q1 at gain = 32 and DR = 20 SPS (1.95 μV_{PP}) is taken from Table 1. The noise is divided by the average sensitivity of a K-type thermocouple (41 µV/°C), as shown in Equation 45.

$$\text{Temperature Resolution} = 1.95\ \mu V / 41\ \mu V/°C = 0.048°C \quad (45)$$

9.2.2.2.6 Register Settings

The register settings for this design are shown in Table 35. The inputs are selected to measure the thermocouple and the internal reference is enabled and selected. The excitation current sources are also enabled and selected. Although this configuration consumes some power, this setting allows for a quick transition for the cold-junction measurement.

Table 35. Register Settings for the Thermocouple Measurement

REGISTER ADDRESS	REGISTER NAME	SETTING	DESCRIPTION
00h	MUX0	01h	Select AIN_P = AIN0, AIN_N = AIN1
01h	VBIAS	00h	—
02h	MUX1	30h	Internal reference enabled, internal reference selected
03h	SYS0	52h	PGA gain = 32, DR = 20 SPS
04h	OFC0	xxh	—
05h	OFC1	xxh	—
06h	OFC2	xxh	—
07h	FSC0	xxh	—
08h	FSC1	xxh	—
09h	FSC2	xxh	—
0Ah	IDAC0	x6h	IDAC magnitude set to 1 mA
0Bh	IDAC1	89h	IDAC1 set to IEXC1, IDAC2 set to IEXC2
0Ch	GPIOCFG	00h	—
0Dh	GPIOCDIR	00h	—
0Eh	GPIODAT	00h	—

Changing to the cold-junction measurement, the registers are set to measure the RTD. This measurement requires changing the input, the reference input, the gain, and any calibration settings required for the measurement accuracy. Table 36 shows the register settings for the RTD measurement used for cold-junction compensation.

Table 36. Register Settings for the Cold-Junction Measurement

REGISTER ADDRESS	REGISTER NAME	SETTING	DESCRIPTION
00h	MUX0	13h	Select AIN_P = AIN2, AIN_N = AIN3
01h	VBIAS	00h	—
02h	MUX1	20h	Internal reference enabled, REFP0 and REFN0 selected
03h	SYS0	22h	PGA gain = 4, DR = 20 SPS
04h	OFC0	xxh	Calibration values are different between measurement settings
05h	OFC1	xxh	—
06h	OFC2	xxh	—
07h	FSC0	xxh	—
08h	FSC1	xxh	—
09h	FSC2	xxh	—
0Ah	IDAC0	x6h	IDAC magnitude set to 1 mA
0Bh	IDAC1	89h	IDAC1 set to IEXC1, IDAC2 set to IEXC2
0Ch	GPIOCFG	00h	—
0Dh	GPIOCDIR	00h	—
0Eh	GPIODAT	00h	—

9.3 Do's and Don'ts

- Do partition the analog, digital, and power supply circuitry into separate sections on the PCB.
- Do use a single ground plane for analog and digital grounds.
- Do place the analog components close to the ADC pins using short, direct connections.
- Do keep the SCLK pin free of glitches and noise.
- Do verify that the analog input voltages are within the specified PGA input voltage range under all input conditions.
- Do float unused analog input pins to minimize input leakage current. Connecting unused pins to AVDD is the next best option.
- Do provide current limiting to the analog inputs in case overvoltage faults occur.
- Do use a low-dropout linear regulator (LDO) to reduce ripple voltage generated by switch-mode power supplies, which is especially true for AVDD where the supply noise can negatively affect the performance.
- Don't cross analog and digital signals.
- Don't allow the analog and digital power supply voltages to exceed 5.5 V under any conditions, even during power-up and power-down.

Figure 76 illustrates the Do's and Don'ts of the ADC circuit connections.

Do's and Don'ts (continued)

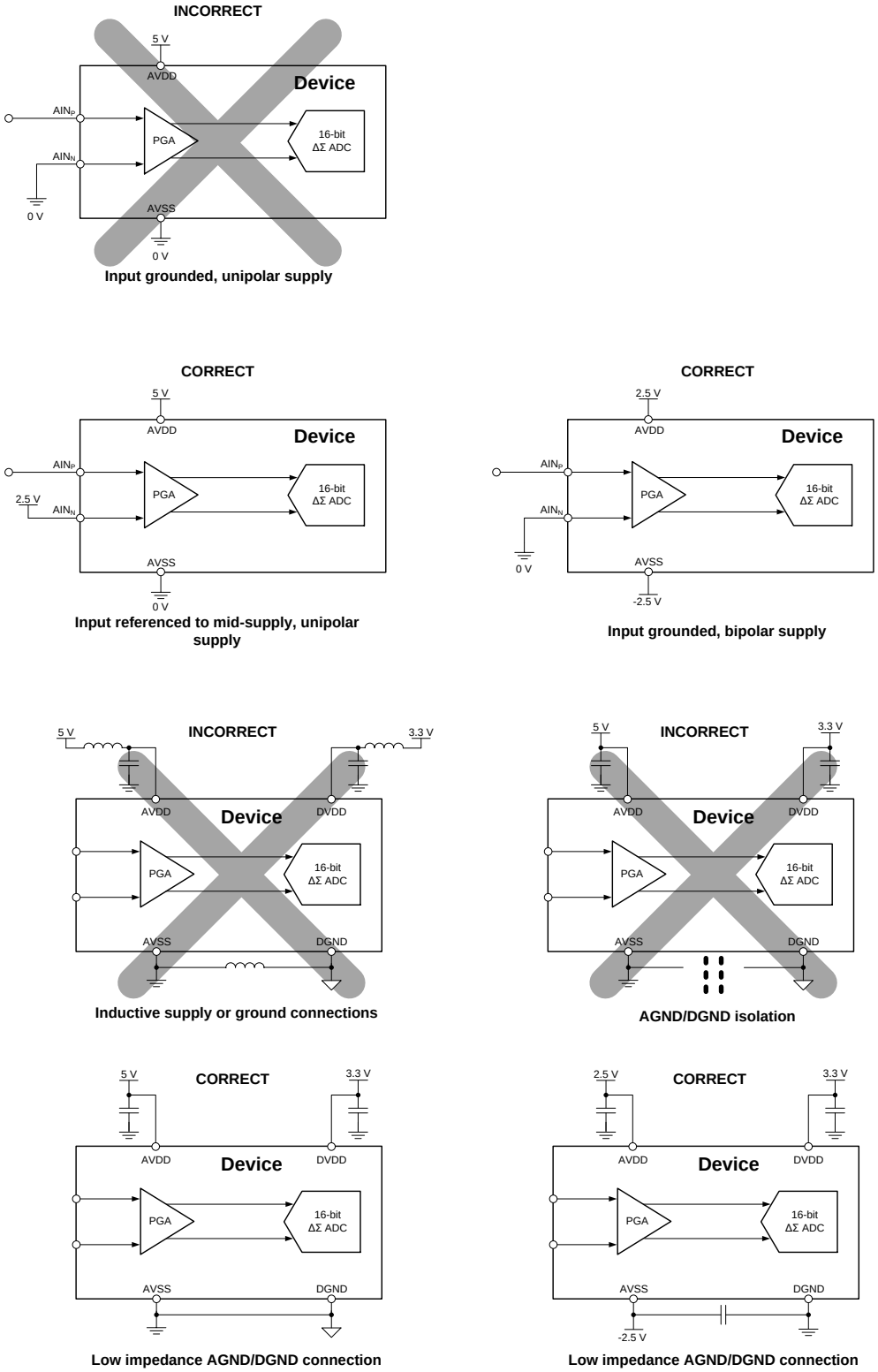


Figure 76. Do's and Don'ts, Circuit Connections

10 Power Supply Recommendations

The device requires two power supplies: analog (AVDD, AVSS) and digital (DVDD, DGND). The analog power supply can be bipolar (for example, AVDD = 2.5 V, AVSS = –2.5 V) or unipolar (for example, AVDD = 3.3 V, AVSS = 0 V) and is independent of the digital power supply. The digital supply sets the digital I/O levels (with the exception of the GPIO levels that are set by the analog supply of AVDD to AVSS).

10.1 Power Supply Sequencing

The power supplies can be sequenced in any order but in no case must any analog or digital inputs exceed the respective analog or digital power-supply voltage limits. Wait at least 2^{16} t_{CLK} cycles after all power supplies are stabilized before communicating with the device to allow the power-on reset process to complete.

10.2 Power Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD, AVSS (when using a bipolar supply), and DVDD must be decoupled with at least a 0.1-µF capacitor, as shown in Figure 77. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. Use multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins can offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Connect analog and digital ground together as close to the device as possible.

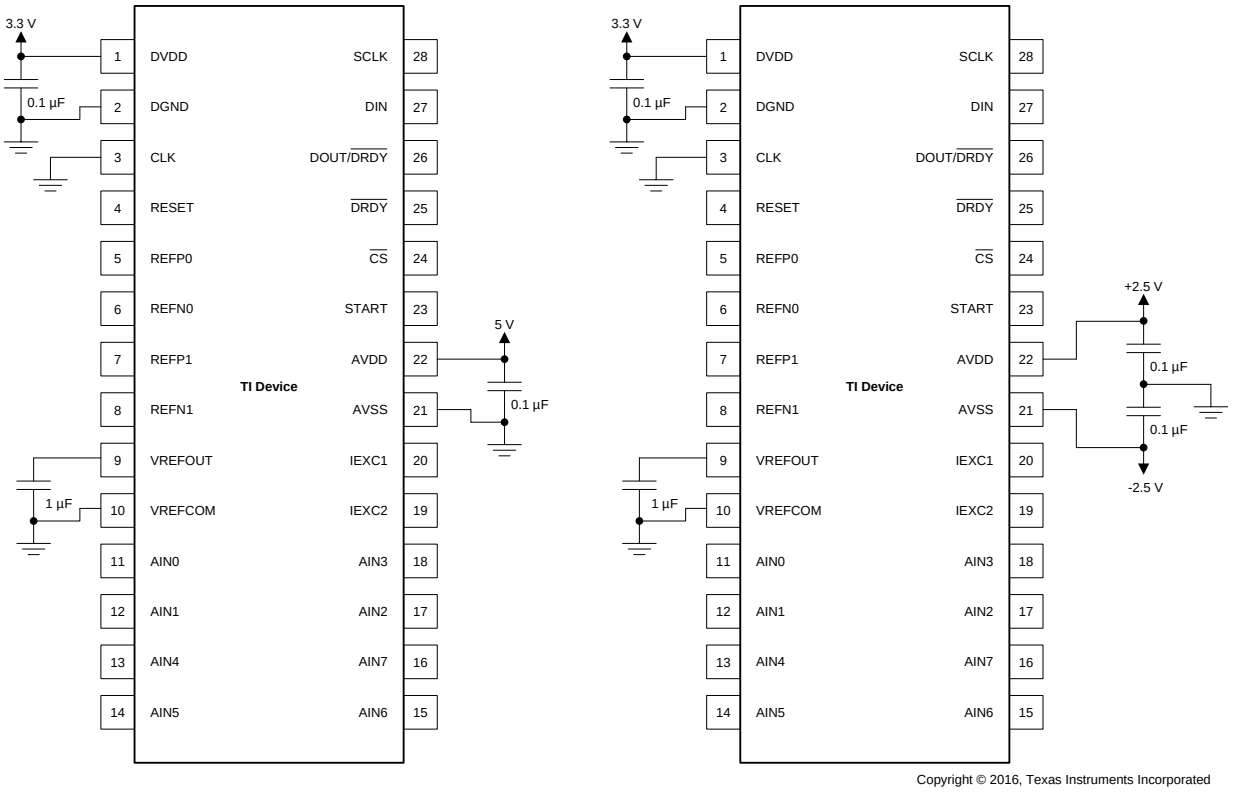


Figure 77. Power-Supply Decoupling for Unipolar and Bipolar Supply Operation

11 Layout

11.1 Layout Guidelines

Use best design practices when laying out a printed-circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog multiplexers (MUXs)] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 78. Although Figure 78 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

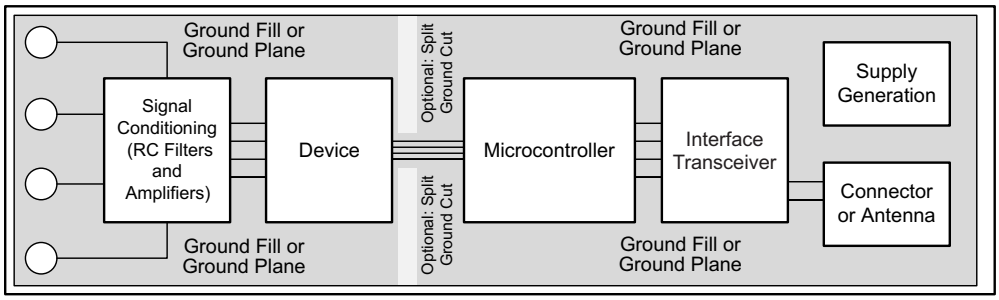


Figure 78. System Component Placement

The following list outlines some basic recommendations for the layout of the ADS1148-Q1 to get the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate analog and digital signals. To start, partition the board into analog and digital sections where the layout permits. Route digital lines away from analog lines. This routing prevents digital noise from coupling back into analog signals.
- The ground plane can be split into an analog plane (AGND) and digital plane (DGND), but is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected to together at the ADC.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents flow on the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing right next to the signal trace, another path must be found to return to the source and complete the circuit. If is forced into a larger path, the signal can increasingly possibly radiate. Sensitive signals are more susceptible to EMI interference.
- Use bypass capacitors on supplies to reduce high frequency noise. Do not place vias between bypass capacitors and the active device. Placing the bypass capacitors on the same layer as close to the active device yields the best results.
- Consider the resistance and inductance of the routing. Often, traces for the inputs have resistances that react with the input bias current and cause an added error voltage. Reducing the loop area enclosed by the source signal and the return current reduces the inductance in the path. Reducing the inductance reduces the EMI pickup and reduce the high frequency impedance detected by the device.
- Watch for parasitic thermocouples in the layout. Dissimilar metals going from each analog input to the sensor can create a parasitic themocouple that can add an offset to the measurement. Differential inputs must be matched for both the inputs going to the measurement source.
- Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Best input combinations for differential measurements use adjacent analog input lines such as AIN0, AIN1 and AIN2, AIN3. The differential capacitors must be of high quality. The best ceramic chip capacitors are C0G (NPO), which have stable properties and low noise characteristics.

11.2 Layout Example

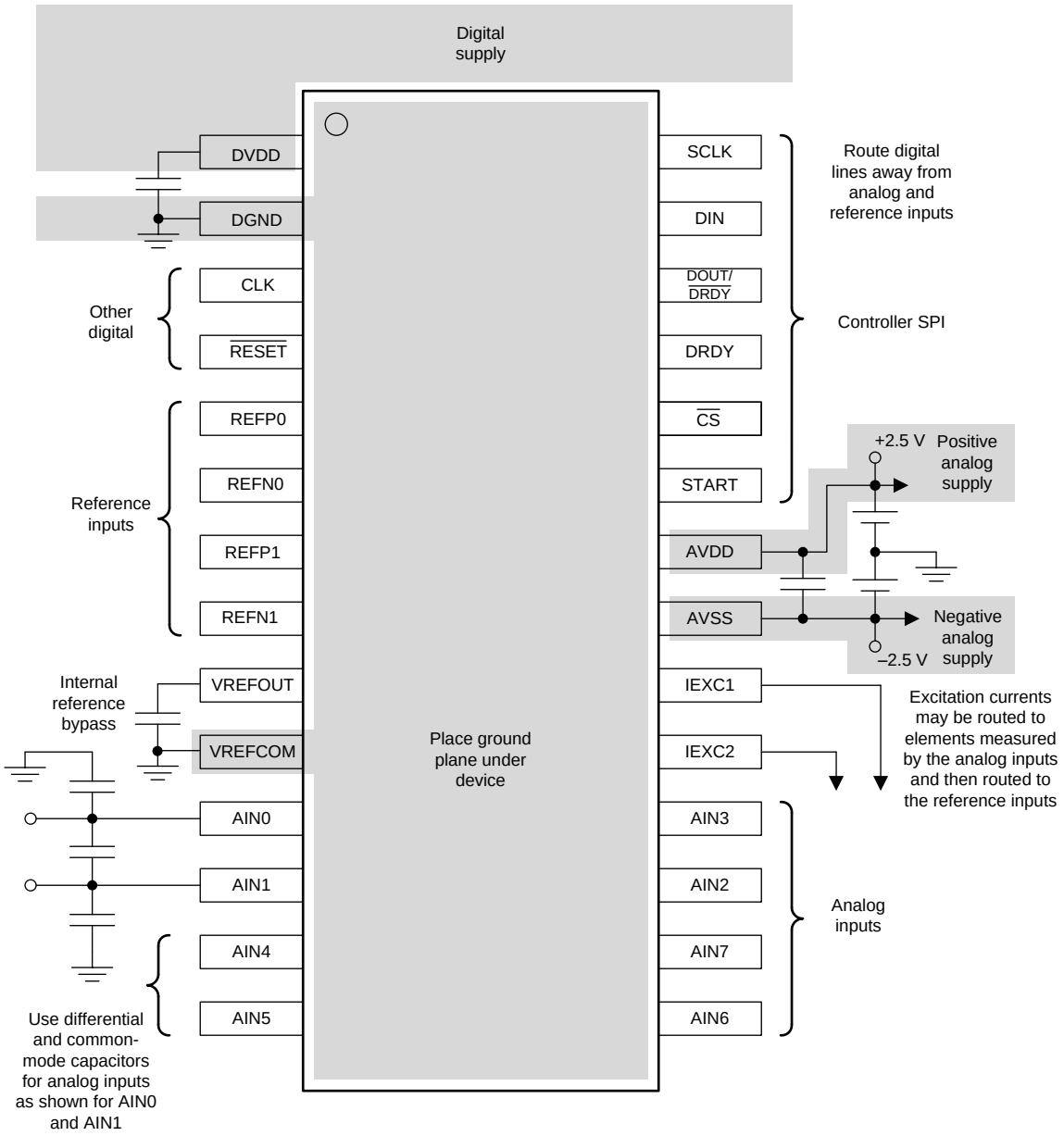


Figure 79. Layout Example

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *温度测量 应用示例 《使用 ADS1247 和 ADS1248》*（文献编号：SBAA180）
- *《使用 ADS1148 和 ADS1248 系列器件进行 RTD 比例测量和滤波》*（文献编号：SBAA201）
- *《3 线 RTD 测量系统参考设计（–200°C 到 850°C）》*（文献编号：SLAU520）
- *《模数转换规范及性能特性术语表》*（文献编号：SBAA147）

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1148QPWRQ1	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ADS1148Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

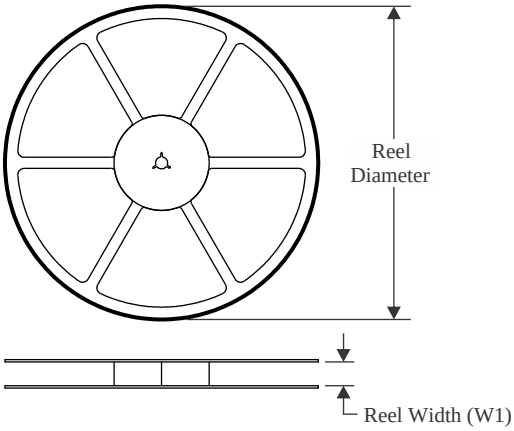
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

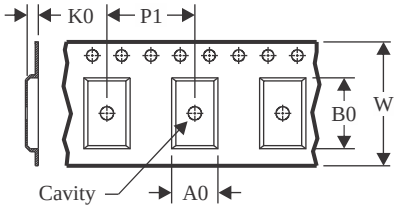
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

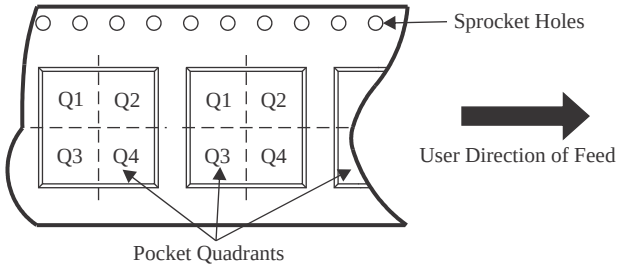


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

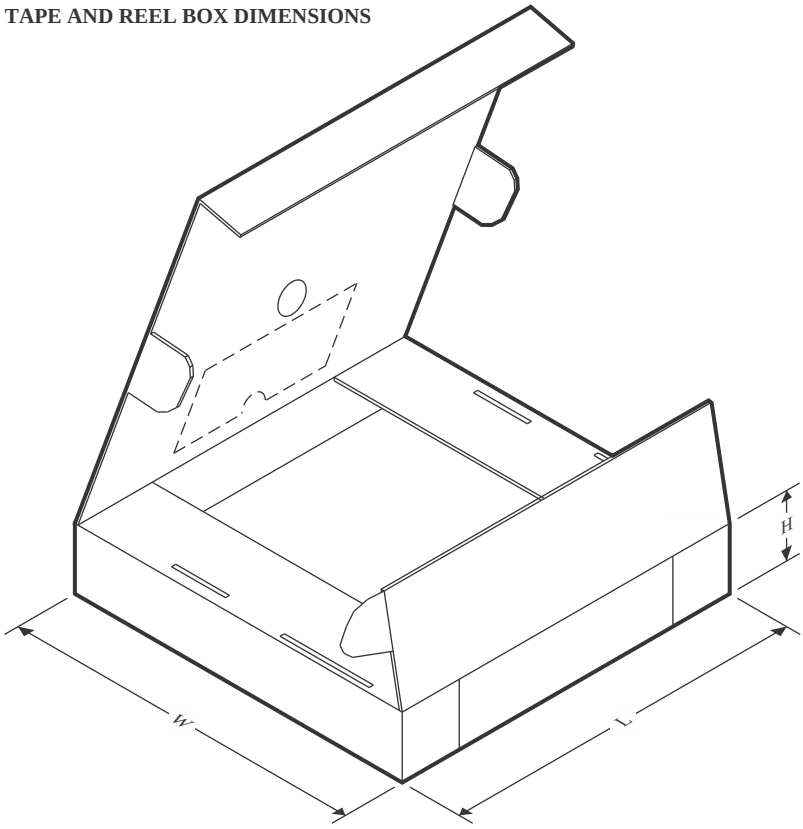
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1148QPWRQ1	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

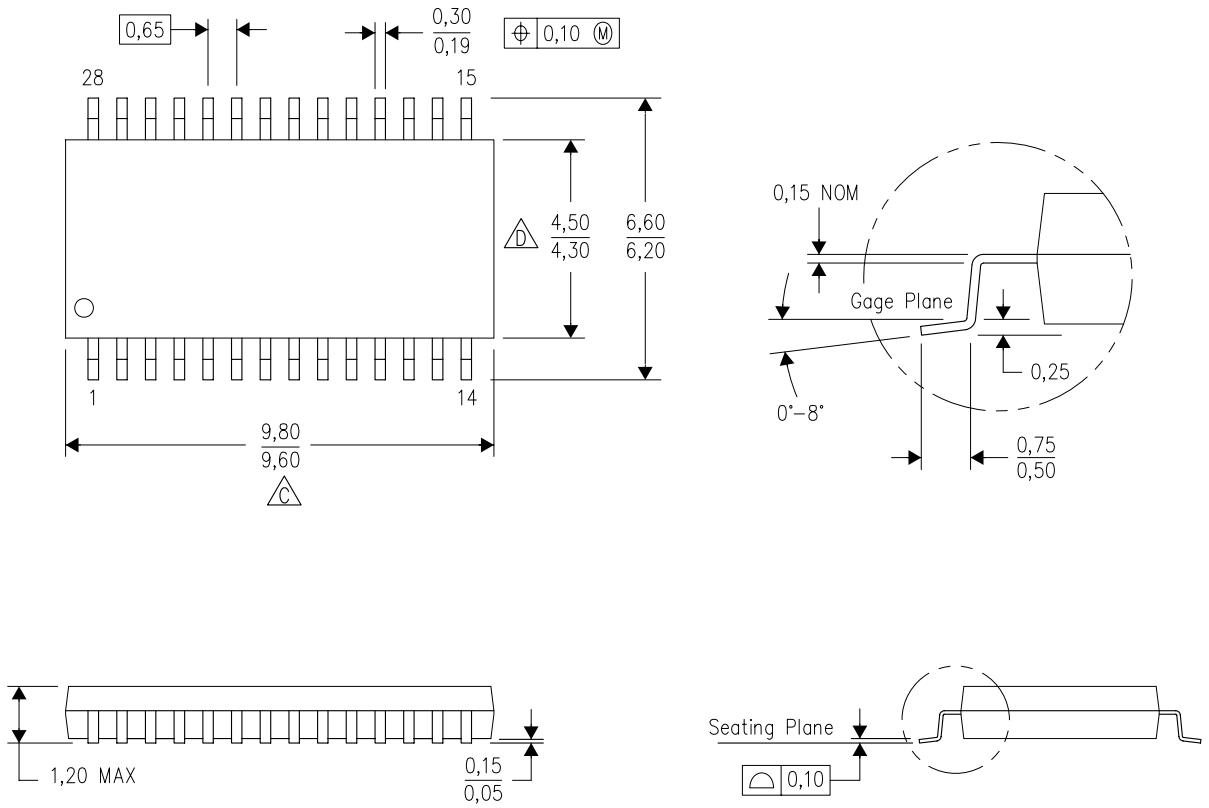
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1148QPWRQ1	TSSOP	PW	28	2000	356.0	356.0	35.0

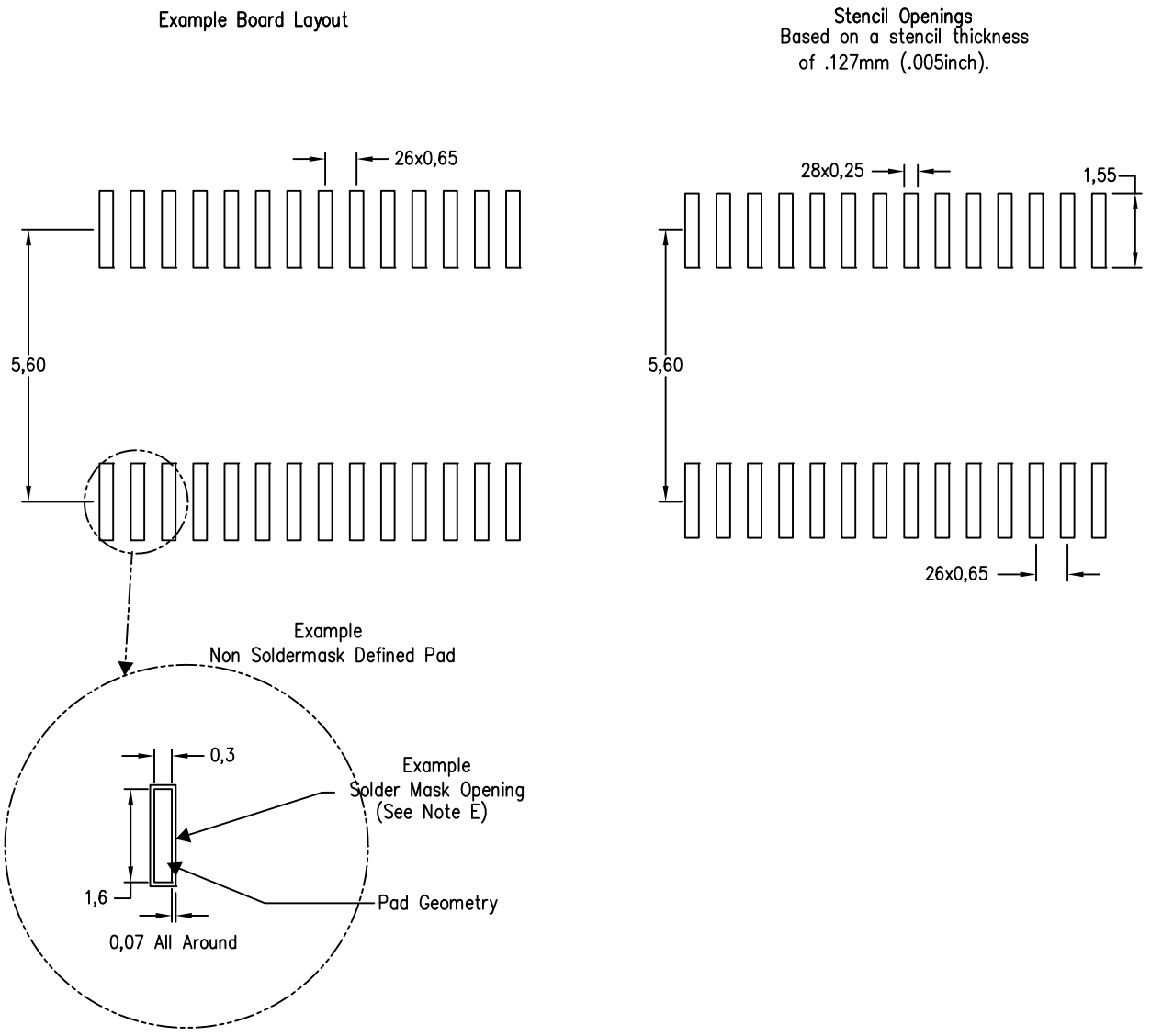
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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