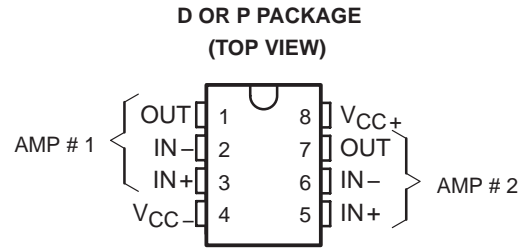


RC4559

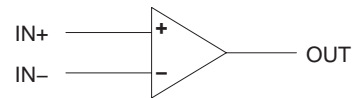
DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

SLOS074 – D2785, OCTOBER 1983 — REVISED JUNE 1988

- **Matched Gain and Offset Between Amplifiers**
- **Unity-Gain Bandwidth . . . 3 MHz Min**
- **Slew Rate . . . 1.5 V/ns Min**
- **Low Equivalent Input Noise Voltage**
2 μ V/Hz Max (20 Hz to 20 kHz)
- **No Frequency Compensation Required**
- **No Latch Up**
- **Wide Common-Mode Voltage Range**
- **Low Power Consumption**
- **Designed to be Interchangeable with Raytheon RC4559**



symbol (each amplifier)



AVAILABLE OPTIONS

| SYMBOLIZATION | | OPERATING TEMPERATURE RANGE | V_{IO} max at 25°C |
|---------------|----------------|-----------------------------|----------------------|
| DEVICE | PACKAGE SUFFIX | | |
| RC4559 | D, P | -0°C to 70°C | 6 mV |

The D packages are available taped and reeled. Add the suffix R to the device type when ordering. (i.e., RC4559DR)

description

The RC4559 is a dual high-performance operational amplifier. The high common-mode input voltage and the absence of latch-up make this amplifier ideal for low-noise signal applications such as audio preamplifiers and signal conditioners. This amplifier features a guaranteed dynamic performance and output drive capability that far exceeds that of the general-purpose type amplifiers.

The RC4559 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--|----------------|
| Supply voltage V_{CC+} (see Note 1) | 18 V |
| Supply voltage V_{CC-} (see Note 1) | -18 V |
| Differential input voltage (see Note 2) | ± 30 V |
| Input voltage (any input, see Notes 1 and 3) | ± 15 V |
| Duration of output short-circuit to ground, one amplifier at a time (see Note 4) | unlimited |
| Continuous total dissipation | 500 mW |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | -65°C to 125°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

- NOTES: 1. All voltage values, unless otherwise noted, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC+} and V_{CC-} .
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
4. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.

RC4559

DUAL HIGH-PERFORMANCE OPERATIONAL AMPLIFIER

electrical characteristics at specified free-air temperature, $V_{CC+} = 15\text{ V}$, $V_{CC-} = -15\text{ V}$

| PARAMETER | | TEST CONDITIONS† | T_A ‡ | MIN | TYP | MAX | UNIT |
|-----------------|--|--|------------|------|-----|-----|------------------------|
| V_{IO} | Input offset voltage | $V_O = 0$ | 25°C | | 2 | 6 | mV |
| | | | Full Range | | | 7.5 | |
| I_{IO} | Input offset current | $V_O = 0$ | 25°C | | 5 | 100 | nA |
| | | | Full range | | | 200 | |
| I_{IB} | Input bias current | $V_O = 0$ | 25°C | | 40 | 250 | nA |
| | | | Full range | | | 500 | |
| V_I | Input voltage range | | 25°C | ±12 | ±13 | | V |
| V_{OM} | Maximum peak output voltage swing | $R_L \geq 3\text{ k}\Omega$ | 25°C | ±12 | ±13 | | V |
| | | $R_L = 600\ \Omega$ | 25°C | ±9.5 | ±10 | | |
| | | $R_L \geq 2\text{ k}\Omega$ | Full range | ±10 | | | |
| V_I | Input voltage range | $V_O = \pm 10\text{ V}$, $R_L = 2\text{ k}\Omega$ | 25°C | 20 | 300 | | V/mV |
| | | | Full range | 15 | | | |
| B_{OM} | Maximum output-swing bandwidth | $V_{OPP} = 20\text{ V}$, $R_L = 2\text{ k}\Omega$ | 25°C | 24 | 32 | | kHz |
| B_1 | Unity-gain bandwidth | | 25°C | 3 | 4 | | MHz |
| r_i | Input resistance | | 25°C | 0.3 | 1 | | M Ω |
| CMRR | Common-mode rejection ratio | $V_O = 0$ | 25°C | 80 | 100 | | dB |
| k_{SVS} | Supply voltage sensitivity ($\Delta V_{IO}/\Delta V_{CC}$) | $V_O = 0$ | 25°C | | 10 | 75 | $\mu\text{V}/\text{V}$ |
| V_n | Equivalent input noise voltage (closed loop) | $A_{VD} = 100$, $R_S = 1\text{ k}\Omega$, $f = 20\text{ Hz to } 20\text{ kHz}$ | 25°C | | 1.4 | 2 | μV |
| I_n | Equivalent input noise current | $f = 20\text{ Hz to } 20\text{ kHz}$ | 25°C | | 25 | | pA |
| I_{CC} | Supply current (both amplifiers) | No load, No signal | 25°C | | 3.3 | 5.6 | mA |
| | | | 0°C | | 4 | 6.6 | |
| | | | 70°C | | 3 | 5 | |
| V_{O1}/V_{O2} | Crosstalk attenuation | $A_{VD} = 100$, $R_S = 1\text{ k}\Omega$, $f = 10\text{ kHz}$ | 25°C | | 90 | | dB |

† All characteristics are specified under open-loop operation, unless otherwise noted.

‡ Full range operating free-air temperature range is 0°C to 70°C.

matching characteristics at $V_{CC+} = 15\text{ V}$, $V_{CC-} = -15\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|--|-----|------|-----|------|
| V_{IO} | Input offset voltage | $V_O = 0$ | | ±0.2 | | mV |
| I_{IO} | Input offset current | $V_O = 0$ | | ±7.5 | | nA |
| I_{IB} | Input bias current | $V_O = 0$ | | ±15 | | nA |
| A_{VD} | Large-signal differential voltage amplification | $V_O = \pm 10\text{ V}$, $R_L = 2\text{ k}\Omega$ | | ±1 | | dB |

operating characteristics, $V_{CC+} = 15\text{ V}$, $V_{CC-} = -15\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-------------------------|---|-----|-----|-----|------------------|
| t_r | Rise time | $V_I = 20\text{ mV}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$ | | 80 | | μs |
| | Overshoot | | | 18% | | |
| SR | Slew rate at unity gain | $V_I = 10\text{ mV}$, $R_L = 2\text{ k}\Omega$, $C_L = 100\text{ pF}$ | 1.5 | 2 | | V/ μs |



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| RC4559D | ACTIVE | SOIC | D | 8 | 75 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RC4559 | Samples |
| RC4559DR | ACTIVE | SOIC | D | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | RC4559 | Samples |
| RC4559P | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | RC4559P | Samples |
| RC4559PE4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | RC4559P | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

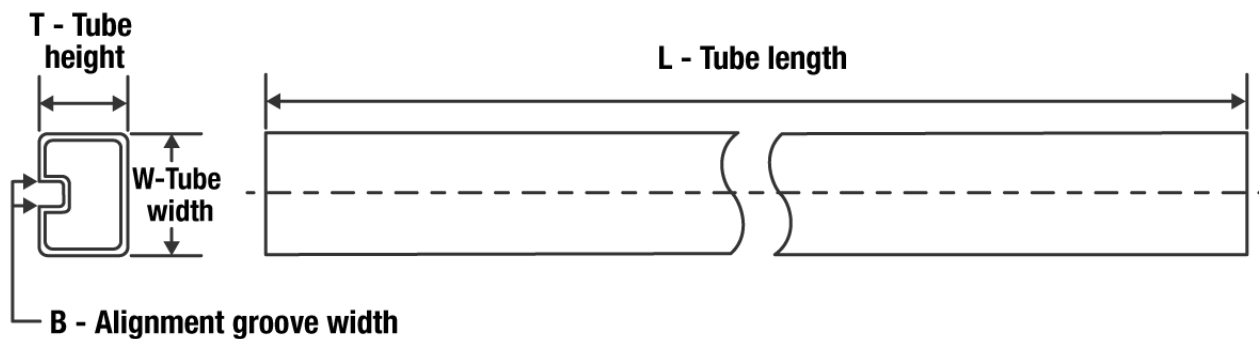

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| RC4559DR | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------|--------------|-----------------|------|------|-------------|------------|-------------|
| RC4559DR | SOIC | D | 8 | 2500 | 340.5 | 336.1 | 25.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| RC4559D | D | SOIC | 8 | 75 | 507 | 8 | 3940 | 4.32 |
| RC4559P | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| RC4559PE4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

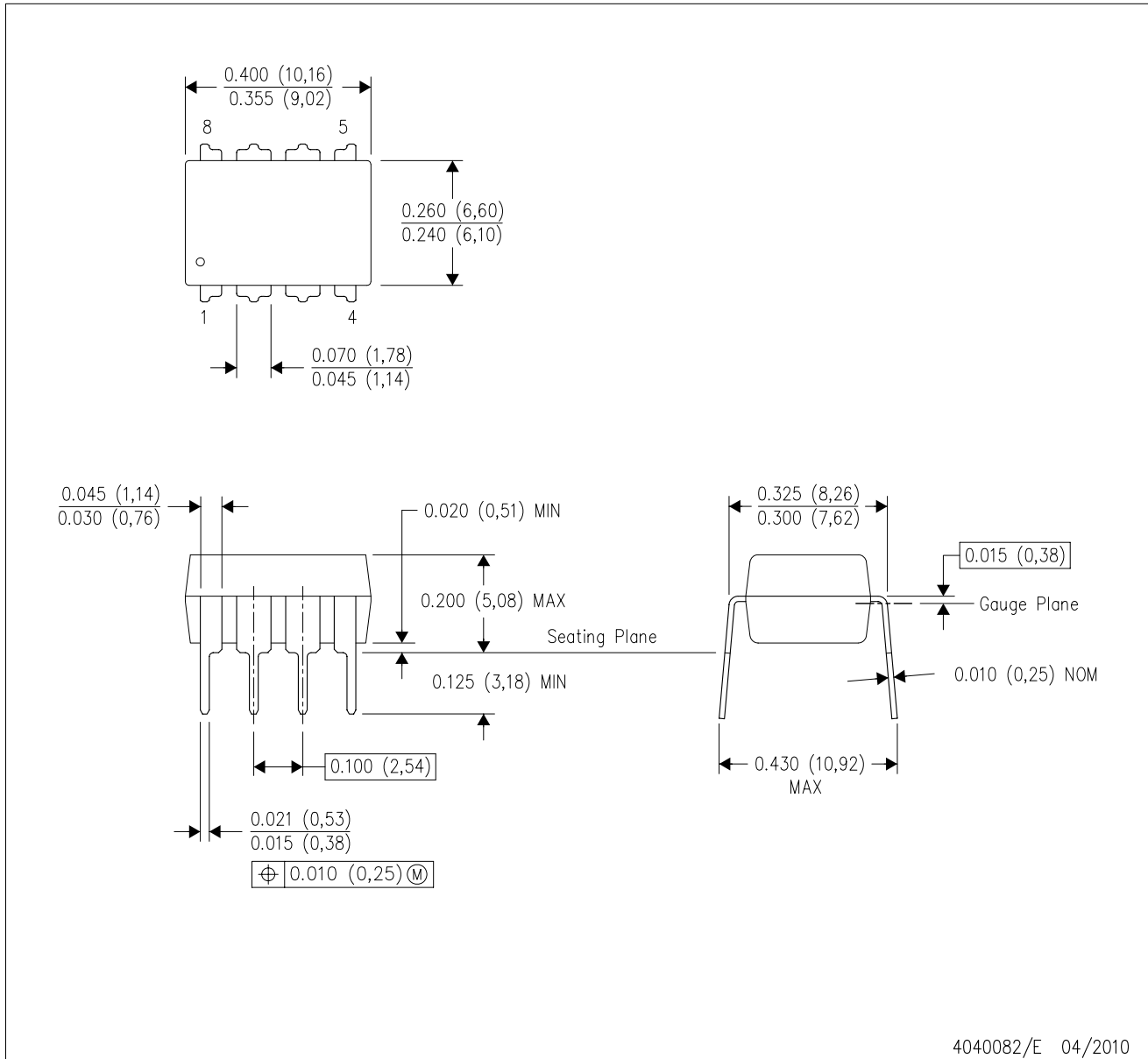
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



4040082/E 04/2010

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

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