SN75ALS181 差分驱动器和接收器对

1 特性

- 符合 TIA/EIA-422-B、TIA/EIA-485-A 和 CCITT 建议 V.11 和 X.27
- 低电源电流要求...
  30 mA（最大值）
- 驱动器输出容量...±60mA
- 热关断保护
- 驱动器共模输出电压范围为 -7V 至 12V
- 接收器输入阻抗：12kΩ 最小值
- 接收器输入灵敏度：±200mV
- 接收器输入迟滞：60 mV（典型值）
- ±12V 的接收器共模输入电压范围
- 由 5V 单电源供电
- 无干扰上电和断电保护

2 说明

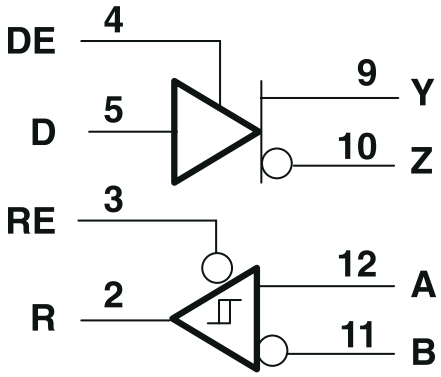
SN75ALS181 是一款差分驱动器和接收器对，专为多点总线传输线路上的双向数据通信而设计。此设计提供平衡传输线路，并符合 TIA/EIA-422-B 和 TIA/EIA-485-A 以及 CCITT 建议 V.10、V.11、X.26 和 X.27。

SN75ALS181 将三态差分线路驱动器与差分输入线路接收器相结合，共同由单个 5V 电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出端和接收器差分输入端连接到单独的引脚以实现更大的灵活性，这些端口用于在禁用驱动器或 V_{CC} = 0 时为总线提供最小负载。这些端口具有较宽的正负共模电压变化，使得该器件适用于合用线应用。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
SN75ALS181	N (PDIP) 14 引脚	19.3mm x 6.35mm
	NS (SO) 14 引脚	10.3 mm x 5.3 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



逻辑图（正逻辑）

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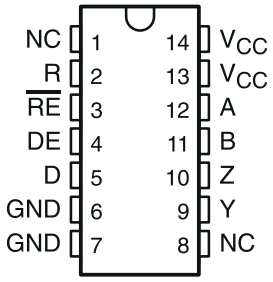
3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (August 2013) to Revision E (October 2022)	Page
• Added the *Pin Configuration and Functions*	3
• Deleted the Package thermal impedance from the *Absolute Maximum Ratings*	4
• Added the *Thermal Information* table	4
• Added the *Detailed Description* section	10

Changes from Revision C (May 2010) to Revision D (August 2013)	Page
• Fixed typographical error in MAX value for $\Delta\|V_{OD}\|$.	5
• Fixed typographical error in UNITS for $\Delta\|V_{OC}\|$	5
• Removed Ordering Information table	10
• Fixed graphical error in schematic	10

4 Pin Configuration and Functions



N.C. – No internal connection

图 4-1. N OR NS Package (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
NC	1, 8	No Connect	Not electrically connected
R	2	Digital Output	Logic output RS485 data
$\overline{RE}$	3	Digital Input	Receiver enable, active low
DE	4	Digital Input	Driver enable, active high
D	5	Digital Input	Driver data input
GND	6, 7	Ground	Device ground
Y	9	Bus Output	Bus Output Y (Complementary to Z)
Z	10	Bus Output	Bus Output Z (Complementary to Y)
B	11	Bus Input	Bus Input B (Complementary to A)
A	12	Bus Input	Bus Input A (Complementary to B)
V_{CC}	13, 14	Power	5 V Supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) see (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range(2)			7	V
	Input voltage range	D, DE, and $\overline{RE}$ inputs		7	V
	Output voltage range	Driver	–9	14	V
	Input voltage range	Receiver	–14	14	V
	Receiver differential input voltage range(3)		–14	14	V
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds			260	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input voltage, are with respect to network ground terminal.
(3) Differential input voltage is measured at the non-inverting terminal with respect to the inverting terminal.

5.2 Thermal Information

THERMAL METRIC(1)		N (PDIP)	NS (SO)	UNIT
		14-Pins	14-Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.2	88.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	41.6	49.12	°C/W
ψ_{JT}	Junction-to-top characterization parameter	34.0	14.17	°C/W
ψ_{JB}	Junction-to-board characterization parameter	21.1	48.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{OC}	Common-mode output voltage(1)	Driver	–7		12	V
V_{IC}	Common-mode input voltage(1)	Receiver	–12		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature		0		70	°C

(1) The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this table for common-mode output voltage level only.

5.4 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = – 18 mA				– 1.5	V
V_O	Output voltage	I_O = 0		0		6	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5		6	V
$\|V_{OD2}\|$	Differential output voltage	V_{CC} = 5 V, R_L = 100 Ω	See 图 6-1	1/2 V_{OD1}			V
				2			
		R_L = 54 Ω		1.5	2.3	5	
$\|V_{OD3}\|$	Differential output voltage	V_{test} = – 7 V to 12 V,	See 图 6-2	1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	R_L = 54 Ω or 100 Ω,	See 图 6-1			±0.2	V
V_{OC}	Common mode output voltage	R_L = 54 Ω or 100 Ω,	See 图 6-1			3	V
						– 1	
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(2)	R_L = 54 Ω or 100 Ω,	See 图 6-1			±0.2	V
I_{OZ}	High-impedance-state output current	V_O = – 7 V to 12 V(3)				±100	μA
I_{IH}	High-level input current	V_{IH} = 2.4 V				20	μA
I_{IL}	Low-level input current	V_{IL} = 0.4 V				– 100	μA
I_{OS}	Short circuit output current	V_O = – 7 V				– 250	mA
		V_O = V_{CC}				250	
		V_O = 12 V				250	
		V_O = 0 V				– 150	
I_{CC}	Supply current (total package)	No load	Outputs enabled		21	30	mA
			Outputs disabled		14	21	

(1) All typical values are at V_{CC} = 5 V and TA = 25°C.
(2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(3) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions

5.5 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{dD}	Differential output delay time, tdDH or tdDL	R_L = 54 Ω, C_L = 50 pF,	See 图 6-3	9	13	20	ns
$t_{sk(p)}$	Pulse skew (|tdDH – tdDL|)	R_L = 54 Ω, C_L = 50 pF,	See 图 6-3		1	8	ns
t_t	Differential output transition time	R_L = 54 Ω, C_L = 50 pF,	See 图 6-3	3	10	16	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See 图 6-4		36	53	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See 图 6-5		39	56	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See 图 6-4		20	31	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See 图 6-5		9	20	ns

(1) All typical values are at V_{CC} = 5 V and TA = 25°C.

5.6 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{T+}	Positive-going threshold voltage, differential input	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
V_{T-}	Negative-going threshold voltage, differential input	V_O = 0.5 V,	I_O = 8 mA		–0.2			V
V_{hys}	Input hysteresis (V_{T+} – V_{T-})					60		mV
V_{IK}	Input clamp voltage, $\overline{RE}$	I_I = –18 mA					–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = –400 μA,	See 图 6-6	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = 200 mV,	I_{OL} = 8 mA,	See 图 6-6			0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input at 0 V(2),	V_I = 12 V				1	mA
			V_I = –7 V				–0.8	
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = –7 V					–100	μA
R_I	Input resistance				12			kΩ
I_{OS}	Short circuit output current	V_{ID} = 200 mV,	V_O = 0 V		–15		–85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled			21	30	mA
			Outputs disabled			14	21	

(1) All typical values are at V_{CC} = 5 V and TA = 25°C.
(2) This applies for both power on and power off. Refer to TIA/EIA-485-A for exact conditions

5.7 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PHL}	Differential output delay time, tdDH or tdDL	V_{ID} = –1.5 V to 1.5 V	10	16	25	ns
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = –1.5 V to 1.5 V	10	16	25	ns
$t_{sk(p)}$	Pulse skew (|tdDH – tdDL|)	V_{ID} = –1.5 V to 1.5 V		1	8	ns
t_{PZH}	Output enable time to high level			7	15	ns
t_{PZL}	Output enable time to low level			9	19	ns
t_{PHZ}	Output disable time from high level			18	27	ns
t_{PLZ}	Output disable time from low level			10	15	ns

(1) All typical values are at V_{CC} = 5 V and TA = 25°C.

Parameter Measurement Information

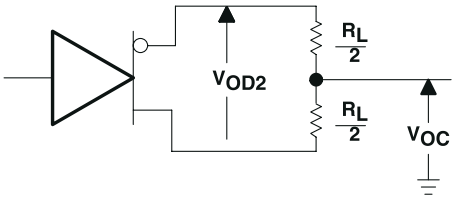


图 6-1. Driver Test Circuit, V_{OD} and V_{OC}

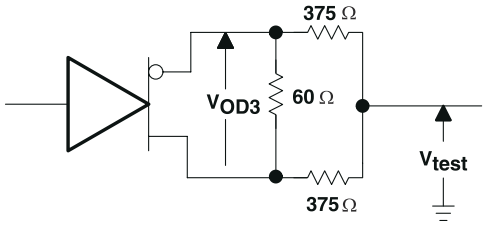
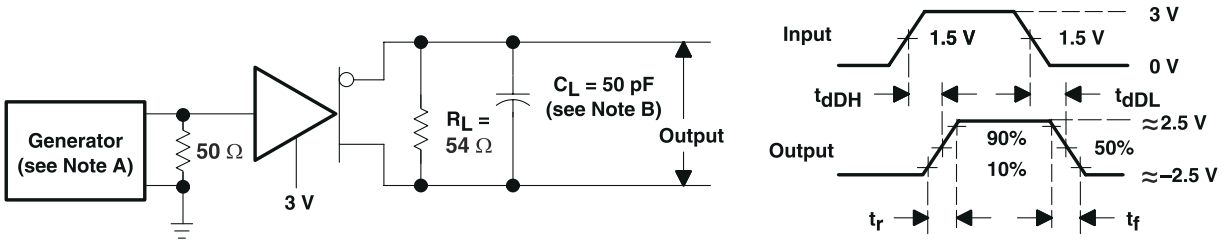


图 6-2. Driver Circuit, V_{OD3}

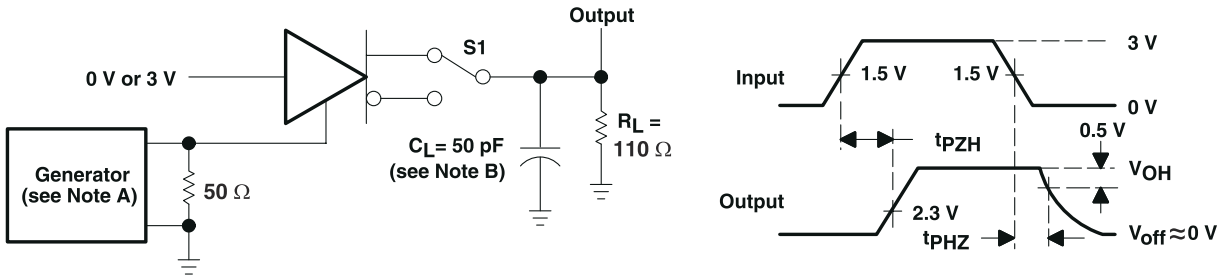


TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω

B. C_L includes probe and jig capacitance.

图 6-3. Driver Differential-Output Delay and Transition Times

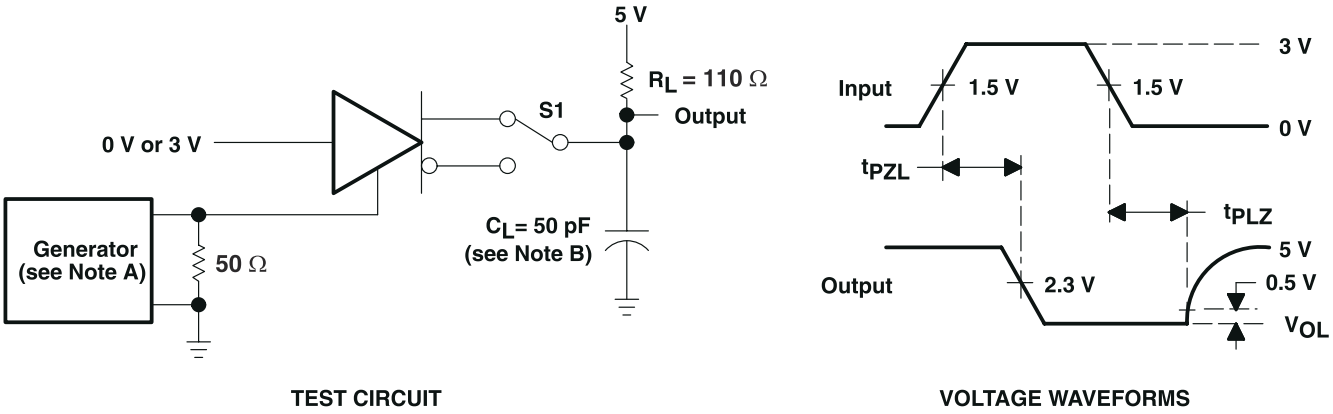


TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω

B. C_L includes probe and jig capacitance.

图 6-4. Driver Enable and Disable Times



TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω

B. C_L includes probe and jig capacitance.

图 6-5. Driver Enable and Disable Times

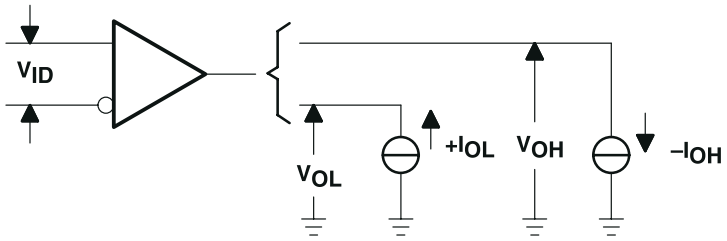
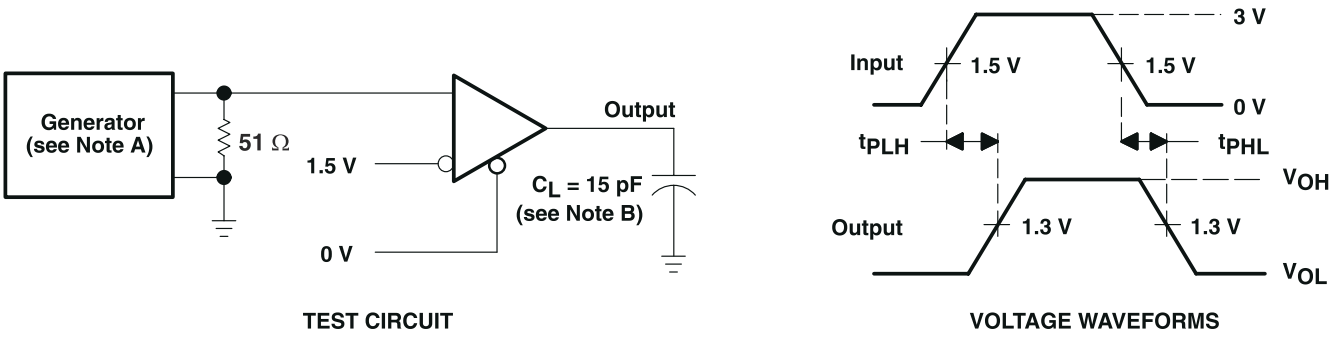


图 6-6. Receiver, V_{OH} and V_{OL}

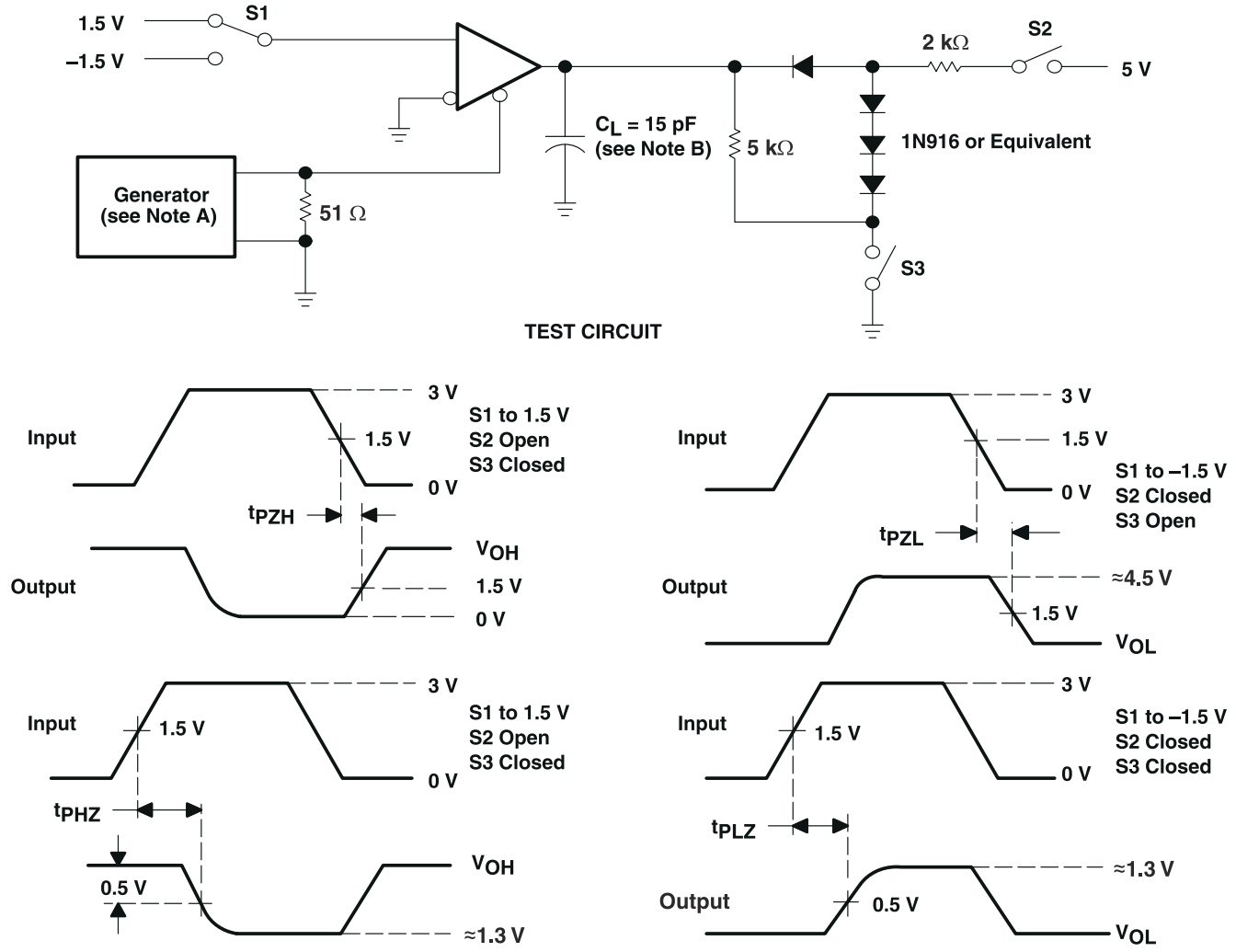


TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω

B. C_L includes probe and jig capacitance.

图 6-7. Receiver Propagation-Delay Times



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω

B. C_L includes probe and jig capacitance.

图 6-8. Receiver Output Enable and Disable Times

6 Detailed Description

6.1 Device Functional Modes

6.1.1 Function Tables

Each Driver

INPUTS D	ENABLE DE	OUTPUTS Y	OUTPUTS Z
H	H	H	L
L	H	L	H
X	L	Z	Z

Each Receiver(1)

DIFFERENTIAL A – B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geqslant 0.2$ V	L	H
– 0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leqslant$ – 0.2 V	L	L
X	H	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

6.1.2 Schematics

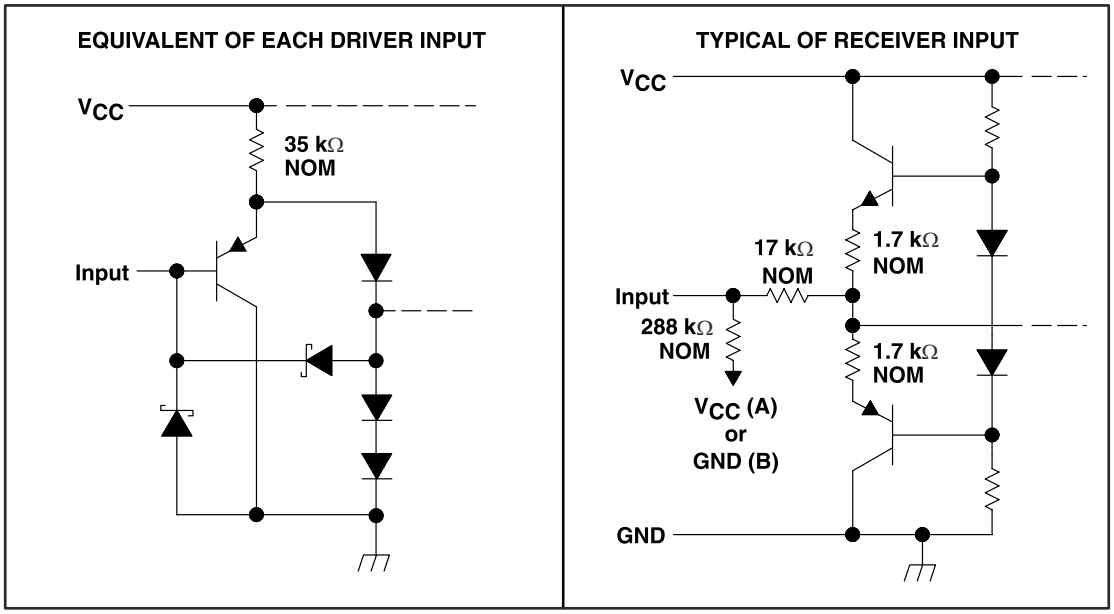


图 6-1. SCHEMATICS OF INPUTS

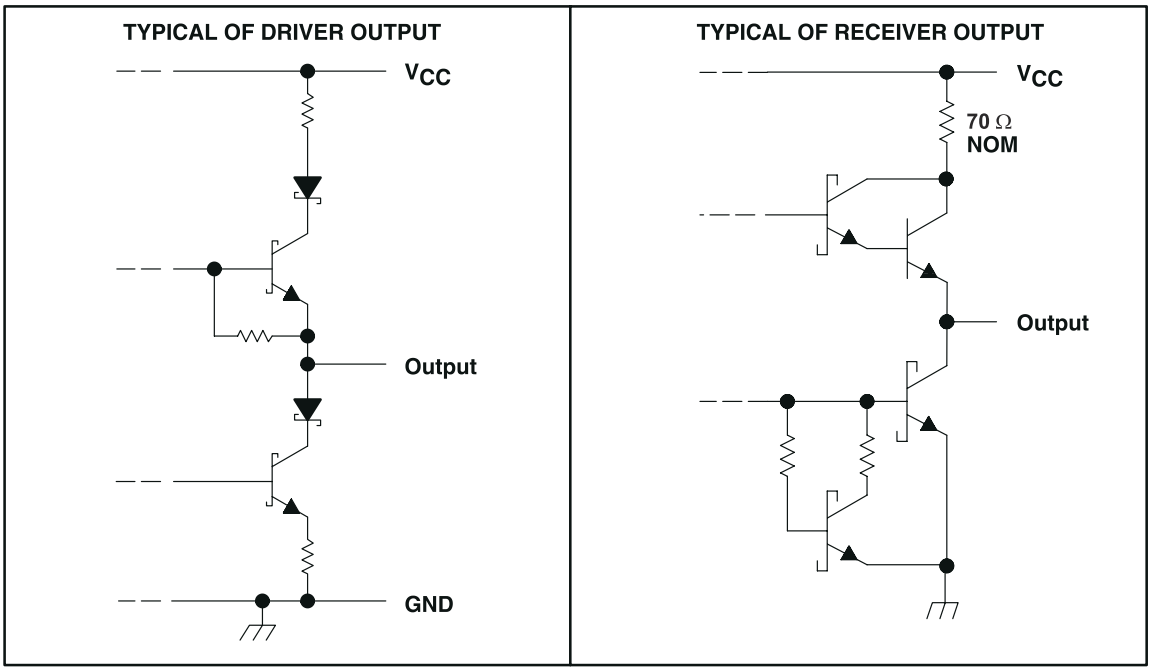


图 6-2. SCHEMATICS OF OUTPUTS

7 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

7.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

7.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

7.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS181N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS181N	Samples
SN75ALS181NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS181	Samples
SN75ALS181NSRG4	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS181	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

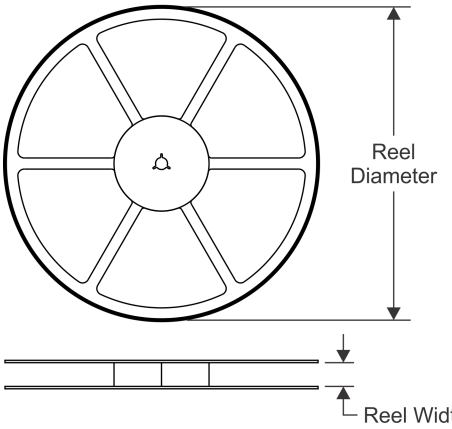
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

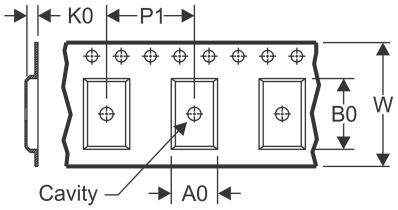
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

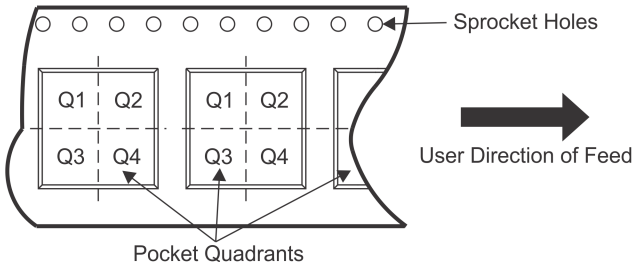


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

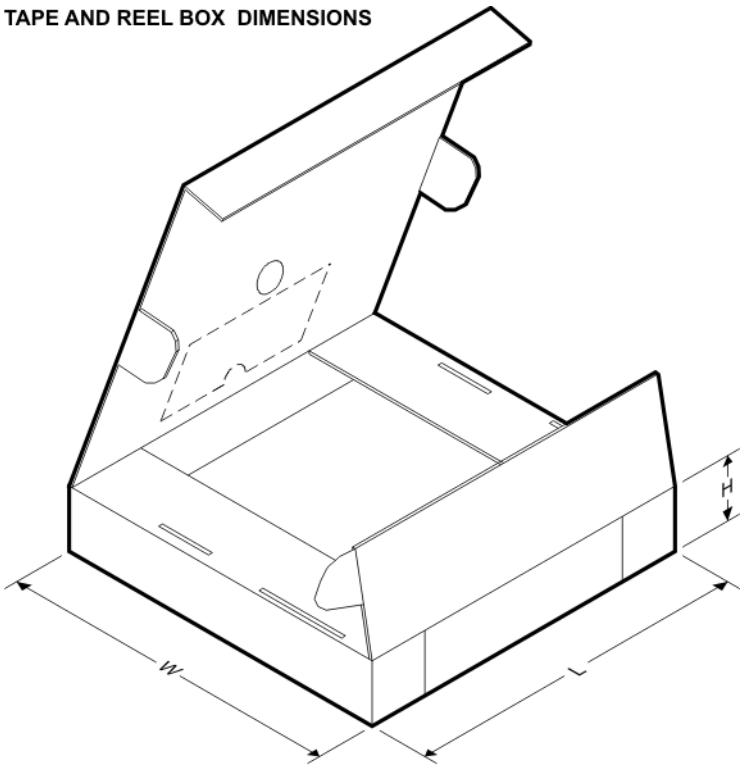
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS181NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

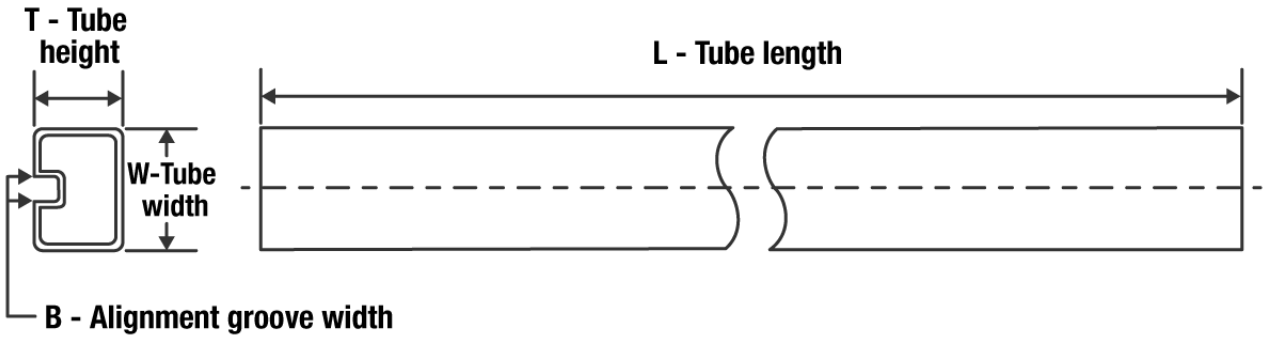
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS181NSR	SO	NS	14	2000	367.0	367.0	38.0

TUBE



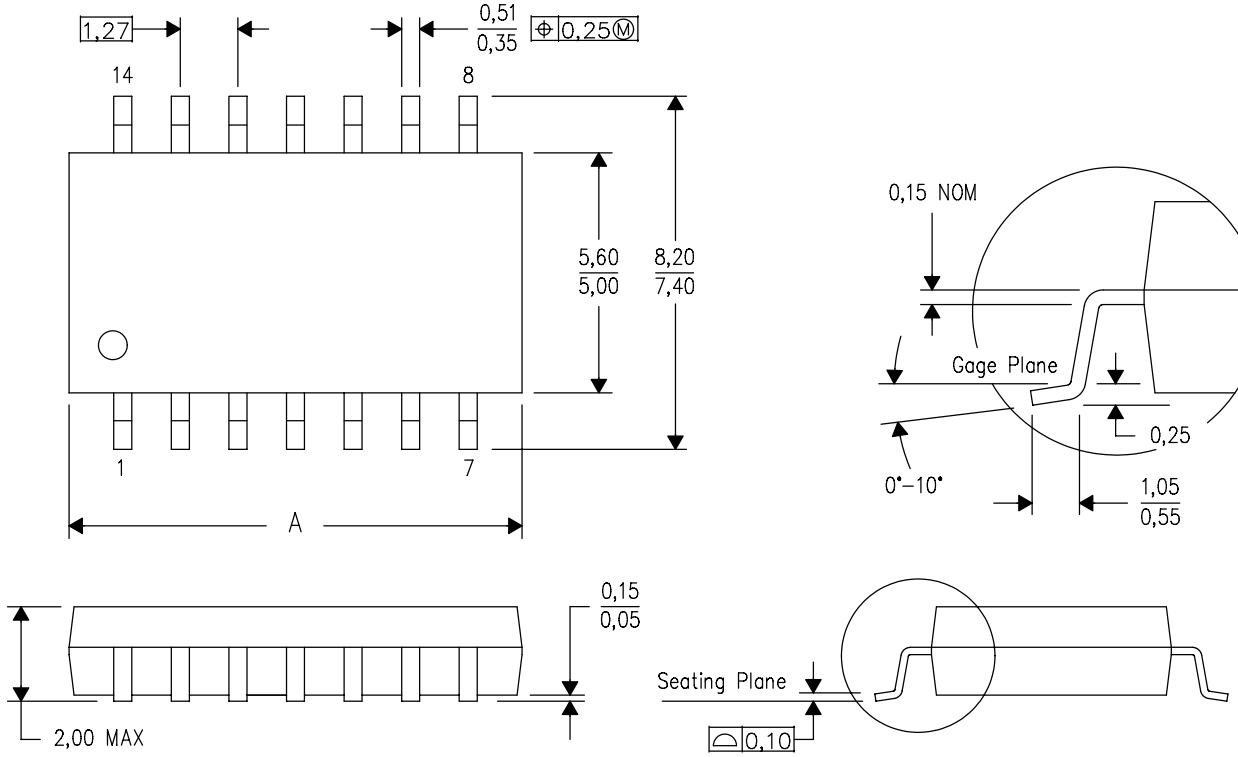
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS181N	N	PDIP	14	25	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

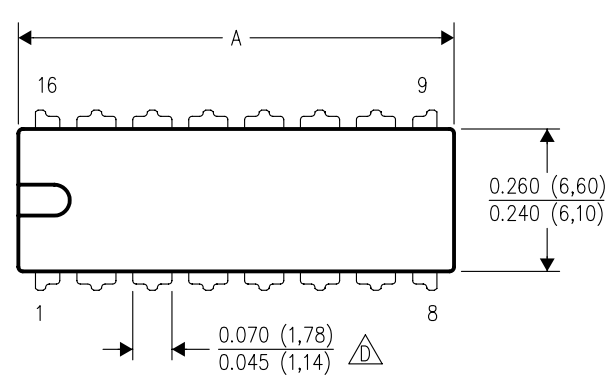
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

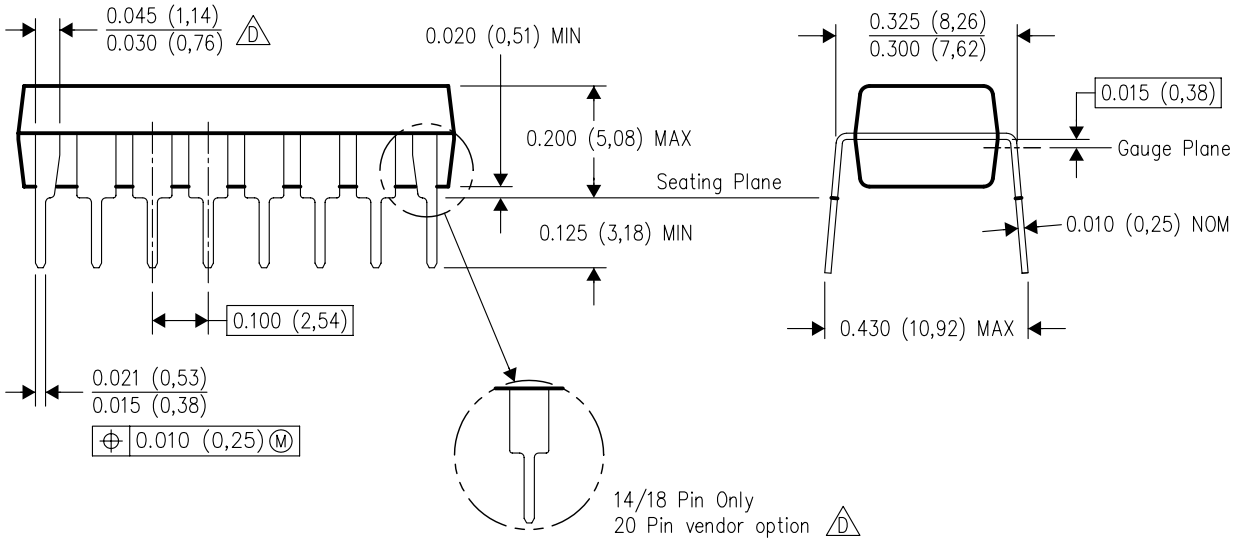
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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