具有中断输出、复位和配置寄存器的 PCA9538 远程 8 位 I2C 和 SMBus 低功耗 I/O 扩展器

1 特性

- 1 µA 低待机电流消耗（最大值）
- I^2C 至并行端口扩展器
- 开漏电路低电平有效中断输出
- 低电平有效复位输入
- 工作电源电压范围为 2.3V 至 5.5V
- 可耐受 5V 电压的 I/O 端口
- 400kHz 快速 I^2C 总线
- 两个硬件地址引脚允许在 I2C/SMBus 上使用多达四个器件
- 输入和输出配置寄存器
- 极性反转寄存器
- 加电时所有通道均被配置为输入
- 加电时无干扰
- SCL/SDA 输入端上的噪声滤波器
- 具有最大高电流驱动能力的锁存输出，适用于直接驱动 LED
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - 1000V 带电器件模型 (C101)

2 说明

PCA9538 是一款符合两线双向 I2C 总线（或 SMBus）协议、用于通用并行输入/输出 (I/O) 扩展的 8 位 I/O 扩展器。此器件的工作电源电压范围为 2.3V 至 5.5V。此器件支持 100kHz（标准模式）和 400kHz（快速模式）两种时钟频率。当开关、传感器、按钮、LED、风扇等需要额外的 I/O 时，此器件及其他 I/O 扩展器可提供简单的解决方案。

PCA9538 包括一项功能：当输入端口状态发生变化时，在 INT 引脚上生成中断。硬件可选地址引脚 A0 和 A1 最多允许四个 PCA9538 器件位于同一 I2C 总线上。也可以使用复位功能或通过下电上电生成上电复位，从而将此器件复位为默认状态。

INT 可连接至一个微控制器的中断输入。通过在这条线路上发送一个中断信号，远程 I/O 可通知微控制器在其端口上是否存在输入数据，而无须通过 I2C 总线进行通信。因此，PCA9538 还可作为简单的从器件。

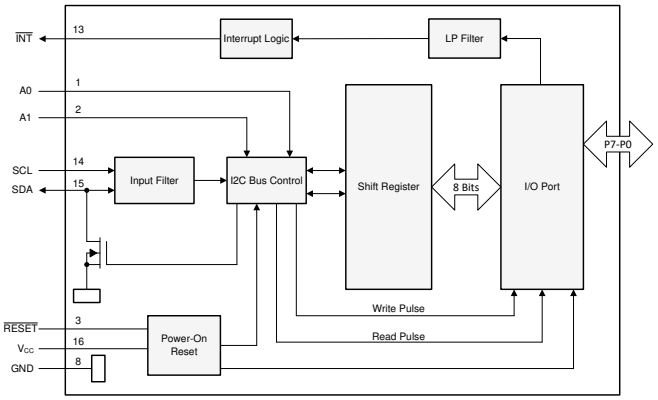
该器件的输出（已锁存）具有高电流驱动能力，用于直接驱动 LED。它具有低电流消耗。

两个硬件引脚（A0 和 A1）用于编程和改变固定的 I2C 地址，并允许多达四个器件共享同一个 I2C 总线或 SMBus。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
PCA9538	SSOP (16)	6.20mm x 5.30mm
	TVSOP (16)	3.60mm × 4.40mm
	SOIC (16)	10.30mm x 7.50mm
	TSSOP (16)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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3 Revision History

Changes from Revision F (May 2014) to Revision G (March 2021) **Page**

- 更新了说明 并添加了方框图 图像.....1
- Deleted RGV and RGT packages from the *Pin Configuration and Functions* section.....3
- Moved the "Storage temperature range" to the *Absolute Maximum Ratings* 4
- Moved the "Package thermal impedance" to the *Thermal Resistance Characteristic* 4
- Changed the V_{IH} High-level input voltage (SDL, SDA) Max value From: 5.5 V To: V_{CC} in the *Recommended Operating Conditions* 4
- Changed the V_{IH} High-level input voltage (A0, A1, A2, P7 – P0) MIN value From: 2 V To: 0.7 x V_{CC} in the *Recommended Operating Conditions* 4
- Changed the V_{IL} Low-level input voltage (A0, A1, A2, P7 – P0) MAX value From: 0.8 V To: 0.3 x V_{CC} in the *Recommended Operating Conditions* 4
- Added the *Thermal Information* table.....5
- Changed the V_{PORR} TYP value From: 1.5 V to: 1.2 Vand the MAX value From: 1.65 V To: 1.5 V in the *Electrical Characteristics* 5
- Added the V_{PORF} row in the *Electrical Characteristics* 5
- Changed the I_{OL} ($\overline{INT}$) row TYP value Fron: 10 mA to: 7 mA in the *Electrical Characteristics* 5
- Changed the I_{CC} Standby mode values in the *Electrical Characteristics* 5
- Changed the ΔI_{CC} Additional current in standby mode (5.5 V) mAX value From: 1 mA To: 4 mA in the *Electrical Characteristics* 5
- Added Note 4 to the *Electrical Characteristics* 5
- Changed the *Typical Characteristics* graphs.....9
- Changed the *Power Supply Recommendations* 26

Changes from Revision E (September 2008) to Revision F (May 2014) **Page**

- Added $\overline{RESET}$ Errata section.....16
- Added Interrupt Errata section 17

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4 Pin Configuration and Functions

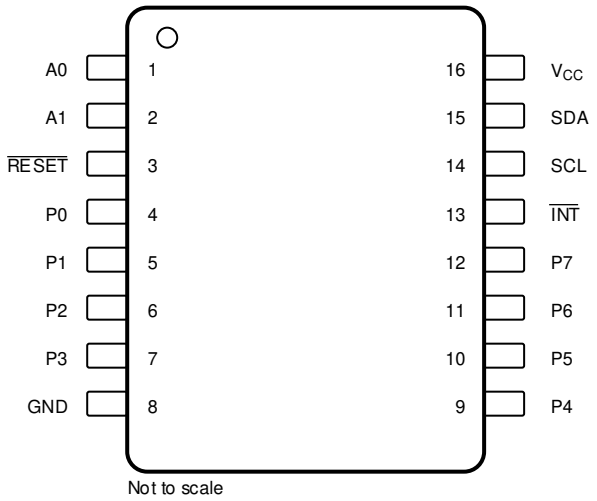

图 4-1. DBQ, DB, PW, DGV Package, 16-Pin, Top View

表 4-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
A0	1	Address input. Connect directly to V_{CC} or ground
A1	2	Address input. Connect directly to V_{CC} or ground.
GND	8	Ground
$\overline{INT}$	13	Interrupt output. Connect to V_{CC} through a pullup resistor
P0	4	P-port input-output. Push-pull design structure
P1	5	P-port input-output. Push-pull design structure
P2	6	P-port input-output. Push-pull design structure
P3	7	P-port input-output. Push-pull design structure
P4	9	P-port input-output. Push-pull design structure
P5	10	P-port input-output. Push-pull design structure
P6	11	P-port input-output. Push-pull design structure
P7	12	P-port input-output. Push-pull design structure
$\overline{RESET}$	3	Active-low reset input. Connect to V_{CC} through a pullup resistor if no active connection is used
SCL	14	Serial clock bus. Connect to V_{CC} through a pullup resistor
SDA	15	Serial data bus. Connect to V_{CC} through a pullup resistor
V_{CC}	16	Supply voltage

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6	V
V_I	Input voltage(2)		–0.5	6	V
V_O	Output voltage(2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	V_{CC}	V
		A0, A1, $\overline{RESET}$, P7 – P0	0.7 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A0, A1, $\overline{RESET}$, P7 – P0	–0.5	0.3 × V_{CC}	
I_{OH}	High-level output current	P7 – P0		–10	mA
I_{OL}	Low-level output current	P7 – P0		25	mA
T_A	Operating free-air temperature		–40	85	°C

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5.4 Thermal Information

THERMAL METRIC[1]		PCA9538					UNIT
		DB (SSOP)	DBQ (SSOP)	DGV (TVSOP)	DW (SOIC)	PW (TSSOP)	
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113.2	90	86	46	122	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = – 18 mA	2.3 V to 5.5 V	– 1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	$V_I = V_{CC}$ or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{C7} falling	$V_I = V_{CC}$ or GND, I_O = 0		0.75	1		V
V_{OH}	P-port high-level output voltage[2]	I_{OH} = – 8 mA	2.3 V	1.8			V
			3 V	2.6			
			4.5 V	4.1			
			4.75 V	4.1			
		I_{OH} = – 10 mA	2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	8		mA
	P port[3]	V_{OL} = 0.5 V	2.3 V	8	10		
			3 V	8	14		
			4.5 V	8	17		
			4.75 V	8	35		
		V_{OL} = 0.7 V	2.3 V	10	13		
			3 V	10	19		
			4.5 V	10	24		
			4.75 V	10	45		
	$\overline{INT}$	V_{OL} = 0.4 V	2.3 V to 5.5 V	3	7		
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V			±1	µA
	A0, A1, $\overline{RESET}$ [4]					±1	
I_{IH}	P port	$V_I = V_{CC}$	2.3 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND	2.3 V to 5.5 V			– 1	µA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{scl} = 400 kHz, no load	5.5 V		104	175	µA
			3.6 V		50	90	
			2.7 V		20	65	
		$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{scl} = 100 kHz, no load	5.5 V		60	150	
			3.6 V		15	40	
			2.7 V		8	20	
	Standby mode	$V_I = V_{CC}$ or GND, I_O = 0, I/O = inputs, f_{scl} = 0 kHz, no load	5.5 V		1.9	3.5	
			3.6 V		1.1	1.8	
			2.7 V		1	1.6	

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5.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.3 V to 5.5 V			1.5	mA
		All LED I/Os at V_I = 4.3 V, f_{scl} = 0 kHz	5.5 V			4	
C_i	SCL	$V_I = V_{CC}$ or GND	2.3 V to 5.5 V		4	5	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.3 V to 5.5 V		5.5	6.5	pF
	P port				8	9.5	

(1) All typical values are at nominal supply voltage (2.5-, 3.3-, or 5-V V_{CC}) and T_A = 25°C.
(2) The total current sourced by all I/Os must be limited to 85 mA.
(3) Each I/O must be externally limited to a maximum of 25 mA, and the P port (P7 – P0) must be limited to a maximum current of 200 mA.
(4) RESET = V_{CC} (held high) when all other input voltages, V_I = GND.

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5.6 I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see 图 6-1)

			MIN	MAX	UNIT
STANDARD MODE					
f_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		μs
t_{scl}	I²C clock low time		4.7		μs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between Stop and Start		4.7		μs
t_{sts}	I²C Start or repeated Start condition setup		4.7		μs
t_{sth}	I²C Start or repeated Start condition hold		4		μs
t_{sps}	I²C Stop condition setup		4		μs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid	300		ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.3	3.45	μs
C_b	I²C bus capacitive load			400	ns
FAST MODE					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		μs
t_{scl}	I²C clock low time		1.3		μs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		$20 + 0.1C_b$ (1)	300	ns
t_{icf}	I²C input fall time		$20 + 0.1C_b$ (1)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	$20 + 0.1C_b$ (1)	300	ns
t_{buf}	I²C bus free time between Stop and Start		1.3		μs
t_{sts}	I²C Start or repeated Start condition setup		0.6		μs
t_{sth}	I²C Start or repeated Start condition hold		0.6		μs
t_{sps}	I²C Stop condition setup		0.6		μs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid	50		ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low	0.1	0.9	μs
C_b	I²C bus capacitive load			400	ns

(1) C_b = Total capacitance of one bus in pF

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5.7 $\overline{\text{RESET}}$ Timing Requirements

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
STANDARD MODE and FAST MODE				
t_W	Reset pulse duration	4		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset	400		ns

5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see 图 6-2 and 图 6-3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
STANDARD MODE and FAST MODE						
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	μs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	μs
t_{pv}	Output data valid	SCL	P7 – P0		200	ns
t_{ps}	Input data setup time	P port	SCL	100		ns
t_{ph}	Input data hold time	P port	SCL	1		μs

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5.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

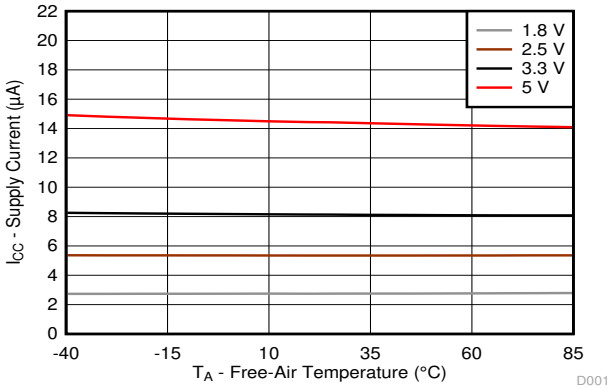

图 5-1. Supply Current (I_{CC}, Operating Mode) vs Temperature (T_A) at Four Supply Voltages

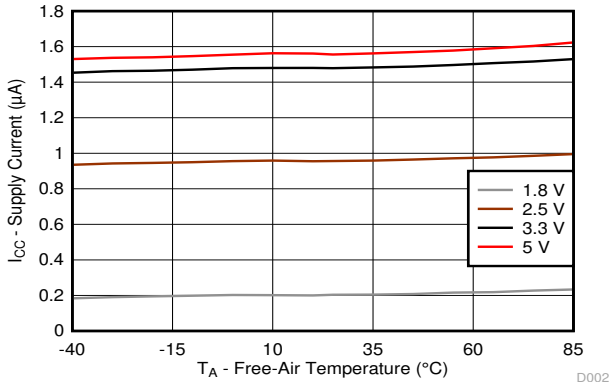

图 5-2. Supply Current (ICC, Standby Mode) vs Temperature (T_A) at Four Supply Voltages

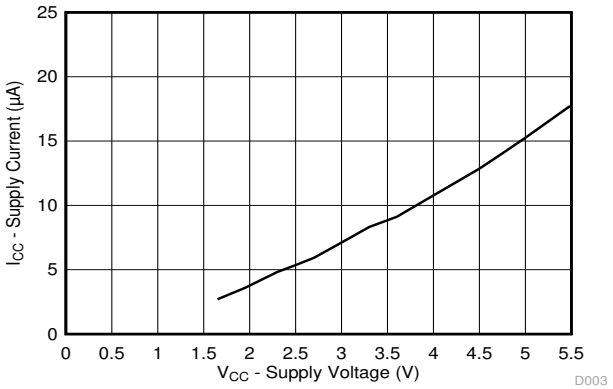

图 5-3. Supply Current (I_{CC}, Operating Mode) vs Supply Voltage (V_{CC})

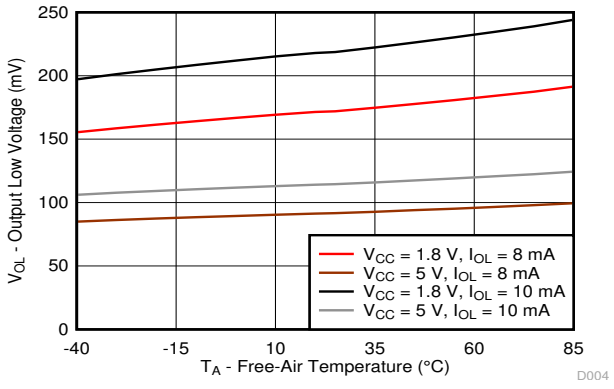

图 5-4. Output Low Voltage (V_{OL}) vs Temperature (T_A) for P-Port I/Os

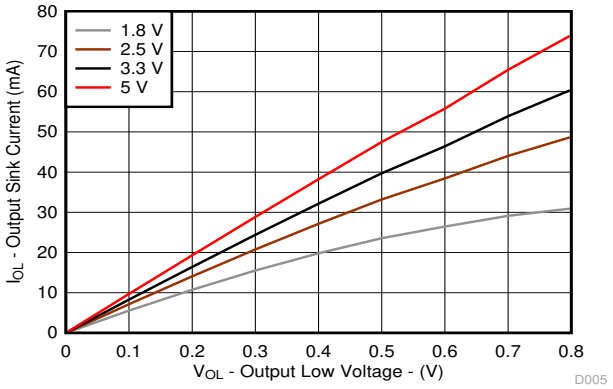

图 5-5. Sink Current (I_{OL}) vs Output Low Voltage (V_{OL}) for P-Ports at Four Supply Voltages

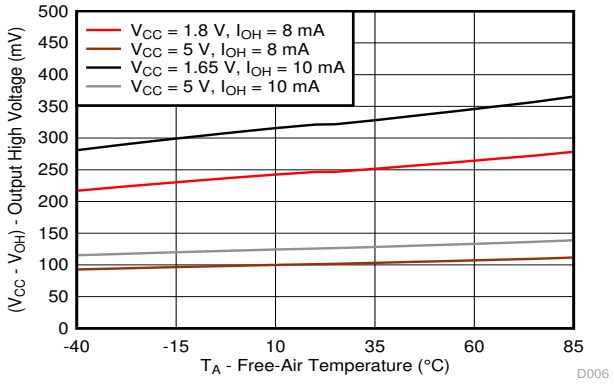

图 5-6. Output High Voltage (V_{CC} – V_{OH}) vs Temperature (T_A) for P-Ports

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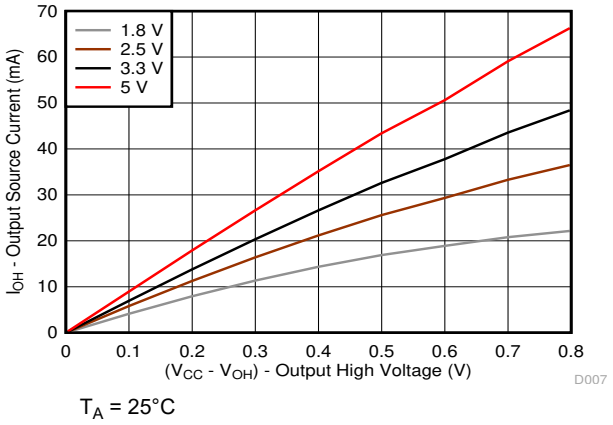
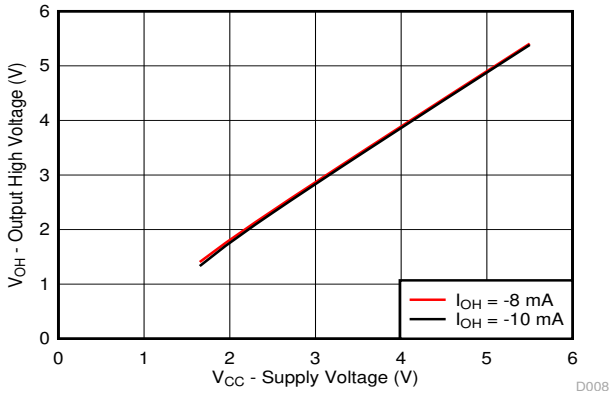
5.9 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)



T_A = 25°C

图 5-7. Source Current (I_{OH}) vs Output High Voltage (V_{OH}) for P-Ports at Four Supply Voltages



T_A = 25°C

图 5-8. Output High Voltage (V_{OH}) vs Supply Voltage (V_{CC}) for P-Ports

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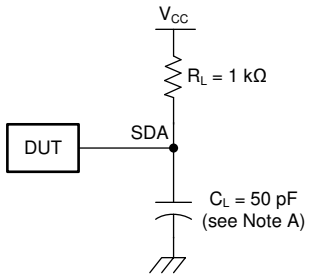
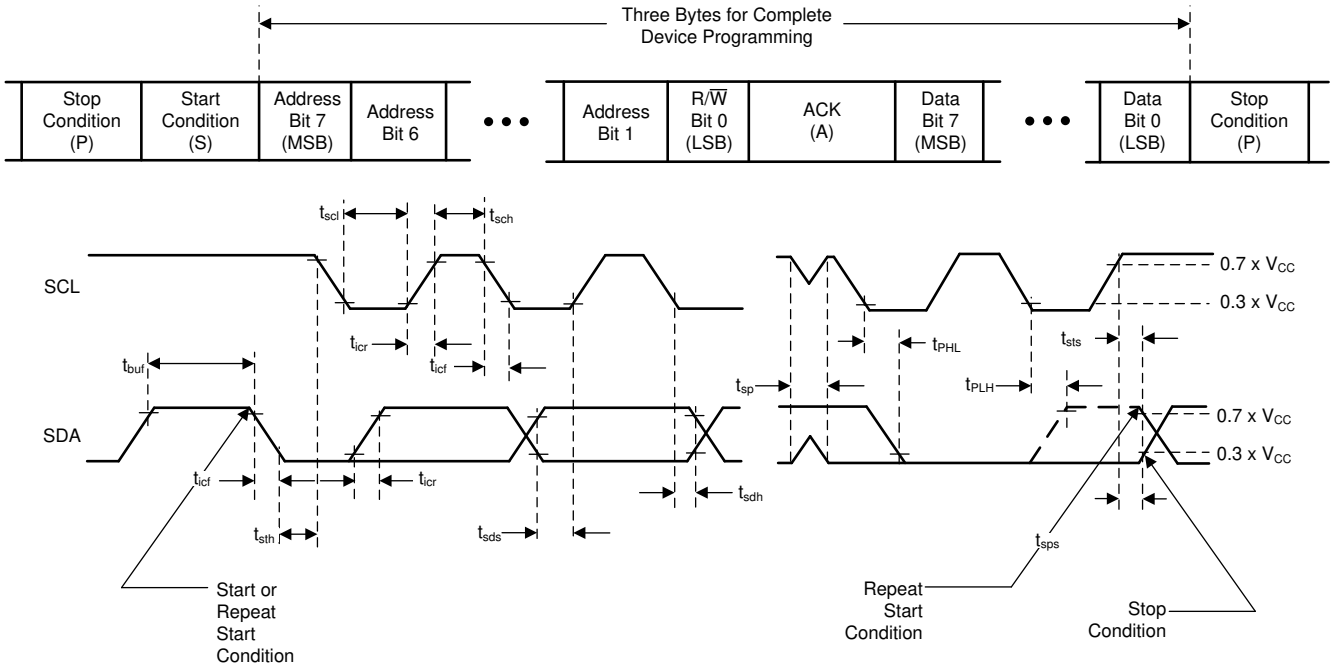
6 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, Z_O = 50 Ω, t_r/t_f ⩽ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

图 6-1. I²C Interface Load Circuit and Voltage Waveforms

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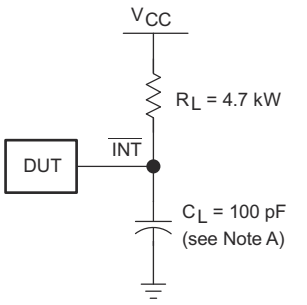
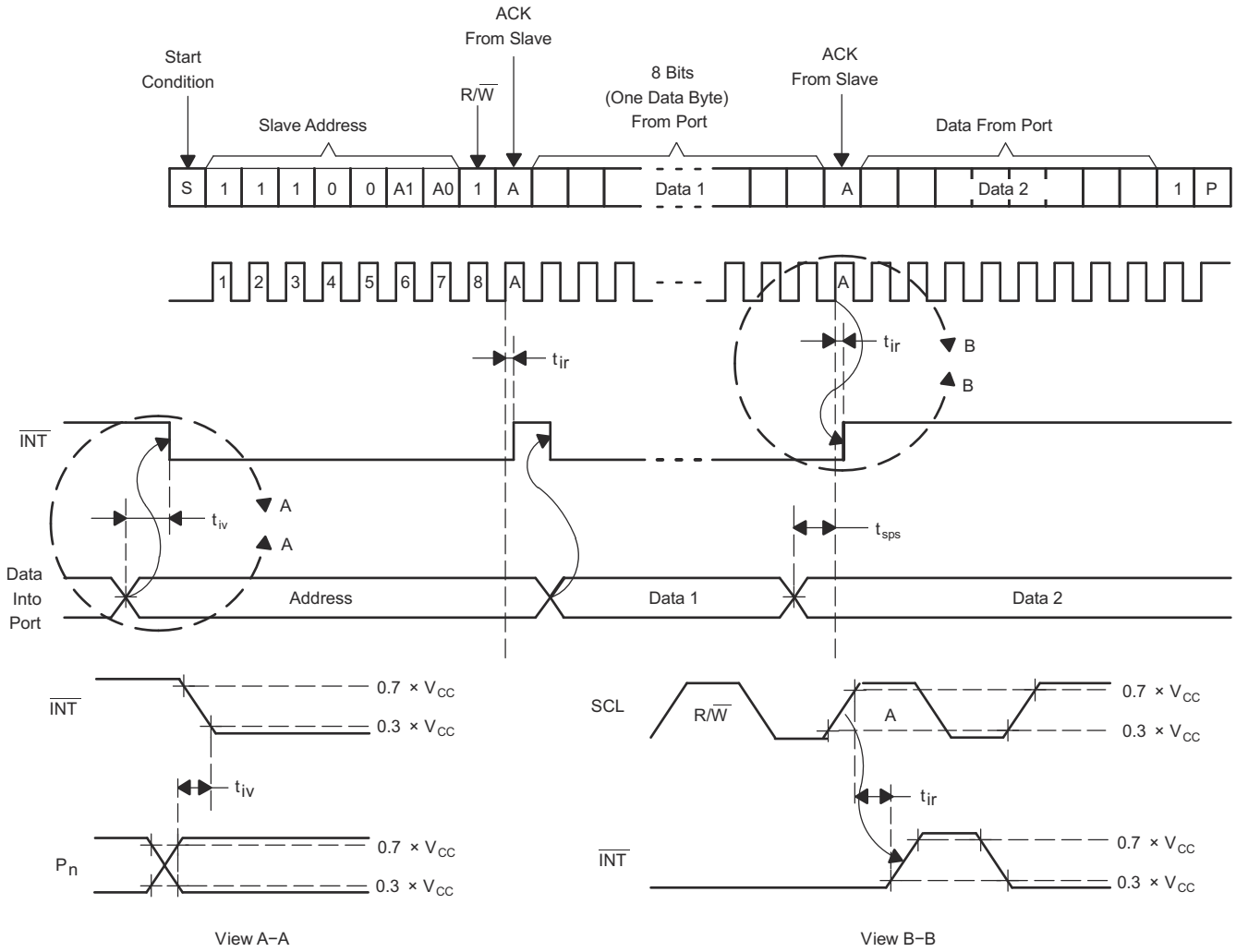


INTERRUPT LOAD CONFIGURATION



View A–A View B–B

A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. All parameters and waveforms are not applicable to all devices.

图 6-2. Interrupt Load Circuit and Voltage Waveforms

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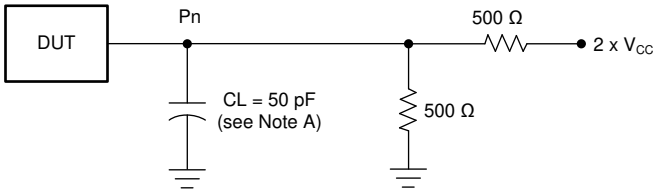
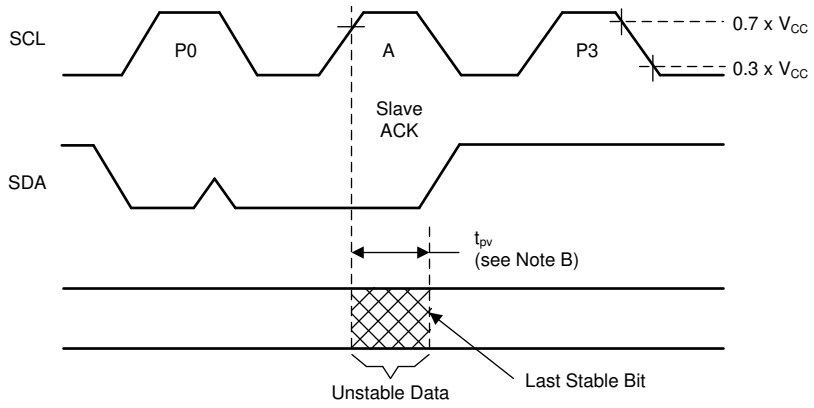
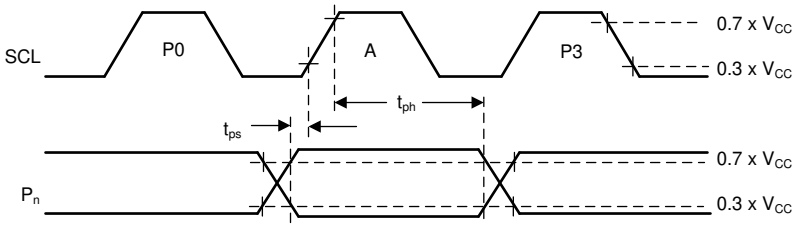


P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. All parameters and waveforms are not applicable to all devices.

图 6-3. P-Port Load Circuit and Voltage Waveforms

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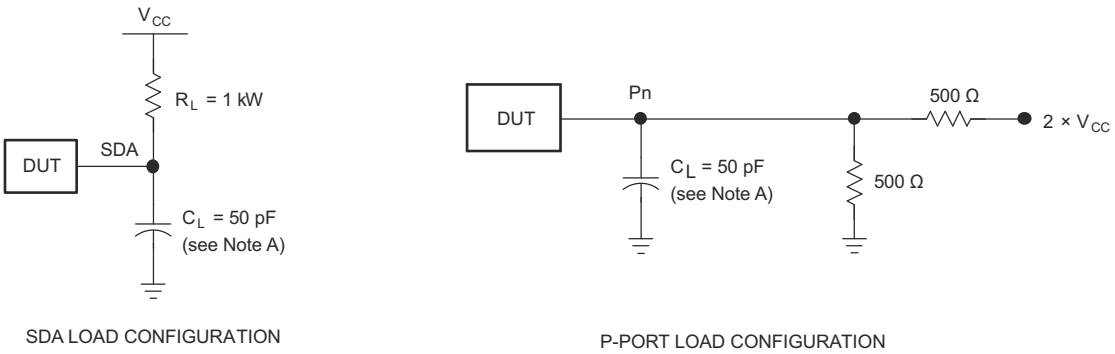

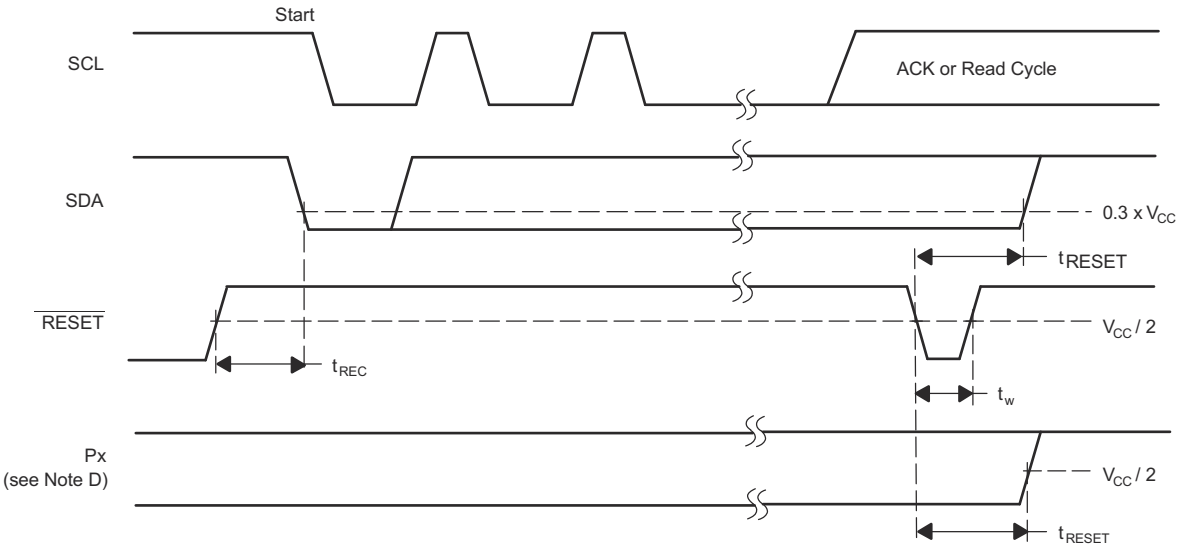

A. C_L includes probe and jig capacitance.
B. All inputs are supplied by generators having the following characteristics: PRR ⩽ 10 MHz, Z_O = 50 Ω, t_r/t_f ⩽ 30 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. I/Os are configured as inputs.
E. All parameters and waveforms are not applicable to all devices.

图 6-4. Reset Load Circuits and Voltage Waveforms

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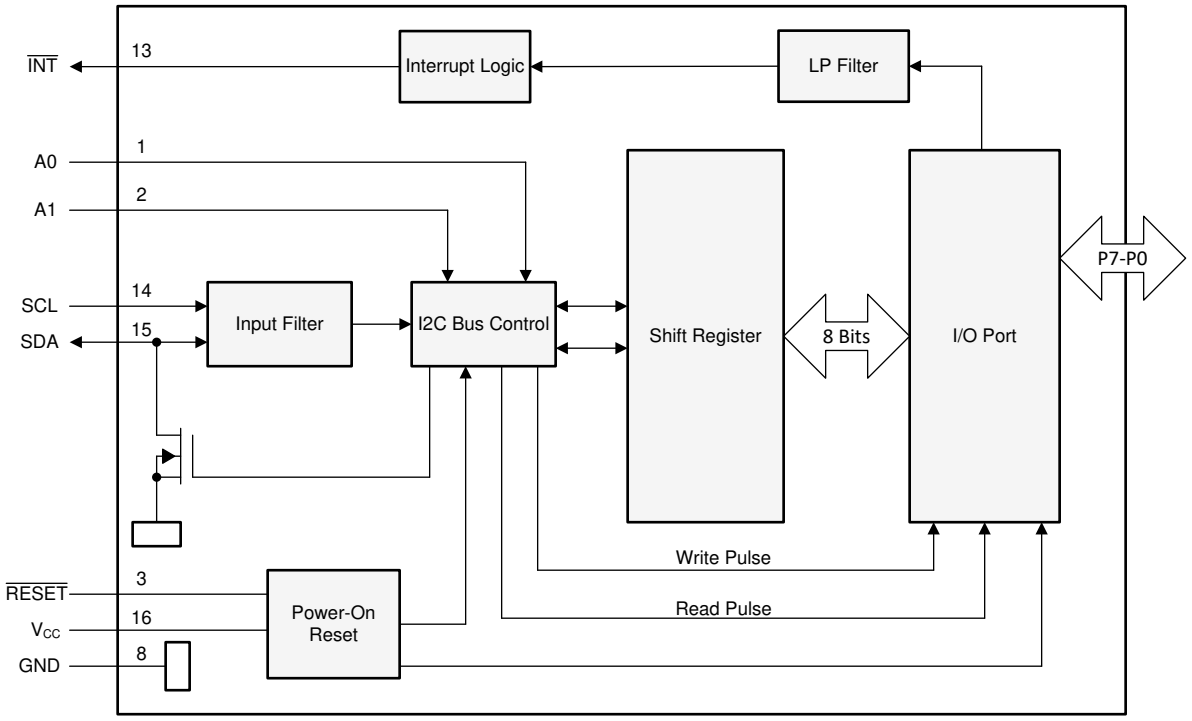
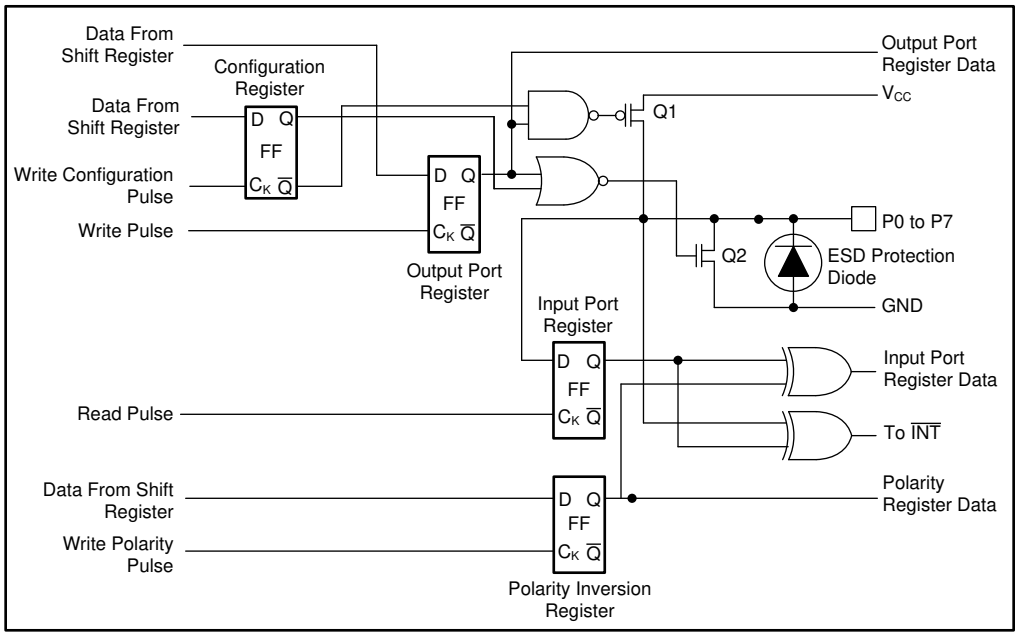
7 Detailed Description

7.1 Functional Block Diagram



Pin numbers shown are for the DB, DBQ, DGV, DW, or PW package.

图 7-1. Functional Block Diagram



At power-on reset, all registers return to default values.

图 7-2. Simplified Schematic Of P0 To P7

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7.2 Device Functional Modes

7.2.1 $\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input can be asserted to reset the system while keeping the V_{CC} at its operating level. A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The PCA9538 registers and I^2C/SMBus state machine are changed to their default states once $\overline{\text{RESET}}$ is low (0). Once $\overline{\text{RESET}}$ is high (1), the I/O levels at the P port can be changed externally or through the master. This input requires a pullup resistor to V_{CC} if no active connection is used.

7.2.1.1 $\overline{\text{RESET}}$ Errata

If $\overline{\text{RESET}}$ voltage set higher than VCC, current flows from $\overline{\text{RESET}}$ pin to VCC pin.

System Impact

VCC is pulled above its regular voltage level.

System Workaround

Design such that $\overline{\text{RESET}}$ voltage is same or lower than VCC.

7.2.2 Power-On Reset

When power (from 0 V) is applied to V_{CC}, an internal power-on reset holds the PCA9538 in a reset condition until V_{CC} has reached V_{POR}. At that point, the reset condition is released and the PCA9538 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below 0.2 V and then back up to the operating voltage for a power-reset cycle.

7.2.3 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 (in Simplified Schematic Of P0 To P7) are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

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7.2.4 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting, data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal.

Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register. Because each 8-pin port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1 or vice versa.

The $\overline{INT}$ output has an open-drain structure and requires pullup resistor to V_{CC}.

7.2.4.1 Interrupt Errata

The INT will be improperly de-asserted if the following two conditions occur:

1. The last I²C command byte (register pointer) written to the device was 00h.

Note

This generally means the last operation with the device was a Read of the input register. However, the command byte may have been written with 00h without ever going on to read the input register. After reading from the device, if no other command byte written, it remains 00h.

2. Any other slave device on the I²C bus acknowledges an address byte with the R/W bit set high

System Impact

Can cause improper interrupt handling as the Master sees the interrupt as being cleared.

System Workaround

Minor software change: User must change command byte to something besides 00h after a Read operation to the PCA9538 device or before reading from another slave device.

Note

Software change are compatible with other versions (competition and TI redesigns) of this device.

7.3 Programming

7.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply through a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a master sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see 图 7-3). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/ $\overline{W}$).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A0 – A1) of the slave device must not be changed between the Start and the Stop conditions.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see 图 7-4).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see 图 7-3).

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Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 图 7-5). When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

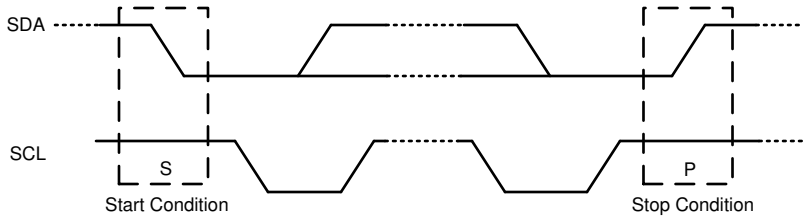

图 7-3. Definition Of Start And Stop Conditions

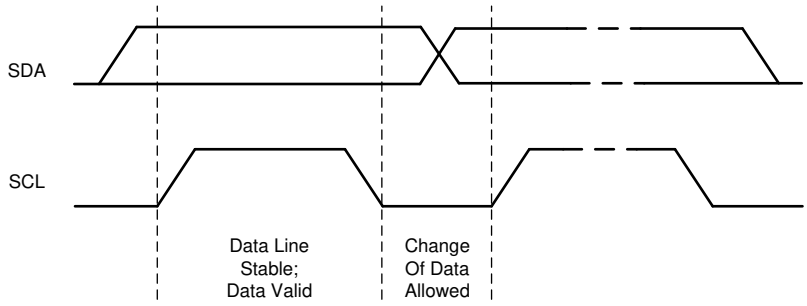

图 7-4. Bit Transfer

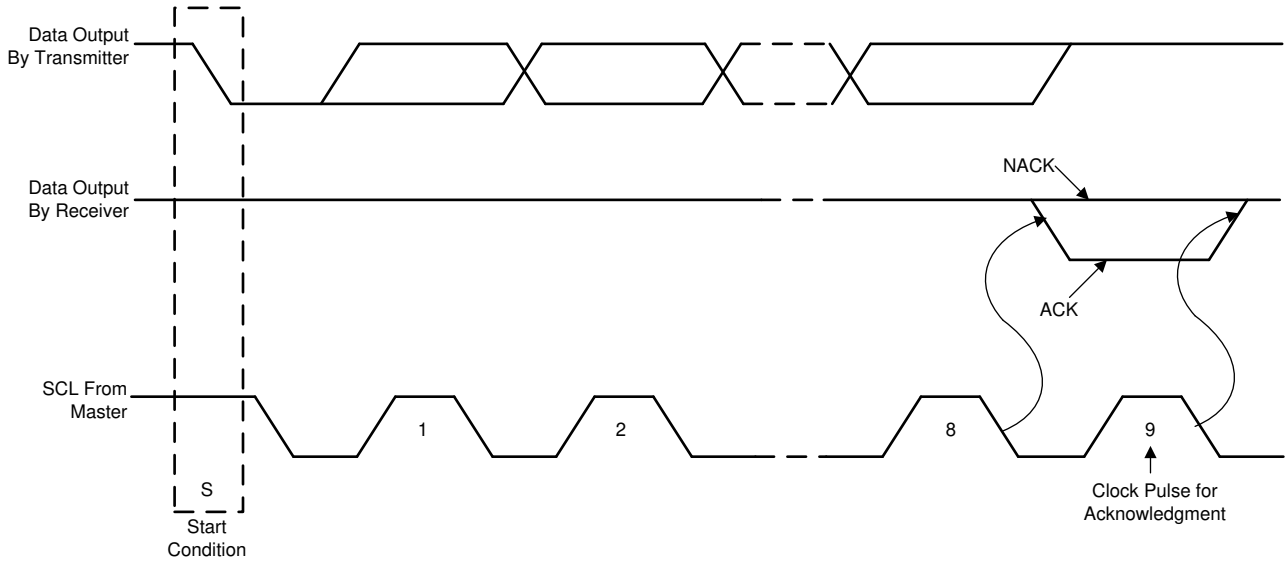

图 7-5. Acknowledgment On I^2C Bus

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7.4 Register Maps

表 7-1 shows the address byte of the PCA9538.

表 7-1. Interface Definition Table

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	H	H	H	L	L	A1	A0	R/ $\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

7.4.1 Device Address

图 7-6 shows the address byte of the PCA9538.

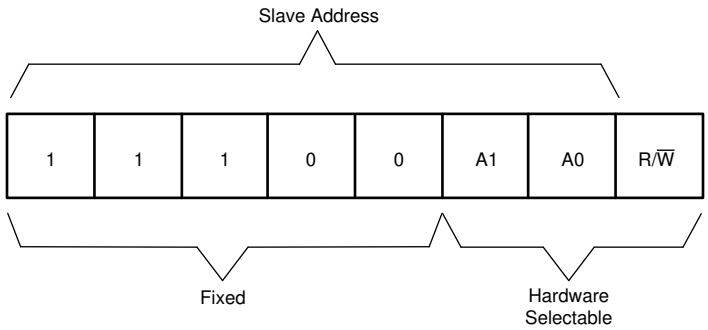

图 7-6. PCA9538 Address

表 7-2 shows the PCA9538 address reference.

表 7-2. Address Reference Table

INPUTS		I²C BUS SLAVE ADDRESS
A1	A0	
L	L	112 (decimal), 70 (hexadecimal)
L	H	113 (decimal), 71 (hexadecimal)
H	L	114 (decimal), 72 (hexadecimal)
H	H	115 (decimal), 73 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected while a low (0) selects a write operation.

7.4.2 Control Register And Command Byte

Following the successful Acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the PCA9538 (see 图 7-7). Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that are affected. This register can be written or read through the I²C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

图 7-7 shows the PCA9538 control register bits and 表 7-3 shows the command byte.

0	0	0	0	0	0	B1	B0

图 7-7. Control Register Bits

表 7-3. Command Byte Table

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0×00	Input Port	Read byte	XXXX XXXX
0	1	0×01	Output Port	Read/write byte	1111 1111
1	0	0×02	Polarity Inversion	Read/write byte	0000 0000
1	1	0×03	Configuration	Read/write byte	1111 1111

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7.4.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register is accessed next. See 表 7-4.

表 7-4. Register 0 (Input Port Register) Table

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See 表 7-5.

表 7-5. Register 1 (Output Port Register) Table

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained. See 表 7-6.

表 7-6. Register 2 (Polarity Inversion Register) Table

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See 表 7-7.

表 7-7. Register 3 (Configuration Register) Table

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

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7.4.4 Bus Transactions

Data is exchanged between the master and PCA9538 through write and read commands.

7.4.4.1 Writes

Data is transmitted to the PCA9538 by sending the device address and setting the least-significant bit (LSB) to a logic 0 (see 图 7-6 for device address). The command byte is sent after the address and determines which register receives the data that follows the command byte (see 图 7-8 and 图 7-9). There is no limitation on the number of data bytes sent in one write transmission.

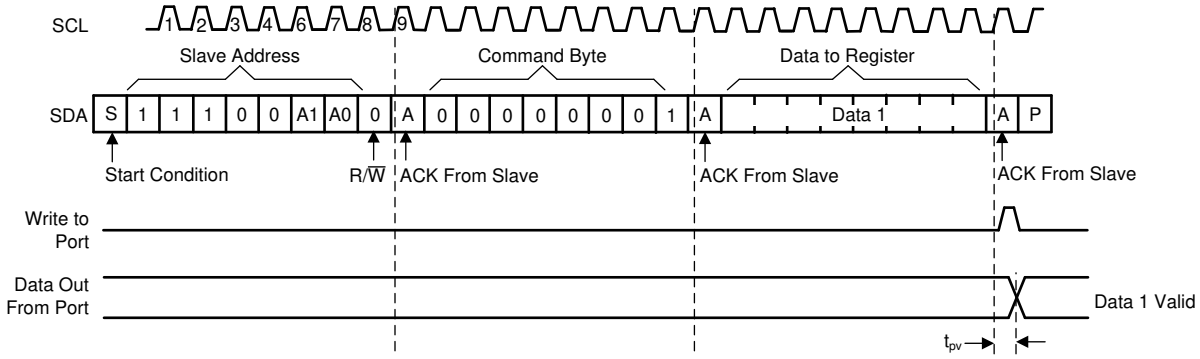

图 7-8. Write To Output Port Register

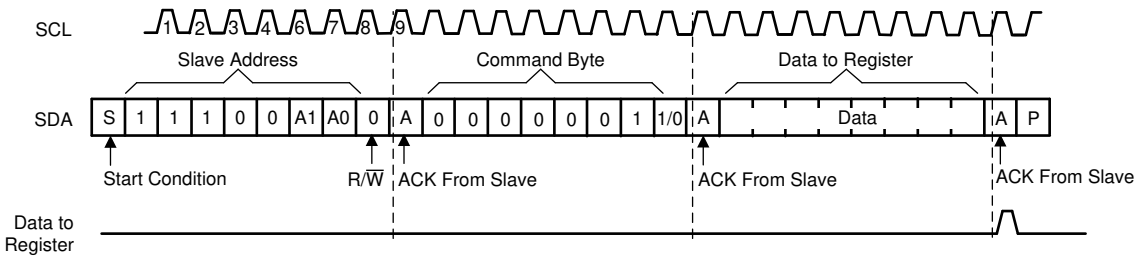

图 7-9. Write To Configuration Or Polarity Inversion Registers

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7.4.4.2 Reads

The bus master first must send the PCA9538 address with the LSB set to a logic 0 (see 图 7-6 for device address). The command byte is sent after the address and determines which register is accessed. After a restart, the device address is sent again but, this time, the LSB is set to a logic 1. Data from the register defined by the command byte then is sent by the PCA9538 (see 图 7-10 and 图 7-11). After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.

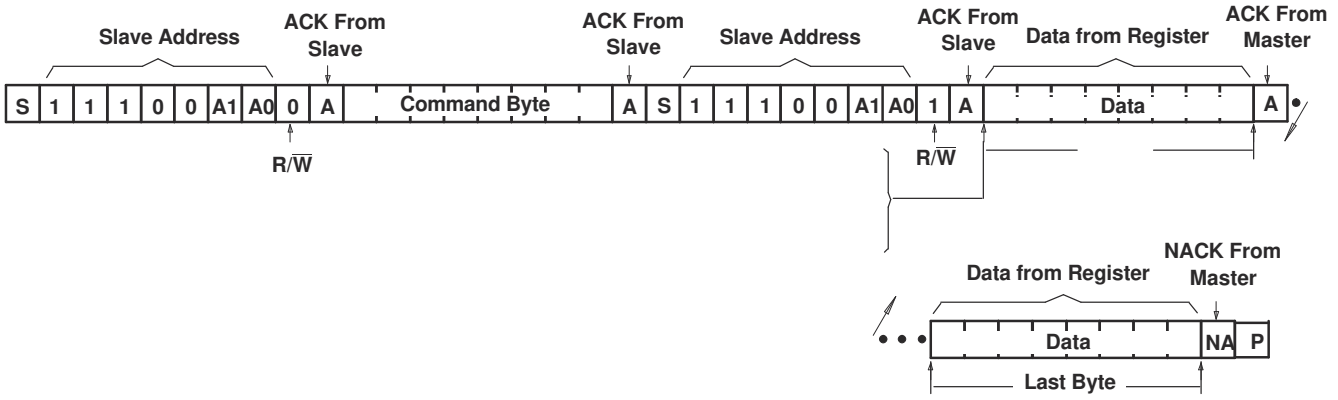
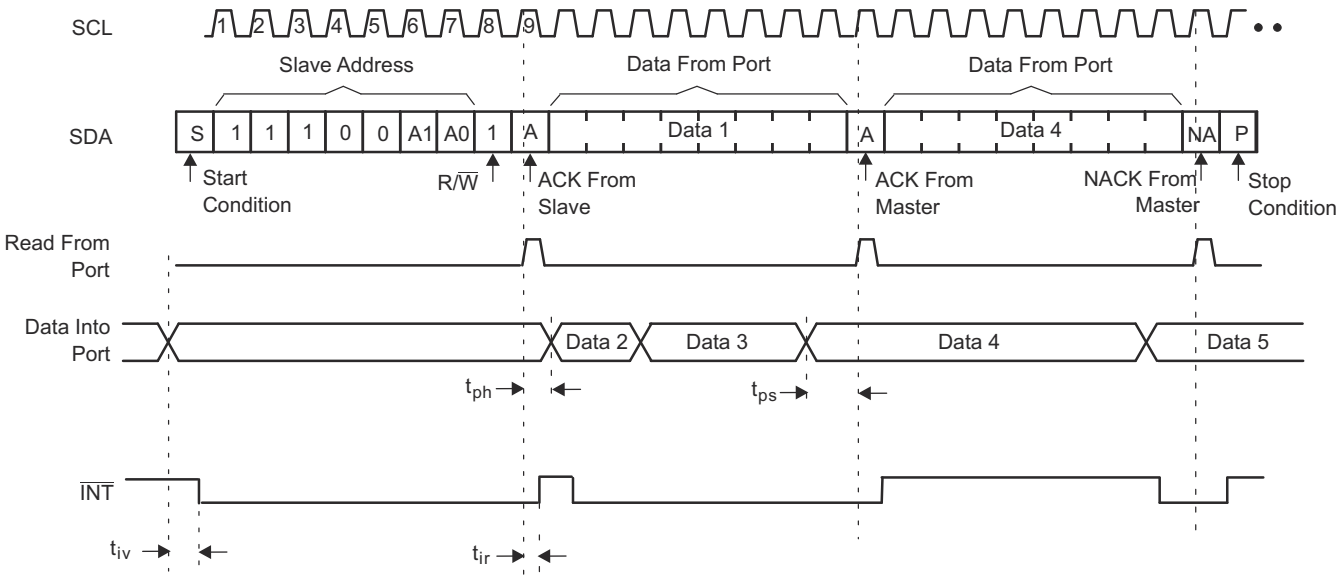


图 7-10. Read From Register



A. This figure assumes the command byte has previously been programmed with 00h.
B. Transfer of data can be stopped at any moment by a Stop condition.
C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port. See 图 7-10 for these details.

图 7-11. Read From Input Port Register

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8 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

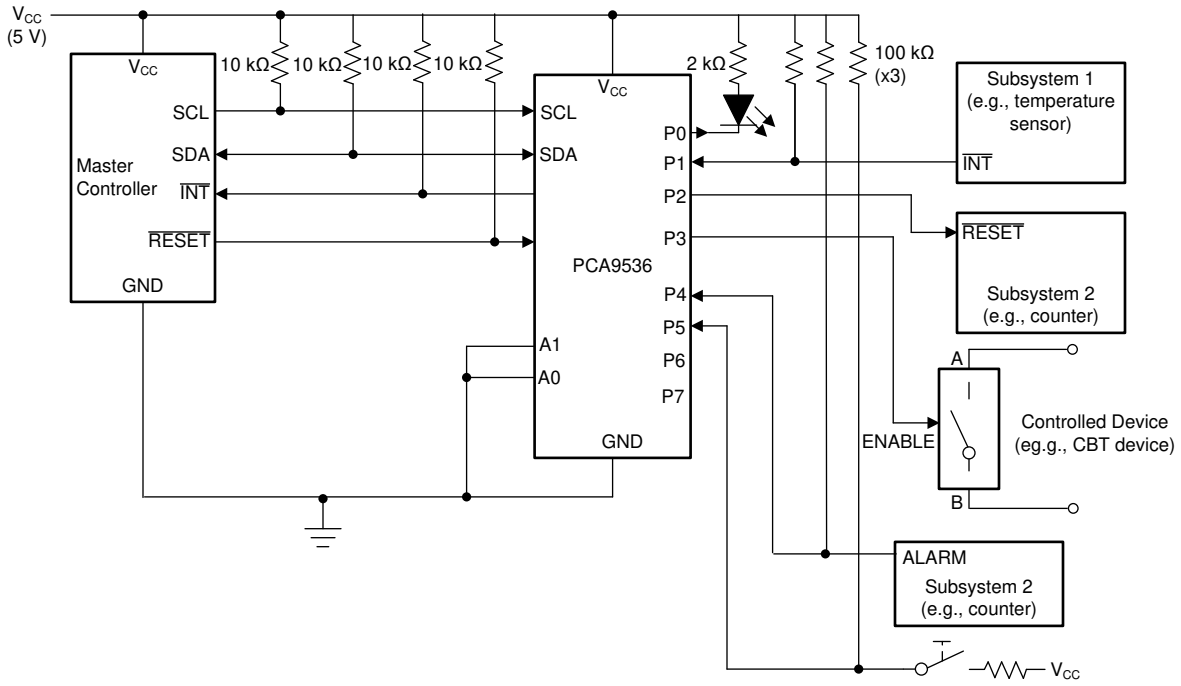
8.1 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.2 Typical Application

图 8-1 shows an application in which the PCA9538 can be used.



A. Device address is configured as 1110000 for this example.
B. P0, P2, and P3 are configured as outputs.
C. P1, P4, and P5 are configured as inputs.
D. P6 and P7 are not used and must be configured as outputs.

图 8-1. Typical Application

8.2.1 Detailed Design Procedure

8.2.1.1 Minimizing I_{CC} When I/Os Control Leds

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in 图 8-1. The LED acts as a diode, so when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. I_{CC} in Electrical Characteristics shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}.

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For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC} when the LED is off to minimize current consumption. 图 8-2 shows a high-value resistor in parallel with the LED. 图 8-3 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{IN} at or above V_{CC} and prevents additional supply current consumption when the LED is off.

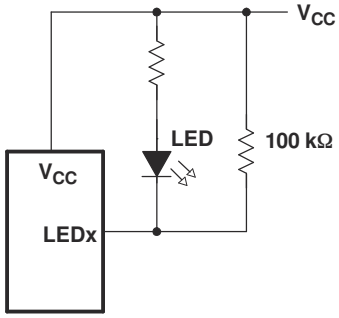

图 8-2. High-Value Resistor in Parallel with Led

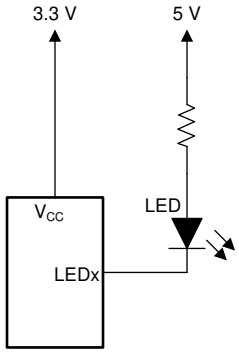

图 8-3. Device Supplied by a Lower Voltage

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9 Power Supply Recommendations

9.1 Power-On Reset Requirements

In the event of a glitch or data corruption, PCA9538 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 图 9-1 and 图 9-2.

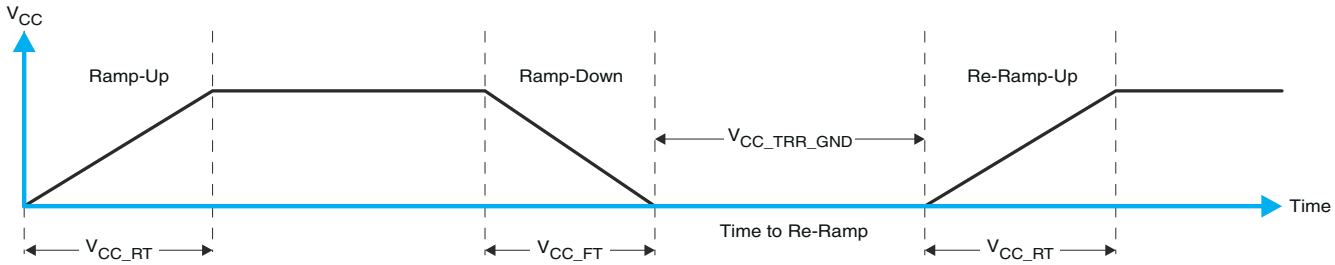

图 9-1. V_{CC} Is Lowered Below 0.2 V Or 0 V And Then Ramped Up To V_{CC}

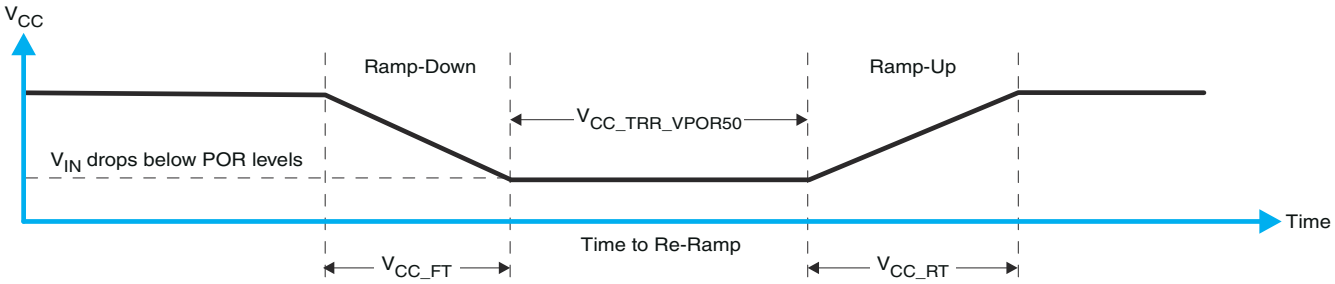

图 9-2. V_{CC} Is Lowered Below The Por Threshold, Then Ramped Back Up To V_{CC}

表 9-1 specifies the performance of the power-on reset feature for PCA9538 for both types of power-on reset.

表 9-1. Recommended Supply Sequencing And Ramp Rates(1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 图 9-1	1		100	ms
V_{CC_RT}	Rise rate	See 图 9-1	0.01		100	ms
$V_{CC\_TRR\_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 图 9-1	0.001			ms
$V_{CC\_TRR\_POR50}$	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV)	See 图 9-2	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 μs	See 图 9-3			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See 图 9-3				μs
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.767		1.144	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.033		1.428	V

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and the device impedance are factors that affect power-on reset performance. 图 9-3 and 表 9-1 provide more information on how to measure these specifications.

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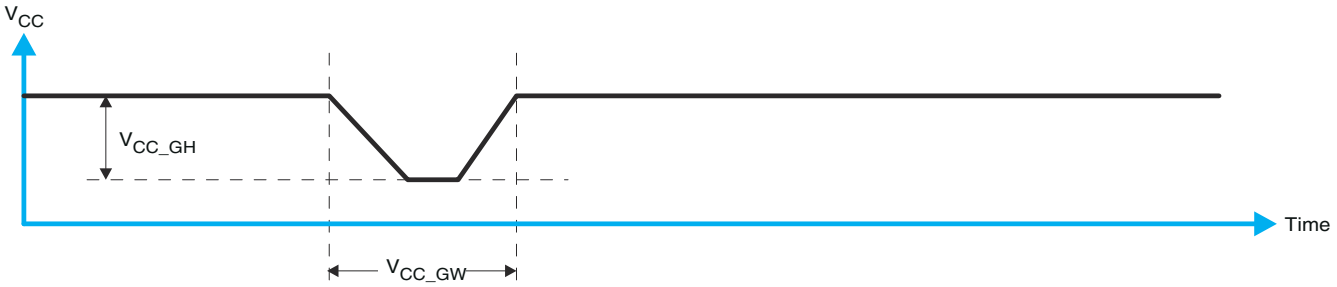

图 9-3. Glitch Width And Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 图 9-4 and 表 9-1 provide more details on this specification.

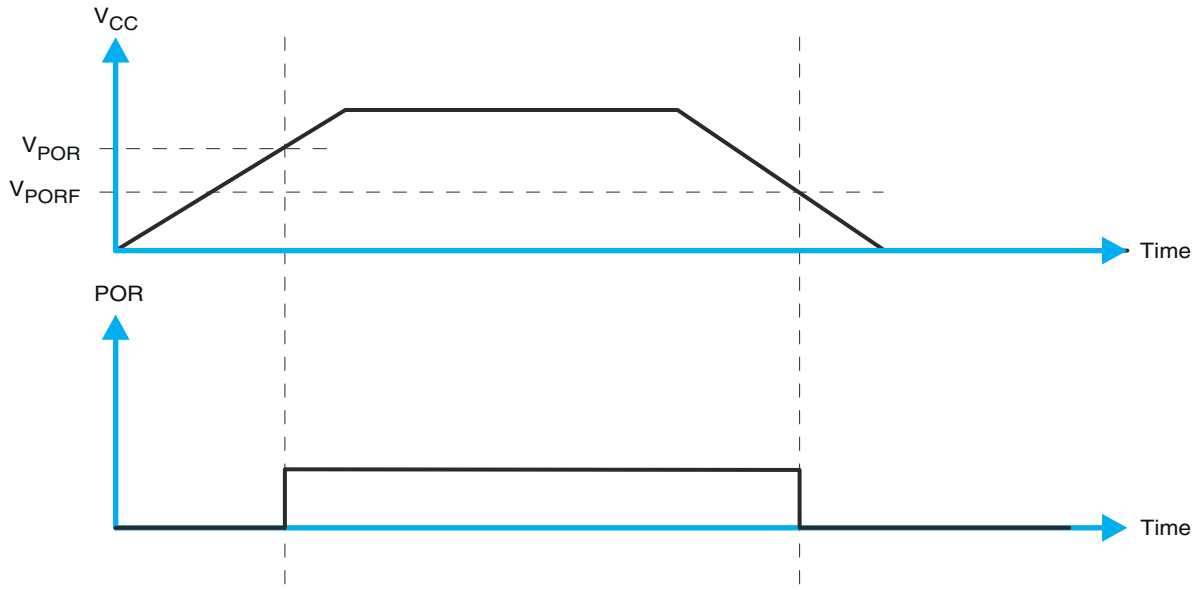

图 9-4. V_{POR}

10 Device and Documentation Support

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

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10.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCA9538DB	ACTIVE	SSOP	DB	16	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD538	Samples
PCA9538DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD538	Samples
PCA9538DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD538	Samples
PCA9538DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9538	Samples
PCA9538DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCA9538	Samples
PCA9538PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PD538	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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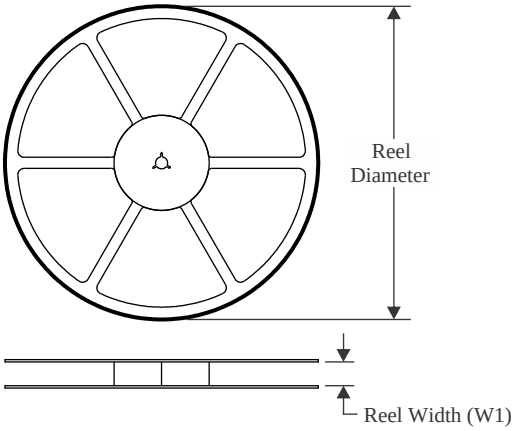
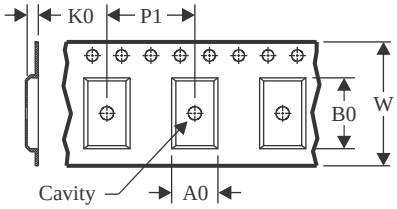
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

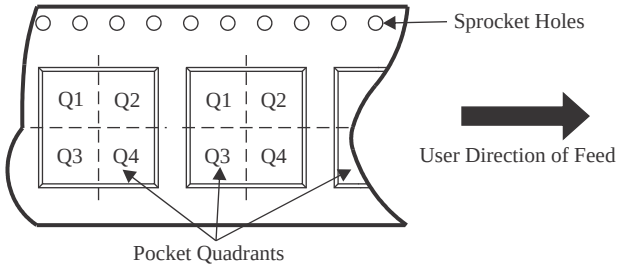


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

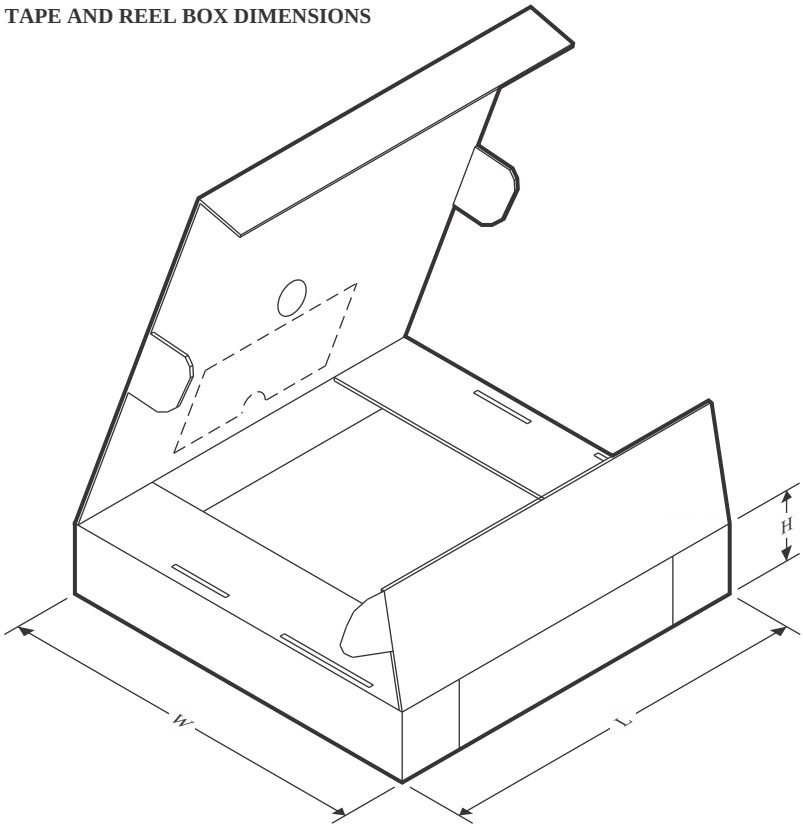
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCA9538DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
PCA9538DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
PCA9538DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
PCA9538PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCA9538PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

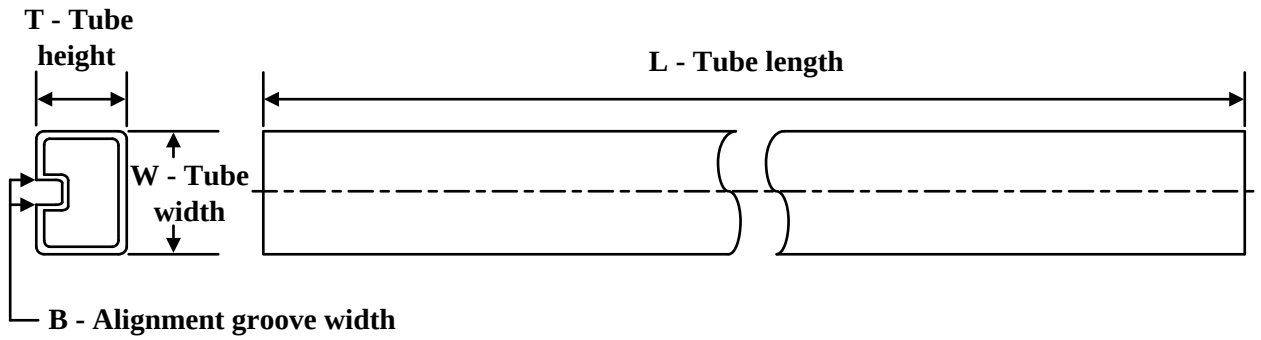
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCA9538DBR	SSOP	DB	16	2000	356.0	356.0	35.0
PCA9538DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
PCA9538DWR	SOIC	DW	16	2000	350.0	350.0	43.0
PCA9538PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
PCA9538PWR	TSSOP	PW	16	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

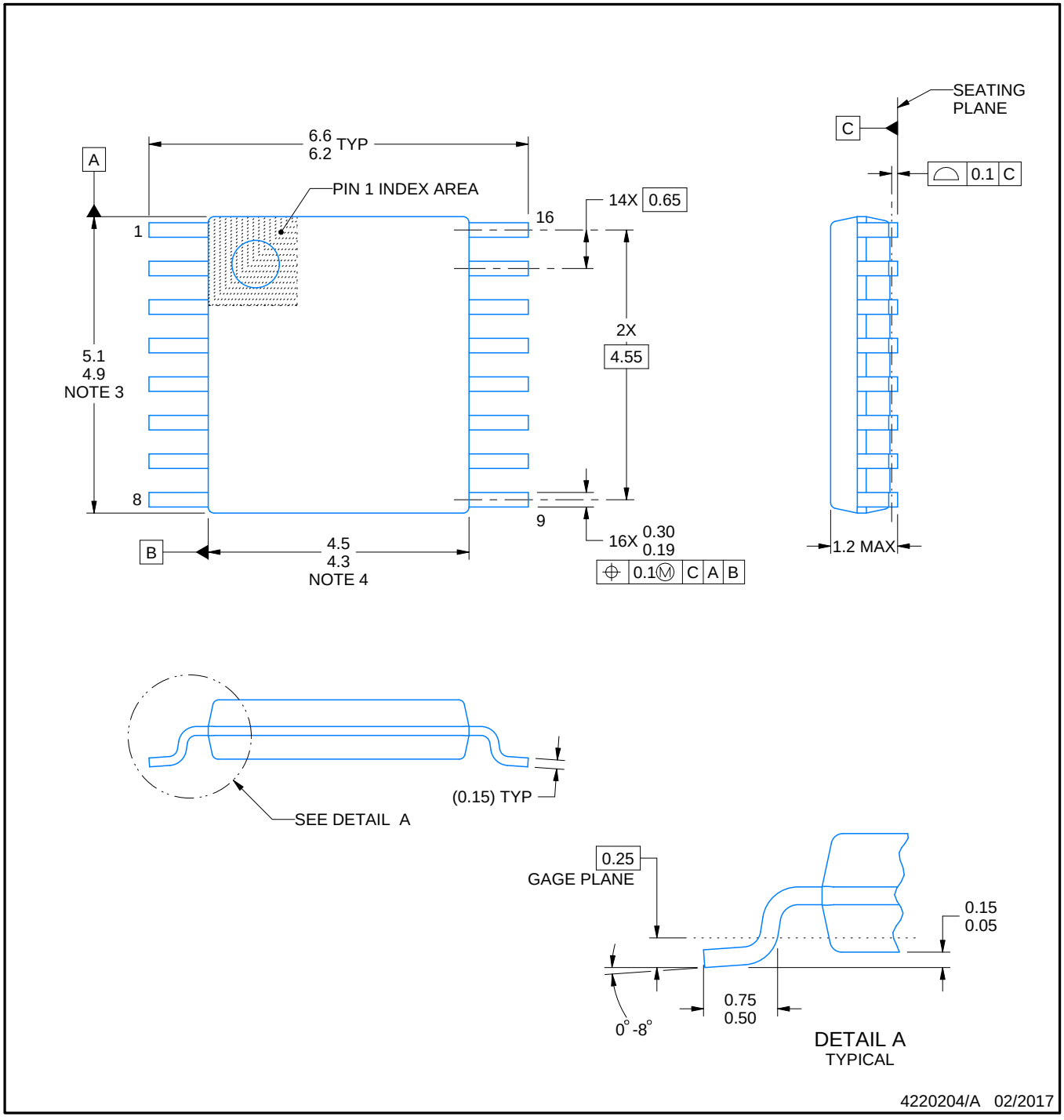
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PCA9538DB	DB	SSOP	16	80	530	10.5	4000	4.1
PCA9538DW	DW	SOIC	16	40	506.98	12.7	4826	6.6

PACKAGE OUTLINE

PW0016A

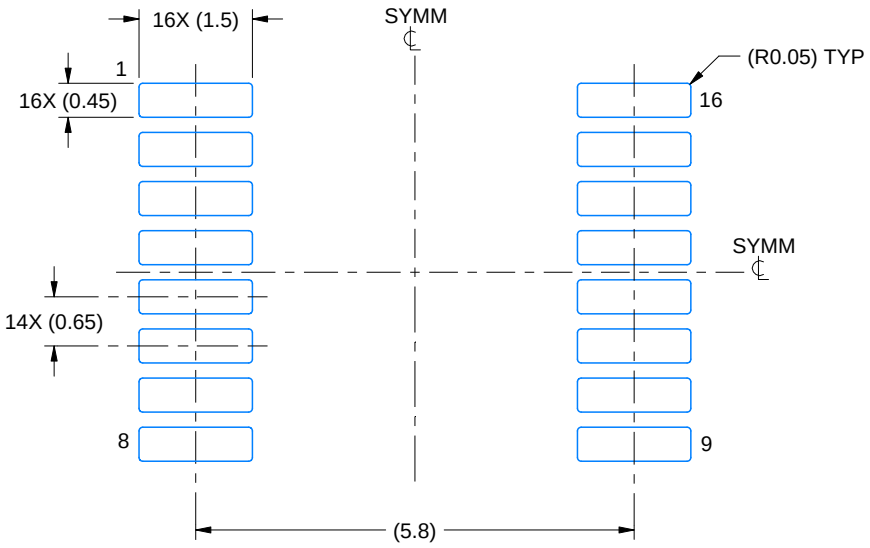
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

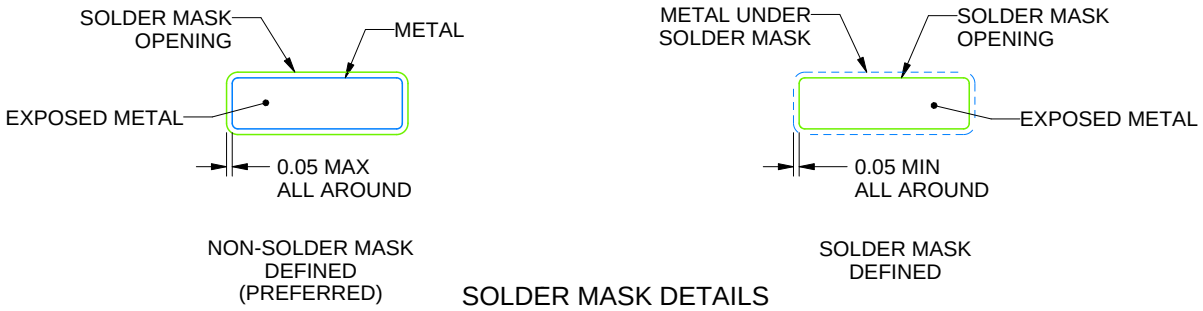


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

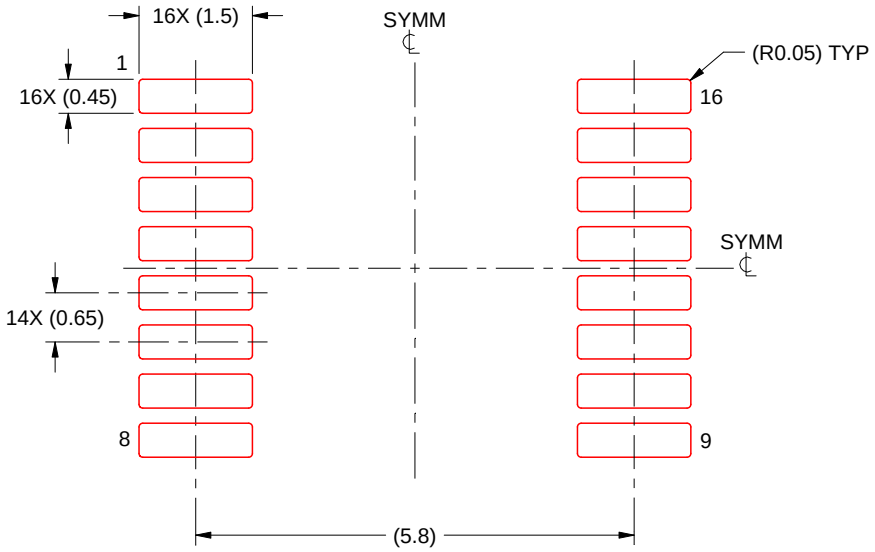


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

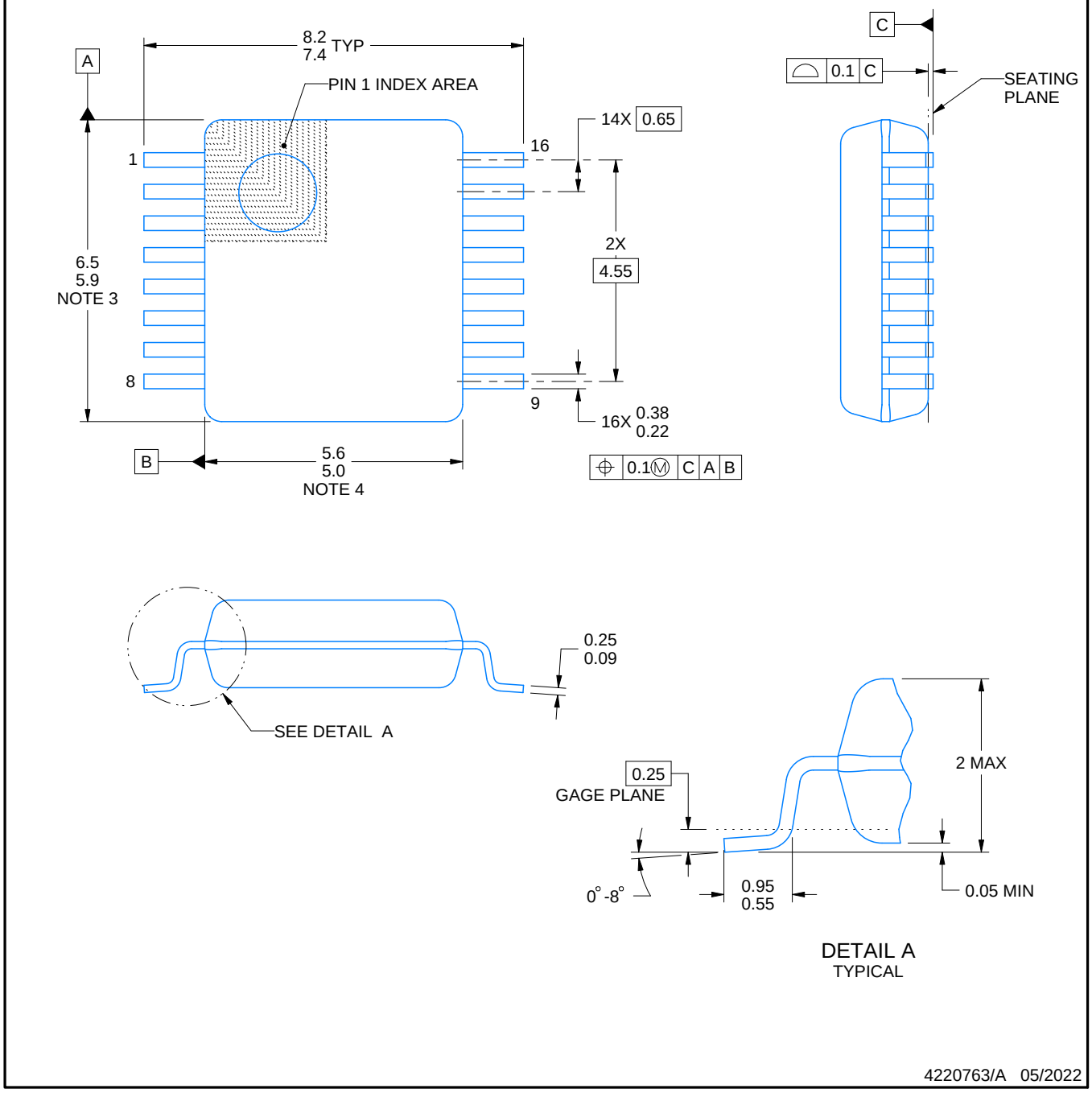
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

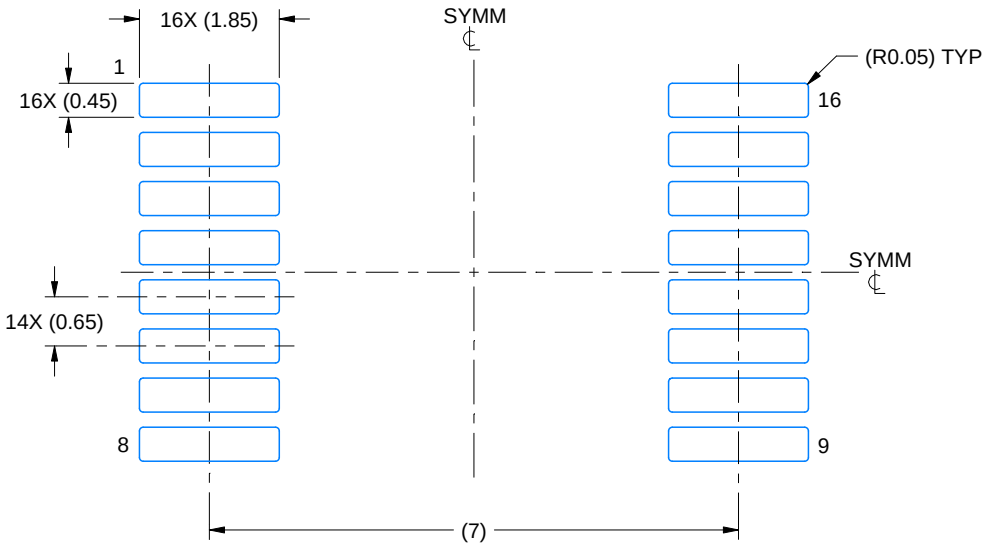
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

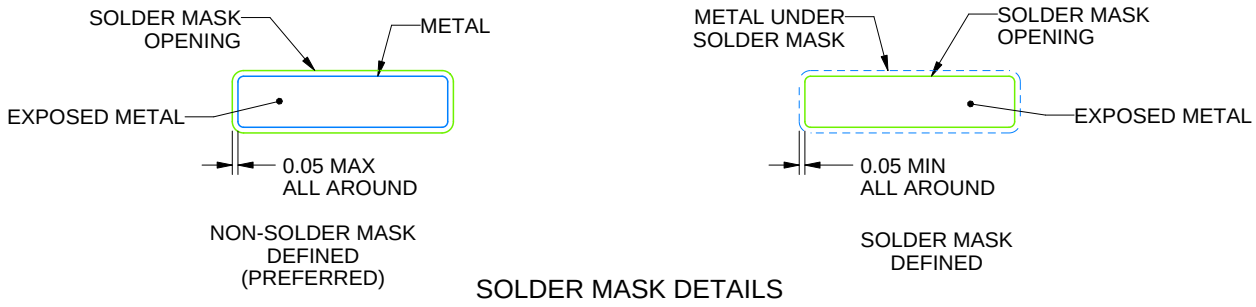


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

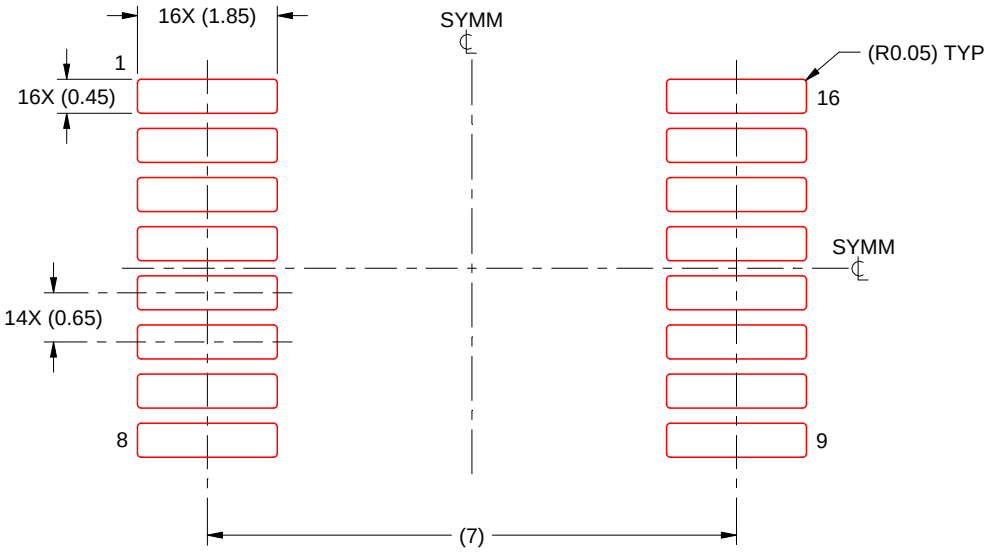


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

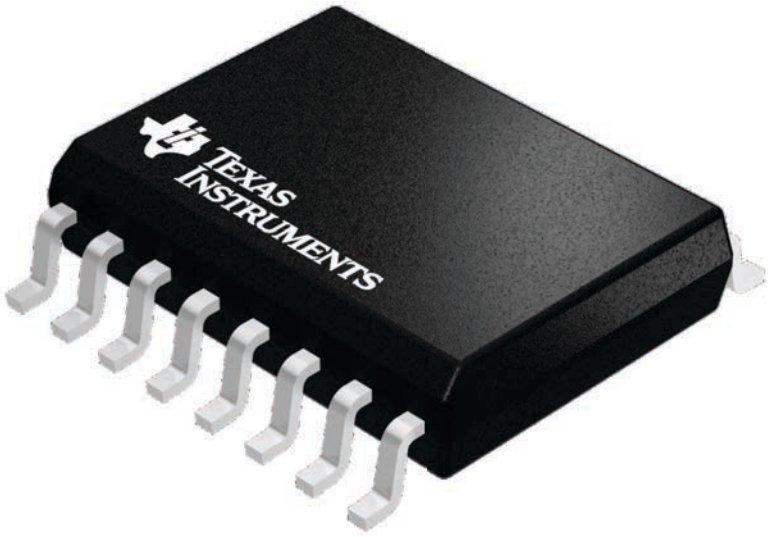
DW 16

SOIC - 2.65 mm max height

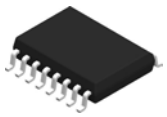
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

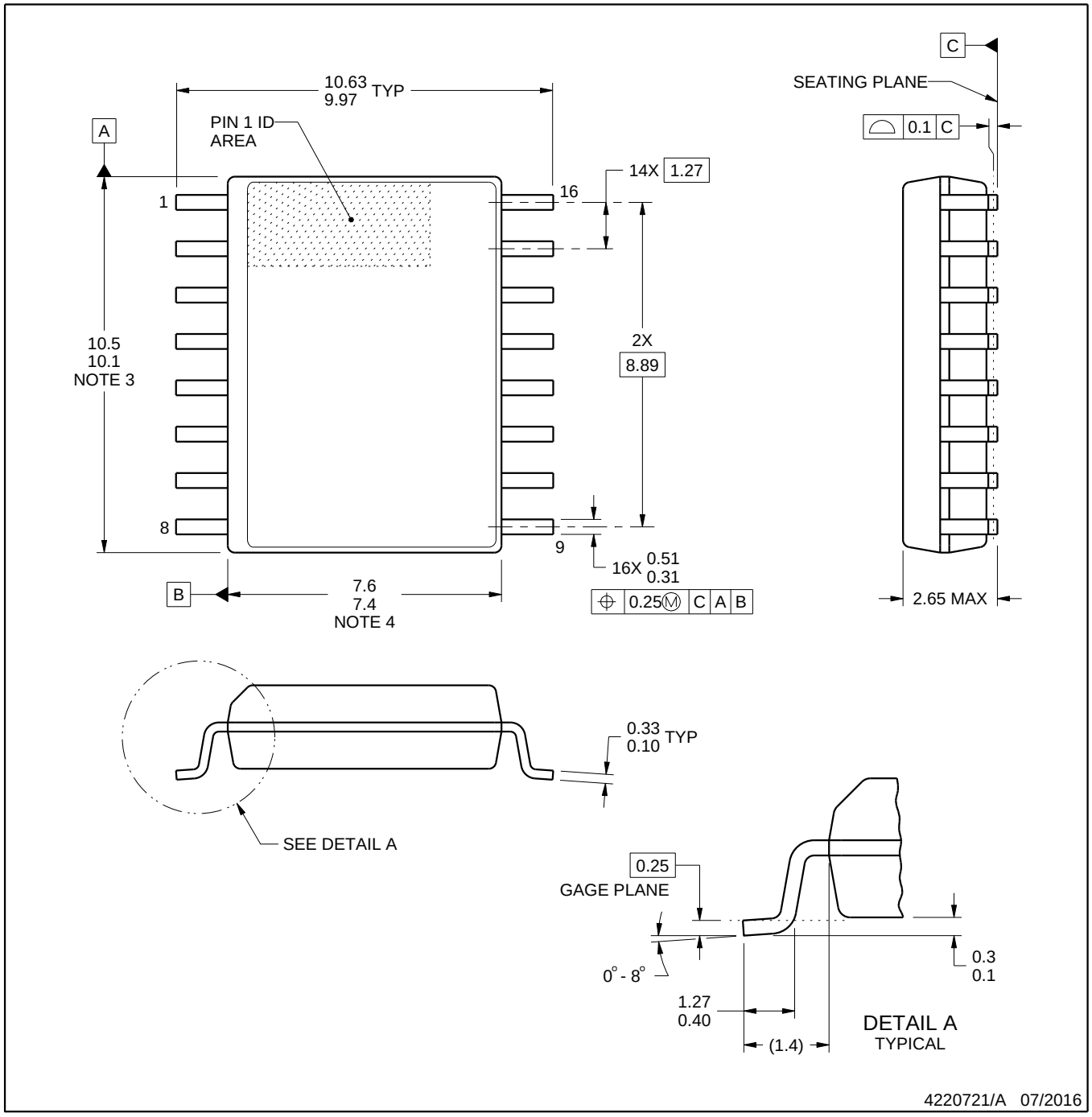


PACKAGE OUTLINE

DW0016A

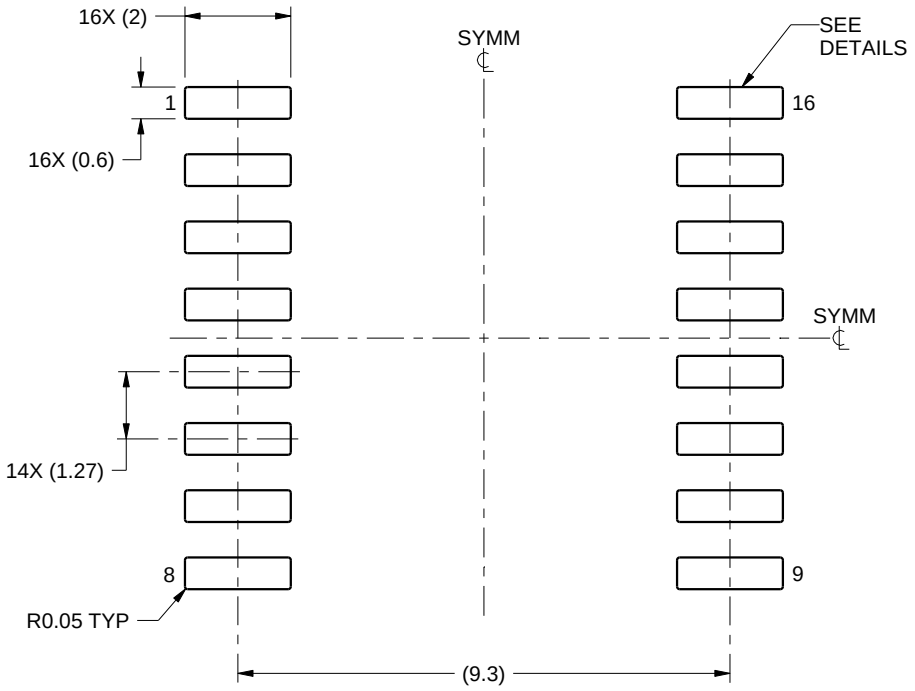
SOIC - 2.65 mm max height

SOIC

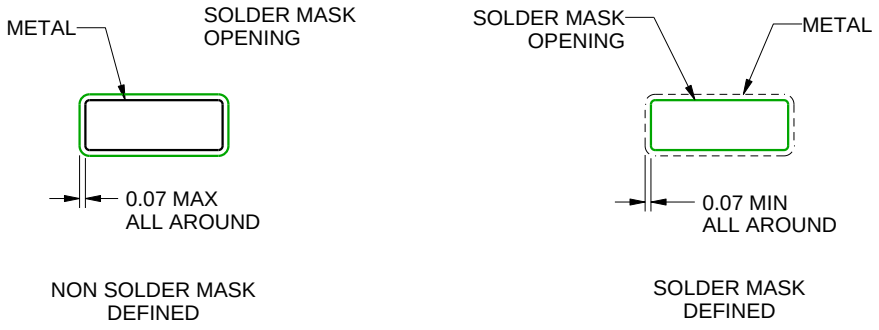


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

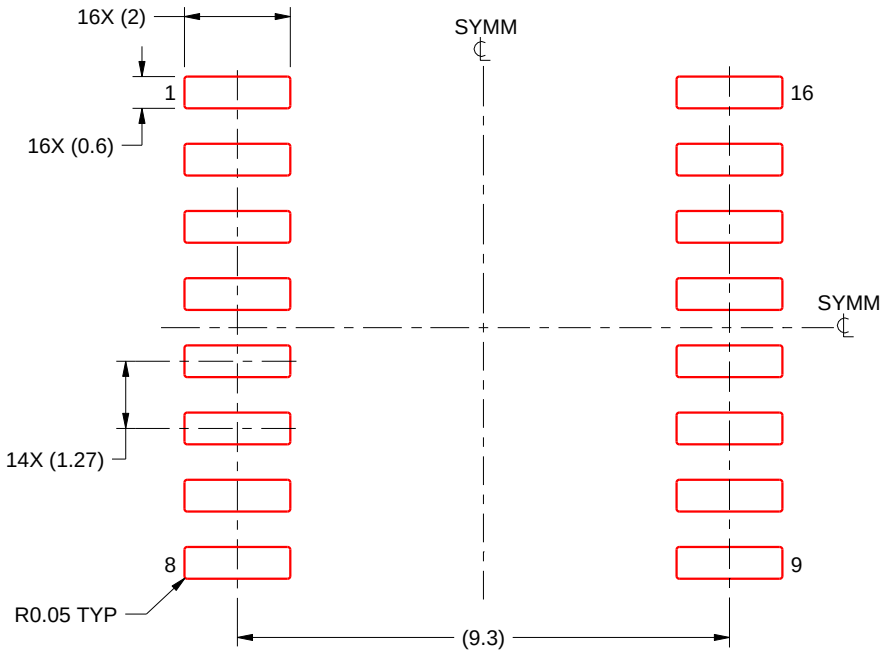


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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