SN65HVD26x 支持 CAN FD（灵活数据速率）和冗余的 Turbo CAN 收发器

1 特性

- 满足 ISO11898-2 标准的要求
- Turbo CAN：
  - 指定用于 2Mbps CAN FD（具有灵活数据速率的 CAN）
  - 短时和对称传播延迟时间以及针对增强型时序裕量的快速环路时间
  - CAN 网络中更快的数据速率
- I/O 电压范围支持 3.3V 和 5V MCU
- 未上电时的理想无源特性
  - 总线和逻辑引脚处于高阻态（无负载）
  - 上电/掉电时总线上无毛刺脉冲
- 保护 特性
  - 人体放电模式 (HBM) 静电放电 (ESD) 保护超过 ±12kV
  - 总线故障保护 -27V 至 40V
  - 电源引脚欠压保护
  - 驱动器显性超时 (TXD DTO)
  - SN65HVD267：接收器主计时功能 (RXD DTO)
  - SN65HVD267：故障输出引脚
  - 热关断保护
- 额定运行温度范围 -40°C 至 125°C

2 应用

- 具有灵活数据速率的 CAN 网络中的 2Mbps 操作
- 高负载 CAN 网络以及低至 10kbps 的网络（使用 TXD DTO）中的 1Mbps 操作
- 工业自动化、控制、传感器和驱动系统
- 楼宇安全和恒温控制自动化
- 电信基站状态和控制
- SN65HVD267：带有冗余和多拓扑 CAN 网络的功能安全
- 诸如 CANopen，DeviceNet，NMEA2000，ARNIC825，ISO11783，，CANaerospace 的 CAN 总线标准

3 （说明

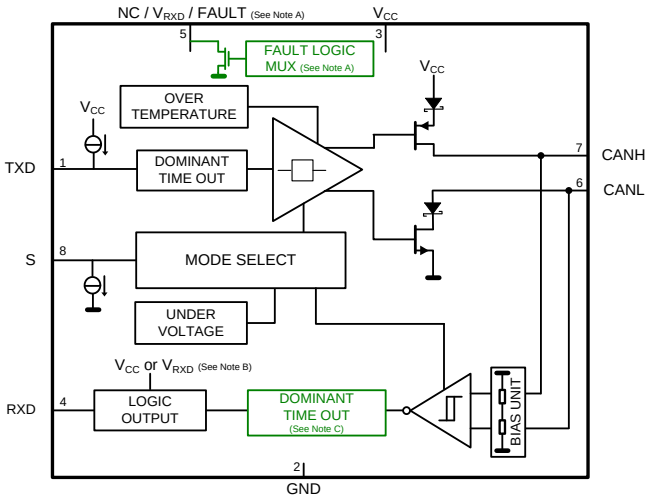
这款 CAN 收发器符合 ISO1189-2 高速 CAN（控制器局域网）物理层标准。其在 CAN FD（具有灵活数据速率的 CAN）网络中的数据速率为 2Mbps（兆比特每秒），在小型 CAN 网络中的数据速率高达 1Mbps 以上，并且在大型高负载网络中具有更高的时序余裕和数据速率。这款器件提供多种保护 功能， 从而提高器件和 CAN 网络的稳定性。SN65HVD267 新增了一些 特性，以便能够轻松设计具有故障指示的冗余和多拓扑网络，从而使 CAN 系统获得更高级别的安全特性。

器件信息 (1)

部件号	封装	封装尺寸
SN65HVD26xD	SOIC (8)	4.90mm x 3.91mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

功能框图



引脚 5 的功能取决于具体器件：SN65HVD265 为 NC，SN65HVD266 为 RXD 输出电平转换器件的 V_{RXD}，SN65HVD267 为故障输出。

RXD 逻辑输出被驱动至电源电压仅为 5V 的器件上的 V_{CC} (SN65HVD265，SN65HVD267) 并被驱动至输出电平位移器件 (SN65HVD266) 上的 V_{RXD}。

RXD（接收器）主状态计时是一个只在 SN65HVD267 上提供的由器件决定的选项。

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2013) to Revision A **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*开关特性*表，*特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建*议部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1
- Changed *Typical Redundant Physical Layer Topology Using the SN65HVD267*, Figure 19 23

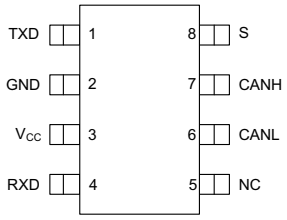
5 Device Comparison Table

PART NUMBER	I/O SUPPLY for RXD	TXD DTO	RXD DTO	FAULT Output	COMMENT
SN65HVD265	No	Yes	No	No	'251 and '1050 functional upgrade with Turbo CAN fast loop times and TXD DTO protection allowing data rates down to 10kbps
SN65HVD266	Yes	Yes	No	No	'251 and '1050 functional upgrade with Turbo CAN fast loop times and TXD DTO protection allowing data rates down to 10kbps. RXD output level shifting via RXD supply input.
SN65HVD267	No	Yes	Yes	Yes	'251 and '1050 functional upgrade with Turbo CAN fast loop times, TXD and RXD DTO protection allowing data rates down to 10kbps and fault output terminal

6 Pin Configurations and Functions

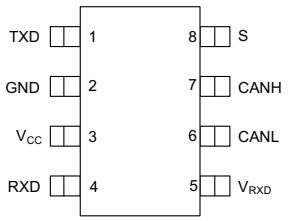
D Package
8-Pin SOIC
Top View

SN65HVD265



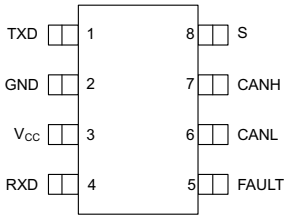
5V Supply

SN65HVD266



5V Supply with RXD Level-Shifting

SN65HVD267



5V Supply and Fault Output

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	TXD	I	CAN transmit data input (LOW for dominant and HIGH for recessive bus states)
2	GND	GND	Ground connection
3	V_{CC}	Supply	Transceiver 5V supply voltage
4	RXD	O	CAN receive data output (LOW for dominant and HIGH for recessive bus states)
5	NC	NC	SN65HVD265: No Connect
	V_{RXD}	Supply	SN65HVD266: RXD output supply voltage
	FAULT	O	SN65HVD267: open drain FAULT output terminal
6	CANL	I/O	Low level CAN bus line
7	CANH	I/O	High level CAN bus line
8	S	I	Mode select: S (silent mode) select terminal (active high)

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted).(1)(2)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.3	6	V
V_{RXD}	RXD Output supply voltage	SN65HVD266	–0.3	6 and $V_{RXD} \le V_{CC} + 0.3$	V
V_{BUS}	CAN Bus I/O voltage (CANH, CANL)		–27	40	V
$V_{(Logic\_Input)}$	Logic input terminal voltage (TXD, S)		–0.3	6	V
$V_{(Logic\_Output)}$	Logic output terminal voltage (RXD)	SN65HVD265, SN65HVD267	–0.3	6	V
		SN65HVD266	–0.3	6 and $V_I \le V_{RXD} + 0.3$	V
$I_{O(RXD)}$	RXD (Receiver) output current			12	mA
$I_{O(FAULT)}$	FAULT output current	SN65HVD267		20	mA
T_J	Operating virtual junction temperature (see *Thermal Information*)		–40	150	°C
T_A	Ambient temperature (see *Thermal Information*)		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

7.2 ESD Ratings: AEC

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2500	V
			CAN bus pins (CANH, CANL)(2)	±12000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)		±750	
		Machine Model		±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Test method based upon JEDEC Standard 22 Test Method A114, CAN bus stressed with respect to GND.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings: IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61400-4-2 according to GIFT-ICT CAN EMC test spec(1)	±8000	V

(1) IEC 61400-4-2 is a system level ESD test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. Different system level configurations may lead to different results.

7.4 Transient Protection

			VALUE	UNIT
ISO7637 Transients according to GIFT - ICT CAN EMC test spec(1)	CAN bus pins (CANH, CANL)	Pulse 1	–100	V
		Pulse 2	+75	V
		Pulse 3a	–150	V
		Pulse 3b	+100	V

(1) ISO7637 is a system level transient test. Results given here are specific to the GIFT-ICT CAN EMC Test specification conditions. Different system level configurations may lead to different results.

7.5 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{RXD}	RXD supply (SN65HVD266 only)		2.8	5.5	V
V_I or V_{IC}	CAN bus terminal voltage (separately or common mode)		–2	7	V
V_{ID}	CAN bus differential voltage		-6	6	V
V_{IH}	Logic HIGH level input (TXD, S)		2	5.5	V
V_{IL}	Logic LOW level input (TXD, S)		0	0.8	V
$I_{OH(DRVR)}$	CAN BUS Driver High level output current		–70		mA
$I_{OL(DRVR)}$	CAN BUS Driver Low level output current			70	mA
$I_{OH(RXD)}$	RXD terminal HIGH level output current		–2		mA
$I_{OL(RXD)}$	RXD terminal LOW level output current			2	mA
$I_{O(FAULT)}$	FAULT terminal LOW level output current	SN65HVD267		2	mA
T_A	Operational free-air temperature (see Thermal Information)		–40	125	°C

7.6 Thermal Information

THERMAL METRIC[1]		SN65HVD265, SN65HVD266, SN65HVD267	UNIT
		D (SOIC)	
		8 PINS	
$R_{\theta JA}$	Junction-to-air thermal resistance, High-K thermal resistance	107.5	°C/W
$R_{\theta JC(top)}$	Junction-to-board thermal resistance	48.9	°C/W
$R_{\theta JB}$	Junction-to-case (top) thermal resistance	56.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.7 Electrical Characteristics

Over recommended operating conditions (unless otherwise noted): T_A = –40°C to 125°C, SN65HVD266 device V_{RXD} = V_{CC}.

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
SUPPLY CHARACTERISTICS							
I_{CC}	5-V Supply current	Normal Mode (Driving Dominant)	See Figure 4, TXD = 0 V, R_L = 50 Ω, C_L = open, R_{CM} = open, S = 0V		60	85	mA
		Normal Mode (Driving Dominant – bus fault)	See Figure 4, TXD = 0 V, S = 0V, CANH = -12V, R_L = open, C_L = open, R_{CM} = open		130	180	
		Normal Mode (Driving Dominant)	See Figure 4, TXD = 0 V, R_L = open (no load), C_L = open, R_{CM} = open, S = 0V		10	20	
		Normal Mode (Recessive)	See Figure 4, TXD = V_{CC}, R_L = 50 Ω, C_L = open, R_{CM} = open, S = 0V		10	20	
		Silent Mode	See Figure 4, TXD = V_{CC}, R_L = 50 Ω,C_L = open, R_{CM} = open, S = V_{CC}		2.5	5	
$I_{(RXD)}$	RXD Supply current (SN65HVD266 only)	All modes	RXD Floating, TXD = 0V			500	µA
UV_{VCC}	Undervoltage detection on V_{CC} for protected mode			3.5		4.45	V
$V_{HYS(UVVCC)}$	Hysteresis voltage on UV_{VCC}				200		mV

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and $V_{(RXD)}$ = 5 V, R_L = 60 Ω.

Electrical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted): T_A = –40°C to 125°C, SN65HVD266 device $V_{RXD} = V_{CC}$.

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
SUPPLY CHARACTERISTICS (CONTINUED)							
$UV_{(RXD)}$	Undervoltage detection on V_{RXD} for protected mode (SN65HVD266 only)			1.3		2.75	V
$V_{HYS(UVRXD)}$	Hysteresis voltage on UV_{RXD} (SN65HVD266 only)				80		mV
S TERMINAL (MODE SELECT INPUT)							
V_{IH}	HIGH-level input voltage			2			V
V_{IL}	LOW-level input voltage					0.8	V
I_{IH}	HIGH-level input leakage current		S = V_{CC} = 5.5 V	7		100	µA
I_{IL}	Low-level input leakage current		S = 0 V, V_{CC} = 5.5 V	–1	0	1	µA
$I_{lkg(OFF)}$	Unpowered leakage current		S = 5.5 V, V_{CC} = 0 V, $V_{(RXD)}$ = 0 V	7	35	100	µA
TXD TERMINAL (CAN TRANSMIT DATA INPUT)							
V_{IH}	HIGH level input voltage			2			V
V_{IL}	LOW level input voltage					0.8	V
I_{IH}	HIGH level input leakage current		TXD = V_{CC} = 5.5 V	–2.5	0	1	µA
I_{IL}	Low level input leakage current		TXD = 0 V, V_{CC} = 5.5 V	–100	-25	–7	µA
$I_{lkg(OFF)}$	Unpowered leakage current		TXD = 5.5 V, V_{CC} = 0 V, $V_{(RXD)}$ = 0 V	–1	0	1	µA
C_I	Input Capacitance				3.5		pF
RXD TERMINAL (CAN RECEIVE DATA OUTPUT)							
V_{OH}	HIGH level output voltage		See Figure 5, I_O = –2 mA. For devices with $V_{(RXD)}$ supply V_{OH} = 0.8 × $V_{(RXD)}$	0.8×V_{CC}			V
V_{OL}	LOW level output voltage		See Figure 5, I_O = 2 mA			0.4	V
$I_{lkg(OFF)}$	Unpowered leakage current		RXD = 5.5 V, V_{CC} = 0 V, $V_{(RXD)}$ = 0 V	–1	0	1	µA
DRIVER ELECTRICAL CHARACTERISTICS							
$V_{O(D)}$	Bus output voltage (dominant	CANH	See Figure 14 and Figure 4, TXD = 0 V, S = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	2.75		4.5	V
		CANL		0.5		2.25	
$V_{O(R)}$	Bus output voltage (recessive)		See Figure 14 and Figure 4, TXD = V_{CC}, $V_{(RXD)}$ = V_{CC}, S = V_{CC} or 0 V (2), R_L = open (no load), R_{CM} = open	2	0.5×V_{CC}	3	V
$V_{OD(D)}$	Differential output voltage (dominant)		See Figure 14 and Figure 4, TXD = 0 V, S = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = 330 Ω, –2 V ≤ V_{CM} ≤ 7 V, 4.75 V≤ V_{CC} ≤ 5.25 V	1.5		3	V
			See Figure 14 and Figure 4, TXD = 0 V, S = 0 V, 45 Ω ≤ R_L ≤ 65 Ω, C_L = open, R_{CM} = 330 Ω, –2 V ≤ V_{CM} ≤ 7 V, 4.5V ≤ V_{CC} ≤ 5.5 V	1.25		3.2	
$V_{OD(R)}$	Differential output voltage (recessive)		See Figure 14 and Figure 4, TXD = V_{CC}, S = 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–0.12		0.012	V
			See Figure 14 and Figure 4, TXD = V_{CC}, S = 0 V, R_L = open (no load), C_L = open, R_{CM} = open, –40°C ≤ T_A ≤ 85°C	–0.100		0.050	
V_{SYM}	Output symmetry (dominant or recessive) (V_{CC} – $V_{O(CANH)}$ – $V_{O(CANL)}$)		See Figure 14 and Figure 4, S at 0 V, R_L = 60 Ω, C_L = open, R_{CM} = open	–0.4		0.4	V

(2) For the bus output voltage (recessive) will be the same if the device is in normal mode with S terminal LOW or if the device is in silent mode with the S terminal is HIGH.

Electrical Characteristics (continued)

Over recommended operating conditions (unless otherwise noted): T_A = –40°C to 125°C, SN65HVD266 device $V_{RXD} = V_{CC}$.

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DRIVER ELECTRICAL CHARACTERISTICS (CONTINUED)						
$I_{OS(SS\_DOM)}$	Short circuit steady-state output current, Dominant	See Figure 14 and Figure 10, V_{CANH} = 0 V, CANL = open, TXD = 0 V	–160			mA
		See Figure 14 and Figure 10, V_{CANL} = 32 V, CANH = open, TXD = 0 V			160	
$I_{OS(SS\_REC)}$	Short circuit steady-state output current, Recessive	See Figure 14 and Figure 10, –20 V ≤ V_{BUS} ≤ 32 V, Where V_{BUS} = CANH = CANL, TXD = V_{CC}, Normal and Silent Modes	–8		8	mA
RECEIVER ELECTRICAL CHARACTERISTICS						
V_{IT+}	Positive-going input threshold voltage, normal mode	See Figure 5, Table 6 and Table 1			900	mV
$V_{IT–}$	Negative-going input threshold voltage, normal mode		500			mV
V_{HYS}	Hysteresis voltage (V_{IT+} - $V_{IT–}$)			125		mV
$I_{lkg(IOFF)}$	Power-off (unpowered) bus input leakage current	C_{ANH} = C_{ANL} = 5 V, V_{CC} = 0 V, $V_{(RXD)}$ = 0 V			5.5	µA
C_I	Input capacitance to ground (CANH or CANL)	TXD = V_{CC}, $V_{(RXD)}$ = V_{CC}, V_I = 0.4 sin (4E6 π t) + 2.5 V		25		pF
C_{ID}	Differential input capacitance	TXD = V_{CC}, $V_{(RXD)}$ = V_{CC}, V_I = 0.4 sin (4E6 π t)		10		pF
R_{ID}	Differential input resistance	TXD = V_{CC} = $V_{(RXD)}$ = 5 V, S = 0 V	30		80	kΩ
R_{IN}	Input resistance (CANH or CANL)		15		40	kΩ
$R_{IN(M)}$	Input resistance matching: [1 – $R_{IN(CANH)}$ / $R_{IN(CANL)}$] × 100%	$V_{(CANH)}$ = $V_{(CANL)}$, –40°C ≤ T_A ≤ 85°C	–3%		3%	
FAULT terminal (Fault Output), SN65HVD267 only						
I_{CH}	Output current high level	FAULT = V_{CC}, See Figure 3	–10		10	µA
I_{CL}	Output current low level	FAULT = 0.4 V, See Figure 3	5	12		mA
POWER DISSIPATION						
P_D	Average power dissipation	V_{CC} = 5 V, V_{RXD} = 5 V, T_J = 27°C, R_L = 60 Ω, S at 0 V, Input to TXD at 250 kHz, 25% duty cycle square wave, C_{L_RXD} = 15 pF. Typical CAN operating conditions at 500kbps with 25% transmission (dominant) rate.		115		mW
		V_{CC} = 5.5 V, V_{RXD} = 5.5 V, T_J = 150°C, R_L = 50 Ω, S at 0 V, Input to TXD at 500 kHz, 50% duty cycle square wave, C_{L_RXD} = 15 pF. Typical high load CAN operating conditions at 1mbps with 50% transmission (dominant) rate and loaded network.		268		
THERMAL SHUTDOWN						
	Thermal shutdown temperature			170		°C
	Thermal shutdown hysteresis			5		°C

7.8 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
DEVICE SWITCHING CHARACTERISTICS						
$t_{PROP(LOOP1)}$	Total loop delay, driver input (TXD) to receiver output (RXD), recessive to dominant	See Figure 7, S = 0 V, R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF			150	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input (TXD) to receiver output (RXD), dominant to recessive				150	
$t_{REC(2Mbps)}$	Loop Delay Symmetry for 2Mbps CAN with Flexible Data Rate.(2)	See Figure 8 , S = 0 V, R_L = 60Ω, C_L = 100pF, $C_{L(RXD)}$ = 15pF, t_{BIT} = 500ns	400		550	
I_{MODE}	Mode change time, from Normal to Silent or from Silent to Normal	See Figure 6			20	µS
DRIVER SWITCHING CHARACTERISTICS						
t_{pHR}	Propagation delay time, HIGH TXD to Driver Recessive	See Figure 4, S = 0 V, R_L = 60 Ω, C_L = 100 pF, R_{CM} = open		50	70	ns
t_{pLD}	Propagation delay time, LOW TXD to Driver Dominant			40	70	
$t_{sk(p)}$	Pulse skew ($\lvert t_{pHR} - t_{pLD} \rvert$)			10		
t_R	Differential output signal rise time			10	30	
t_F	Differential output signal fall time			17	30	
$t_{R(10k)}$	Differential output signal rise time, R_L = 10 kΩ	See Figure 4, S = 0 V, R_L = 10 kΩ, C_L = 10 pF, R_{CM} = open			35	ns
$t_{F(10k)}$	Differential output signal fall time, R_L = 10 kΩ				100	
t_{TXD_DTO}	Dominant timeout(3)	See Figure 9, R_L = 60 Ω, C_L = open	1175		3700	µs
RECEIVER SWITCHING CHARACTERISTICS						
t_{pRH}	Propagation delay time, recessive input to high output	See Figure 5, $C_{L(RXD)}$ = 15 pF		70	90	ns
t_{pDL}	Propagation delay time, dominant input to low output			70	90	ns
t_R	Output signal rise time			4	20	ns
t_F	Output signal fall time			4	20	ns
$t_{(RXD\_DTO)}$ (4)	Receiver dominant time out (SN65HVD267 only) See Figure 2, $C_{L(RXD)}$ = 15 pF		1380		4200	µs

(1) All typical values are at 25°C and supply voltages of V_{CC} = 5 V and $V_{(RXD)}$ = 5 V, R_L = 60 Ω.
(2) Loop delay symmetry for CAN with flexible data rate or "improved CAN" for data rates in excess of 1Mbps. Specified in accordance with working draft 2Mbps specification from physical layer task force within CAN in Automation.
(3) The TXD dominant timeout ($t_{(TXD\_DTO)}$) disables the driver of the transceiver once the TXD has been dominant longer than $t_{(TXD\_DTO)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after TXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(TXD\_DTO)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / $t_{(TXD\_DTO)}$ = 11 bits / 1175 µs = 9.4 kbps.
(4) The RXD timeout ($t_{(RXD\_DTO)}$) disables the driver of the transceiver once the RXD has been dominant longer than $t_{(RXD\_DTO)}$, which releases the bus lines to recessive, preventing a local failure from locking the bus dominant. The driver may only transmit dominant again after RXD has been returned HIGH (recessive). While this protects the bus from local faults, locking the bus dominant, it limits the minimum data rate possible. The CAN protocol allows a maximum of eleven successive dominant bits (on RXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the $t_{(RXD\_DTO)}$ minimum, limits the minimum bit rate. The minimum bit rate may be calculated by: Minimum Bit Rate = 11 / $t_{(RXD\_DTO)}$ = 11 bits / 1380 µs = 8 kbps.

7.9 Typical Characteristics

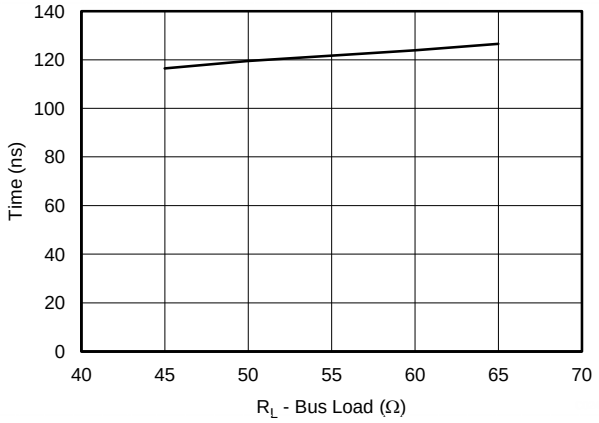


Figure 1. Typical Loop Delay With Respect To Bus Load

8 Parameter Measurement Information

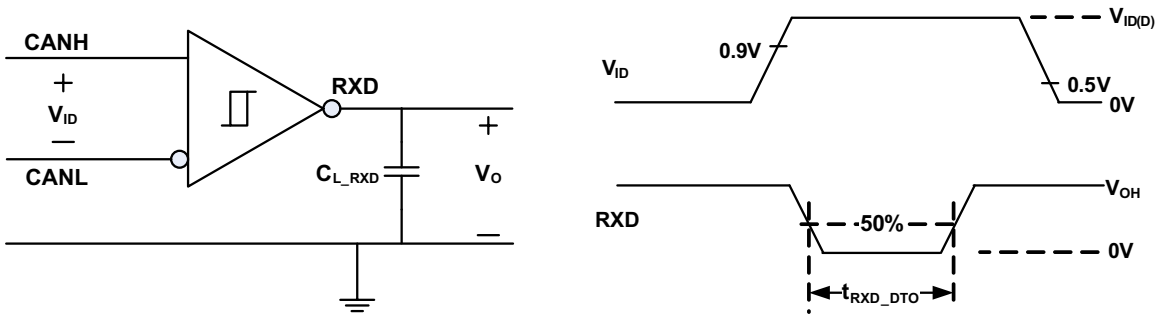


Figure 2. RXD Dominant Timeout Test Circuit and Measurement

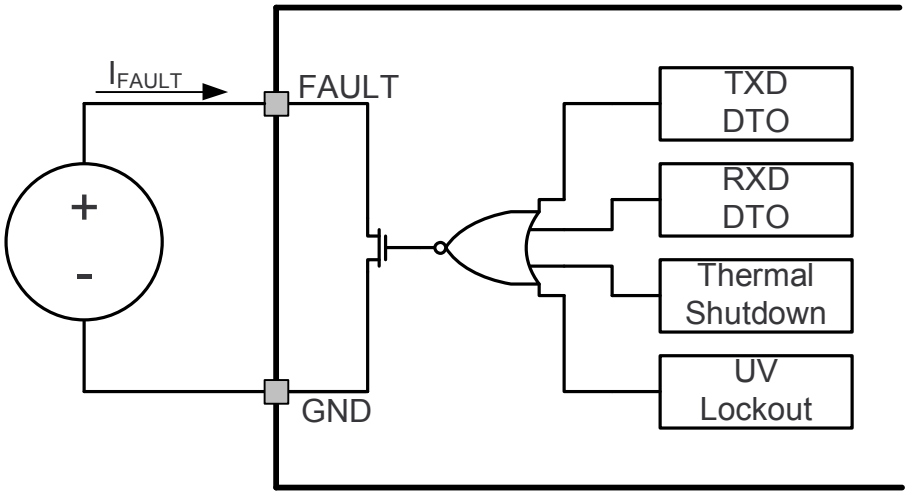


Figure 3. FAULT Test and Measurement

Parameter Measurement Information (continued)

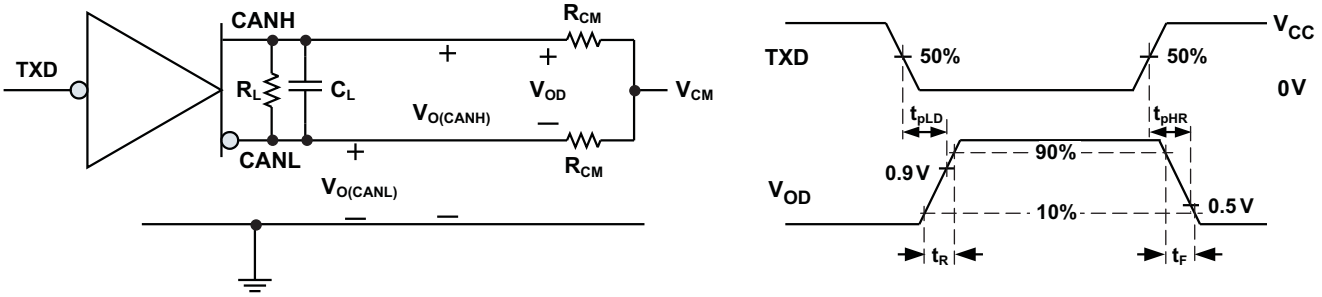


Figure 4. Driver Test Circuit and Measurement

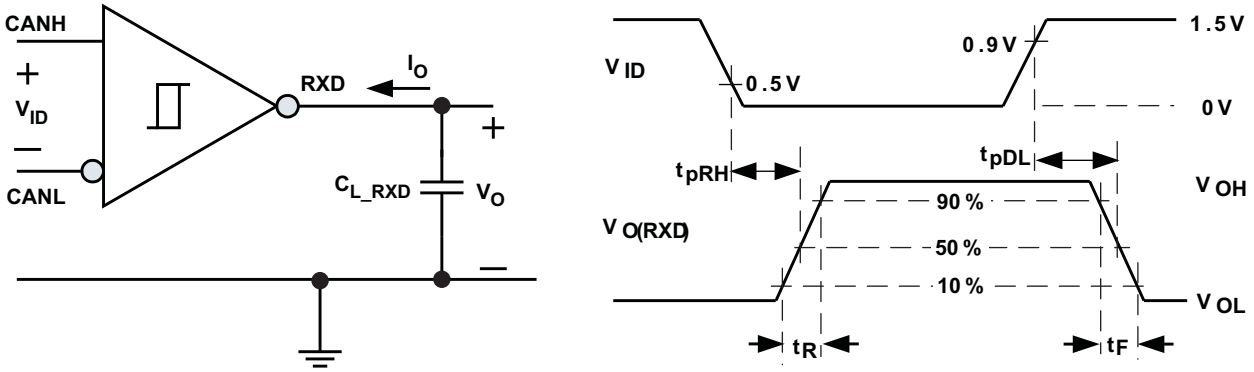


Figure 5. Receiver Test Circuit and Measurement

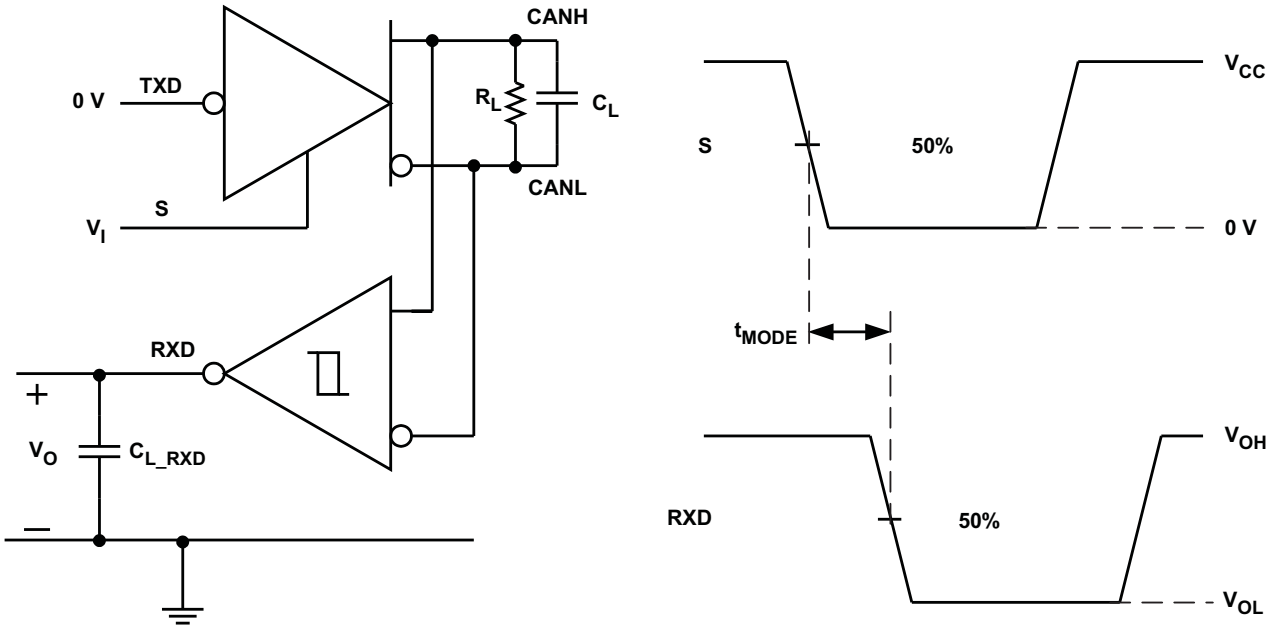


Figure 6. t_{MODE} Test Circuit and Measurement

Parameter Measurement Information (continued)

Table 1. Receiver Differential Input Voltage Threshold Test

INPUT			OUTPUT	
V_{CANH}	V_{CANL}	$\lvert V_{ID}\rvert$	R_{XD}	
-1.1V	-2.0 V	900 mV	L	V_{OL}
7.0 V	6.1 V	900 mV	L	
-1.5 V	-2.0 V	500 mV	H	V_{OH}
7.0 V	6.5 V	500 mV	H	
Open	Open	X	H	

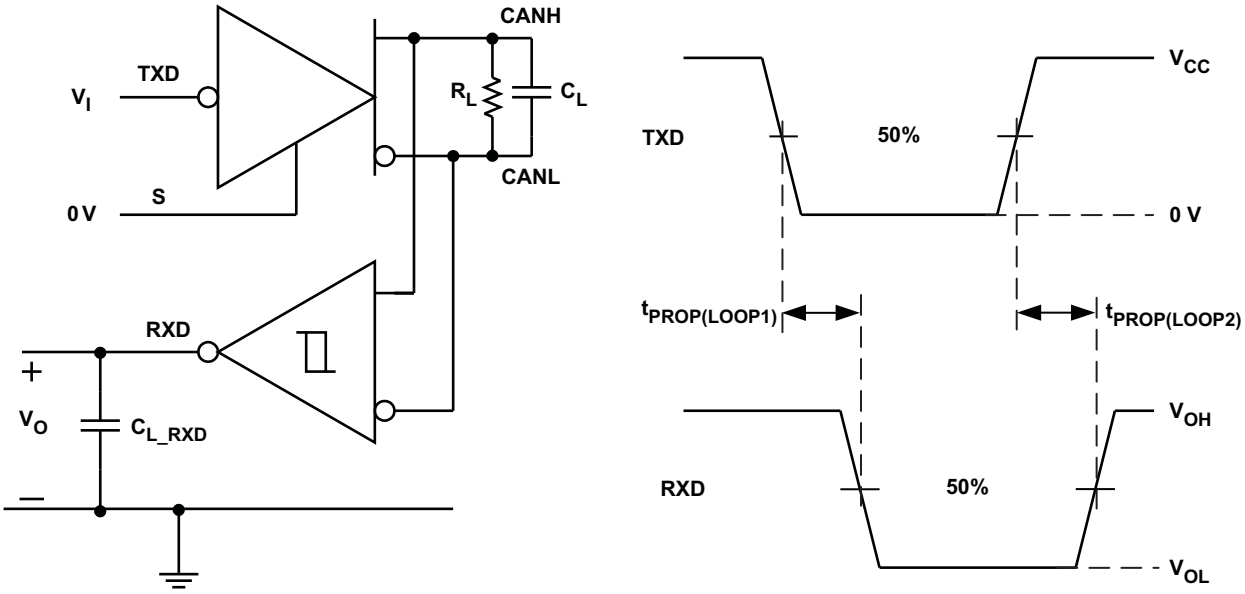
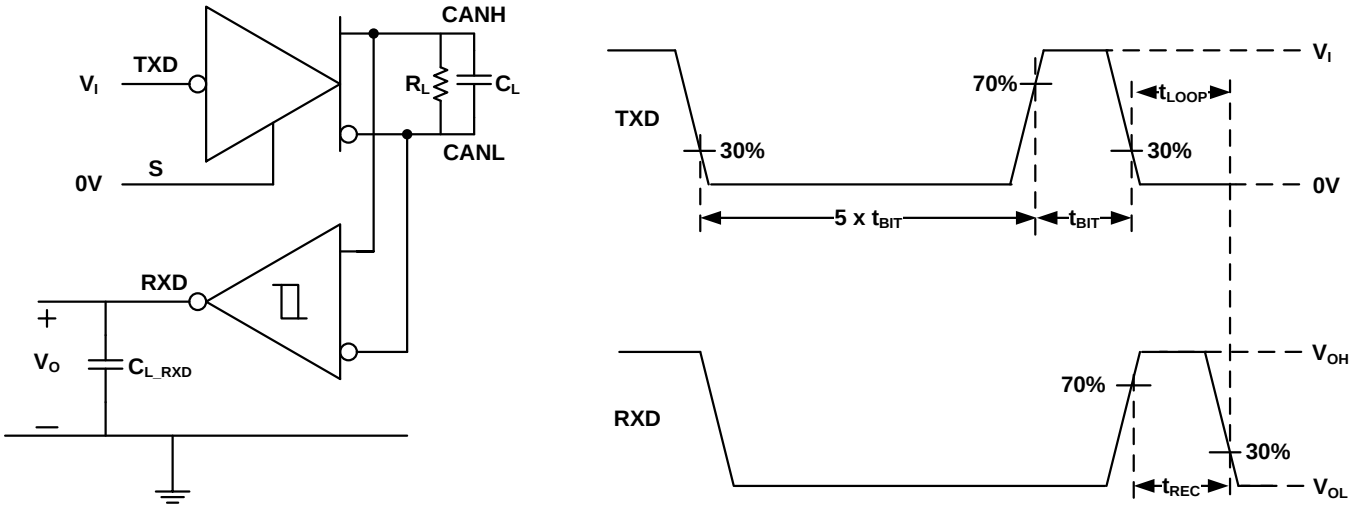


Figure 7. $T_{PROP(LOOP)}$ Test Circuit and Measurement



Note: t_{LOOP} is equivalent to $t_{PROP(LOOP)}$ from CAN timing.

Figure 8. Loop Delay Symmetry Test Circuit and Measurement

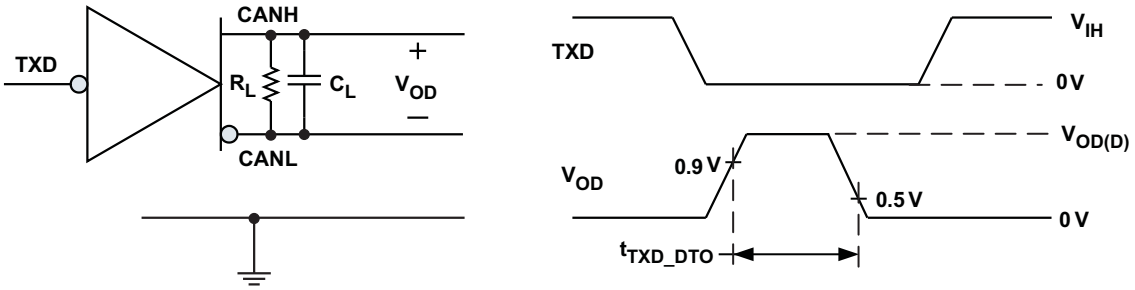


Figure 9. TXD Dominant Timeout Test Circuit and Measurement

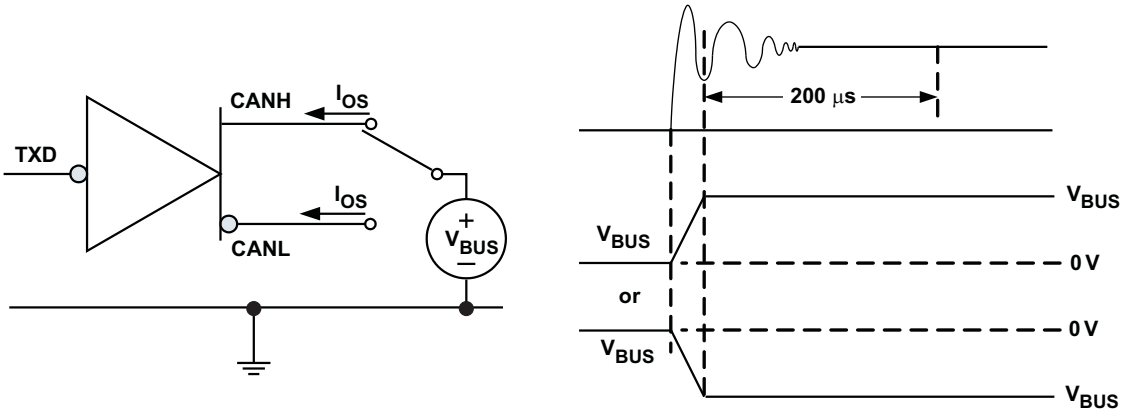


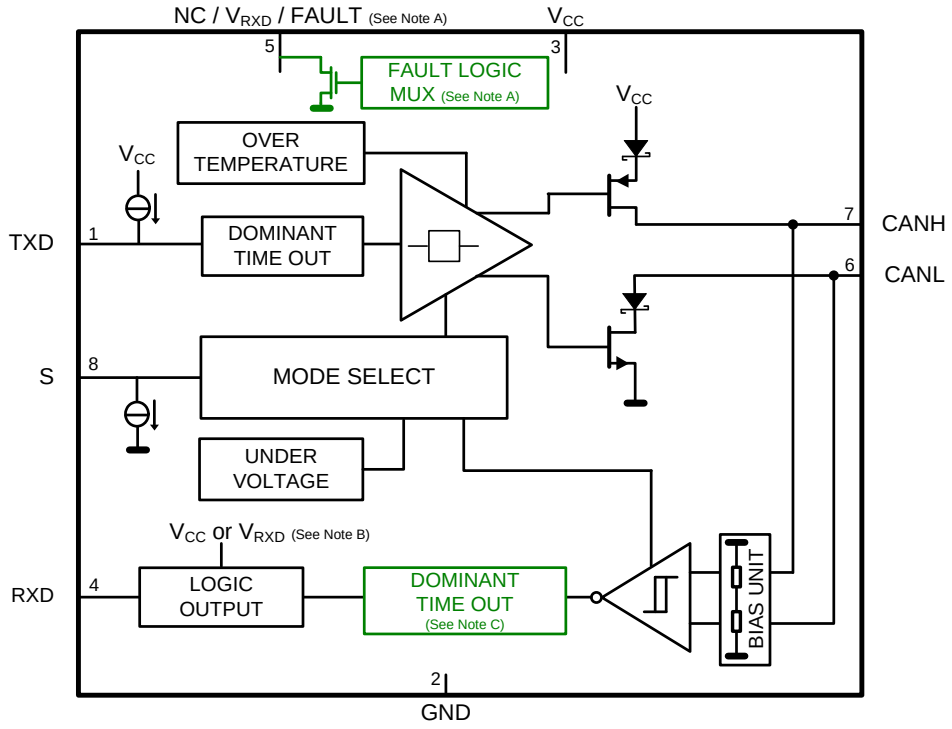
Figure 10. Driver Short Circuit Current Test and Measurement

9 Detailed Description

9.1 Overview

This CAN transceiver meets the ISO1189-2 High Speed CAN (Controller Area Network) physical layer standard. It is designed for data rates in excess of 2 Mpbs (megabits per second) for CAN FD (CAN with flexible data rate), greater than 1 Mbps for CAN in short networks, and enhanced timing margin and higher data rates in long and highly-loaded networks. The device provides many protection features to enhance device and CAN-network robustness. The SN65HVD267 adds additional features, allowing easy design of redundant and multi-topology networks with fault indication for higher levels of safety in the CAN system.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 TXD Dominant Timeout (DTO)

During normal mode (the only mode where the CAN driver is active), the TXD DTO circuit prevents the transceiver from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period t_{TXD_DTO}. The DTO circuit timer starts on a falling edge on TXD. The DTO circuit disables the CAN bus driver if no rising edge is seen before the timeout period expires. This frees the bus for communication between other nodes on the network. The CAN driver is re-activated when a recessive signal is seen on TXD terminal, thus clearing the TXD DTO condition. The receiver and RXD terminal still reflect the CAN bus, and the bus terminals are biased to recessive level during a TXD dominant timeout.

NOTE

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{TXD_DTO} minimum, limits the minimum data rate. Calculate the minimum transmitted data rate by: Minimum Data Rate = 11 / t_{TXD_DTO}.

Feature Description (continued)

9.3.1.1 RXD Dominant Timeout (SN65HVD267)

The SN65HVD267 device has a RXD dominant timeout (RXD DTO) circuit that prevents a bus stuck dominant fault from permanently driving the RXD output dominant (low) when the bus is held dominant longer than the timeout period t_{RXD_DTO}. The RXD DTO timer starts on a falling edge on RXD (bus going dominant). If no rising edge (bus returning recessive) is seen before the timeout constant of the circuit expires (t_{RXD_DTO}), the RXD terminal returns high (recessive). The RXD output is re-activated to mirror the bus receiver output when a recessive signal is seen on the bus, clearing the RXD dominant timeout. The CAN bus terminals are biased to the recessive level during a RXD DTO.

NOTE

APPLICATION NOTE: The minimum dominant RXD time allowed by the RXD DTO limits the minimum possible received data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits for the worst case transmission, where five successive dominant bits are followed immediately by an error frame. This, along with the t_{RXD_DTO} minimum, limits the minimum data rate. The minimum received data rate may be calculated by: Minimum Data Rate = 11 / t_{RXD_DTO}.

9.3.1.2 Thermal Shutdown

If the junction temperature of the device exceeds the thermal shut down threshold the device turns off the CAN driver circuits thus blocking the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature drops below the thermal shutdown temperature of the device.

NOTE

During thermal shutdown the CAN bus drivers turn off; thus no transmission is possible from TXD to the bus. The CAN bus terminals are biased to recessive level during a thermal shutdown, and the receiver to RXD path remains operational.

9.3.1.3 Undervoltage Lockout

The supply terminals have undervoltage detection that places the device in protected mode. This protects the bus during an undervoltage event on either the V_{CC} or V_{RXD} supply terminals.

Table 2. Undervoltage Lockout 5-V Only Devices (SN65HVD265 and SN65HVD267)

V_{CC}	DEVICE STATE	BUS OUTPUT	RXD
GOOD	Normal	Per Device State and TXD	Mirrors Bus
BAD	Protected	High Impedance	High Impedance (3-state)

Table 3. Undervoltage Lockout 5-V and V_{RXD} Device (SN65HVD266)

V_{CC}	V_{RXD}	DEVICE STATE	BUS OUTPUT	RXD
GOOD	GOOD	Normal	Per Device State and TXD	Mirrors Bus
BAD	GOOD	Protected	High Impedance	High (Recessive)
GOOD	BAD	Protected	Recessive	High Impedance (3-state)
BAD	BAD	Protected	High Impedance	High Impedance (3-state)

NOTE

After an undervoltage condition is cleared and the supplies have returned to valid levels, the device typically resumes normal operation in 300 µs.

9.3.1.4 Fault Terminal (SN65HVD267)

If one or more of the faults (TXD-Dominant Timeout, RXD dominant Timeout, Thermal Shutdown or Undervoltage Lockout) occurs, the FAULT terminal (open-drain) turns off, resulting in a high level when externally pulled up to V_{CC} or IO supply.

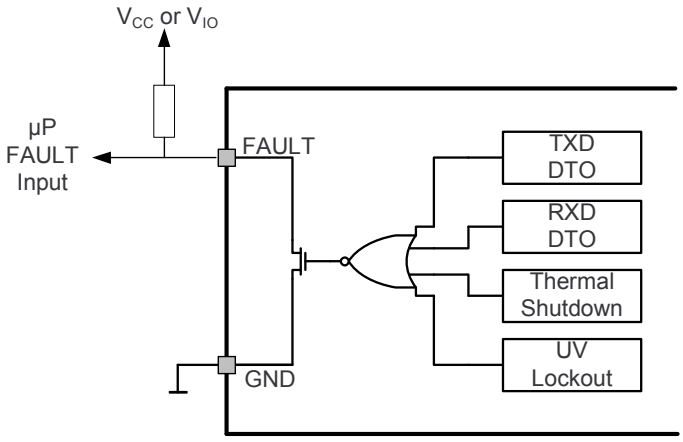


Figure 11. FAULT Terminal Function Diagram and Application

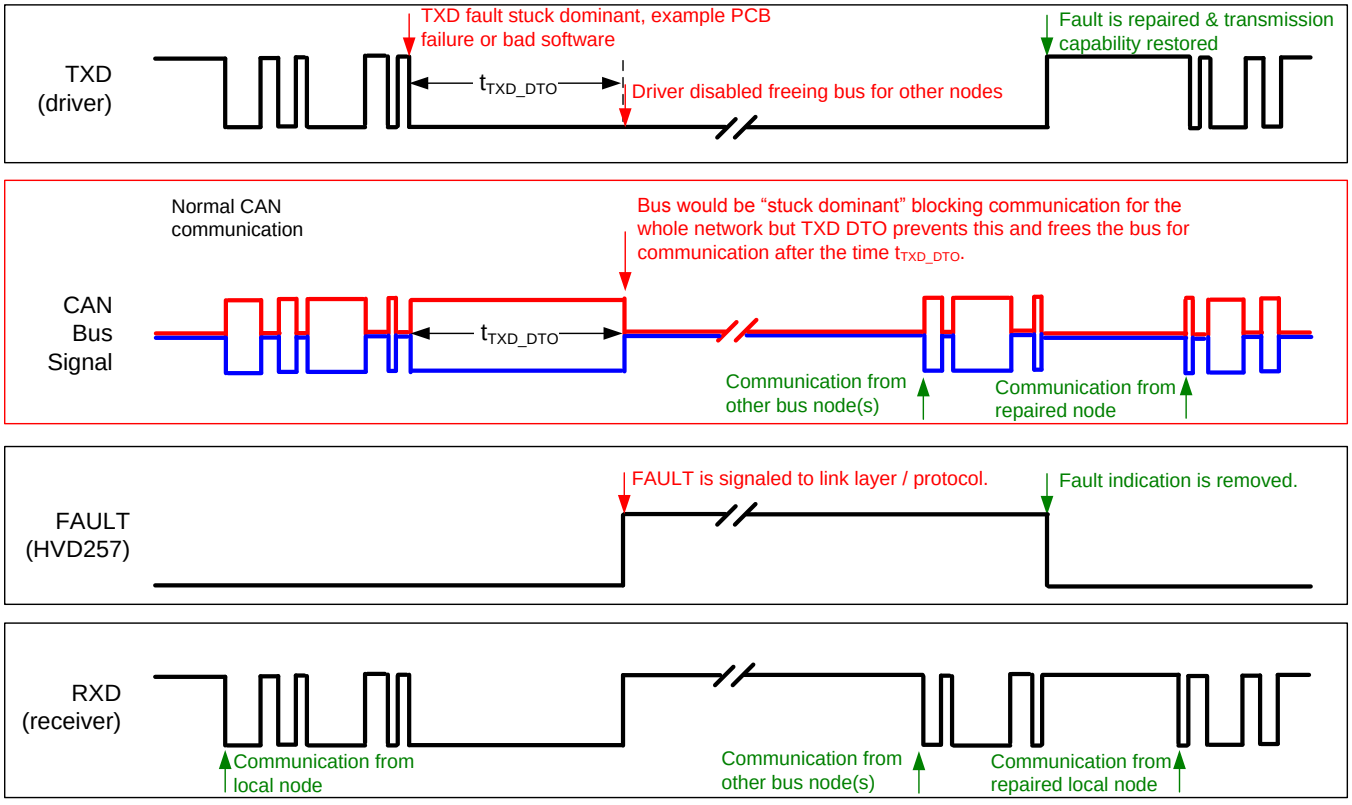


Figure 12. Example Timing Diagram for TXD DTO and FAULT Terminal

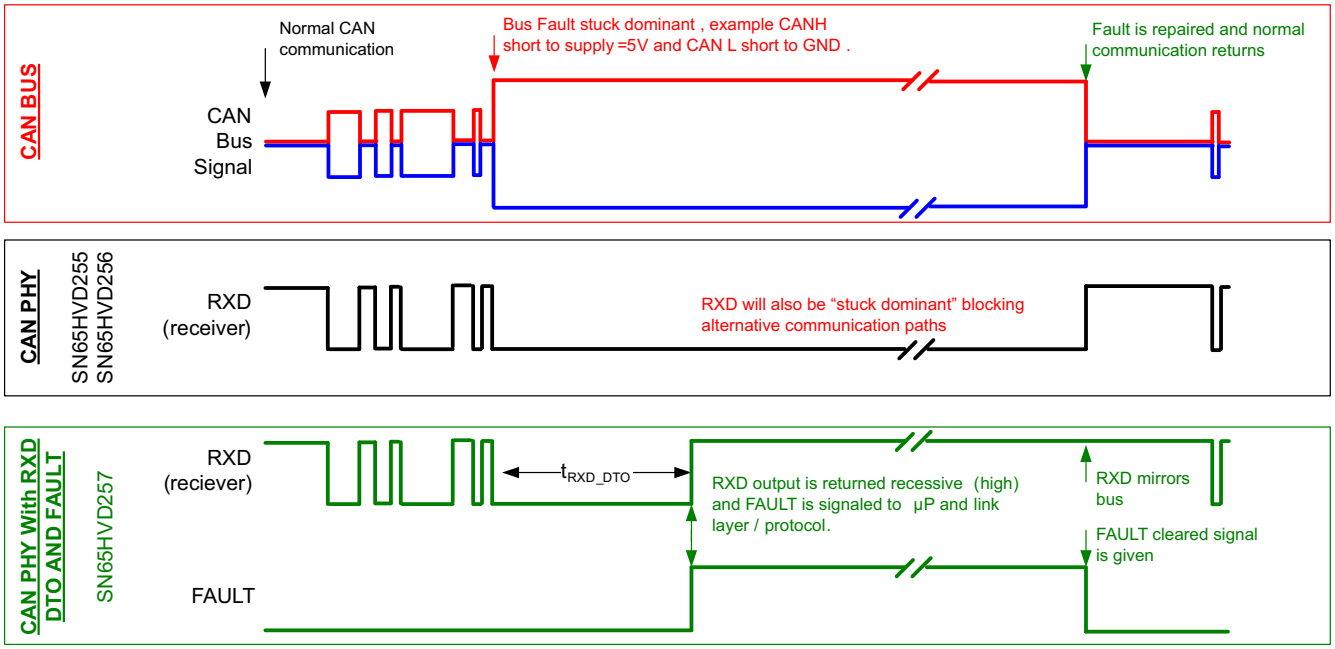


Figure 13. Example Timing Diagram for Devices With and Without RXD DTO and FAULT Terminal

9.3.1.5 Unpowered Device

The device is designed to be an 'ideal passive' or 'no load' to the CAN bus if it is unpowered. The bus terminals (CANH, CANL) have extremely low leakage currents when the device is unpowered so they will not load down the bus. This is critical if some nodes of the network will be unpowered while the rest of the of network remains in operation. The logic terminals also have extremely low leakage currents when the device is unpowered to avoid loading down other circuits that may remain powered.

9.3.1.6 Floating Terminals

The device has internal pull ups and pull downs on critical terminals to place the device into known states if the terminals float. The TXD terminal is pulled up to V_{CC} to force a recessive input level if the terminal floats. The S terminal is pulled down to GND to force the device into normal mode if the terminal floats.

9.3.1.7 CAN Bus Short Circuit Current Limiting

The device has several protection features that limit the short circuit current when a CAN bus line is shorted. These include driver current limiting (dominant and recessive). The device has TXD dominant state time out to prevent permanent higher short circuit current of the dominant state during a system fault. During CAN communication the bus switches between dominant and recessive states with the data and control fields bits, thus the short circuit current may be viewed either as the instantaneous current during each bus state, or as a DC average current. For system current (power supply) and power considerations in the termination resistors and common-mode choke ratings, use the average short circuit current. Determine the ratio of dominant and recessive bits by the data in the CAN frame plus the following factors of the protocol and PHY that force either recessive or dominant at certain times:

- Control fields with set bits
- Bit stuffing
- Interframe space
- TXD dominant time out (fault case limiting)

These ensure a minimum recessive amount of time on the bus even if the data field contains a high percentage of dominant bits.

NOTE

The short circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short circuit currents. The average short circuit current may be calculated with the following formula:

$$I_{OS(AVG)} = \%Transmit \times [(\%REC\_Bits \times I_{OS(SS)\_REC}) + (\%DOM\_Bits \times I_{OS(SS)\_DOM})] + [\%Receive \times I_{OS(SS)\_REC}] \quad (1)$$

Where:

- $I_{OS(AVG)}$ is the average short circuit current
- %Transmit is the percentage the node is transmitting CAN messages
- %Receive is the percentage the node is receiving CAN messages
- %REC_Bits is the percentage of recessive bits in the transmitted CAN messages
- %DOM_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)\_REC}$ is the recessive steady state short circuit current
- $I_{OS(SS)\_DOM}$ is the dominant steady state short circuit current

NOTE

Consider the short circuit current and possible fault cases of the network when sizing the power ratings of the termination resistance and other network components.

9.4 Device Functional Modes

The device has two main operating modes: normal mode and silent mode. Operating mode selection is made via the S input terminal.

Table 4. Operating Modes

S Terminal	MODE	DRIVER	RECEIVER	RXD Terminal
LOW	Normal Mode	Enabled (ON)	Enabled (ON)	Mirrors Bus State(1)
HIGH	Silent Mode	Disabled (OFF)	Enabled (ON)	Mirrors Bus State

(1) Mirrors bus state: low if CAN bus is dominant, high if CAN bus is recessive.

9.4.1 Can Bus States

The CAN bus has two states during powered operation of the device; *dominant* and *recessive*. A dominant bus state is when the bus is driven differentially, corresponding to a logic low on the TXD and RXD terminal. A recessive bus state is when the bus is biased to V_{CC} / 2 via the high-resistance internal input resistors R_{IN} of the receiver, corresponding to a logic high on the TXD and RXD terminals. See Figure 14 and Figure 15.

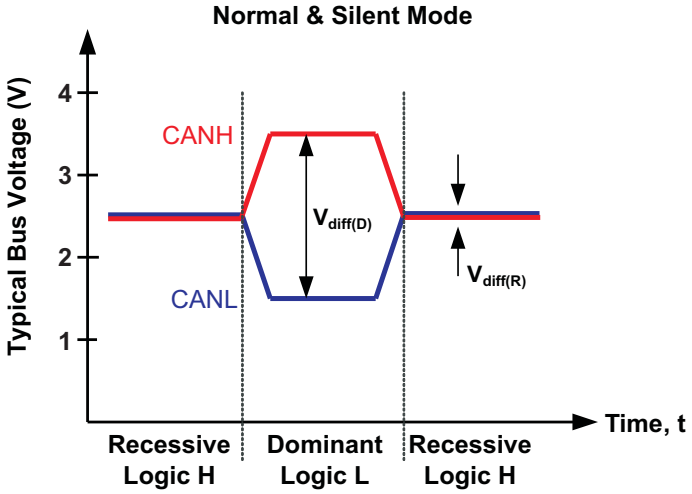


Figure 14. Bus States (Physical Bit Representation)

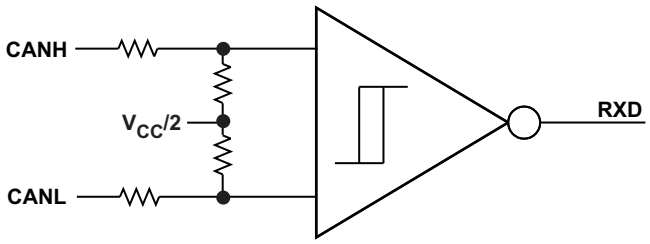


Figure 15. Bias Unit (Recessive Common Mode Bias) and Receiver

9.4.2 Normal Mode

Select the *normal mode* of device operation by setting S low. The CAN driver and receiver are fully operational and CAN communication is bi-directional. The driver is translating a digital input on TXD to a differential output on CANH and CANL. The receiver is translating the differential signal from CANH and CANL to a digital output on RXD.

9.4.3 Silent Mode

Activate *silent mode* (receive only) by setting S high. The CAN driver is turned off while the receiver remains active and RXD outputs the received bus state.

NOTE

Silent mode may be used to implement *babbling idiot* protection, to ensure that the driver does not disrupt the network during a local fault. Silent mode may also be used in redundant systems to select or de-select the redundant transceiver (driver) when needed.

9.4.4 Driver and Receiver Function Tables

Table 5. Driver Function Table

DEVICE	INPUTS		OUTPUTS		DRIVEN BUS STATE
	S(1) (2)	TXD(1) (3)	CANH(1)	CANL(1)	
All Devices	L or Open	L	H	L	Dominant
		H or Open	Z	Z	Recessive
	H	X	Z	Z	Recessive

(1) H = high level, L = low level, X= irrelevant, Z = common mode (recessive) bias to V_{CC} / 2. See Figure 14 and Figure 15 for bus state and common mode bias information.
(2) Devices have an internal pull down to GND on S terminal. If S terminal is open the terminal will be pulled low and the device will be in normal mode.
(3) Devices have an internal pull up to V_{CC} on TXD terminal. If the TXD terminal is open the terminal will be pulled high and the transmitter will remain in recessive (non-driven) state.

Table 6. Receiver Function Table

DEVICE MODE	CAN DIFFERENTIAL INPUTS $V_{ID} = V_{CANH} - V_{CANL}$	BUS STATE	RXD TERMINAL(1)
Normal or Silent	$V_{ID} \geq 0.9$ V	Dominant	L(2)
	0.5 V < V_{ID} < 0.9 V	?	?
	$V_{ID} \leq 0.5$ V	Recessive	H
	Open ($V_{ID} \approx 0$ V)	Open	H

(1) H = high level, L = low level, ? = indeterminate.
(2) RXD output remains dominant (low) as long as the bus is dominant. On SN65HVD267 device with RXD dominant timeout, once the bus has been dominant longer than the dominant timeout, t_{RXD_DTO}, the RXD terminal will return recessive (high). See RXD Dominant Timeout (SN65HVD267) for a description of behavior during receiving a bus stuck dominant condition.

9.4.5 Digital Inputs and Outputs

9.4.5.1 5-V V_{CC} Only Devices (SN65HVD265 and SN65HVD267)

The 5-V V_{CC} device is supplied by a single 5-V rail. The digital inputs are 5 V and 3.3 V compatible. This device has a 5-V (V_{CC}) level RXD output. TXD is internally pulled up to V_{CC} and S is internally pulled down to GND.

NOTE

TXD is internally pulled up to V_{CC} and the S terminal is internally pulled down to GND. However, the internal bias may only put the device into a known state if the terminals float. The internal bias may be inadequate for system-level biasing. TXD pullup strength and CAN bit timing require special consideration when the SN65HVD26x devices are used with an open-drain TXD output on the CAN controller. An adequate external pullup resistor must be used to ensure that the CAN controller output of the μP maintains adequate bit timing input to the SN65HVD26x.

9.4.5.2 5-V V_{CC} with V_{RXD} RXD Output Supply Devices (SN65HVD266)

This device is a 5-V V_{CC} CAN transceiver with a separate supply for the RXD output, V_{RXD}. The digital inputs are 5 V and 3.3 V compatible. These devices have a V_{RXD}-level RXD output. TXD remains weakly pulled up to V_{CC}.

NOTE

On device versions with a V_{RXD} supply that shifts the RXD output level, the input terminals of the device remain the same. TXD remains weakly pulled up to V_{CC} internally. Thus, a small I_{IH} current flows if the TXD input is used below V_{CC} levels.

9.4.5.3 5-V V_{CC} with FAULT Open-Drain Output Device (SN65HVD267)

This device has a FAULT output terminal (open-drain). FAULT must be pulled up to V_{CC} or I/O supply level via an external resistor.

NOTE

Because the FAULT output terminal is open-drain, it actively pulls down when there is no fault, and becomes high-impedance when a fault condition is detected. An external pullup resistor to the V_{CC} or I/O supply of the system must be used to pull the terminal high to indicate a fault to the host microprocessor. The open-drain architecture makes the fault terminal compatible with 3.3 V and 5 V I/O-level systems. The pullup current, selected by the pullup resistance value, should be as low as possible while achieving the desired voltage level output in the system with margin against noise.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

These CAN transceivers are typically used in applications with a host microprocessor or FPGA that includes the link layer portion of the CAN protocol. Below are typical application configurations for both 5 V and 3.3 V microprocessor applications. The bus termination is shown for illustrative purposes.

10.2 Typical Application

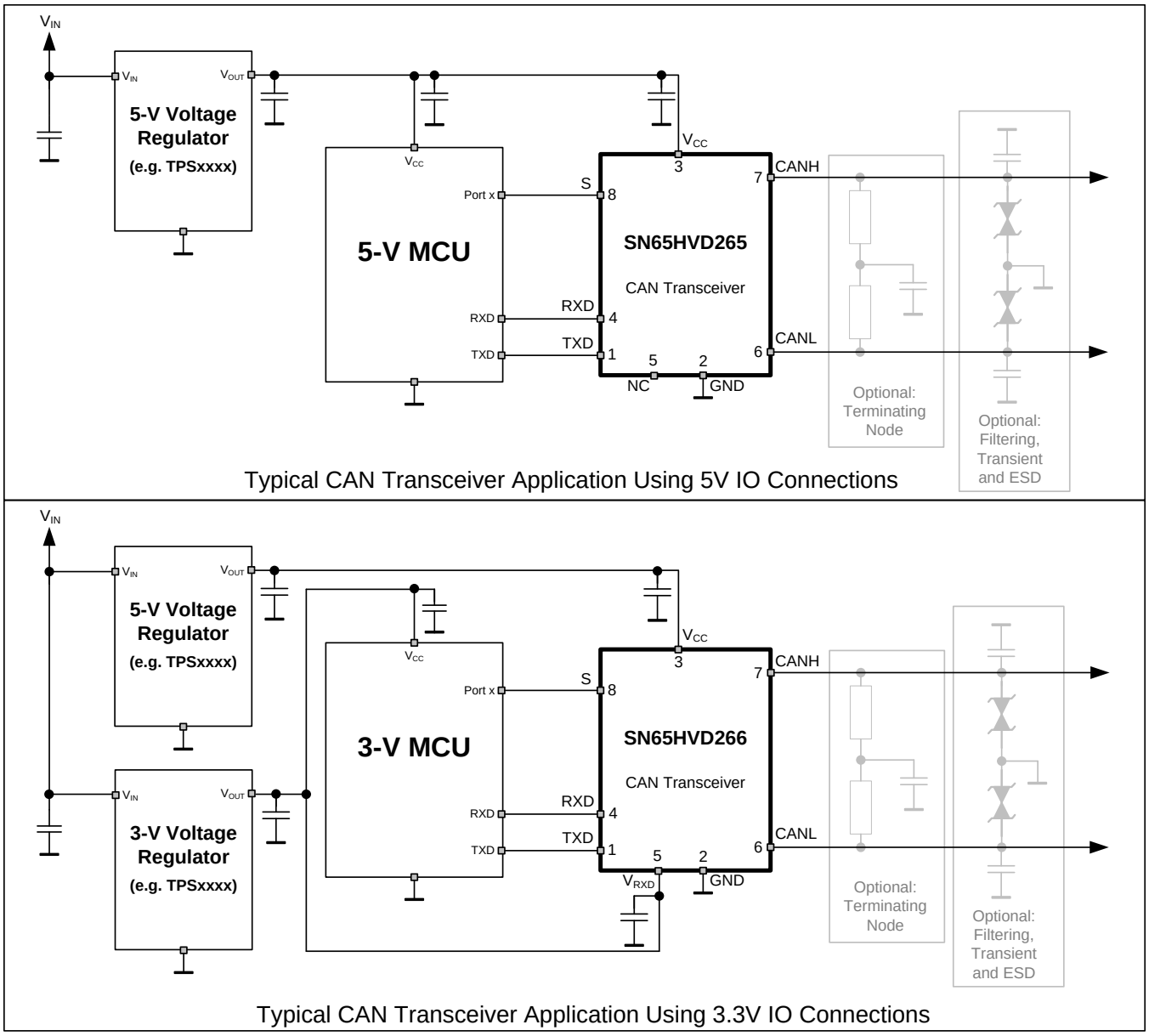


Figure 16. Typical 5-V Application

Typical Application (continued)

10.2.1 Design Requirements

10.2.1.1 Bus Loading, Length and Number of Nodes

The ISO11898 Standard specifies a maximum bus length of 40m and maximum stub length of 0.3m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A large number of nodes requires a transceiver with high input impedance such as the SN65HVD26x family.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO11898. They have made system level trade offs for data rate, cable length, and parasitic loading of the bus. Examples of some of these specifications are ARINC825, CANopen, DeviceNet and NMEA2000.

A CAN network design is a series of tradeoffs, but these devices operate over wide common-mode range. In ISO11898-2 the driver differential output is specified with a 60Ω load (the two 120Ω termination resistors in parallel) and the differential output must be greater than 1.5V. The SN65HVD26x family is specified to meet the 1.5V requirement with a 45Ω load incorporating the worst case including parallel transceivers. The differential input resistance of the SN65HVD26x is a minimum of 30KΩ. If 167 SN65HVD26x family transceivers are in parallel on a bus, this is equivalent to a 180Ω differential load worst case. That transceiver load of 180Ω in parallel with the 60Ω gives a total 45Ω. Therefore, the SN65HVD26x family theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2V minimum differential input at each node. However for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO11898 standard of 40m by careful system design and datarate tradeoffs. For example CANopen network design guidelines allow the network to be up to 1km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO11898 CAN standard. In using this flexibility comes the responsibility of good network design and balancing these tradeoffs.

10.2.2 Detailed Design Procedures

10.2.2.1 CAN Termination

The ISO11898 standard specifies the interconnect to be a twisted pair cable (shielded or unshielded) with 120 Ω characteristic impedance (Z_O). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be on the cable or in a node, but if nodes may be removed from the bus the termination must be carefully placed so that it is not removed from the bus.

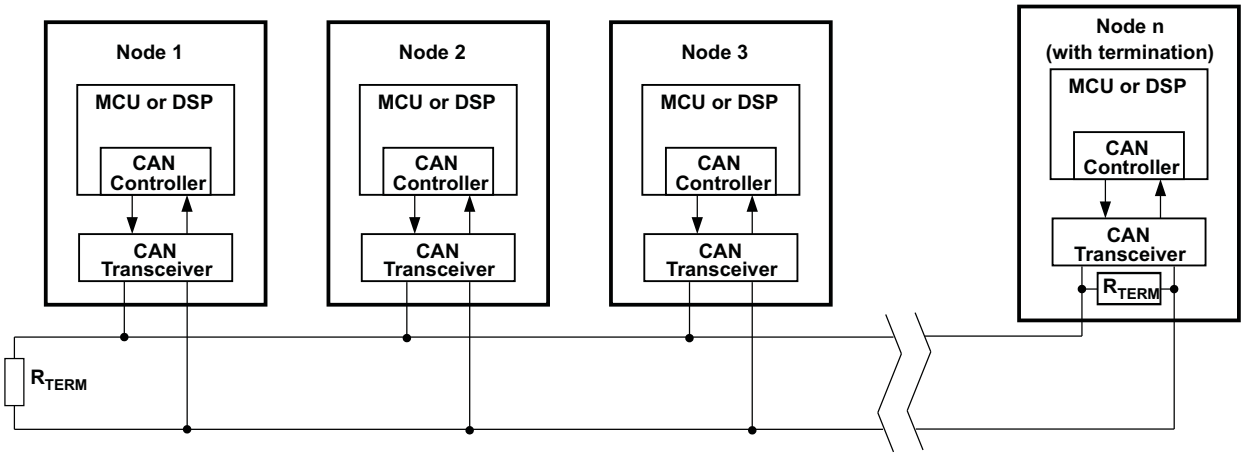


Figure 17. Typical CAN Bus

Typical Application (continued)

Termination may be a single 120 Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. (See Figure 18). Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions.

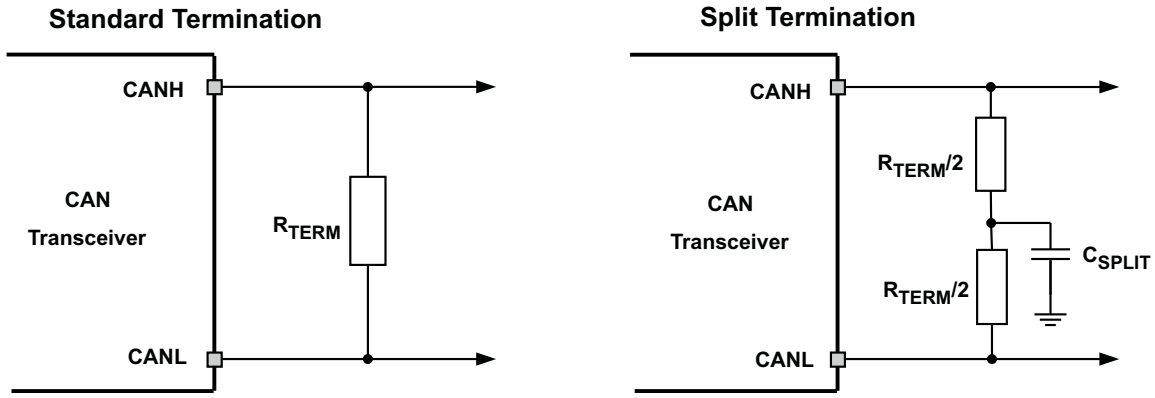


Figure 18. CAN Bus Termination Concepts

10.2.2.2 Functional Safety Using the SN65HVD267 in a Redundant Physical Layer CAN Network Topology

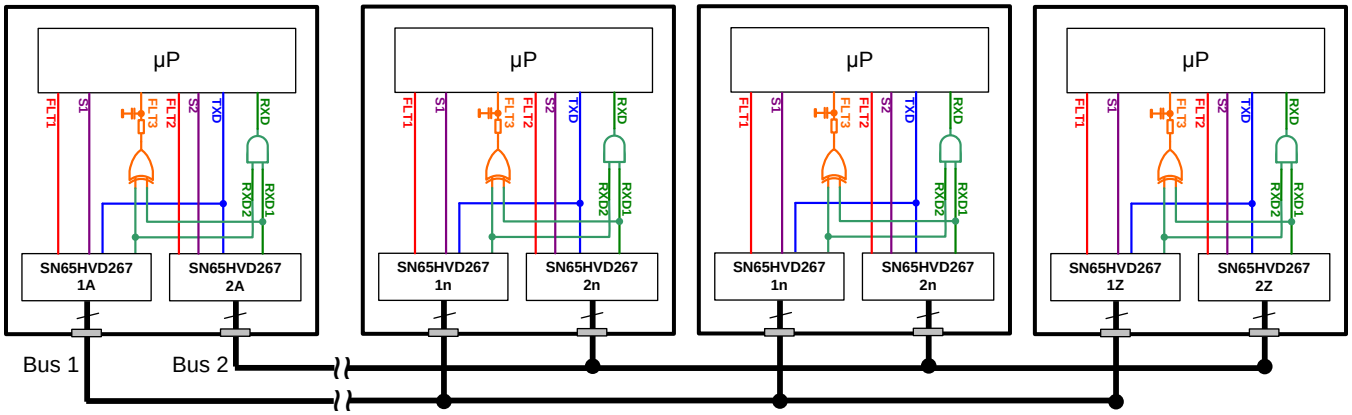
CAN is a standard linear bus topology using 120 Ω twisted pair cabling. The SN65HVD267 CAN device includes several features to use the CAN physical layer in nonstandard topologies with only one CAN link layer controller (μP) interface. This allows much greater flexibility in the physical topology of the bus while reducing the digital controller and software costs. The combination of RXD DTO and the FAULT output allows great flexibility, control and monitoring of these applications.

A simple example of this flexibility is to use two SN65HVD267 devices in parallel with an AND gate to achieve redundancy (parallel) of the physical layer (cabling and PHYs) in a CAN network.

For the CAN bit-wise arbitration to work, the RXD outputs of the transceivers must connect via AND gate logic so that a dominant bit (low) from any of the branches is received by the link layer logic (μP), and appears to the link layer and above as a single physical network. The RXD DTO feature prevents a bus stuck dominant fault in a single branch from taking down the entire network by forcing the RXD terminal for the transceivers on the branch with the fault back to the recessive after the t_{RXD_DTO} time. The remaining branch of the network continues to function. The FAULT terminal of the transceivers on the branch with the fault indicates this via the FAULT output to their host processors, which diagnose the failure condition. Adding a logic XOR with a filter adds automatic detection for a fault where one of the 2 networks goes open (recessive) in addition to the faults detected by the SN65HVD267. The S terminal (silent mode terminal) may be used to put a branch in silent mode to check each branch for other faults. Thus it is possible to implement a robust and redundant CAN network topology in a simple and low cost manner.

These concepts can be expanded into more complicated and flexible CAN network topologies to solve various system level challenges with a networked infrastructure.

Typical Application (continued)



A. CAN nodes with termination are PHY 1A, PHY 2A, PHY 1Z and PHY 2Z.

B. RXD DTO prevents a single branch-stuck-dominant condition from blocking the redundant branch via the AND logic on RXD. The transceivers signal a received bus stuck dominant fault via the FAULT terminal. The system detects which branch is stuck dominant, and issues a system warning. Other network faults on a single branch that appear as recessive (not blocking the redundant network) may be detected through a logic XOR with a filter and diagnostic routines, and using the Silent Mode of the PHYs to use only one branch at a time for transmission during diagnostic mode. This combination allows robust fault detection and recovery within single branches so that they may be repaired and again provide redundancy of the physical layer.

Figure 19. Typical Redundant Physical Layer Topology Using the SN65HVD267

10.2.3 Application Curve

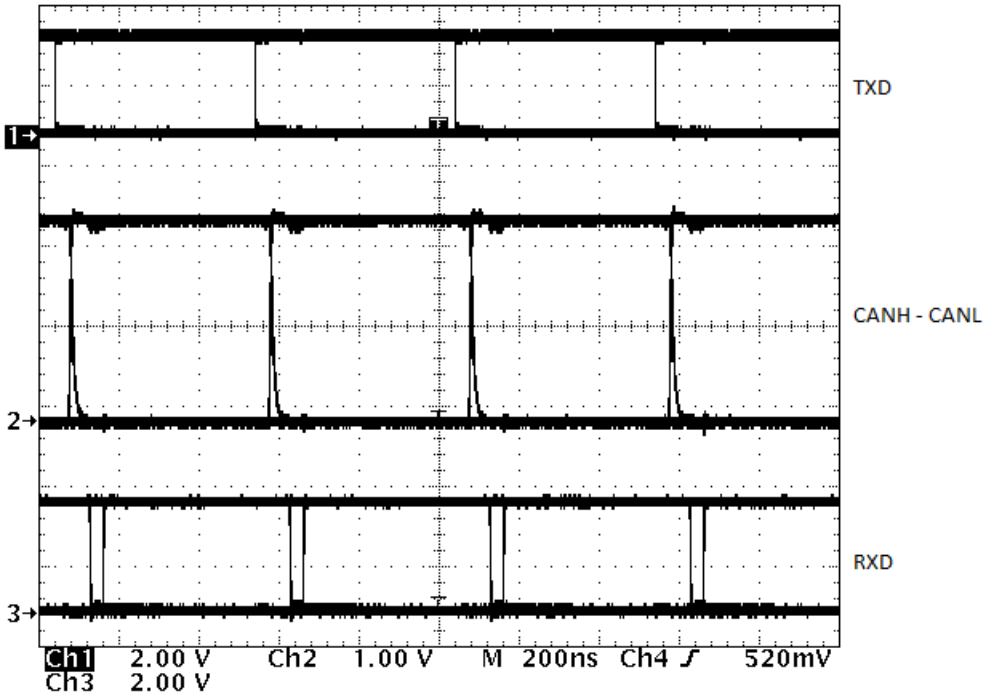


Figure 20. Typical CAN Transceiver Operation Using 3.3V IO Connections

11 Power Supply Recommendations

These devices are designed to operate from main V_{CC} input voltage supply range between 4.5 V and 5.5 V. Some devices have an output level shifting supply input, V_{RXD}, designed for a range between 2.8 V and 5.5 V. Both supply inputs must be well regulated. A bulk capacitance, typically 4.7 μF, should be placed near the CAN transceiver's main V_{CC} supply terminal in addition to bypass capacitors. A bulk capacitance, typically 1 μF, should be placed near the CAN transceiver's V_{RXD} supply terminal in addition to bypass capacitors.

12 Layout

12.1 Layout Guidelines

For the PCB design to be successful, start with design of the protection and filtering circuitry. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design. On chip IEC ESD protection is good for laboratory and portable equipment but is usually not sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices at the bus connectors. Placement at the connector also prevents these noisy events from propagating further into the PCB and system.

- Place the protection and filtering circuitry as close to the bus connector, J1, to prevent transients, ESD and noise from penetrating onto the board. In this layout example for protection a Transient Voltage Suppression (TVS) device, D1, has been used. The production solution can be either bi-directional TVS diode or varistor with ratings matching the application requirements. This example also shows optional bus filter capacitors C8 and C9.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Use supply (V_{CC}) and ground planes to provide low inductance. Note: high frequency current follows the path of least inductance and not the path of least impedance.
- Use at least two vias for supply (V_{CC}) and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver, examples C2, C3 (V_{CC}) and for the dual supply devices additionally C5 and C6 (V_{RXD}).
- Bus termination: this layout example shows split termination. This is where the termination is split into two resistors, R7 and R8, with the center or split tap of the termination connected to ground via capacitor C7. Split termination provides common mode filtering for the bus. When bus termination is placed on the board instead of directly on the bus, additional care must be taken to ensure the terminating node is not removed from the bus thus also removing the termination. See the application section for information on power ratings needed for the termination resistor(s).
- To limit current of digital lines serial resistors may be used. Examples are R2, R3, R4 and R5.
- To filter noise on the digital IO lines a capacitor may be used close to the input side of the IO as shown by C1 and C4.
- Terminal 5: This example is showing a flexible layout covering all three of the devices in this CAN transceiver family on terminal 5. SN65HVD265: this terminal is a no connect so external connections are un-important and the components R4, R5, C5 and C6 do not matter. SN65HVD266: this terminal is the RXD output supply terminal, VRXD. The bypass and bulk capacitor pads of C5 and C6 should be populated and R5 and R6 are not used. SN65HVD267: this terminal is the FAULT output (open drain). The pull resistor R6 is needed. R5 is shown if current limiting is desired to the host processor. If noise filtering is desired C5 should be used.
- 1k to 10kΩ pull-up or down resistors should be used where required to limit noise during transient events.
- Terminal 1: R1 is shown optionally for the TXD input of the device. If an option drain host processor is used this is mandatory to ensure the bit timing into the device is met.
- Terminal 8: is shown assuming the mode terminal, S, will be used. If the device will only be used in normal mode R3 is not needed and the pads of C4 could be used for the pull down resistor to GND.

12.2 Layout Example

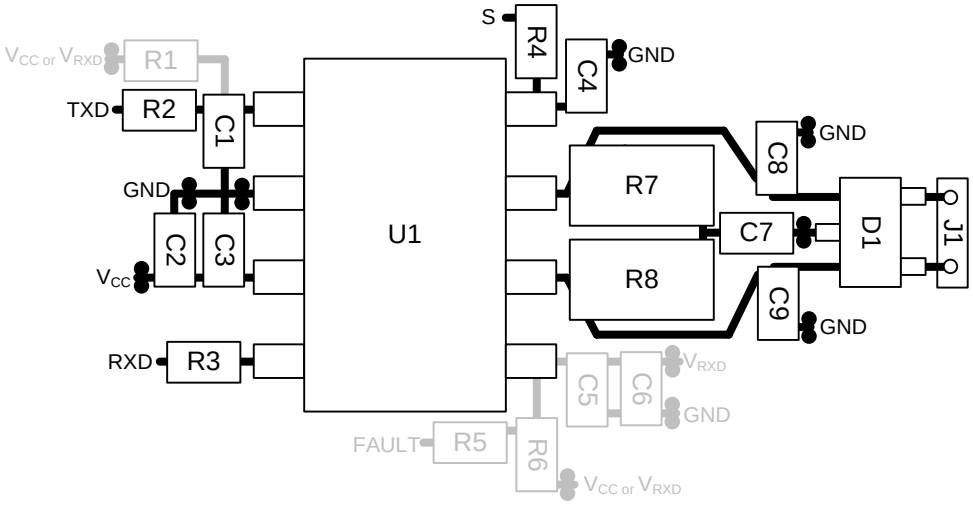


Figure 21. Layout Example

13 器件和文档支持

13.1 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持和社区资源、工具和软件，以及样片或购买的快速访问。

表 7. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
SN65HVD265	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
SN65HVD266	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
SN65HVD267	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD265D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD265	Samples
SN65HVD265DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD265	Samples
SN65HVD266D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD266	Samples
SN65HVD266DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD266	Samples
SN65HVD267D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD267	Samples
SN65HVD267DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD267	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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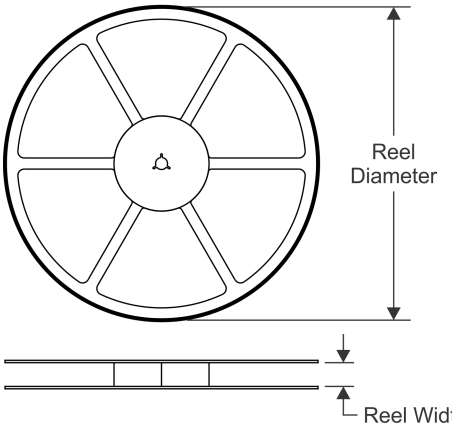
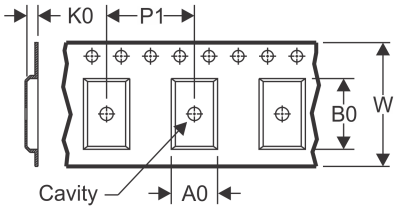
TAPE AND REEL INFORMATION

REEL DIMENSIONS

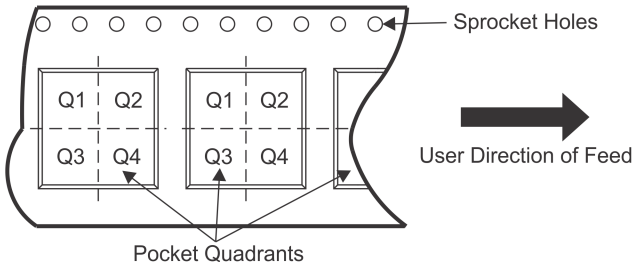


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

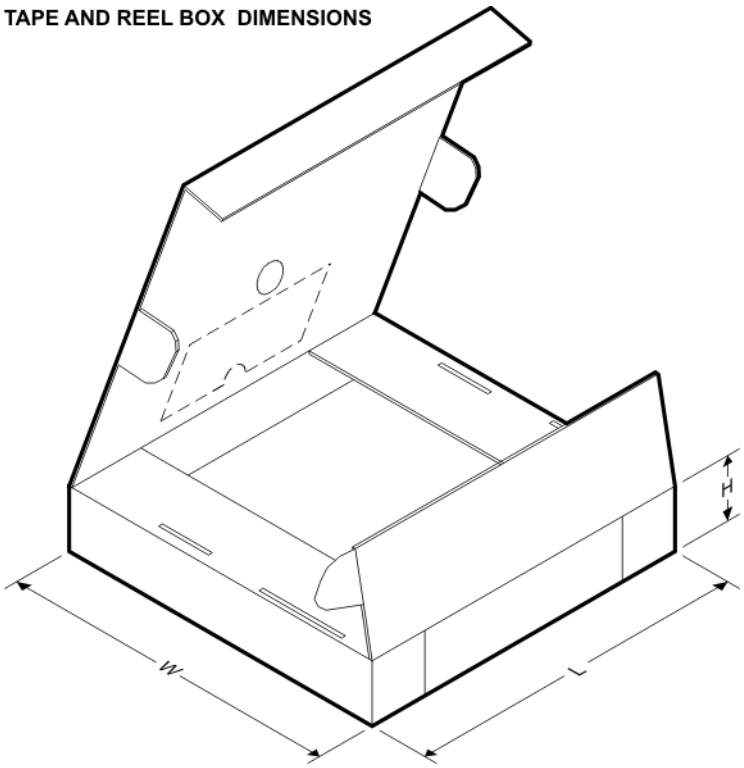
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD265DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD266DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD267DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

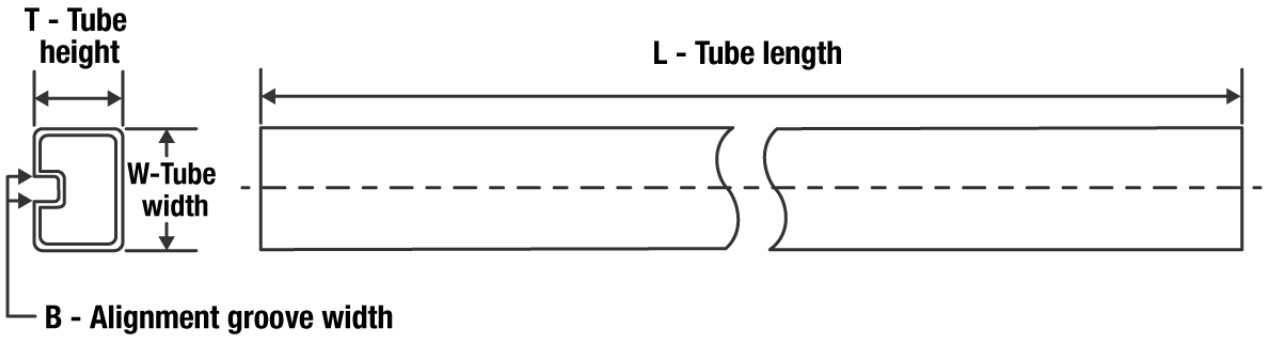
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

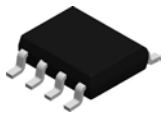
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD265DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD266DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD267DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD265D	D	SOIC	8	75	507	8	3940	4.32
SN65HVD266D	D	SOIC	8	75	507	7.85	3750	2.24
SN65HVD267D	D	SOIC	8	75	507	8	3940	4.32

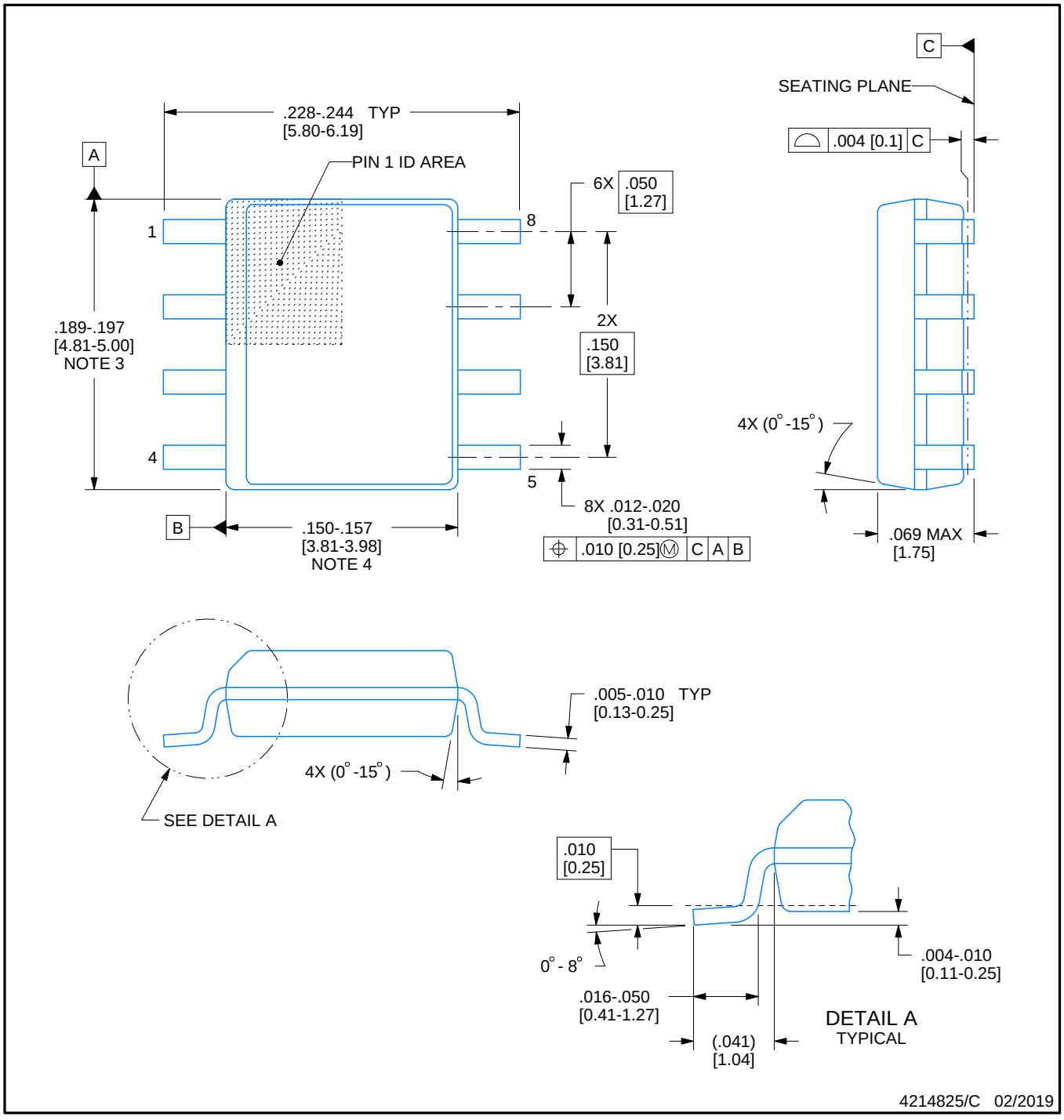


PACKAGE OUTLINE

D0008A

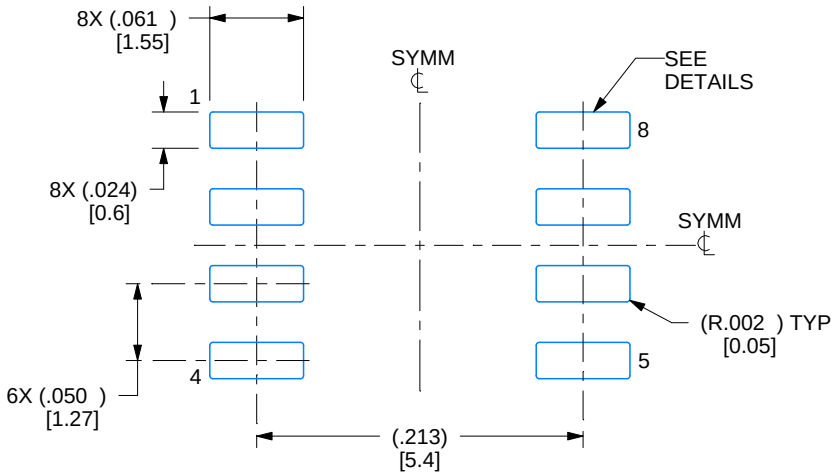
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

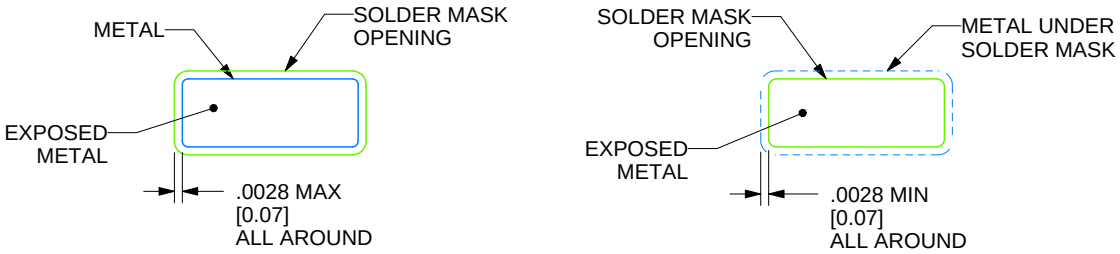


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

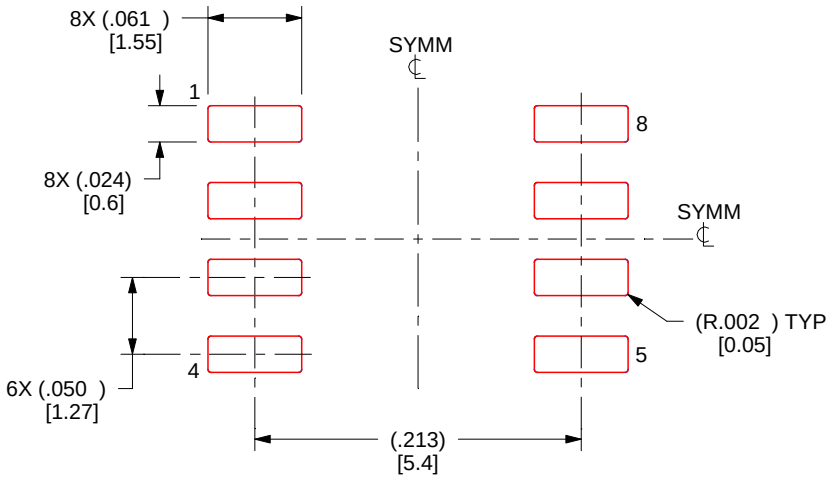
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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