

**Features**

- $I_{off}$  supports partial-power-down mode operation
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- $V_{CC} = 5\text{V} \pm 10\%$

*CY74FCT16245T Features:*

- 64 mA sink current, 32 mA source current
- Typical  $V_{OLP}$  (ground bounce) < 1.0V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

*CY74FCT162245T Features:*

- Balanced output drivers: 24 mA
- Reduced system switching noise
- Typical  $V_{OLP}$  (ground bounce) < 0.6V at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$

*CY74FCT162H245T Features:*

- Bus hold on data inputs
- Eliminates the need for external pull-up or pull-down resistors

**Functional Description**

These 16-bit transceivers are designed for use in bidirectional synchronous communication between two buses, where high speed and low power are required. With the exception of the CY74FCT16245T, these devices can be operated either as two independent octals or a single 16-bit transceiver. Direction of data flow is controlled by (DIR), the Output Enable ( $\overline{\text{OE}}$ ) transfers data when LOW and isolates the buses when HIGH.

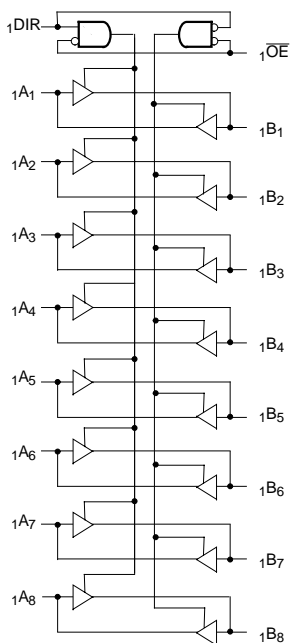
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The CY74FCT16245T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

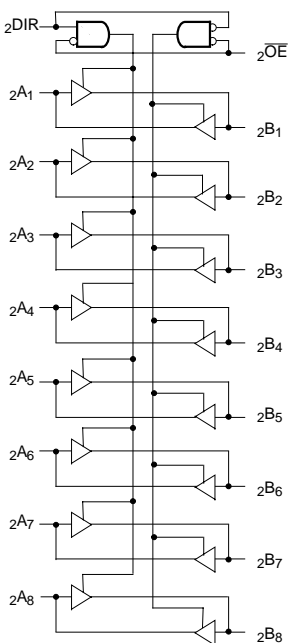
The CY74FCT162245T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162245T is ideal for driving transmission lines.

The CY74FCT162H245T is a 24-mA balanced output part that has bus hold on the data inputs. The device retains the input's last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

**Logic Block Diagrams CY74FCT16245T, CY74FCT162245T, CY74FCT162H245T**



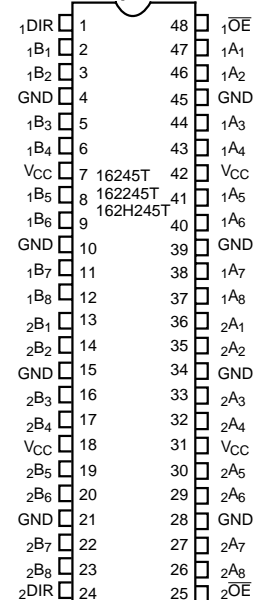
FCT16245-1



FCT16245-2

**Pin Configuration**

**SSOP/TSSOP  
Top View**



FCT16245-3

### Pin Description

Name	Description
OE	Three-State Output Enable Inputs (Active LOW)
DIR	Direction Control
A	Inputs or Three-State Outputs <sup>[1]</sup>
B	Inputs or Three-State Outputs <sup>[1]</sup>

### Function Table<sup>[2]</sup>

Inputs		Outputs
OE	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

### Maximum Ratings<sup>[3, 4]</sup>

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... Com'l -55°C to +125°C

Ambient Temperature with Power Applied..... Com'l -55°C to +125°C

DC Input Voltage ..... -0.5V to +7.0V

DC Output Voltage..... -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) ..... -60 to +120 mA

Power Dissipation ..... 1.0W

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

### Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Industrial	-40°C to +85°C	5V ± 10%

#### Notes:

- On CY74FCT162H245T these pins have bus hold.
- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = High Impedance.
- Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.

### Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage		2.0			V
V <sub>IL</sub>	Input LOW Voltage				0.8	V
V <sub>H</sub>	Input Hysteresis <sup>[6]</sup>			100		mV
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V
I <sub>IH</sub>	Input HIGH Current	Standard	V <sub>CC</sub> =Max., V <sub>I</sub> =V <sub>CC</sub>		±1	μA
		Bus Hold			±100	
I <sub>IL</sub>	Input LOW Current	Standard	V <sub>CC</sub> =Max., V <sub>I</sub> =GND		±1	μA
		Bus Hold			±100	μA
I <sub>BBH</sub> I <sub>BBL</sub>	Bus Hold Sustain Current on Bus Hold Input <sup>[7]</sup>	V <sub>CC</sub> =Min.	V <sub>I</sub> =2.0V	-50		μA
			V <sub>I</sub> =0.8V	+50		
I <sub>BHHO</sub> I <sub>BHLO</sub>	Bus Hold Overdrive Current on Bus Hold Input <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>I</sub> =1.5V			TBD	mA
I <sub>OZH</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.7V			±1	μA
I <sub>OZL</sub>	High Impedance Output Current (Three-State Output pins)	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.5V			±1	μA
I <sub>OS</sub>	Short Circuit Current <sup>[8]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =GND	-80	-140	-200	mA
I <sub>O</sub>	Output Drive Current <sup>[8]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =2.5V	-50		-180	mA
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> ≤4.5V <sup>[9]</sup>			±1	μA

**Output Drive Characteristics for CY74FCT16245T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-3 mA	2.5	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	2.4	3.5		V
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	2.0	3.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA		0.2	0.55	V

**Output Drive Characteristics for CY74FCT162245T, CY74FCT162H245T**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit
I <sub>ODL</sub>	Output LOW Current <sup>[8]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	60	115	150	mA
I <sub>ODH</sub>	Output HIGH Current <sup>[8]</sup>	V <sub>CC</sub> =5V, V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , V <sub>OUT</sub> =1.5V	-60	-115	-150	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-24 mA	2.4	3.3		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =24 mA		0.3	0.55	V

**Notes:**

5. Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
6. This parameter is specified but not tested.
7. Pins with bus hold are described in Pin Description.
8. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
9. Tested at +25°C.

**Capacitance<sup>[6]</sup> (T<sub>A</sub> = +25°C, f = 1.0 MHz)**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	4.5	6.0	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	5.5	8.0	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit	
$I_{CC}$	Quiescent Power Supply Current	$V_{CC}=\text{Max.}$ $V_{IN}\leq 0.2V$ , $V_{IN}\geq V_{CC}-0.2V$	5	500	$\mu A$	
$\Delta I_{CC}$	Quiescent Power Supply Current (TTL inputs HIGH)	$V_{CC}=\text{Max.}$ $V_{IN}=3.4V^{[10]}$	0.5	1.5	mA	
$I_{CCD}$	Dynamic Power Supply Current <sup>[11]</sup>	$V_{CC}=\text{Max.}$ , One Input Toggling, 50% Duty Cycle, Outputs Open, $OE=DIR=GND$	$V_{IN}=V_{CC}$ or $V_{IN}=GND$	60	100	$\mu A/MHz$
$I_C$	Total Power Supply Current <sup>[12]</sup>	$V_{CC}=\text{Max.}$ , $f_1=10$ MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $OE=DIR=GND$	$V_{IN}=V_{CC}$ or $V_{IN}=GND$	0.6	1.5	mA
			$V_{IN}=3.4V$ or $V_{IN}=GND$	0.9	2.3	mA
		$V_{CC}=\text{Max.}$ , $f_1=2.5$ MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $OE=DIR=GND$	$V_{IN}=V_{CC}$ or $V_{IN}=GND$	2.4	4.5 <sup>[13]</sup>	mA
			$V_{IN}=3.4V$ or $V_{IN}=GND$	6.4	16.5 <sup>[13]</sup>	mA

**Notes:**

10. Per TTL driven input ( $V_{IN}=3.4V$ ); all other inputs at  $V_{CC}$  or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$   
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$   
 $I_{CC}$  = Quiescent Current with CMOS input levels  
 $\Delta I_{CC}$  = Power Supply Current for a TTL HIGH input ( $V_{IN}=3.4V$ )  
 $D_H$  = Duty Cycle for TTL inputs HIGH  
 $N_T$  = Number of TTL inputs at  $D_H$   
 $I_{CCD}$  = Dynamic Current caused by an input transition pair (HLH or LHL)  
 $f_0$  = Clock frequency for registered devices, otherwise zero  
 $f_1$  = Input signal frequency  
 $N_1$  = Number of inputs changing at  $f_1$   
 All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the  $I_{CC}$  formula. These limits are specified but not tested.

**Switching Characteristics** Over the Operating Range<sup>[14]</sup>

Parameter	Description	74FCT16245T 74FCT162245T		74FCT16245AT 74FCT162245AT 74FCT162H245AT		Unit	Fig. No. <sup>[15]</sup>
		Min.	Max.	Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output A to B, B to A	1.5	7.0	1.5	4.5	ns	1, 3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OE to A or B	1.5	9.5	1.5	6.2	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE to A or B	1.5	7.5	1.5	5.0	ns	1, 7, 8
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time DIR to A or B	1.5	9.5	1.5	6.2	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time DIR to A or B	1.5	7.5	1.5	5.0	ns	1, 7, 8
t <sub>SK(O)</sub>	Output Skew <sup>[16]</sup>		0.5		0.5	ns	—

Parameter	Description	74FCT16245CT 74FCT162245CT 74FCT162H245CT		Unit	Fig. No. <sup>[15]</sup>
		Min.	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Data to Output A to B, B to A	1.5	4.1	ns	1, 3
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time OE to A or B	1.5	5.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time OE to A or B	1.5	4.8	ns	1, 7, 8
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time DIR to A or B	1.5	5.8	ns	1, 7, 8
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time DIR to A or B	1.5	4.8	ns	1, 7, 8
t <sub>SK(O)</sub>	Output Skew <sup>[16]</sup>		0.5	ns	—

**Note:**

14. Minimum limits are specified but not tested on Propagation Delays.

15. See "Parameter Measurement Information" in the General Information section.

16. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

**Ordering Information CY74FCT16245**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT16245CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245CTPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
4.5	CY74FCT16245ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245ATPVC/PVCT	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT16245TPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16245TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT162245**

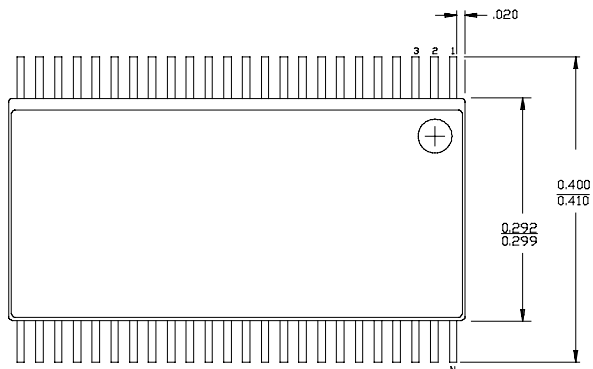
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	CY74FCT162245CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162245CTPVCT	O48	48-Lead (300-Mil) SSOP	
4.5	74FCT162245ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162245ATPVCT	O48	48-Lead (300-Mil) SSOP	
7.0	CY74FCT162245TPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162245TPVC/PVCT	O48	48-Lead (300-Mil) SSOP	

**Ordering Information CY74FCT162H245**

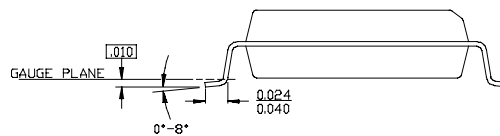
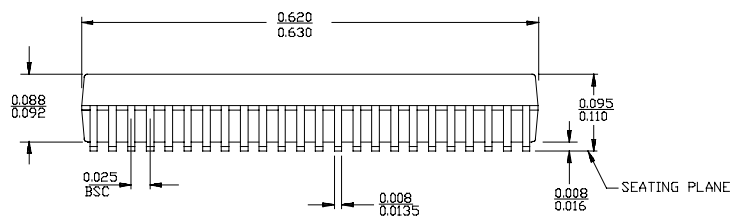
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
4.1	74FCT162H245CTPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162H245CTPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162H245CTPVCT	O48	48-Lead (300-Mil) SSOP	
4.5	74FCT162H245ATPACT	Z48	48-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162H245ATPVC	O48	48-Lead (300-Mil) SSOP	
	74FCT162H245ATPVCT	O48	48-Lead (300-Mil) SSOP	

**Package Diagrams**

**48-Lead Shrunken Small Outline Package O48**

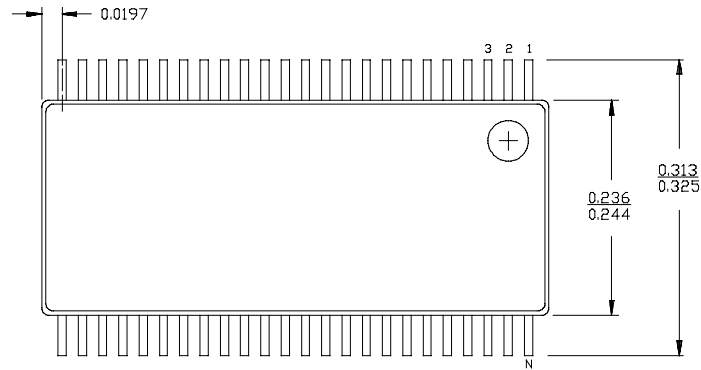


DIMENSIONS IN INCHES MIN.  
MAX.

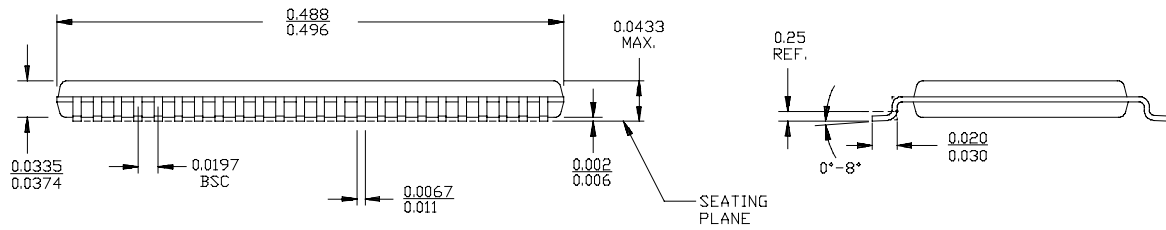


**Package Diagrams**

**48-Lead Thin Shrunk Small Outline Package Z48**



DIMENSIONS IN INCHES MIN.  
MAX.





**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74FCT162245ATPACT	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162245A	<a href="#">Samples</a>
74FCT162245ATPVCT	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162245A	<a href="#">Samples</a>
74FCT162245CTPACT	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162245C	<a href="#">Samples</a>
74FCT16245TPVCG4	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245	<a href="#">Samples</a>
74FCT162H245ATPACT	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162H245A	<a href="#">Samples</a>
74FCT162H245ATPVC	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162H245A	<a href="#">Samples</a>
74FCT162H245CTPACT	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162H245C	<a href="#">Samples</a>
74FCT162H245CTPVC	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162H245C	<a href="#">Samples</a>
CY74FCT162245ATPVC	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162245A	<a href="#">Samples</a>
CY74FCT162245CTPVC	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162245C	<a href="#">Samples</a>
CY74FCT162245TPACT	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162245	<a href="#">Samples</a>
CY74FCT162245TPVC	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162245	<a href="#">Samples</a>
CY74FCT162245TPVCT	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT162245	<a href="#">Samples</a>
CY74FCT16245ATPACT	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245A	<a href="#">Samples</a>
CY74FCT16245ATPVC	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245A	<a href="#">Samples</a>
CY74FCT16245ATPVCT	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245A	<a href="#">Samples</a>
CY74FCT16245CTPACT	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245C	<a href="#">Samples</a>
CY74FCT16245CTPVC	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245C	<a href="#">Samples</a>
CY74FCT16245CTPVCT	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245C	<a href="#">Samples</a>
CY74FCT16245TPACT	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CY74FCT16245TPVC	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245	<a href="#">Samples</a>
CY74FCT16245TPVCT	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FCT16245	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74FCT162245ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74FCT162245ATPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
74FCT162245CTPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74FCT162H245ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
74FCT162H245CTPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CY74FCT162245TPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CY74FCT162245TPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16245ATPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CY74FCT16245ATPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16245CTPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CY74FCT16245CTPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
CY74FCT16245TPACT	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
CY74FCT16245TPVCT	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74FCT162245ATPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
74FCT162245ATPVCT	SSOP	DL	48	1000	367.0	367.0	55.0
74FCT162245CTPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
74FCT162H245ATPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
74FCT162H245CTPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
CY74FCT162245TPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
CY74FCT162245TPVCT	SSOP	DL	48	1000	367.0	367.0	55.0
CY74FCT16245ATPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
CY74FCT16245ATPVCT	SSOP	DL	48	1000	367.0	367.0	55.0
CY74FCT16245CTPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
CY74FCT16245CTPVCT	SSOP	DL	48	1000	367.0	367.0	55.0
CY74FCT16245TPACT	TSSOP	DGG	48	2000	367.0	367.0	45.0
CY74FCT16245TPVCT	SSOP	DL	48	1000	367.0	367.0	55.0

**TUBE**

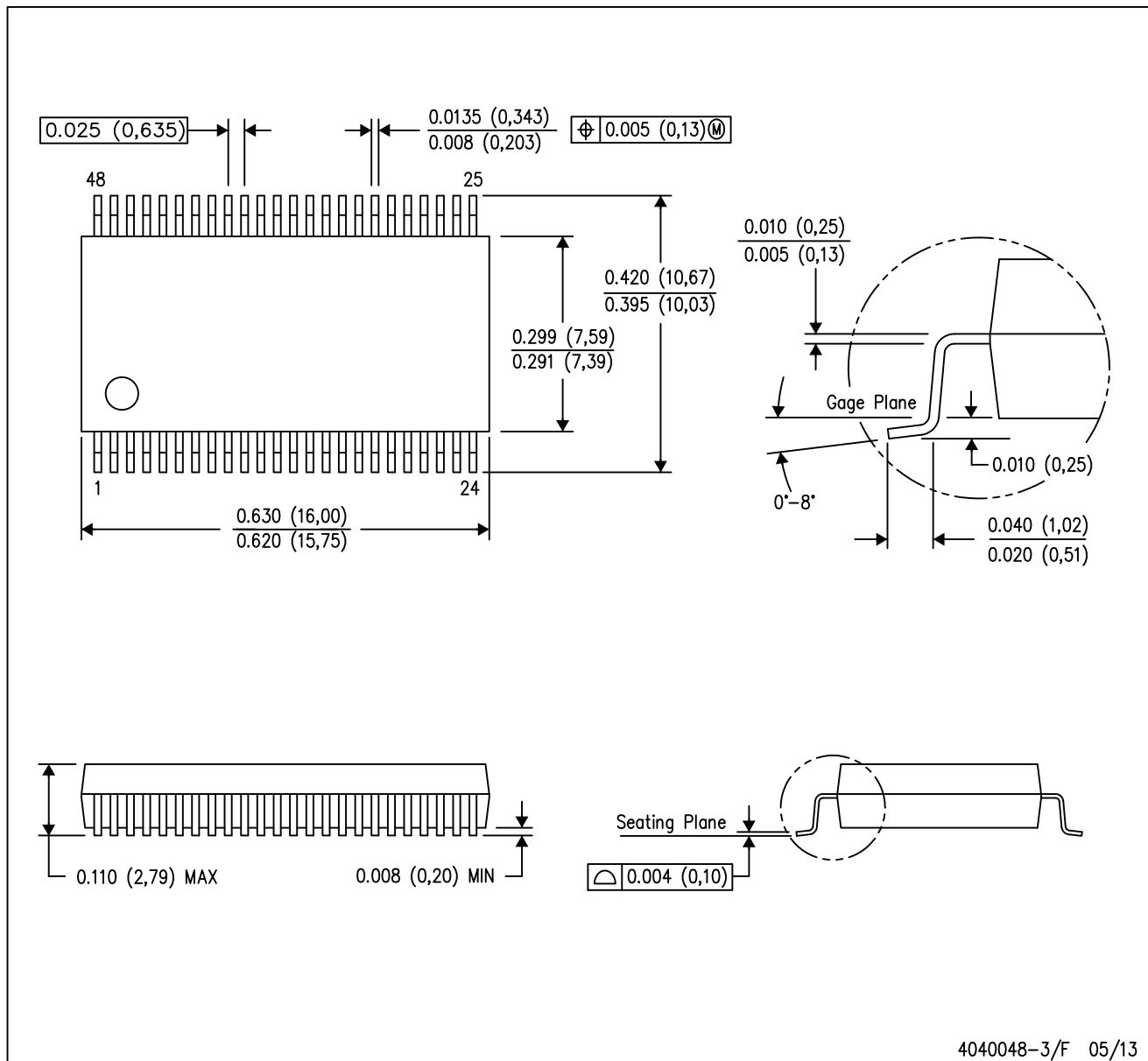

\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
74FCT16245TPVCG4	DL	SSOP	48	25	473.7	14.24	5110	7.87
74FCT162H245ATPVC	DL	SSOP	48	25	473.7	14.24	5110	7.87
74FCT162H245CTPVC	DL	SSOP	48	25	473.7	14.24	5110	7.87
CY74FCT162245ATPVC	DL	SSOP	48	25	473.7	14.24	5110	7.87
CY74FCT162245CTPVC	DL	SSOP	48	25	473.7	14.24	5110	7.87
CY74FCT162245TPVC	DL	SSOP	48	25	473.7	14.24	5110	7.87
CY74FCT16245ATPVC	DL	SSOP	48	25	473.7	14.24	5110	7.87
CY74FCT16245CTPVC	DL	SSOP	48	25	473.7	14.24	5110	7.87
CY74FCT16245TPVC	DL	SSOP	48	25	473.7	14.24	5110	7.87

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.

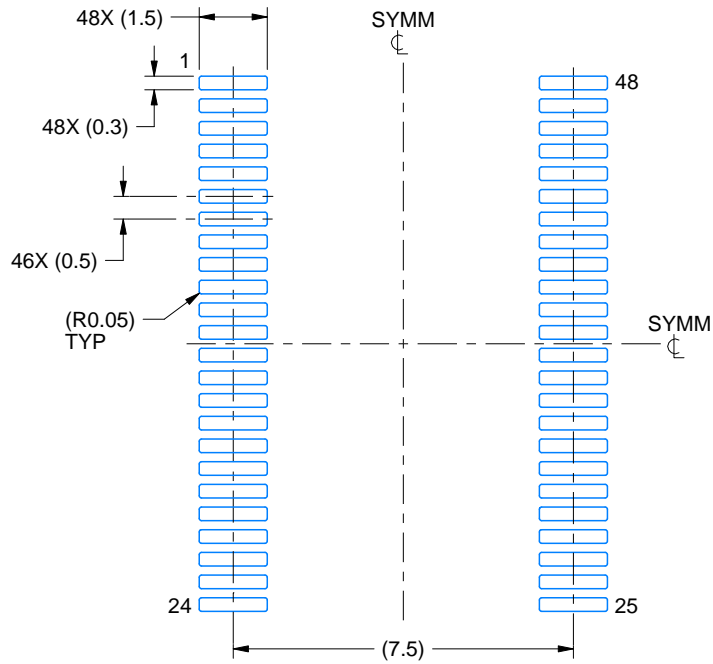


# EXAMPLE BOARD LAYOUT

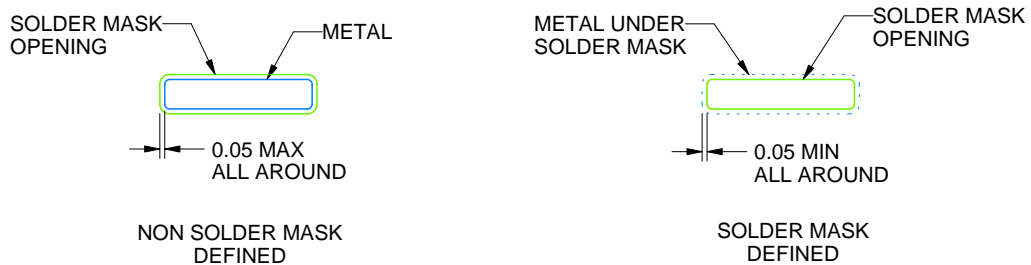
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

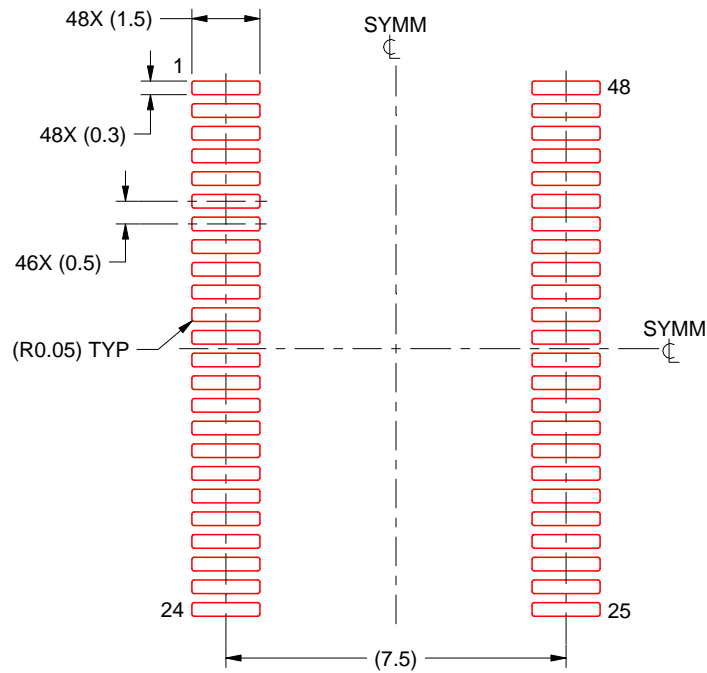


# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated