四通道 1/2 H 桥驱动器集成电路 (IC)

查询样品: DRV8844

特性

- 四通道 **1/2 H** 桥直流 **(DC)** 电机驱动器
  - 能够驱动四个螺线管、两个 **DC** 电机、一个步进电机、或者其它负载
  - 完全独立的半桥控制
  - 低 **MOSFET** 导通电阻
- **24V，25°C** 下 **2.5A** 最大驱动器电流
- 悬空的输入缓冲可支持双（双极）电源（高达 **±30V**）
- 内置 **3.3V，10mA** 低压降 **(LDO)** 稳压器
- 行业标准 **IN/IN** 数字控制接口
- **8V** 至 **60V** 运行电源电压范围
- 耐热增强型表面贴装封装

应用范围

- 纺织机器
- 办公自动化设备
- 游戏机
- 工厂自动化
- 机器人技术

说明

DRV8844 提供四个可独立控制的 1/2 H 桥启动器。 它可被用于驱动两个 DC 电机、一个步进电机、四个螺线管、或者其它负载。 针对每个通道的输出驱动器通道由在一个 1/2 H 桥配置中进行配置的 N 通道功率 MOSFET 组成。

DRV8844 在每个桥的通道上提供高达 2.5A 峰值电流或者 1.75A 均方根 (RMS) 输出电流（在 24V 和 25°C 时具有适当的印刷电路板 (PCB) 散热）。

提供单独控制每个 1/2 H 桥的独立输入。 为了与独立电源一起运行，逻辑输入和 nFAULT 输出以一个独立的悬空接地引脚为基准。

内部关断功能支持过流保护、短路保护、欠压锁定以及过温保护。

DRV8844 采用带有 PowerPAD™ 的 28 引脚散热型薄型小外形尺寸 (HTSSOP) 封装（环保型：符合 RoHS 标准且不含 Sb/Br）。

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PowerPAD™ (HTSSOP) - PWP	Reel of 2000	DRV8844PWPR	DRV8844
		Tube of 50	DRV8844PWP	

(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

DEVICE INFORMATION

Functional Block Diagram

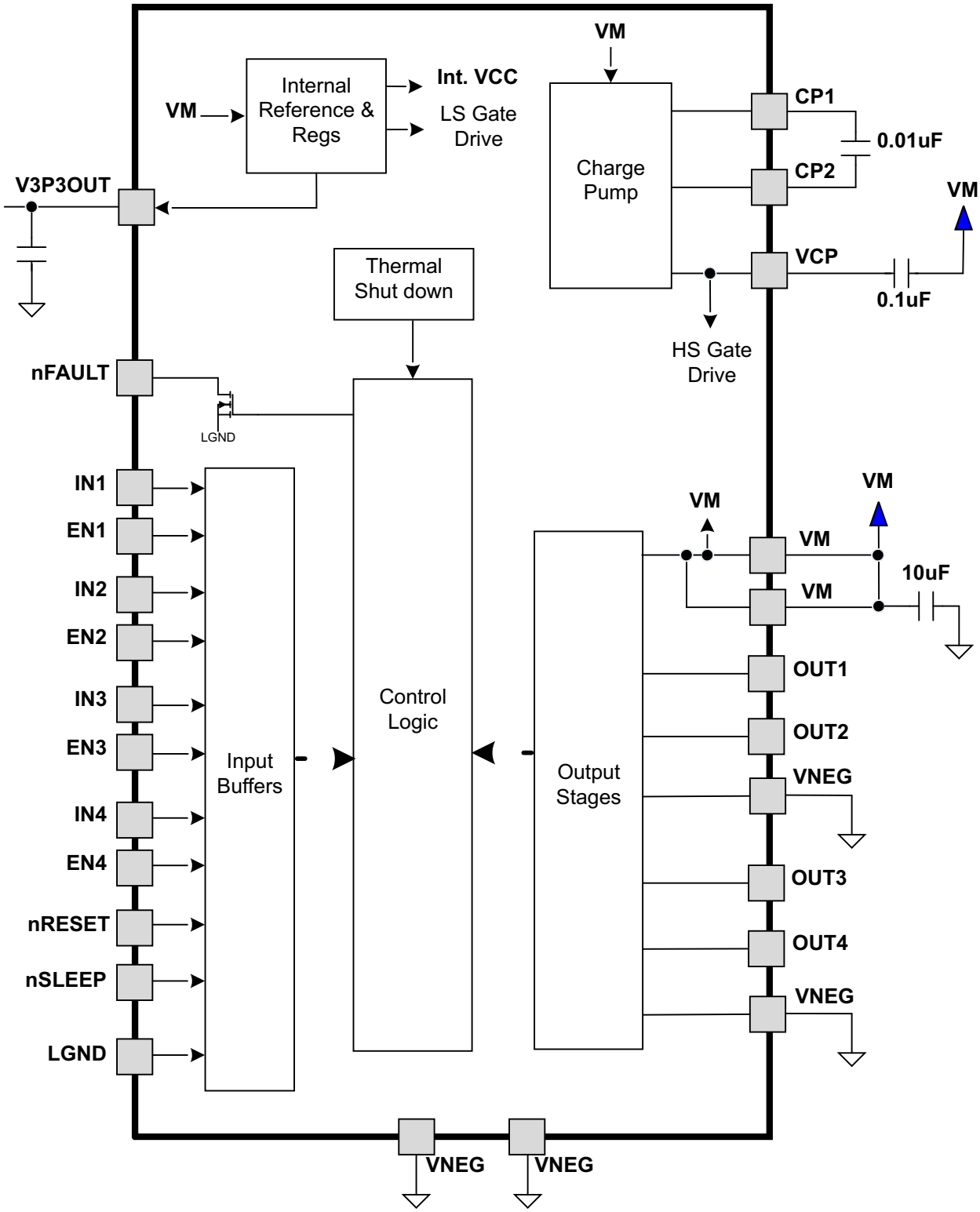
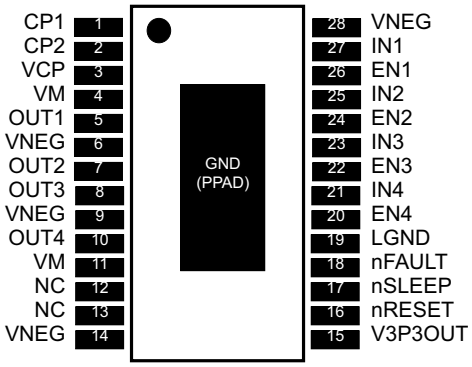


Table 1. TERMINAL FUNCTIONS

NAME	PIN	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
VNEG	6, 9, 14, 28, PPAD	-	Negative power supply (dual supplies) or ground (single supply)	
LGND	19	I	Logic input reference ground	Connect to logic ground. This may be any voltage between VNEG and VM - 8 V.
VM	4, 11	-	Main power supply	Connect to motor supply (8 V - 60 V). Both pins must be connected to same supply. Bypass to VNEG with a 10-µF (minimum) capacitor.
V3P3OUT	15	O	3.3-V regulator output	Bypass to VNEG with a 0.47-µF 6.3-V ceramic capacitor. Can be used to supply VREF.
CP1	1	IO	Charge pump flying capacitor	Connect a 0.01-µF 100-V capacitor between CP1 and CP2.
CP2	2	IO	Charge pump flying capacitor	
VCP	3	IO	High-side gate drive voltage	Connect a 0.1-µF 16-V ceramic capacitor to VM.
CONTROL				
IN1	27	I	Channel 1 input	Logic input controls state of OUT1. Internal pulldown.
EN1	26	I	Channel 1 enable	Logic high enables OUT1. Internal pulldown.
IN2	25	I	Channel 2 input	Logic input controls state of OUT2. Internal pulldown.
EN2	24	I	Channel 2 enable	Logic high enables OUT2. Internal pulldown.
IN3	23	I	Channel 3 input	Logic input controls state of OUT3. Internal pulldown.
EN3	22	I	Channel 3 enable	Logic high enables OUT3. Internal pulldown.
IN4	21	I	Channel 4 input	Logic input controls state of OUT4. Internal pulldown.
EN4	20	I	Channel 4 enable	Logic high enables OUT4. Internal pulldown.
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs. Internal pulldown.
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemp, overcurrent, UVLO). Open-drain output.
OUTPUT				
OUT1	5	O	Output 1	Connect to loads.
OUT2	7	O	Output 2	
OUT3	8	O	Output 3	
OUT4	10	O	Output 4	
NO CONNECT				
NC	12, 13	-	No connect	No connection to these pins

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted) (1) (2)

		VALUE	UNIT
VM	Power supply voltage range	–0.3 to 65	V
	Logic ground voltage range (LGND)	–0.5 to VM - 8	V
	Digital pin voltage range	LGND - 0.5 to LGND + 7	V
	Peak motor drive output current, t < 1 µS	Internally limited	A
	Continuous motor drive output current(3)	2.5	A
T_J	Operating virtual junction temperature range	–40 to 150	°C
T_{stg}	Storage temperature range	–60 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to VNEG terminal, unless otherwise specified.
(3) Power dissipation and thermal limits must be observed.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV8844 PWP 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	31.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	15.9	
θ_{JB}	Junction-to-board thermal resistance(4)	5.6	
ψ_{JT}	Junction-to-top characterization parameter(5)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(6)	5.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.4	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range(1)	8		60	V
I_{V3P3}	V3P3OUT load current	0		10	mA

(1) All V_M pins must be connected to the same supply voltage.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		1	5	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		500	800	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		6.3	8	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.18	3.3	3.52	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			LGND + 0.6	LGND + 0.7	V
V_{IH}	Input high voltage		LGND + 2.2		LGND + 5.25	V
V_{HYS}	Input hysteresis		50		600	mV
I_{IL}	Input low current	VIN = LGND	–5		5	µA
I_{IH}	Input high current	VIN = LGND + 3.3 V			100	µA
R_{PD}	Internal pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			LGND + 0.5	V
I_{OH}	Output high leakage current	V_O = LGND + 3.3 V			1	µA
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.29	0.39	
	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.29	0.39	
I_{OFF}	Off-state leakage current		–2		2	µA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		3			A
t_{DEAD}	Output dead time			90		ns
t_{OCP}	Overcurrent protection deglitch time			5		µs
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

SWITCHING CHARACTERISTICS(1)

over operating free-air temperature range (unless otherwise noted)

NUMBER	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
1	t_1	Delay time, ENx high to OUTx high, INx = 1	130	330	ns
2	t_2	Delay time, ENx low to OUTx low, INx = 1	275	475	ns
3	t_3	Delay time, ENx high to OUTx low, INx = 0	100	300	ns
4	t_4	Delay time, ENx low to OUTx high, INx = 0	200	400	ns
5	t_5	Delay time, INx high to OUTx high	300	500	ns
6	t_6	Delay time, INx low to OUTx low	275	475	ns
7	t_R	Output rise time, resistive load to VNEG	30	150	ns
8	t_F	Output fall time, resistive load to VNEG	30	150	ns

(1) Not production tested – specified by design

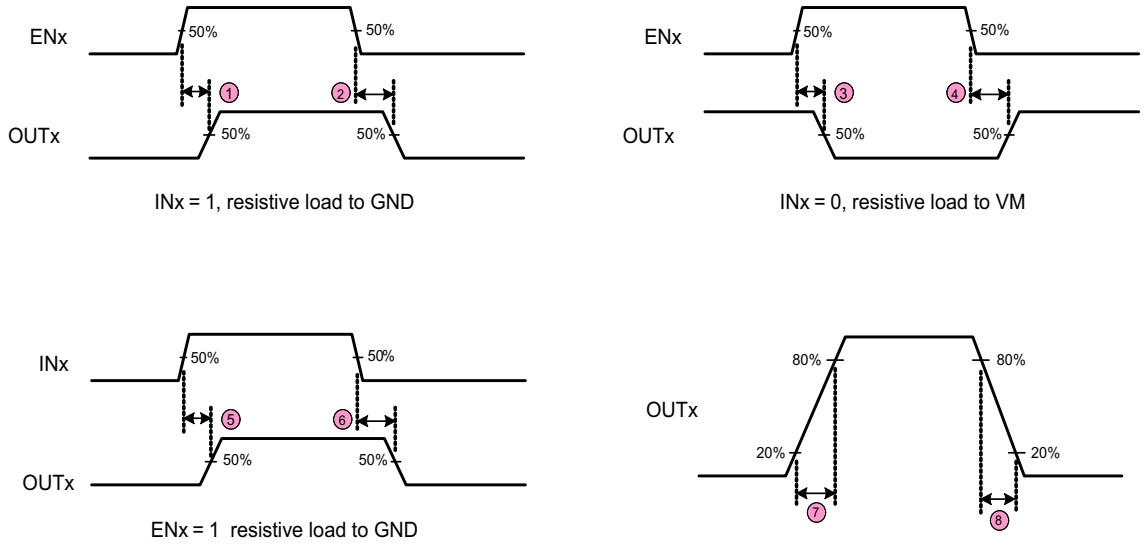


Figure 1. DRV8844 Switching Characteristics

FUNCTIONAL DESCRIPTION

Output Stage

The DRV8844 contains four 1/2-H-bridge drivers using N-channel MOSFETs. A block diagram of the output circuitry is shown in Figure 2.

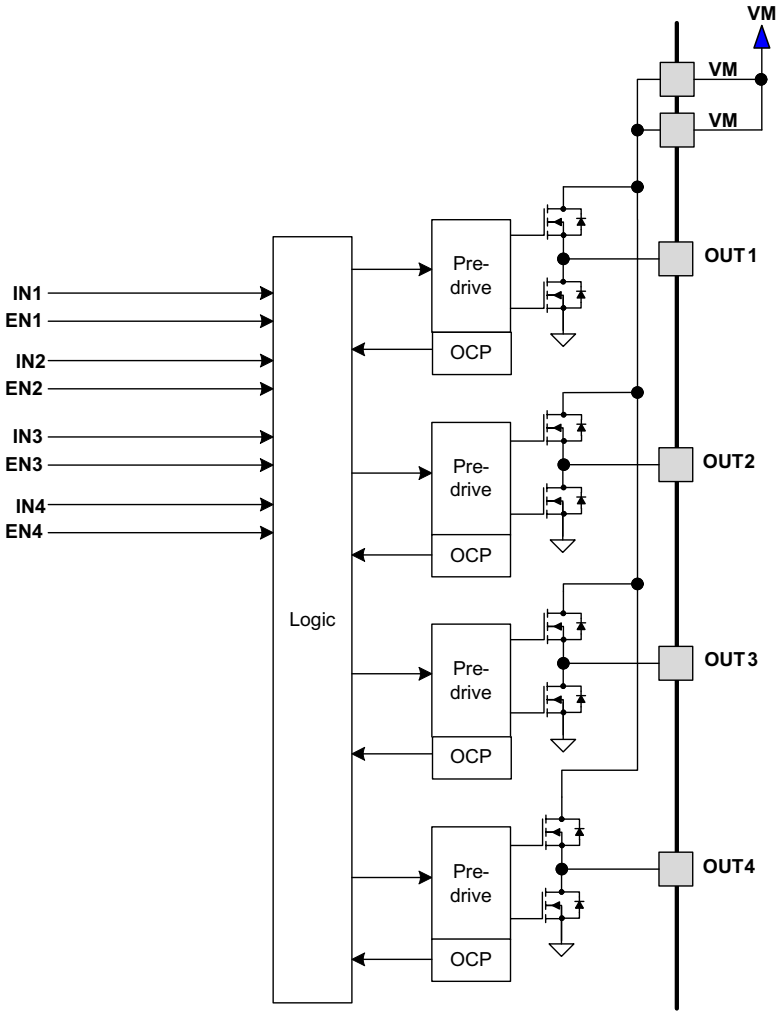


Figure 2. Motor Control Circuitry

The output pins are driven between VM and VNEG. VNEG is normaly ground for single supply applications, and a negative voltage for dual supply applications.

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

Logic Inputs

The logic inputs and nFAULT output are referenced to the LGND pin. This pin would be connected to the logic ground of the source of the logic signals (e.g., microcontroller). This allows LGND to be at a different voltage than VNEG; for example, you could drive a load by with bipolar power supplies by driving VM with +24 V and VNEG with -24 V, and connect LGND to 0 V (ground).

Bridge Control

The INx input pins directly control the state (high or low) of the OUTx outputs; the ENx input pins enable or disable the OUTx driver. Table 2 shows the logic.

Table 2. H-Bridge Logic

INx	ENx	OUTx
X	0	Z
0	1	L
1	1	H

The inputs can also be used for PWM control of, for example, the speed of a DC motor. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to the ENx pin; to use slow decay, the PWM signal is applied to the INx pin. Table 3 is an example of driving a DC motor using OUT1 and OUT2 as an H-bridge:

Table 3. PWM Function

IN1	EN1	IN2	EN2	FUNCTION
PWM	1	0	1	Forward PWM, slow decay
0	1	PWM	1	Reverse PWM, slow decay
1	PWM	0	PWM	Forward PWM, fast decay
0	PWM	1	PWM	Reverse PWM, fast decay

The drawings below show the current paths in different drive and decay modes:

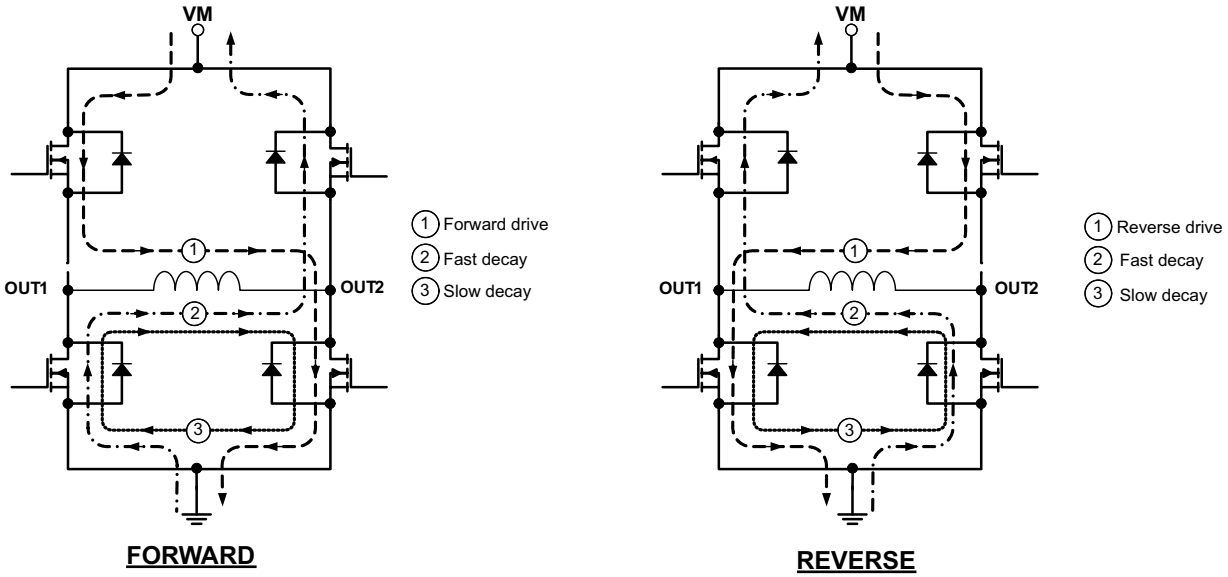


Figure 3. Current Paths

Charge Pump

Since the output stages use N-channel FETs, a gate drive voltage higher than the VM power supply is needed to fully enhance the high-side FETs. The DRV8844 integrates a charge pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. Refer to the block diagram and pin descriptions for details on these capacitors (value, connection, etc.).

The charge pump is shut down when SLEEPn is active low.

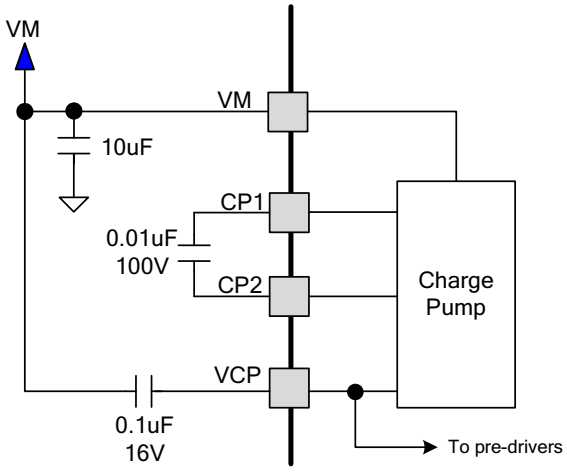


Figure 4. Charge Pump

nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational. Note that nRESET and nSLEEP have internal pulldown resistors of approximately 100 kΩ. These signals need to be driven to logic high for device operation.

The V3P3OUT LDO regulator remains operational in sleep mode.

Protection Circuits

The DRV8844 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP deglitch time, the channel experiencing the overcurrent will be disabled and the nFAULT pin will be driven low. The driver will remain off until either RESET is asserted or VM power is cycled.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all outputs will be disabled, internal logic will be reset, and the nFAULT pin will be driven low. Operation will resume when VM rises above the UVLO threshold.

THERMAL INFORMATION

Thermal Protection

The SDRV8844 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Power Dissipation

Power dissipation in the SDRV8844 is dominated by the power dissipated in the output FET resistance, or RDS(ON). Average power dissipation of each H-bridge when running a DC motor can be roughly estimated by Equation 1.

$$P = 2 \bullet R_{DS(ON)} \bullet (I_{OUT})^2 \quad (1)$$

where P is the power dissipation of one H-bridge, $R_{DS(ON)}$ is the resistance of each FET, and I_{OUT} is the RMS output current being applied to each winding. I_{OUT} is equal to the average current drawn by the DC motor. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current (one high-side and one low-side).

The total device dissipation will be the power dissipated in each of the two H-bridges added together.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, " PowerPAD™ Thermally Enhanced Package" and TI application brief SLMA004, " PowerPAD™ Made Easy", available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8844PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8844	Samples
DRV8844PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8844	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

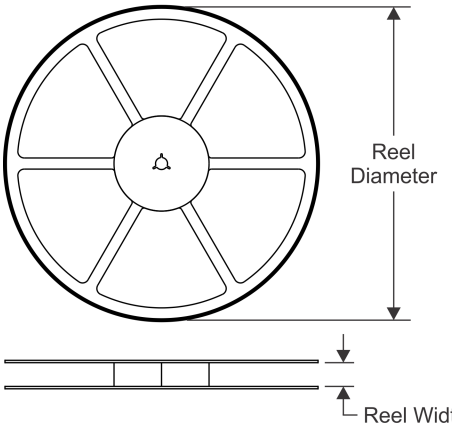
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

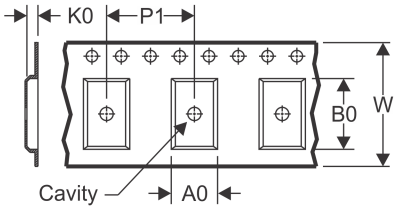
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

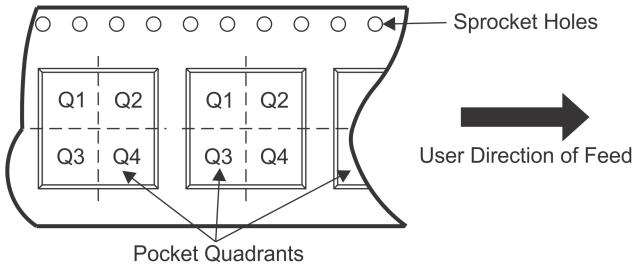


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

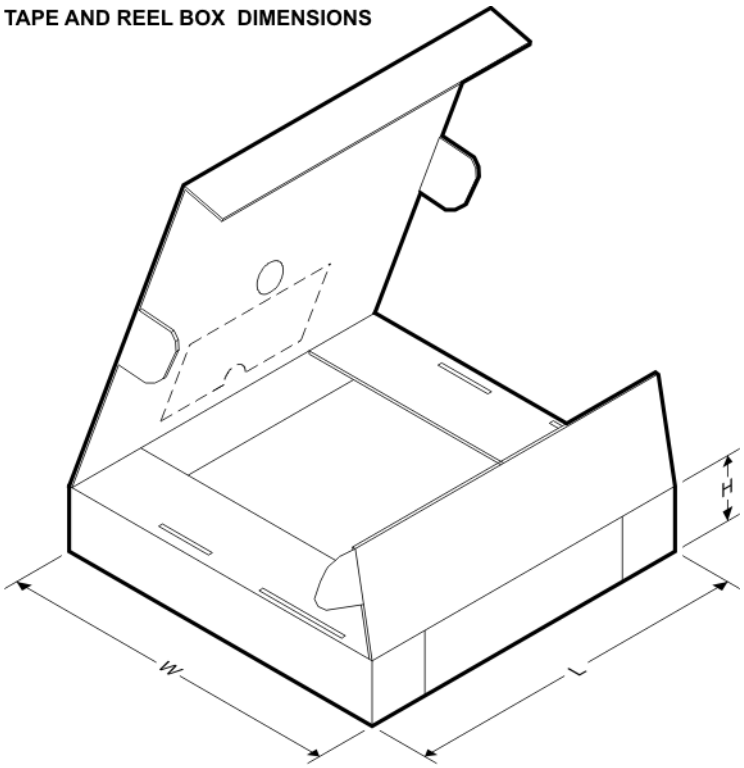
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8844PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

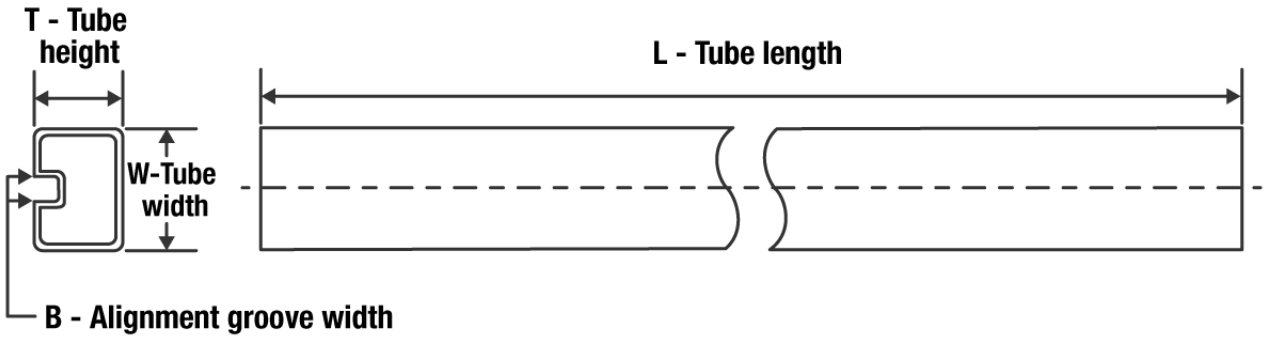
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8844PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8844PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

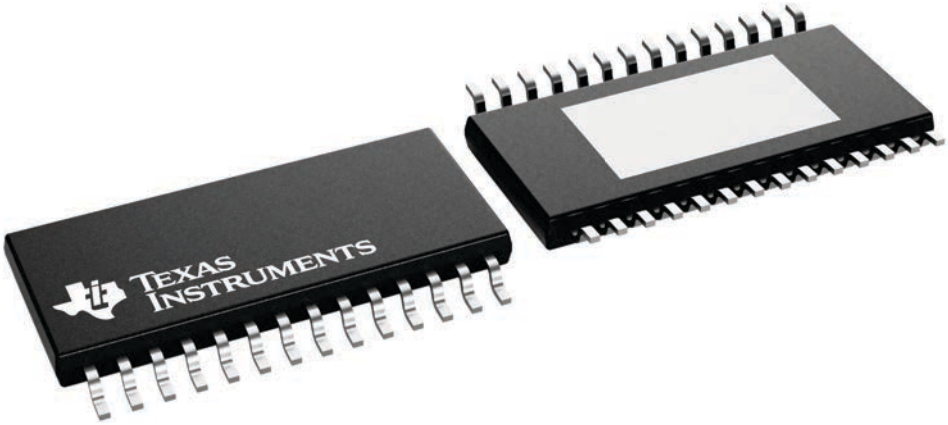
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

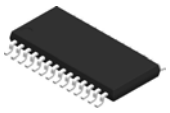
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

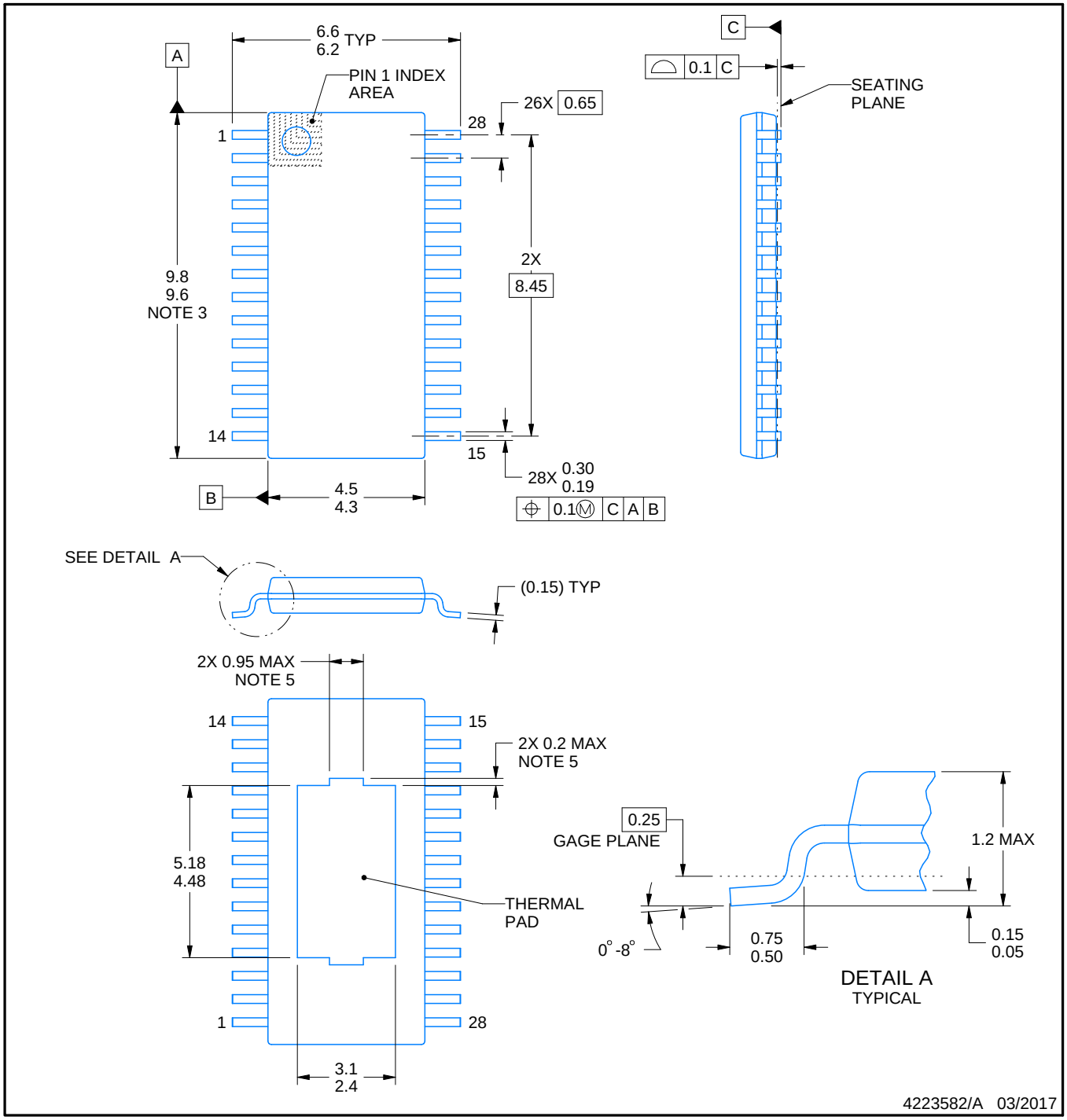
PACKAGE OUTLINE

PWP0028C



PowerPAD™ TSSOP - 1.2 mm max height

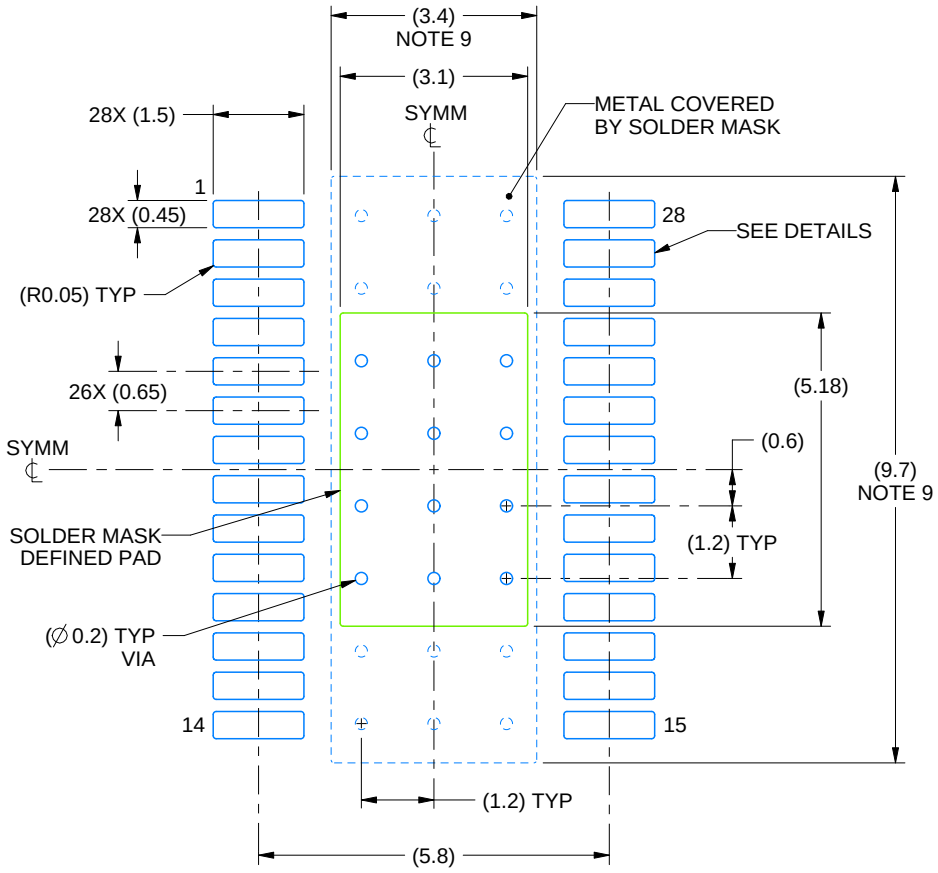
SMALL OUTLINE PACKAGE



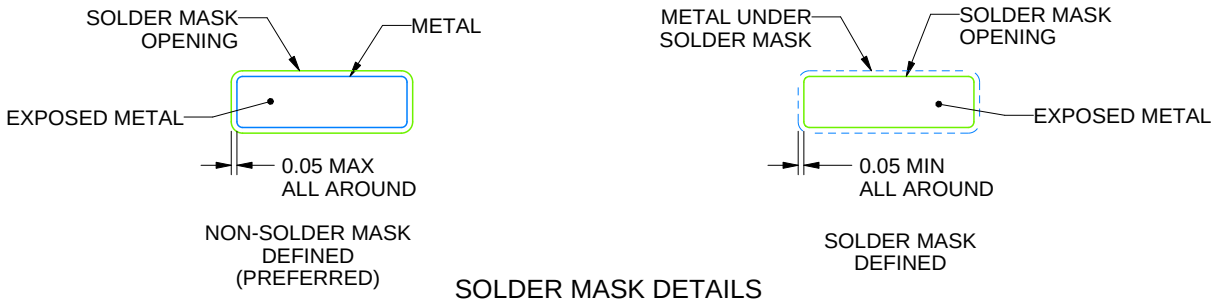
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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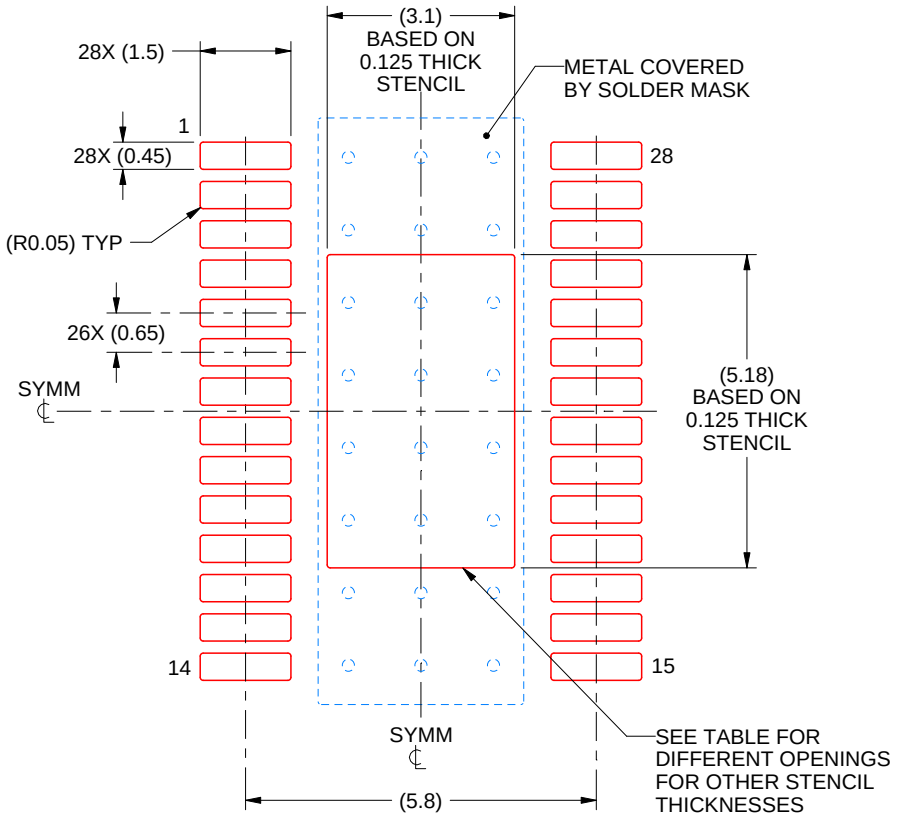
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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