15V/±4A 高效脉宽调制 (PWM) 功率驱动器

查询样品: DRV595

特性

- **±4A** 输出电流
- 宽输入电源电压范围：**4.5V-26V**
- 高效率产生低热量
- 多重开关频率
  - 主器件/从器件同步
  - 高达 **1.2MHz** 开关频率
- 带有高电源抑制比 **(PSRR)** 的反馈电源级架构减少了对于电源供应器 **(PSU)** 的需要
- 单一电源减少了组件数量
- 集成的自保护电路包括过压、欠压、过温和短路保护，并且具有错误报告功能
- 热增强型封装
  - **DAP**（**32** 引脚 **HTSSOP** 封装）
- **-40°C** 至 **85°C** 环境温度范围

应用范围

- 电力线通信 **(PLC)** 驱动器
- 热电冷却器 **(TEC)** 驱动器
- 激光二极管偏置
- 电机驱动器
- 伺服器放大器

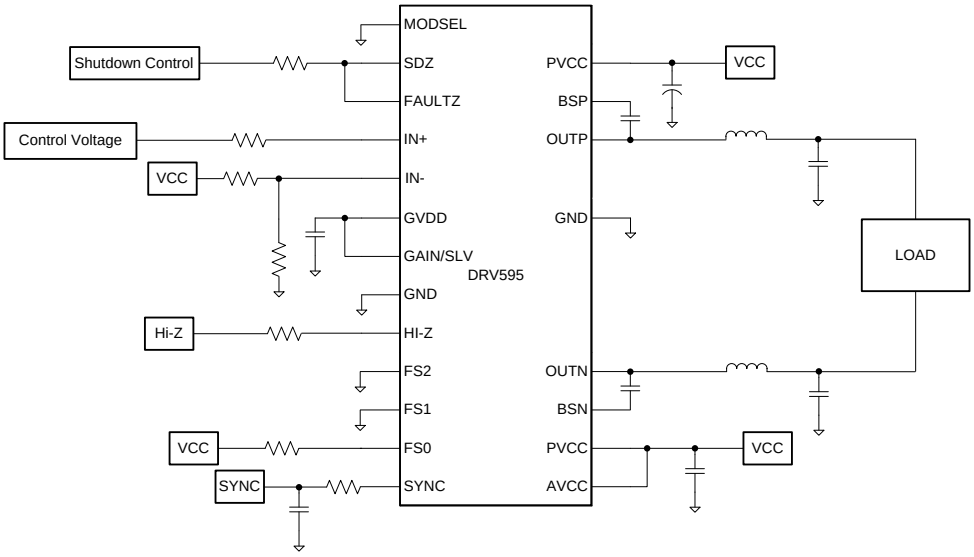
说明

DRV595 是一款高效、高电流功率驱动器，此驱动器非常适合于在电源电压介于 4.5V 至 26V 的系统内驱动多种负载。 PWM 运行和低输出级导通电阻大大降低了放大器内的功率耗散。

DRV595 先进的振荡器/锁相环 (PLL) 电路采用多个开关频率选项；这与一个主控/受控选项一起实现，从而使多个器件同步成为可能。

DRV595 受到短路、过热、过压和欠压保护等的全面保护。 故障被报告给处理器，从而避免过载情况下对器件造成的损坏。

简化应用电路



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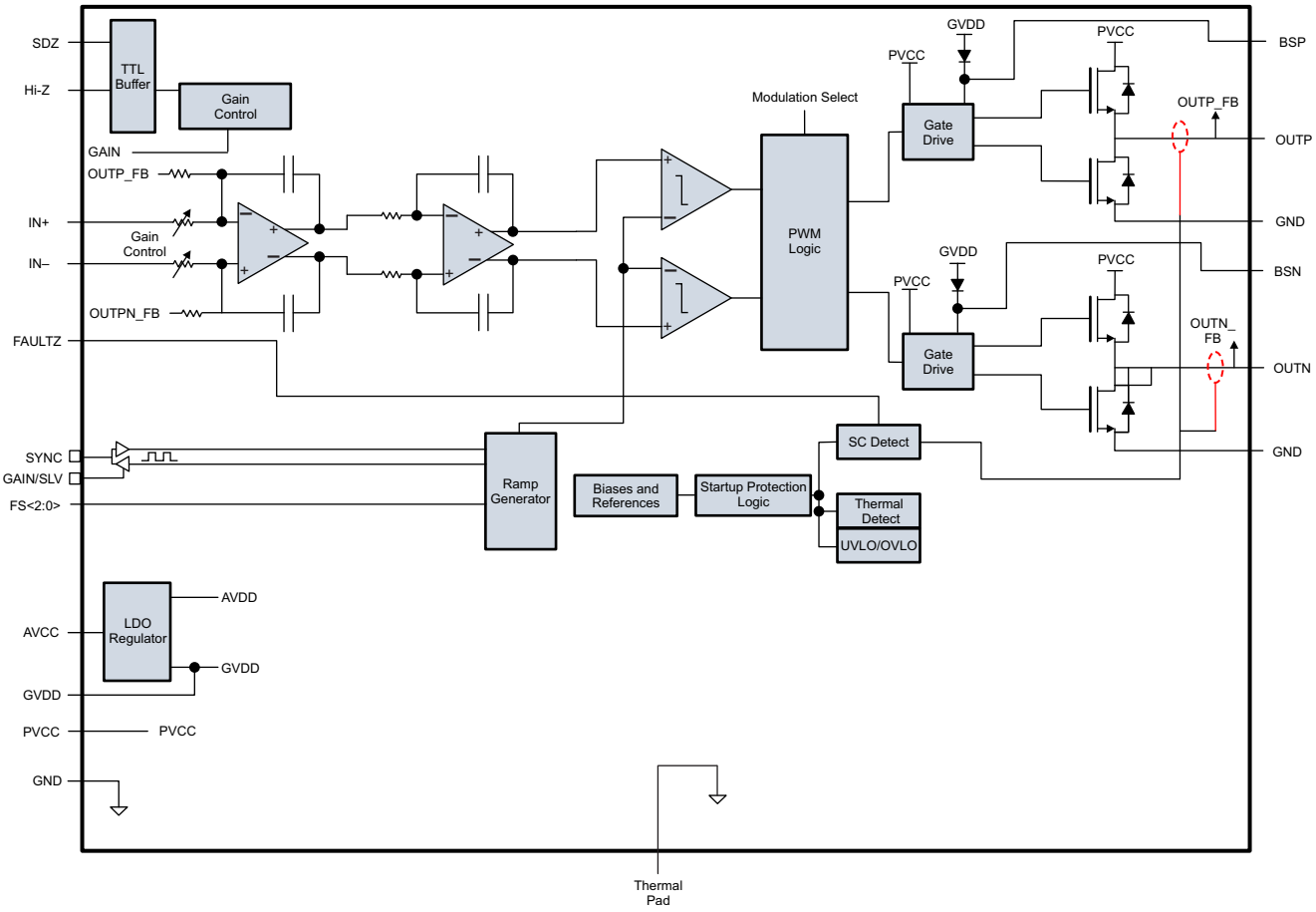
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SYSTEM BLOCK DIAGRAM



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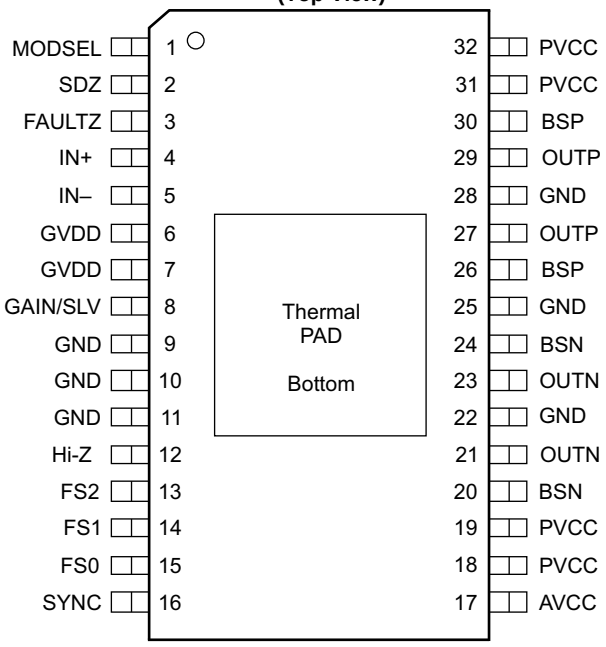
PINOUT CONFIGURATION

DRV595
32-PIN HTSSOP Package (DAP)
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	MODSEL	I	Mode selection logic input (LOW = BD mode, HIGH = 1SPW mode). TTL logic levels with compliance to AVCC.
2	SDZ	I	Shutdown logic input (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
3	FAULTZ	DO	General fault reporting. Open drain. See Table 3 FAULTZ = High, normal operation FAULTZ = Low, fault condition
4	IN+	I	Positive differential input. Biased at 3 V.
5	IN–	I	Negative differential input. Biased at 3 V.
6, 7	GVDD	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the GAIN/SLV resistor divider.
8	GAIN/SLV	I	Selects Gain and selects between Master and Slave mode depending on pin voltage divider.
9, 10, 11	GND	G	Ground
12	Hi-Z	I	Input for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
13	FS2	I	Frequency Selection input, used to select oscillator frequencies from 400kHz to 1200kHz.
14	FS1	I	Frequency Selection input, used to select oscillator frequencies from 400kHz to 1200kHz.
15	FS0	I	Frequency Selection input, used to select oscillator frequencies from 400kHz to 1200kHz.
16	SYNC	DIO	Clock input/output for synchronizing multiple devices. Direction determined by GAIN/SLV terminal.
17	AVCC	P	Analog Supply, can be connected to PVCC for single power supply operation.
18, 19	PVCC	P	Power supply
20, 24	BSN	BST	Boot strap for negative output, connect to 220 nF X5R, or better ceramic cap to OUTN
21	OUTN	PO	Negative output
22	GND	G	Ground
23	OUTN	PO	Negative output
25	GND	G	Ground
26, 30	BSP	BST	Boot strap for positive output, connect to 220 nF X5R, or better ceramic cap to OUTP

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Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
27	OUTP	PO	Positive output
28	GND	G	Ground
29	OUTP	PO	Positive output
31, 32	PVCC	P	Power supply
33	Thermal Pad or PowerPAD™	G	Connect to GND for best system performance. If not connected to GND, leave floating.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Supply voltage, V_{CC}	PV_{CC}, AV_{CC}	–0.3 to 30	V
Input voltage, V_I	IN+, IN–	–0.3 to 6.3	V
	GAIN / SLV, SYNC	–0.3 to GVDD+0.3	V
	SDZ, MODSEL	–0.3 to PVCC+0.3	V
Slew rate, maximum(2)	FS0, FS1, FS2, HI-Z, SDZ, MODSEL	10	V/msec
Operating free-air temperature, T_A		–40 to 85	°C
Operating junction temperature range, T_J		–40 to 150	°C
Storage temperature range, T_{stg}		–40 to 125	°C
Electrostatic discharge: Human body model, ESD		±2	kV
Electrostatic discharge: Charged device model, ESD		±500	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) 100 kΩ series resistor is needed if maximum slew rate is exceeded.

THERMAL INFORMATION

THERMAL METRIC(1)		DRV595 DAP 2 Layer PCB(2) 32 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	22	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	
ψ_{JB}	Junction-to-board characterization parameter	4.8	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) For the PCB layout please see the DRV595EVM user guide.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	PV_{CC}, AV_{CC}	4.5		26	V
V_{IH}	High-level input voltage	FS0, FS1, FS2, Hi-Z, SDZ, SYNC, MODSEL	2			V
V_{IL}	Low-level input voltage	FS0, FS1, FS2, Hi-Z, SDZ, SYNC, MODSEL			0.8	V
V_{OL}	Low-level output voltage	FAULTZ, $R_{PULL-UP}$ = 100 kΩ, PV_{CC} = 26 V			0.8	V
I_{IH}	High-level input current	FS0, FS1, FS2, Hi-Z, SDZ, MODSEL (V_I = 2 V, V_{CC} = 18 V)			50	µA
R_L	Minimum load Impedance	Output filter: L = 10 µH, C = 3.3 µF	1.6			Ω
L_o	Output-filter Inductance	Minimum output filter inductance under short-circuit condition	1			µH

ELECTRICAL CHARACTERISTICS

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 5 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OS} \rvert$	Output offset voltage (measured differentially)	V_I = 0 V, Gain = 36 dB			1.5	15	mV
$\lvert I_{IH} \rvert$	High-level input current	V_{CC} = 24 V, VI = V_{CC}				50	µA
I_{CC}	Quiescent supply current	SDZ = 2 V, No load or filter, PV_{CC} = 12 V			30		mA
		SDZ = 2 V, No load or filter, PV_{CC} = 24 V			50	65	
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	SDZ = 0.8 V, No load or filter, PV_{CC} = 12 V			<50		µA
		SDZ = 0.8 V, No load or filter, PV_{CC} = 24 V			50	65	
$r_{DS(on)}$	Drain-source on-state resistance, measured pin to pin	PV_{CC} = 21 V, I_{out} = 500 mA, T_J = 25°C			60		mΩ
G	Gain (MSTR)	R1 = open, R2 = 20 kΩ	See Table 1	19	20	21	dB
		R1 = 100 kΩ, R2 = 20 kΩ		25	26	27	
		R1 = 100 kΩ, R2 = 39 kΩ		31	32	33	dB
		R1 = 75 kΩ, R2 = 47 kΩ		35	36	37	
G	Gain (SLV)	R1 = 51 kΩ, R2 = 51 kΩ	See Table 1	19	20	21	dB
		R1 = 47 kΩ, R2 = 75 kΩ		25	26	27	
		R1 = 39 kΩ, R2 = 100 kΩ		31	32	33	dB
		R1 = 16 kΩ, R2 = 100 kΩ		35	36	37	
	Full power bandwidth				60		kHz
t_{on}	Turn-on time	SDZ = 2 V			10		ms
t_{OFF}	Turn-off time	SDZ = 0.8 V			2		µs
GVDD	Gate drive supply	IGVDD < 200 µA		6.4	6.9	7.4	V
V_O	Output voltage (measured differentially)	I_O = ±1 A, $r_{ds(on)}$ = 60 mΩ			11.85		V
		I_O = ±3 A, $r_{ds(on)}$ = 60 mΩ			11.55		
PSRR	Power supply ripple rejection	200 mV_{PP} ripple at 1 kHz, Gain = 20 dB, Inputs AC-coupled to GND			–70		dB
V_{ICM}	Input common-mode range			0.5		4.5	V
CMRR	Common-mode rejection ratio	PVCC = 12 V			–56		dB
f_{OSC}	Oscillator frequency (with PWM duty cycle < 96%)	FS2=0, FS1=0, FS0=0		376	400	424	kHz
		FS2=0, FS1=0, FS0=1		470	500	530	
		FS2=0, FS1=1, FS0=0		564	600	636	
		FS2=0, FS1=1, FS0=1		940	1000	1060	
		FS2=1, FS1=0,FS0=0		1128	1200	1278	
		FS2=1, FS1=0, FS0=1		Reserved			
		FS2=1,FS1=1, FS0=0					
		FS2=1, FS1=1,FS0=1					

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ELECTRICAL CHARACTERISTICS (continued)

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V to 24 V, R_L = 5 Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output resistance in shutdown	SDZ = 0.8 V		60		kΩ
Power-on threshold			4.1		V
Power-off threshold			28		V
Thermal trip point			150+		°C
Thermal hysteresis			15		°C
Over current trip point			7.5		A

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TYPICAL CHARACTERISTICS

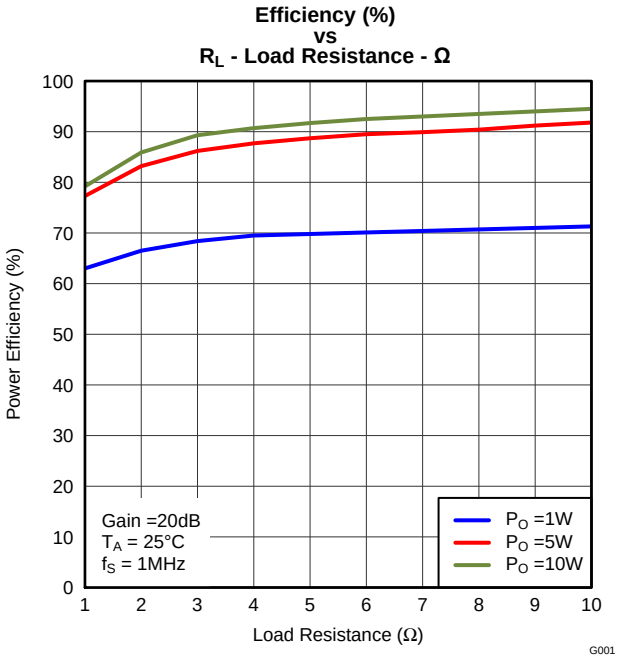

Figure 1.

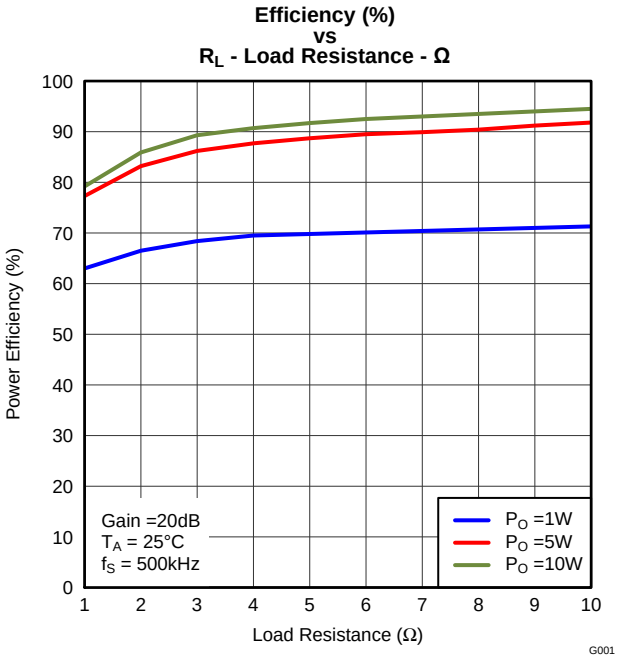

Figure 2.

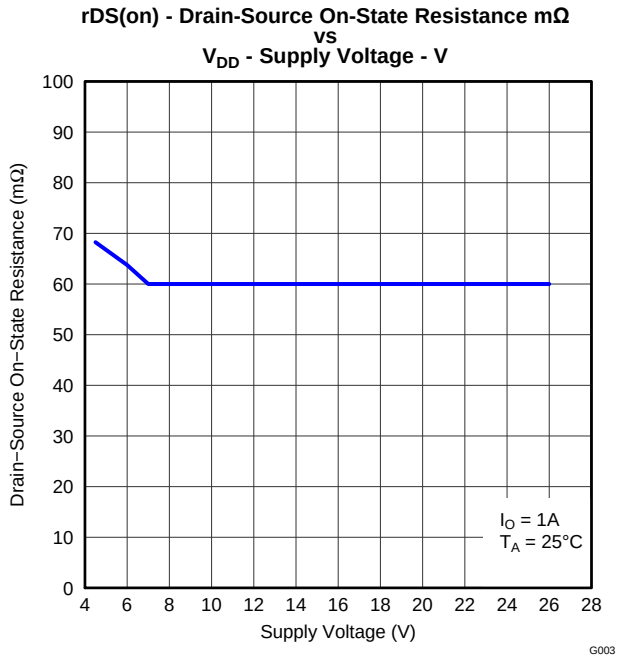

Figure 3.

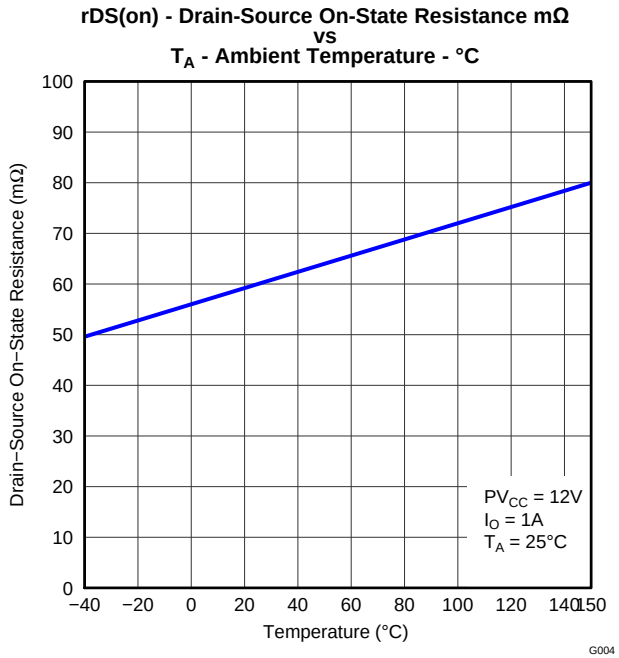

Figure 4.

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TYPICAL CHARACTERISTICS (continued)

I_q - Supply Current - mA
vs
V_{DD} - Supply Voltage - V

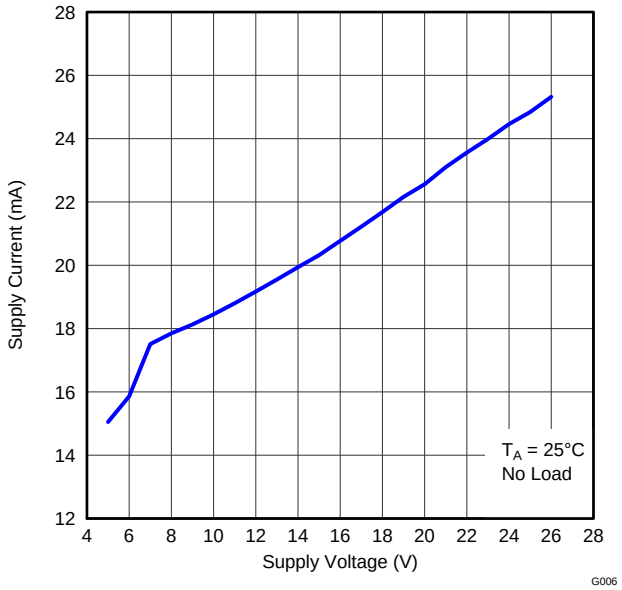

Figure 5.

PSRR-Supply Ripple Rejection Ratio (dB)
vs
f - Frequency - Hz

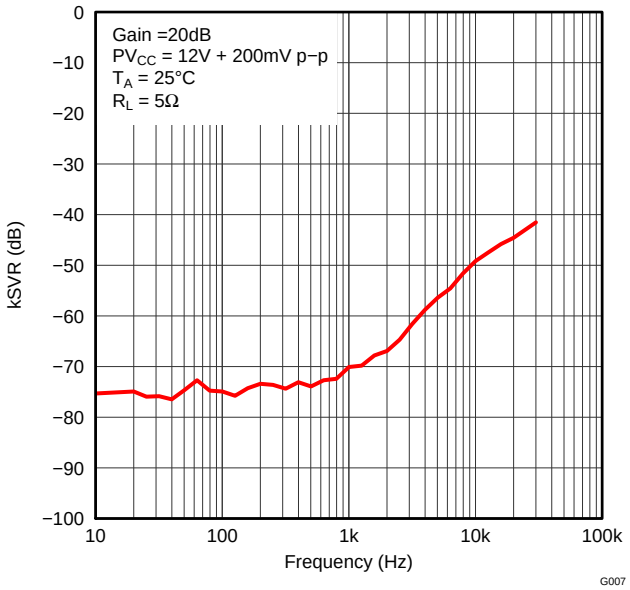

Figure 6.

PSRR-Supply Ripple Rejection Ratio (dB)
vs
f - Frequency - Hz

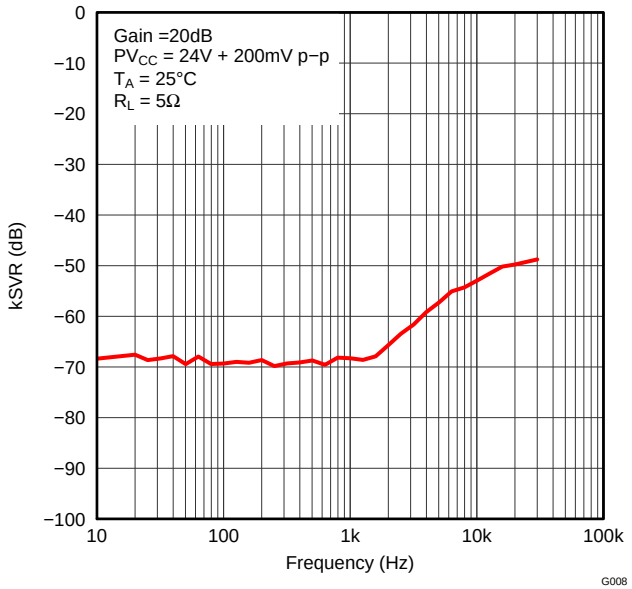

Figure 7.

Gain - V/V; Phase - °
vs
f - Frequency - Hz

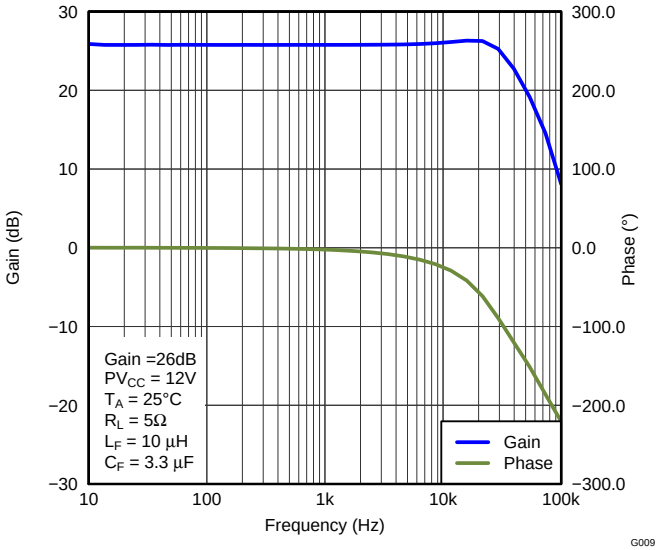

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

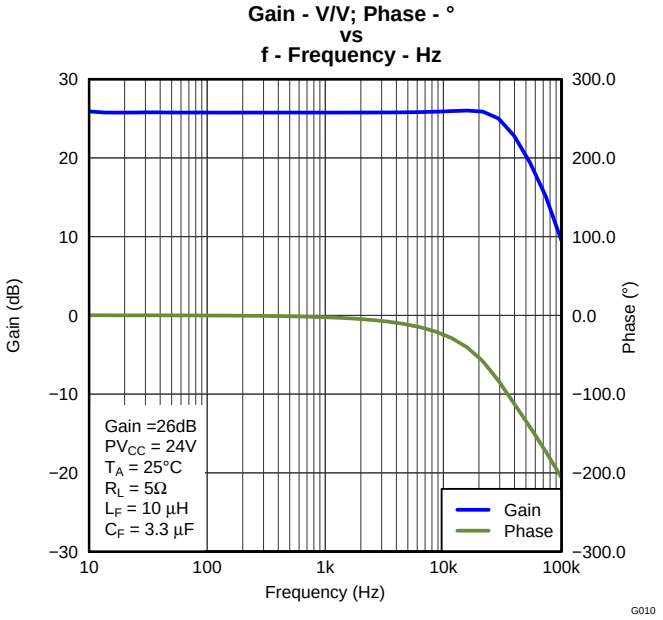

Figure 9.

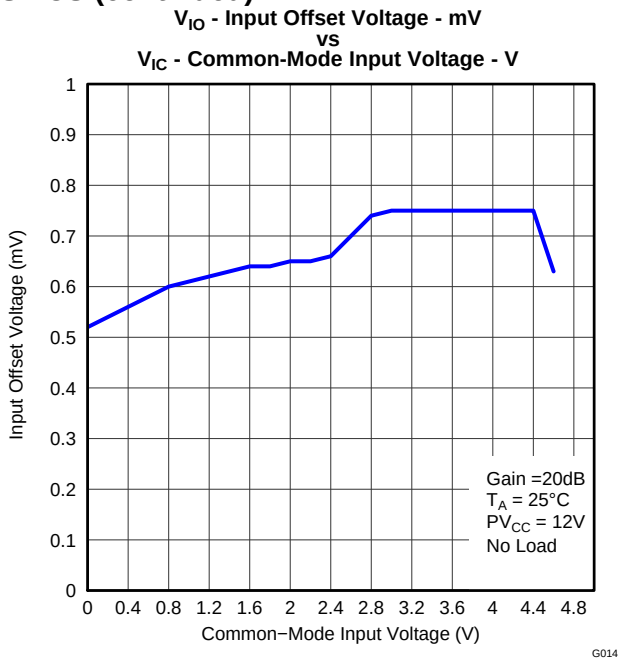

Figure 10.

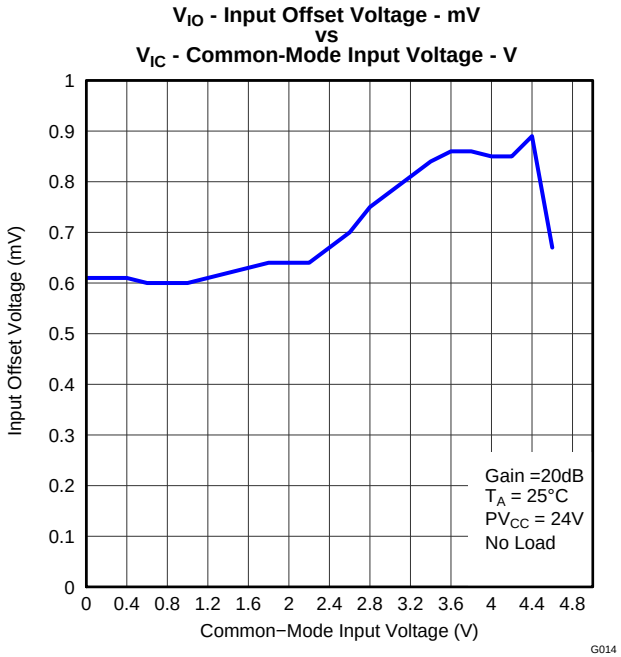

Figure 11.

APPLICATION INFORMATION

OUTPUT FILTER CONSIDERATIONS

The DRV595 can be used to drive a TEC element. The typical circuit used for this application is to have two feedback loops – one for constant current, and the second to monitor the temperature, and provide adjustments to keep a constant temperature on the laser diode. An error amplifier is used to combine the two feedback loops, along with a control signal from the system. The output of the error amplifier is then fed into the DRV595.

An output filter needs to be used to prevent excessive ripple from reaching the TEC element. Some TEC elements may be damaged by ripple; design the filter using the TEC specification to reduce the switching waveform enough to prevent TEC damage. This filter also reduces the amount of electrical noise coupled onto the TEC element.

For most applications, a second-order Butterworth low-pass filter with the cut-off frequency set to a few kilohertz should be sufficient. See Figure 12 for example filter designed with Equation 2, Equation 3, and Equation 4 .

Second-Order Butterworth LPF Transfer Function

$$H(s) = \frac{1}{s^2 + \sqrt{2}s + 1} \tag{1}$$

Using Half-Circuit Analysis

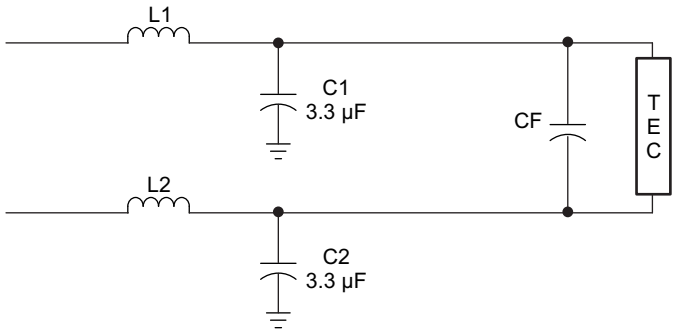

Figure 12. Second Order Butterworth Low-Pass Filter Configuration

$$L_x = \frac{\sqrt{2} \times R_L}{2\omega_o} \tag{2}$$

$$2 \times C_F = \frac{\sqrt{2}}{2 \times \frac{R_L}{2} \times \omega_0} \tag{3}$$

$$\omega_0 = 2\pi \times f \tag{4}$$

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DEVICE INFORMATION

TYPICAL APPLICATION

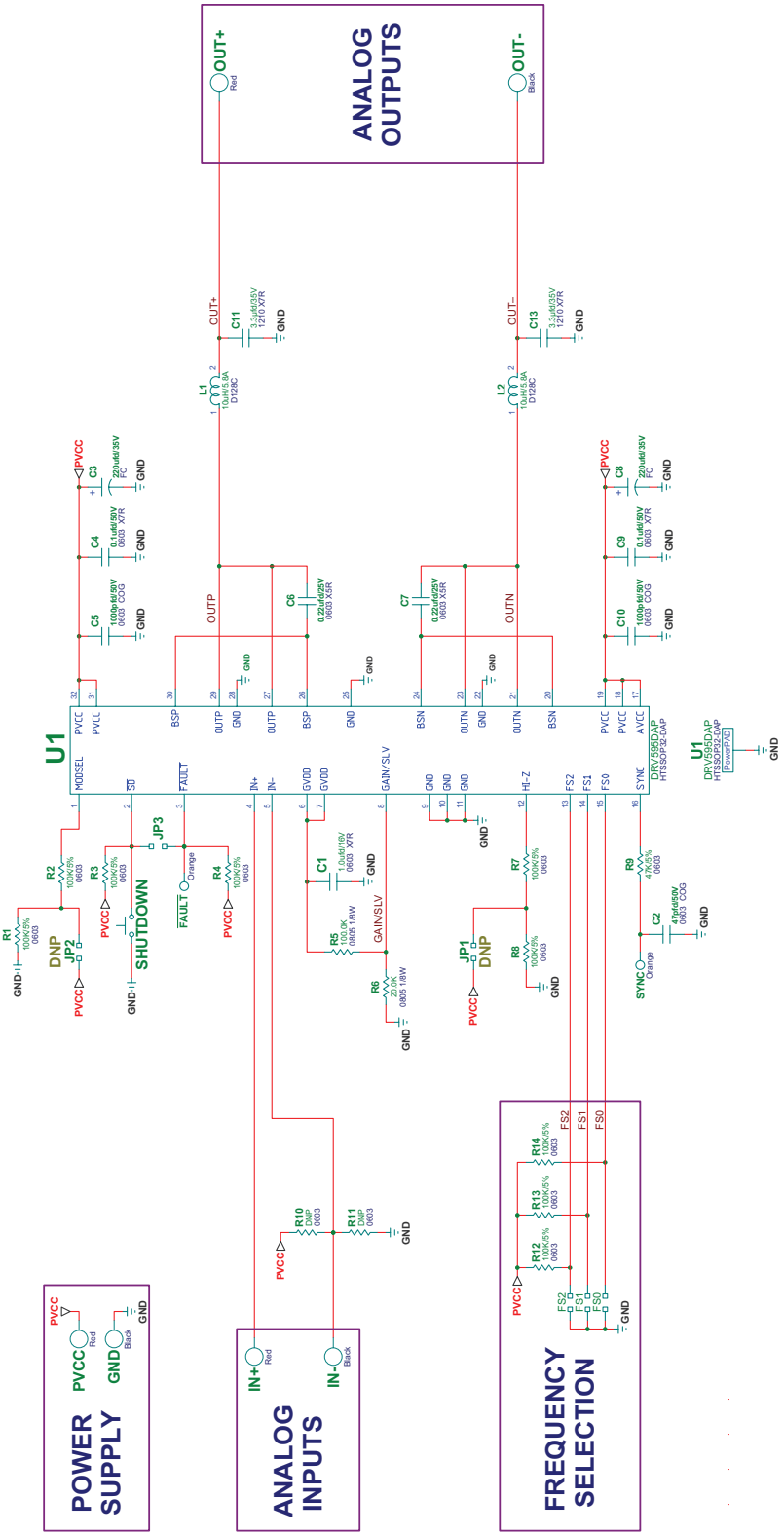


Figure 13. Schematic

START-UP SEQUENCING

To ensure proper operation on power up, wait 10ms after PV_{CC} and AV_{CC} are stable before using the analog inputs, IN– and IN+. Figure 14 illustrates this sequence.

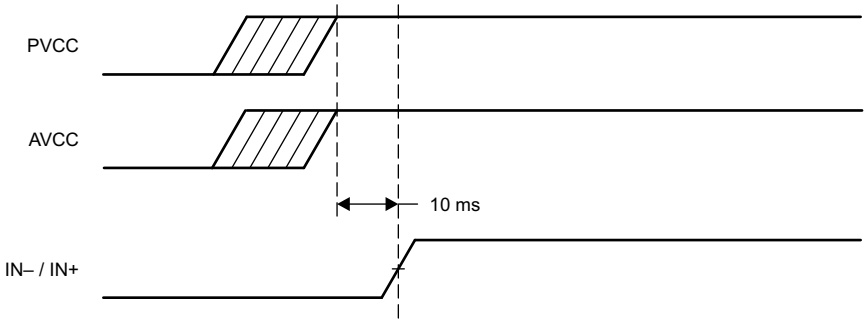


Figure 14. Start-Up Sequencing (1)

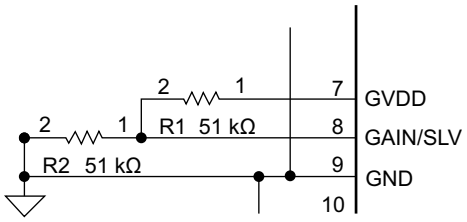
(1) NOTE: The timing relationship between PVCC assertion and AVCC assertion is not critical.

GAIN SETTING AND MASTER / SLAVE

The gain of the DRV595 is set by the voltage divider connected to the GAIN/SLV control pin. Master or slave mode is also controlled by the same pin. An internal ADC is used to detect the 4 input states. The first four states set the DRV595 in Master mode with gains of 20, 26, 32, 36 dB respectively, while the next four states set the DRV595 in Slave mode with gains of 20, 26, 32, 36 dB respectively. The gain setting is latched during power-up and cannot be changed while the device is powered. Table 1 shows the recommended resistor values for each mode and gain combination:

Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GVDD)	R2 (to GND)	INPUT IMPEDANCE
Master	20 dB	OPEN	20 kΩ	60 kΩ
Master	26 dB	100 kΩ	20 kΩ	30 kΩ
Master	32 dB	100 kΩ	39 kΩ	15 kΩ
Master	36 dB	75 kΩ	47 kΩ	9 kΩ
Slave	20 dB	51 kΩ	51 kΩ	60 kΩ
Slave	26 dB	47 kΩ	75 kΩ	30 kΩ
Slave	32 dB	39 kΩ	100 kΩ	15 kΩ
Slave	36 dB	16 kΩ	100 kΩ	9 kΩ



In Master mode, the SYNC terminal is an output, in Slave mode, the SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD.

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INPUT IMPEDANCE

The DRV595 input stage is a fully differential input stage and the input impedance changes with the gain setting from 9 kΩ at 36 dB gain to 60 kΩ at 20 dB gain. Table 1 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so the minimum value will be higher than 7.2 kΩ.

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE
20 dB	60 kΩ
26 dB	30 kΩ
32 dB	15 kΩ
36 dB	9 kΩ

START-UP/SHUTDOWN OPERATION

The DRV595 employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of non use for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low will put the outputs to Hi-Z and the amplifier to enter a low-current state. It is not recommended to leave SDZ unconnected, because amplifier operation would be unpredictable.

GVDD SUPPLY

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the GAIN/SLV voltage divider. Decouple GVDD with a X5R ceramic 1 µF capacitor to GND. The GVDD supply is not intended to be used as an external supply. It is recommended to limit the current consumption by using resistor voltage dividers for GAIN/SLV of 100 kΩ or more.

BSP AND BSN CAPACITORS

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220 nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. (See the application circuit diagram in Figure 13.) The bootstrap capacitors connected between the BSx pins and corresponding output pins function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

DIFFERENTIAL OR SINGLE-ENDED INPUTS

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the DRV595 with a differential source, connect the positive lead of the signal source to the IN+ input and the negative lead of the signal source to the IN– input. To use the DRV595 with a single-ended source, use a voltage divider to bias IN- to 3.0V, and apply the single-ended signal to IN+.

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DEVICE PROTECTION SYSTEM

The DRV595 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against permanent failures due to short circuits, overload, over temperature, and under-voltage. The FAULTZ pin will signal if an error is detected according to the fault table below:

Table 3. Fault Reporting

FAULT	TRIGGERING CONDITION (typical value)	FAULTZ	ACTION	LATCHED/SELF-CLEARING
Over Current	Output short or short to PVCC or GND	Low	Output high impedance	Latched
Over Temperature	T_j > 150°C	Low	Output high impedance	Latched
Under Voltage on PVCC	PVCC < 4.5V	–	Output high impedance	Self-clearing
Over Voltage on PVCC	PVCC > 27V	–	Output high impedance	Self-clearing

SHORT-CIRCUIT PROTECTION AND AUTOMATIC RECOVERY FEATURE

The DRV595 has protection from over current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULTZ pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SDZ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the short-circuit protection latch.

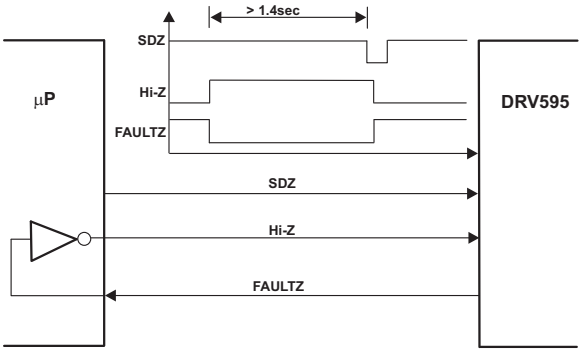

Figure 15. Timing Requirement for SDZ

THERMAL PROTECTION

Thermal protection on the DRV595 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the FAULTZ terminal as a low state.

If automatic recovery from the thermal protection latch is desired, connect the FAULTZ pin directly to the SDZ pin. This allows the FAULTZ pin function to automatically drive the SDZ pin low which clears the thermal protection latch.

DRV595 MODULATION SCHEME

The DRV595 has the option of running in either BD modulation or 1SPW modulation; this is set by the MODSEL pin.

MODSEL = GND: BD-modulation

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This is a modulation scheme that allows for smaller ripple current through the TEC load. Each output switches from 0 volts to the supply voltage. With no input, OUTP and OUTN are in phase with each other so that there is little or no current in the load. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

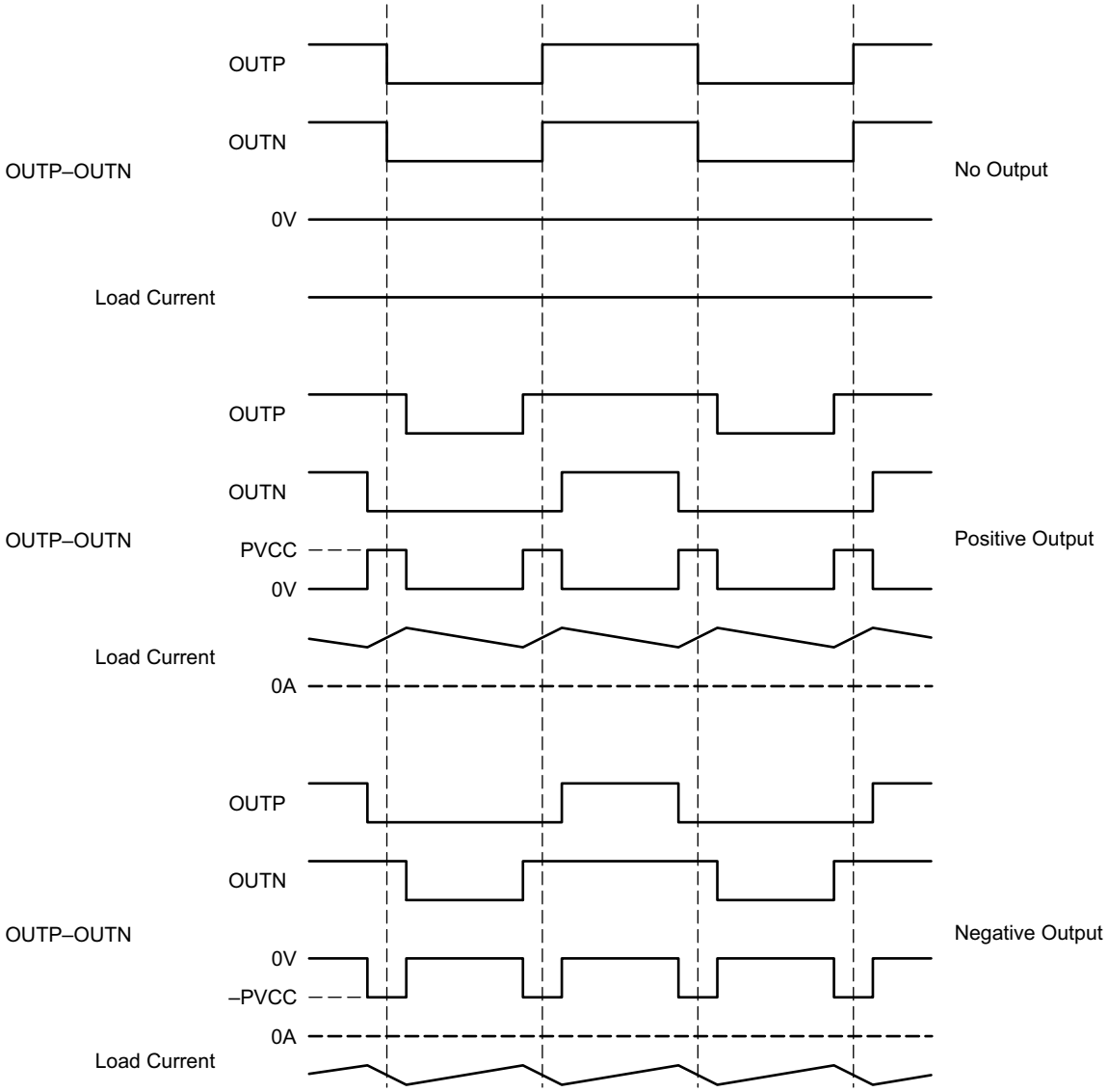

Figure 16. BD Mode Modulation

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MODSEL = HIGH: 1SPW-modulation

The 1SPW mode alters the normal modulation scheme in order to achieve higher efficiency with a slight penalty in ripple current and more attention required in the output filter selection. In 1SPW mode the outputs operate at ~15% modulation during idle conditions. When an input signal is applied one output decreases and one increases. The decreasing output signal quickly rails to GND at which point all the modulation takes place through the rising output. The result is that often only one output is switching. Efficiency is improved in this mode due to the reduction of switching losses. The resulting output signal at each half output has a discontinuity each time the output rails to GND. This can cause ringing in the output filter unless care is taken in the selection of the filter components and type of filter used.

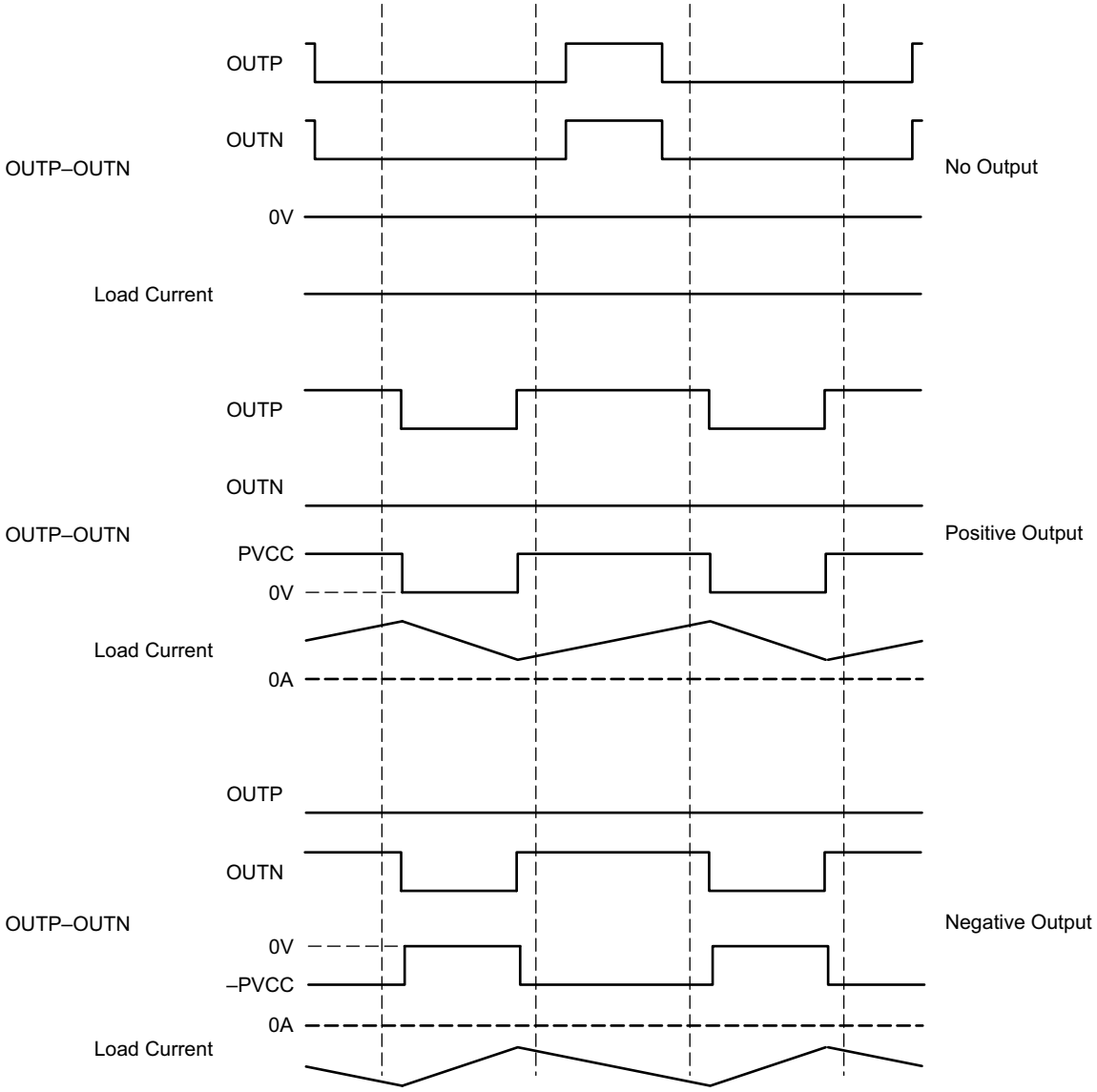

Figure 17. 1SPW Mode Modulation

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POWER DISSIPATION AND MAXIMUM AMBIENT TEMPERATURE

Though the DRV595 is much more efficient than traditional linear solutions, the power drop across the on-resistance of the output transistors does generate some heat in the package, which may be calculated as shown in Equation 5:

$$P_{DISS} = \left(I_{OUT}\right)^2 \times r_{DS(on),\ total} \quad (5)$$

For example, at the maximum output current of 3 A through a total on-resistance of 60 mΩ (at T_J = 25°C), the power dissipated in the package is 1.1 W.

Calculate the maximum ambient temperature using Equation 6:

$$T_A = T_J - \left(\theta_{JA} \times P_{DISS}\right) \quad (6)$$

PRINTED-CIRCUIT BOARD (PCB LAYOUT)

It is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (100 µF or greater) bulk power supply decoupling capacitors should be placed near the DRV595 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1 nF and a larger mid-frequency cap of value between 100 nF and 1 µF also of good quality to the PVCC connections at each end of the chip.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the DRV595.

For an example layout, see the DRV595 Evaluation Module (DRV595EVM) User Manual. Both the EVM user's manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

REVISION HISTORY

Changes from Original (December 2012) to Revision A — **Page**

- 将表题从：15V/±3A 高效脉宽调制 (PWM) 功率驱动器改为：15V/±4A 高效脉宽调制 (PWM) 功率驱动器 1
- 将特性从：±3A 输出电流改为：±4A 输出电流 1
- Changed the Over current trip point TYP value From: 3 A To: 7.5 A 6

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV595DAP	ACTIVE	HTSSOP	DAP	32	46	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV595	Samples
DRV595DAPR	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV595	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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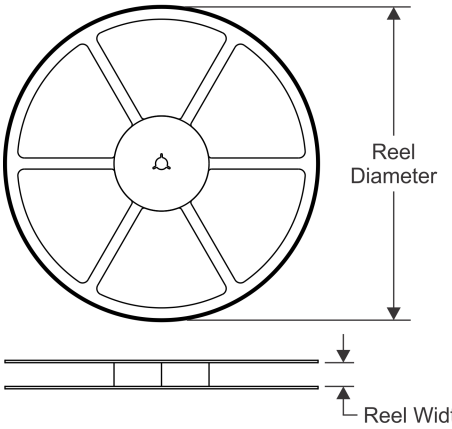
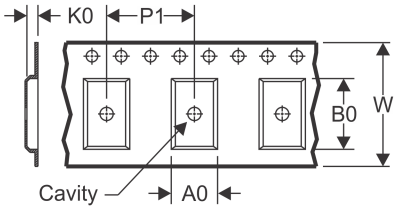
TAPE AND REEL INFORMATION

REEL DIMENSIONS

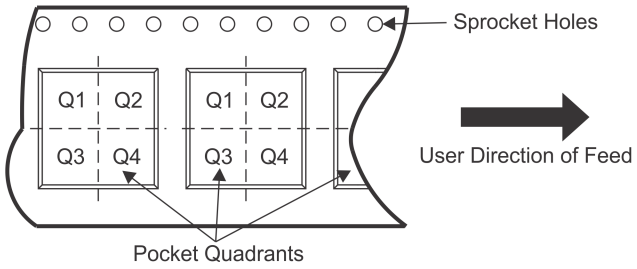


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

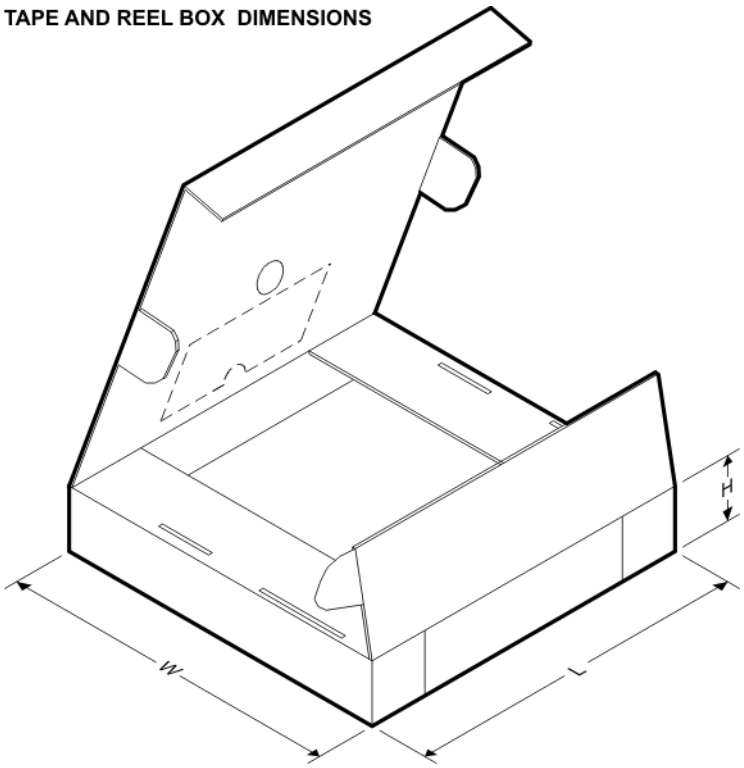
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV595DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

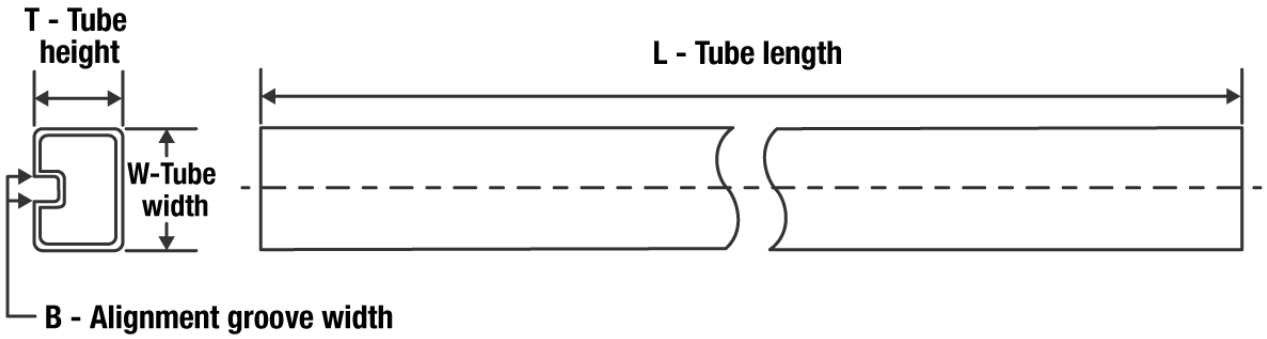
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV595DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV595DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

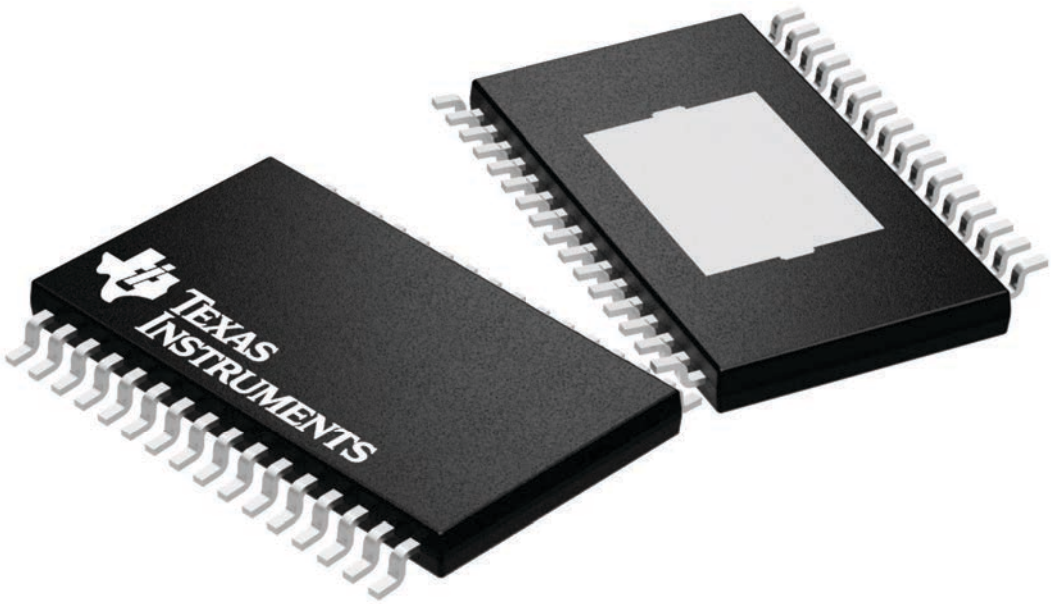
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

8.1 x 11, 0.65 mm pitch

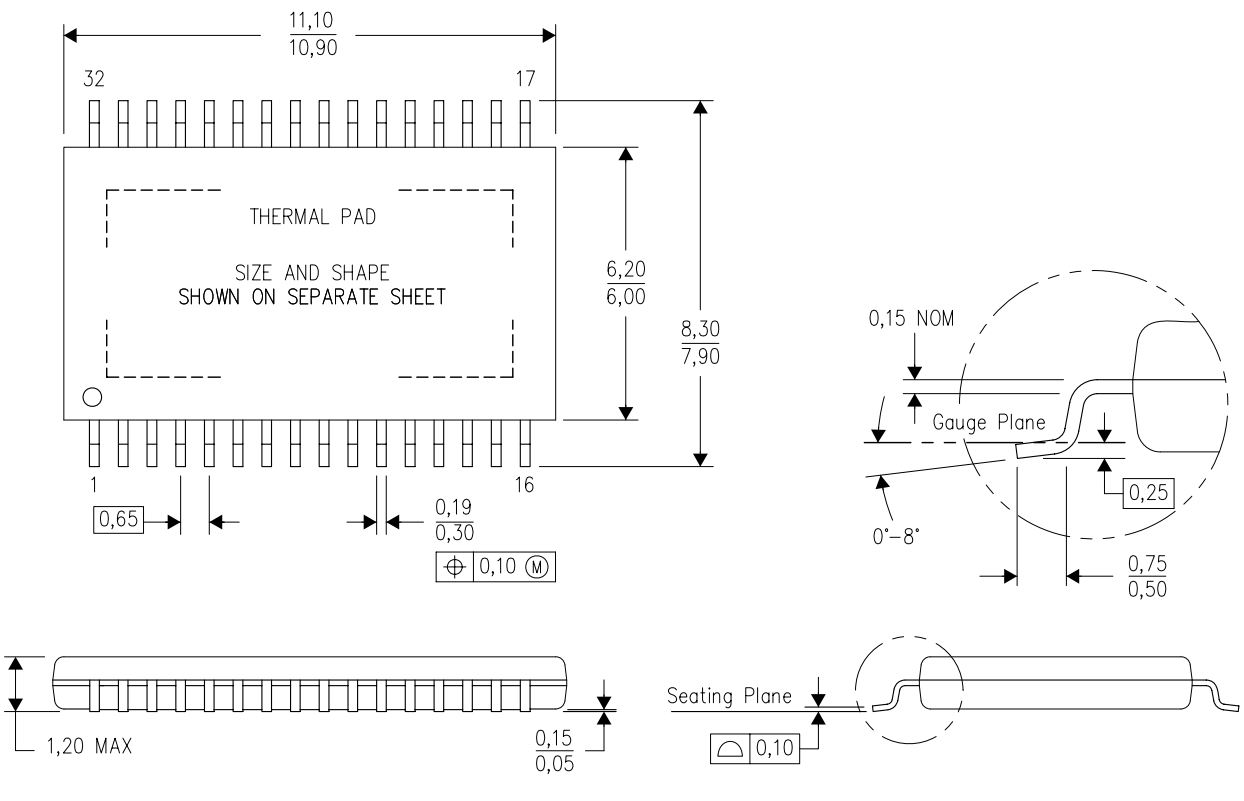
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

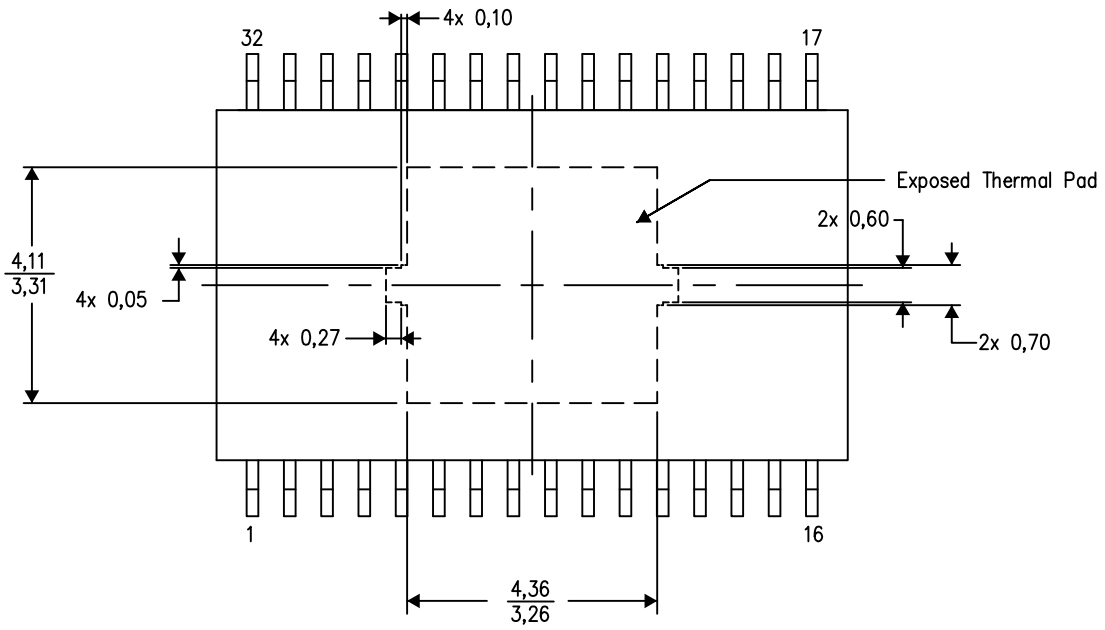
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

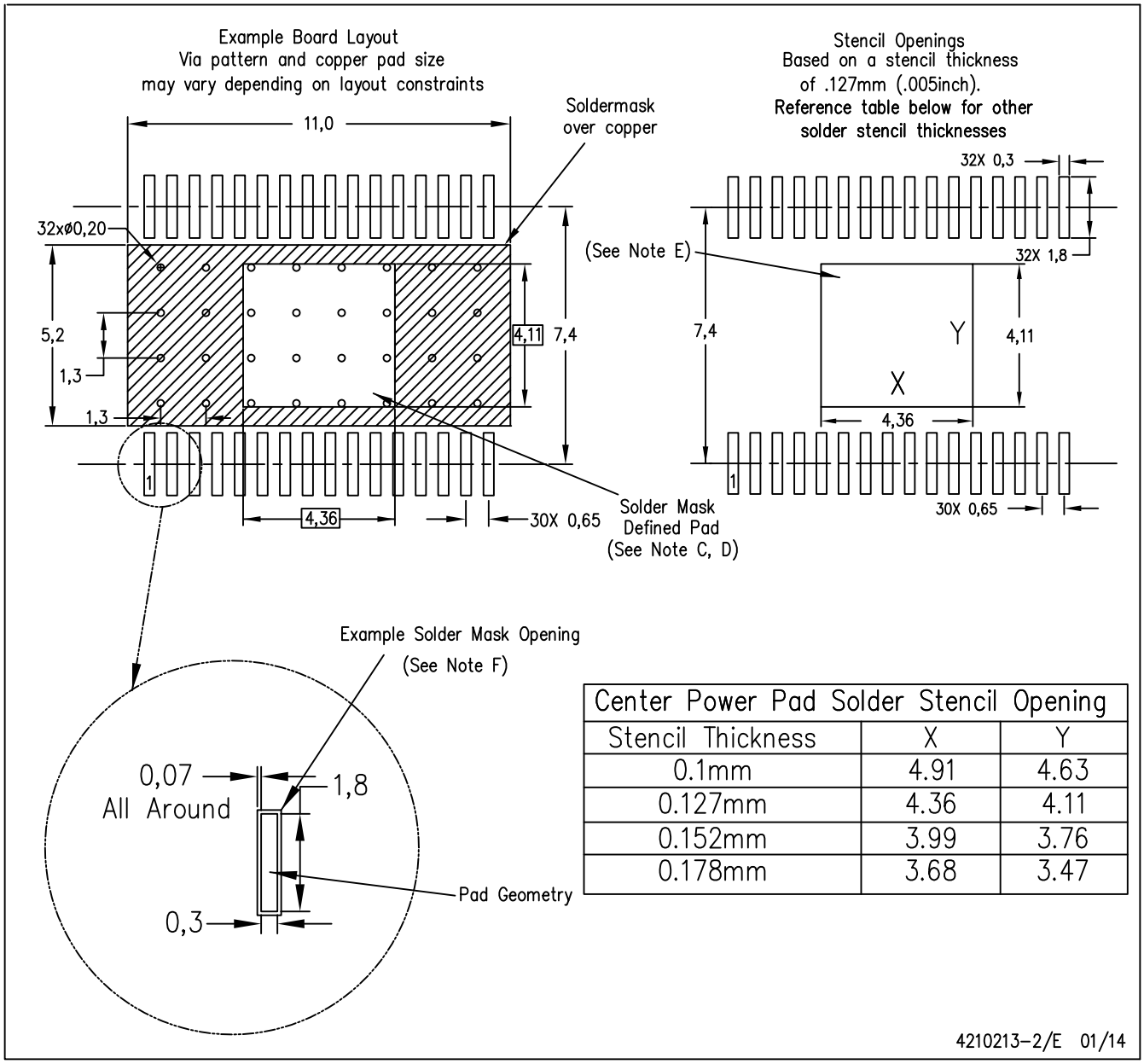
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments.

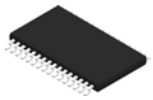
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

PowerPAD is a trademark of Texas Instruments

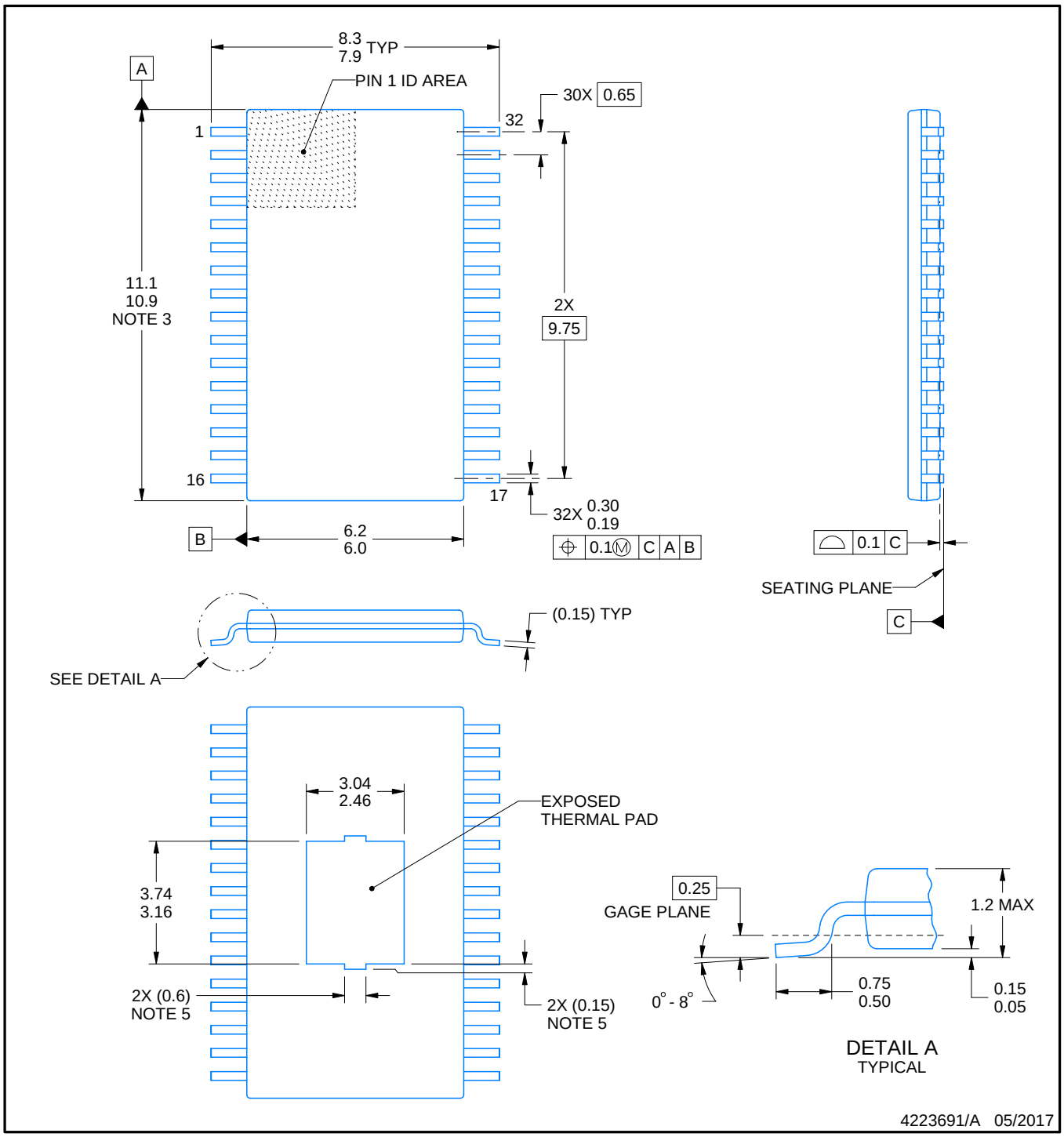


PACKAGE OUTLINE

DAP0032C

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



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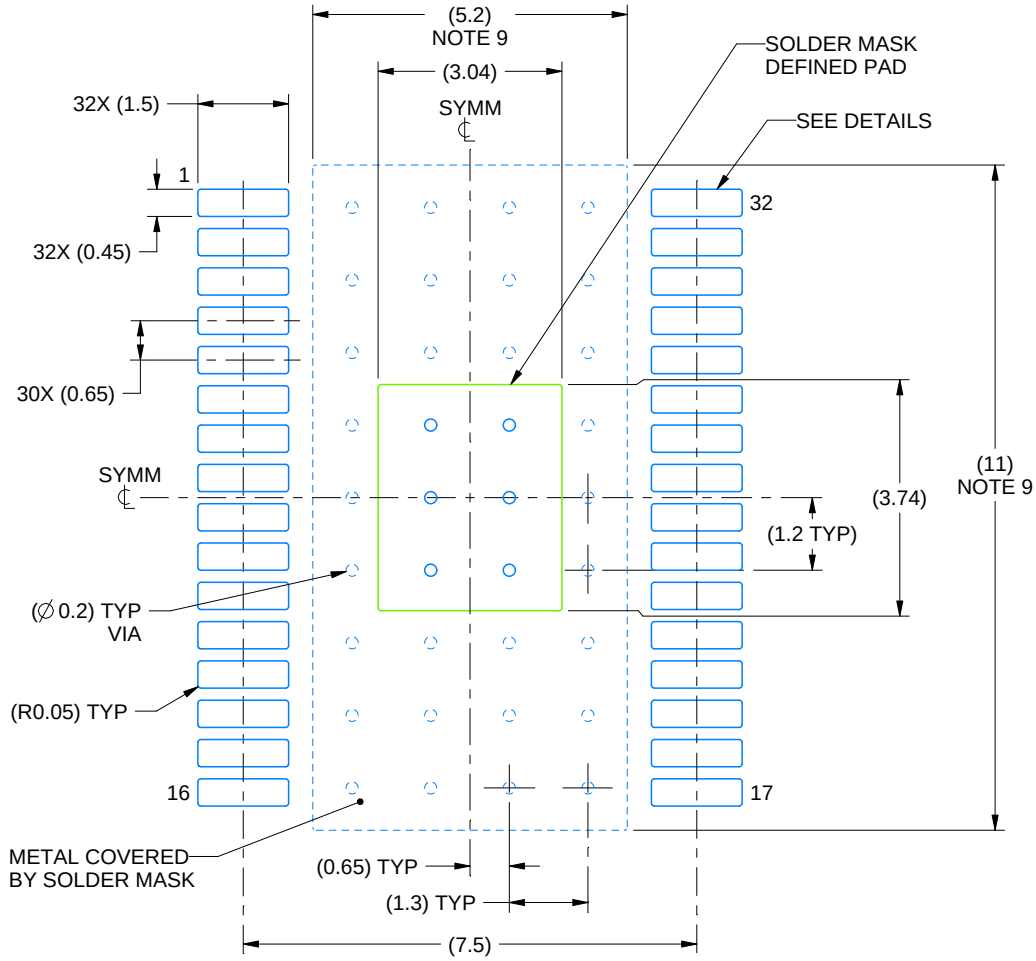
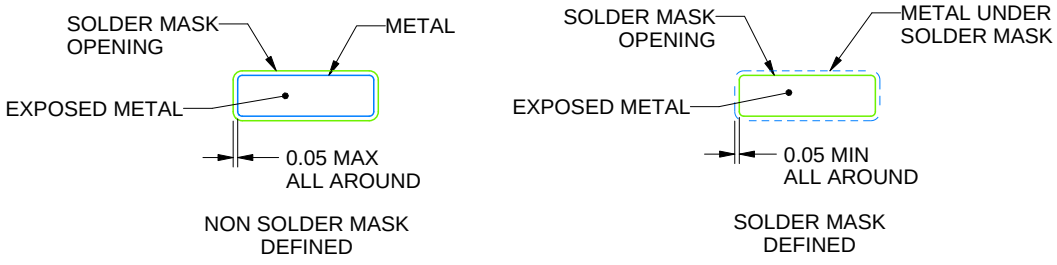
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

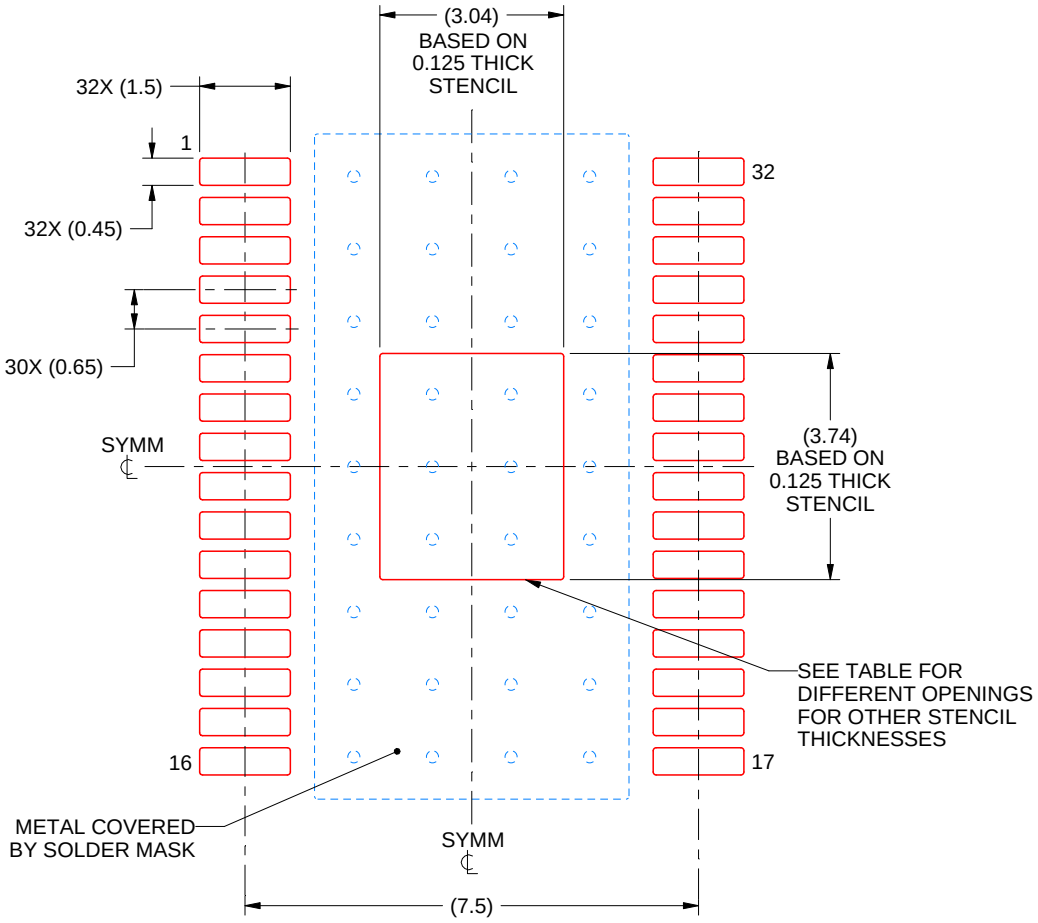


SOLDER MASK DETAILS
NOT TO SCALE

4223691/A 05/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.40 X 4.18
0.125	3.04 X 3.74 (SHOWN)
0.15	2.78 X 3.41
0.175	2.57 X 3.16

4223691/A 05/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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