OPA820 Unity-Gain Stable, Low-Noise, Voltage-Feedback Operational Amplifier

1 Features

- High Bandwidth (240 MHz, G = 2)
- High-Output Current (±110 mA)
- Low-Input Noise (2.5 nV/√Hz)
- Low-Supply Current (5.6 mA)
- Flexible Supply Voltage:
  - Dual ±2.5 V to ±6 V
  - Single 5 V to 12 V
- Excellent DC Accuracy:
  - Maximum 25°C Input Offset Voltage = ±750 µV
  - Maximum 25°C Input Offset Current = ±400 nA

2 Applications

- Low-Cost Video Line Drivers
- ADC Preamplifiers
- Active Filters
- Low-Noise Integrators
- Portable Test Equipment
- Optical Channel Amplifiers
- Low-Power, Baseband Amplifiers
- CCD Imaging Channel Amplifiers
- OPA650 and OPA620 Upgrade

3 Description

The OPA820 device provides a wideband, unity-gain stable, voltage-feedback amplifier with a very-low input-noise voltage and high-output current using a low 5.6-mA supply current. At unity-gain, the OPA820 device gives more than 800-MHz bandwidth with less than 1-dB peaking. The OPA820 device complements this high-speed operation with excellent DC precision in a low-power device. A worst-case input-offset voltage of ±750 µV and an offset current of ±400 nA provide excellent absolute DC precision for pulse amplifier applications.

Minimal input and output voltage-swing headroom allow the OPA820 device to operate on a single 5-V supply with more than 2-V_{PP} output swing. While not a rail-to-rail (RR) output, this swing supports most emerging analog-to-digital converter (ADC) input ranges with lower power and noise than typical RR output op amps.

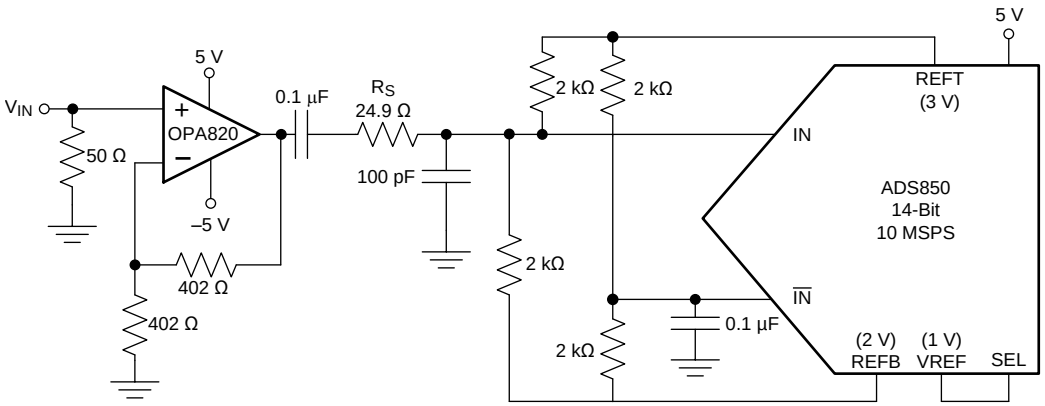
Exceptionally low dG/dP (0.01% or 0.03°) supports low-cost composite-video line-driver applications. Existing designs can use the industry-standard pinout, 8-pin SOIC package while emerging high-density portable applications can use the 5-pin SOT-23. Offering the lowest thermal impedance of the industry in a SOT package, along with full specification over both the commercial and industrial temperature ranges, provides solid performance over a wide temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA820	SOIC (8)	4.90 mm × 3.91 mm
	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

AC-Coupled, 14-Bit ADS850 Interface



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (August 2008) to Revision D **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted *Ordering Information* table; see *Package Option Addendum* at the end of the data sheet ... 1
- Deleted Lead temperature (soldering, 300°C maximum) from *Absolute Maximum Ratings* table ... 3
- Added *Thermal Information* table ... 4
- Changed Open-loop voltage gain test condition in *Electrical Characteristics: V_S = ±5 V* table From: V_O To: V_{CM} ... 5
- Changed Open-loop voltage gain test condition in *Electrical Characteristics: V_S = 5 V* table From: V_O To: V_{CM} ... 8
- Changed R_2 From: 505 Ω To: 517 Ω, C_1 From: 150 pF To: 100 pF, and C_2 From: 100 pF To: 160 pF in *5-MHz Butterworth Low-Pass Active Filter* image ... 28

Changes from Revision B (March 2006) to Revision C **Page**

- Changed Storage Temperature minimum value from –40°C to –65°C ... 3

Changes from Revision A (July 2004) to Revision B **Page**

- Changed the board part number in the *Design-In Tools* section ... 37

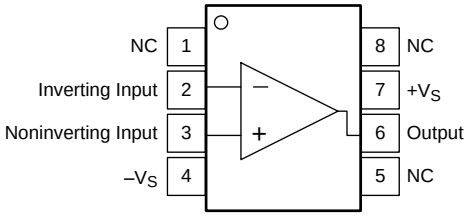
5 Device Comparison Table

Table 1. Related Products

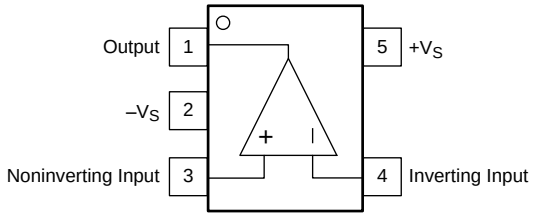
SINGLE CHANNEL	DUAL CHANNEL	TRIPLE CHANNEL	QUAD CHANNEL	FEATURES
OPA354	OPA2354	—	OPA4354	CMOS RR output
OPA690	OPA2690	OPA3690	—	High-slew rate
—	OPA2652	—	—	8-Pin SOT23
—	OPA2822	—	—	Low noise
—	—	—	OPA4820	Quad OPA820

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOIC	SOT-23		
Disable	8	—	I	Disable the op amp (Low = Disable; High = Enable)
Inverting Input	2	4	I	Inverting input
NC	1, 5, 8	—	—	No connection
Noninverting Input	3	3	I	Noninverting input
Output	6	1	O	Output of amplifier
$+V_S$	7	5	—	Positive power supply
$–V_S$	4	2	—	Negative power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply		±6.5	V_{DC}
Internal power dissipation	See *Thermal Information*		
Differential input voltage		±1.2	V
Input common-mode voltage		$±V_S$	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (MM)	±300	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Total supply voltage	5	10	12	V
T_A	Operating ambient temperature	–45	25	85	°C

7.4 Thermal Information

THERMAL METRIC (1)		OPA820		UNIT
		DBV (SOT-23)	D (SOIC)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	125	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	141.1	72.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.9	68.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.5	28.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42	67.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics: V_S = ±5 V

R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted) (1)(2)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
	Small-signal bandwidth	G = 1, V_O = 0.1 V_{PP}, R_F = 0 Ω, Test level = C			800		MHz
		G = 2, V_O = 0.1 V_{PP}, Test level = B	T_A = 25°C	170	240		
			T_A = 0°C to 70°C	160			
			T_A = –40°C to 85°C	155			
		G = 10, V_O = 0.1 V_{PP}, Test level = B	T_A = 25°C	23	30		
			T_A = 0°C to 70°C	21			
			T_A = –40°C to 85°C	20			
	Gain-bandwidth product	G ≥ 20, Test level = B	T_A = 25°C	220	280		MHz
			T_A = 0°C to 70°C	204			
			T_A = –40°C to 85°C	200			
	Bandwidth for 0.1-dB gain flatness	G = 2, V_O = 0.1 V_{PP}, Test level = C			38		MHz
	Peaking at a gain of 1	V_O = 0.1 V_{PP}, R_F = 0 Ω, Test level = C			0.5		dB
	Large-signal bandwidth	G = 2, V_O = 2 V_{PP}, Test level = C			85		MHz
	Slew rate	G = 2, 2-V step, Test level = B	T_A = 25°C	192	240		V/µs
			T_A = 0°C to 70°C	186			
			T_A = –40°C to 85°C	180			
	Rise time and fall time	G = 2, V_O = 0.2-V step, Test level = C			1.5		ns

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) T_J = T_A for 25°C specifications.
(3) T_J = T_A at low temperature limits; T_J = T_A + 9°C at high temperature limit for over temperature.

Electrical Characteristics: V_S = ±5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)[1][2][3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	Settling time	G = 2, V_O = 2-V step, Test level = C	To 0.02%		22		ns
			To 0.1%		18		
	Harmonic distortion, 2nd-harmonic	G = 2, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, Test level = B	T_A = 25°C		–85	–81	dBc
			T_A = 0°C to 70°C			–80	
			T_A = –40°C to 85°C			–79	
		G = 2, f = 1 MHz, V_O = 2 V_{PP}, R_L ≥ 500 Ω, Test level = B	T_A = 25°C		–90	–85	
			T_A = 0°C to 70°C			–83	
			T_A = –40°C to 85°C			–81	
	Harmonic distortion, 3rd-harmonic	G = 2, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, Test level = B	T_A = 25°C		–95	–90	dBc
			T_A = 0°C to 70°C			–89	
			T_A = –40°C to 85°C			–88	
		G = 2, f = 1 MHz, V_O = 2 V_{PP}, R_L ≥ 500 Ω, Test level = B	T_A = 25°C		–110	–105	
			T_A = 0°C to 70°C			–102	
			T_A = –40°C to 85°C			–100	
	Input voltage noise	f > 100 kHz, Test level = B	T_A = 25°C		2.5	2.7	nV/√Hz
			T_A = 0°C to 70°C			2.8	
			T_A = –40°C to 85°C			2.9	
	Input current noise	f > 100 kHz, Test level = B	T_A = 25°C		1.7	2.6	pA/√Hz
			T_A = 0°C to 70°C			2.8	
			T_A = –40°C to 85°C			3	
	Differential gain	G = 2, PAL, V_O = 1.4 V_{PP}, R_L = 150 Ω, Test level = C			0.01%		
	Differential phase	G = 2, PAL, V_O = 1.4 V_{PP}, R_L = 150 Ω, Test level = C			0.03		°
DC PERFORMANCE[4]							
A_{OL}	Open-loop voltage gain	*V_{CM} = 0 V*, Test level = A	T_A = 25°C	62	66		dB
			T_A = 0°C to 70°C	61			
			T_A = –40°C to 85°C	60			
	Input offset voltage	V_{CM} = 0 V, Test level = A	T_A = 25°C		±0.2	±0.75	mV
			T_A = 0°C to 70°C			±1	
			T_A = –40°C to 85°C			±1.2	
	Average input offset voltage drift	V_{CM} = 0 V, Test level = B	T_A = 0°C to 70°C			4	µV/°C
			T_A = –40°C to 85°C			4	
	Input bias current	V_{CM} = 0 V, Test level = A	T_A = 25°C		–9	–17	µA
			T_A = 0°C to 70°C			–19	
			T_A = –40°C to 85°C			–23	
	Average input bias current drift	V_{CM} = 0 V, Test level = B	T_A = 0°C to 70°C			30	nA/°C
			T_A = –40°C to 85°C			50	
	Input offset current	V_{CM} = 0 V, Test level = A	T_A = 25°C		±100	±400	nA
			T_A = 0°C to 70°C			±600	
			T_A = –40°C to 85°C			±700	
	Inverting input bias-current drift	V_{CM} = 0 V, Test level = B	T_A = 0°C to 70°C			5	nA/°C
			T_A = –40°C to 85°C			5	

(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

Electrical Characteristics: V_S = ±5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)[1][2][3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
CMIR	Common-mode input range[5]	Test level = A	T_A = 25°C	±3.8	±4		V
			T_A = 0°C to 70°C	±3.7			
			T_A = –40°C to 85°C	±3.6			
CMRR	Common-mode rejection ratio	V_{CM} = 0 V, Input-referred, Test level = A	T_A = 25°C	76	85		dB
			T_A = 0°C to 70°C	75			
			T_A = –40°C to 85°C	73			
	Input impedance, differential mode	V_{CM} = 0 V, T_A = 25°C, Test level = C			18 || 0.8		kΩ || pF
	Input impedance, common mode	V_{CM} = 0 V, T_A = 25°C, Test level = C			6 || 1		MΩ || pF
OUTPUT							
	Output voltage swing	No load, Test level = A	T_A = 25°C	±3.5	±3.7		V
			T_A = 0°C to 70°C	±3.42			
			T_A = –40°C to 85°C	±3.4			
		R_L = 100 Ω, Test level = A	T_A = 25°C	±3.5	±3.6		
			T_A = 0°C to 70°C	±3.45			
			T_A = –40°C to 85°C	±3.4			
	Output current	V_O = 0 V, Test level = A	T_A = 25°C	±90	±110		mA
			T_A = 0°C to 70°C	±80			
			T_A = –40°C to 85°C	±75			
	Short-circuit output current	Output shorted to ground, Test level = C			±125		mA
	Closed-loop output impedance	G = 2, f ≤ 100 kHz, Test level = C			0.04		Ω
POWER SUPPLY							
	Quiescent current	V_S = ±5 V, Test level = A	T_A = 25°C	5.45	5.6	5.75	mA
			T_A = 0°C to 70°C	5		6.2	
			T_A = –40°C to 85°C	4.8		6.4	
PSRR	Power-supply rejection ratio	Input referred, Test level = A	T_A = 25°C	64	72		dB
			T_A = 0°C to 70°C	63			
			T_A = –40°C to 85°C	62			

(5) Tested at less than 3 dB below the minimum specified CMRR at ± CMIR limits.

7.6 Electrical Characteristics: V_S = 5 V

R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)(1)(2)(3)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE						
Small-signal bandwidth	G = 1, V_O = 0.1 V_{PP}, R_F = 0 Ω, Test level = C			550		MHz
	G = 2, V_O = 0.1 V_{PP}, Test level = B	T_A = 25°C	168	230		
		T_A = 0°C to 70°C	155			
		T_A = –40°C to 85°C	151			
	G = 10, V_O = 0.1 V_{PP}, Test level = B	T_A = 25°C	21	28		
		T_A = 0°C to 70°C	20			
		T_A = –40°C to 85°C	19			
Gain-bandwidth product	G ≥ 20, Test level = B	T_A = 25°C	200	260		MHz
		T_A = 0°C to 70°C	190			
		T_A = –40°C to 85°C	185			
Peaking at a gain of 1	V_O = 0.1 V_{PP}, R_F = 0 Ω, Test level = C			0.5		dB
Large-signal bandwidth	G = 2, V_O = 2 V_{PP}, Test level = C			70		MHz
Slew rate	G = 2, 2-V step, Test level = B	T_A = 25°C	145	200		V/µs
		T_A = 0°C to 70°C	140			
		T_A = –40°C to 85°C	135			
Rise time and fall time	G = 2, V_O = 2-V step, Test level = C			1.7		ns
Settling time	G = 2, V_O = 2-V step, Test level = C	To 0.02%		24		ns
		To 0.1%		21		
Harmonic distortion, 2nd-harmonic	G = 2, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, Test level = B	T_A = 25°C		–80	–76	dBc
		T_A = 0°C to 70°C			–75	
		T_A = –40°C to 85°C			–74	
	G = 2, f = 1 MHz, V_O = 2 V_{PP}, R_L ≥ 500 Ω, Test level = B	T_A = 25°C		–83	–79	
		T_A = 0°C to 70°C			–77	
		T_A = –40°C to 85°C			–75	
Harmonic distortion, 3rd-harmonic	G = 2, f = 1 MHz, V_O = 2 V_{PP}, R_L = 200 Ω, Test level = B	T_A = 25°C		–100	–92	dBc
		T_A = 0°C to 70°C			–91	
		T_A = –40°C to 85°C			–90	
	G = 2, f = 1 MHz, V_O = 2 V_{PP}, R_L ≥ 500 Ω, Test level = B	T_A = 25°C		–98	–95	
		T_A = 0°C to 70°C			–93	
		T_A = –40°C to 85°C			–92	
Input voltage noise	f > 100 kHz, Test level = B	T_A = 25°C		2.5	2.8	nV/√Hz
		T_A = 0°C to 70°C			2.9	
		T_A = –40°C to 85°C			3	
Input current noise	f > 100 kHz, Test level = B	T_A = 25°C		1.6	2.5	pA/√Hz
		T_A = 0°C to 70°C			2.7	
		T_A = –40°C to 85°C			2.9	

(1) Test levels: (A) 100% tested at 25°C. Overtemperature limits by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) T_J = T_A for 25°C specifications.
(3) T_J = T_A at low temperature limits; T_J = T_A + 9°C at high temperature limit for over temperature.

Electrical Characteristics: V_S = 5 V (continued)

R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)[1][2][3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC PERFORMANCE[4]							
A_{OL}	Open-loop voltage gain	V_O = 2.5 V, Test level = A	T_A = 25°C	60	65		dB
			T_A = 0°C to 70°C	59			
			T_A = –40°C to 85°C	58			
	Input offset voltage	V_{CM} = 2.5 V, Test level = A	T_A = 25°C		±0.3	±1.1	mV
			T_A = 0°C to 70°C			±1.4	
			T_A = –40°C to 85°C			±1.6	
	Average input offset voltage drift	V_{CM} = 2.5 V, Test level = B	T_A = 0°C to 70°C			4	µV/°C
			T_A = –40°C to 85°C			4	
	Input bias current	V_{CM} = 2.5 V, Test level = A	T_A = 25°C		–8	–16	µA
			T_A = 0°C to 70°C			–18	
			T_A = –40°C to 85°C			–22	
	Average input bias current drift	V_{CM} = 2.5 V, Test level = B	T_A = 0°C to 70°C			30	nA/°C
			T_A = –40°C to 85°C			50	
	Input offset current	V_{CM} = 2.5 V, Test level = A	T_A = 25°C		±100	±400	nA
			T_A = 0°C to 70°C			±600	
			T_A = –40°C to 85°C			±700	
	Inverting input bias-current drift	V_{CM} = 2.5 V, Test level = B	T_A = 0°C to 70°C			5	nA/°C
			T_A = –40°C to 85°C			5	
INPUT							
	Lease positive input voltage	Test level = A	T_A = 25°C		0.9	1.1	V
			T_A = 0°C to 70°C			1.2	
			T_A = –40°C to 85°C			1.3	
	Most positive input voltage	Test level = A	T_A = 25°C	4.2	4.5		V
			T_A = 0°C to 70°C	4.1			
			T_A = –40°C to 85°C	4			
CMRR	Common-mode rejection ratio	V_{CM} = 2.5 V, Input-referred, Test level = A	T_A = 25°C	74	83		dB
			T_A = 0°C to 70°C	73			
			T_A = –40°C to 85°C	72			
	Input impedance, differential mode	V_{CM} = 2.5 V, T_A = 25°C, Test level = C			15 || 1		kΩ || pF
	Input impedance, common mode	V_{CM} = 2.5 V, T_A = 25°C, Test level = C			5 || 1.3		MΩ || pF

(4) Current is considered positive out-of-node. V_{CM} is the input common-mode voltage.

Electrical Characteristics: V_S = 5 V (continued)

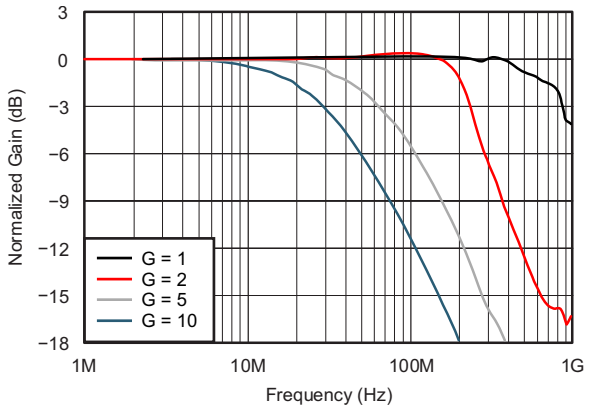
R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)[1][2][3]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Most positive output voltage	No load, Test level = A	T_A = 25°C	3.8	3.9		V
			T_A = 0°C to 70°C	3.75			
			T_A = –40°C to 85°C	3.7			
		R_L = 100 Ω to 2.5 V, Test level = A	T_A = 25°C	3.7	3.8		
			T_A = 0°C to 70°C	3.65			
			T_A = –40°C to 85°C	3.6			
	Least positive output voltage	No load, Test level = A	T_A = 25°C		1.2	1.3	V
			T_A = 0°C to 70°C			1.35	
			T_A = –40°C to 85°C			1.4	
		R_L = 100 Ω to 2.5 V, Test level = A	T_A = 25°C		1.2	1.3	
			T_A = 0°C to 70°C			1.35	
			T_A = –40°C to 85°C			1.4	
	Output current	V_O = 2.5 V, Test level = A	T_A = 25°C	±80	±105		mA
			T_A = 0°C to 70°C	±70			
			T_A = –40°C to 85°C	±65			
	Short-circuit output current	Output shorted to ground, Test level = C			±115		mA
	Closed-loop output impedance	G = 2, f ≤ 100 kHz, Test level = C			0.04		Ω
POWER SUPPLY							
	Quiescent current	V_S = ±5 V, Test level = A	T_A = 25°C	4.4	5	5.4	mA
			T_A = 0°C to 70°C	4.25		5.5	
			T_A = –40°C to 85°C	4.1		5.6	
PSRR	Power-supply rejection ratio	Input referred, T_A = 25°C, Test level = A			68		dB

7.7 Typical Characteristics

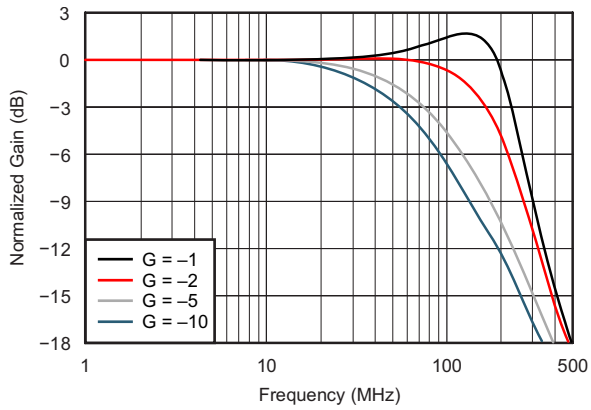
7.7.1 ±5-V Supply Voltage

V_S = ±5 V, R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)



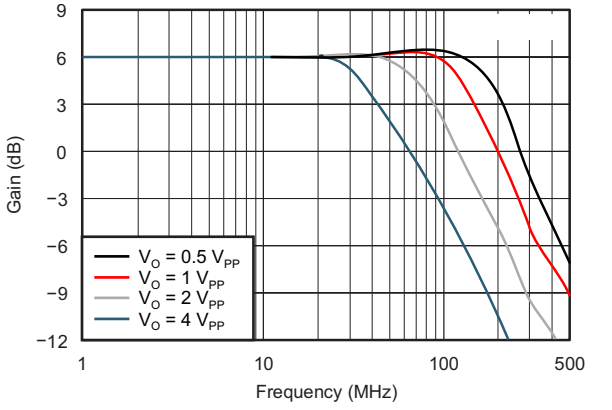
V_O = 0.1 V_{PP} R_F = 0 Ω at G = 1 See Figure 55

Figure 1. Noninverting Small-Signal Frequency Response



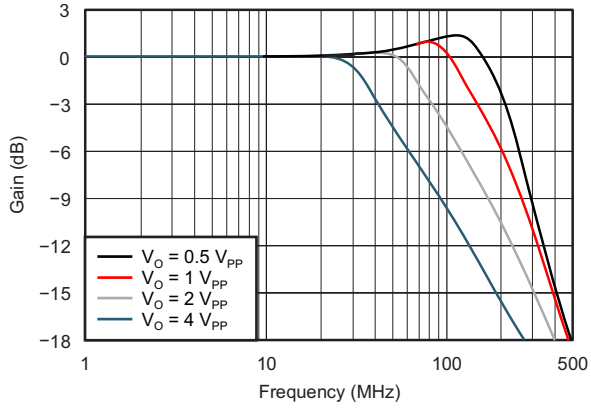
V_O = 0.1 V_{PP} See Figure 56

Figure 2. Inverting Small-Signal Frequency Response



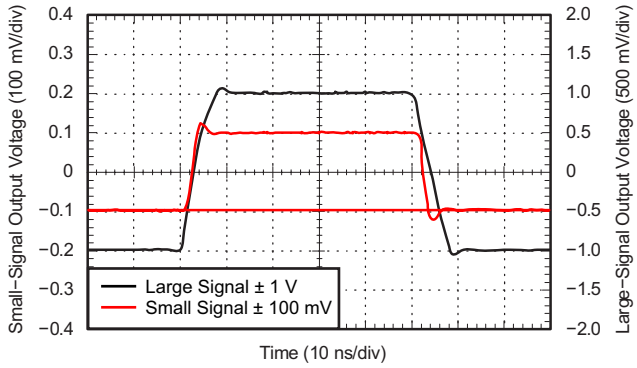
G = 2 See Figure 55

Figure 3. Noninverting Large-Signal Frequency Response



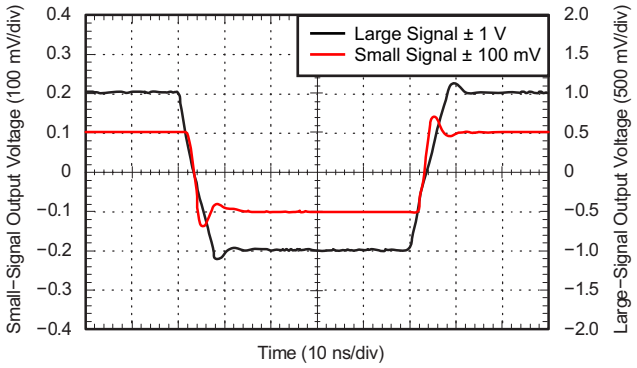
G = –1 See Figure 56

Figure 4. Inverting Large-Signal Frequency Response



G = 2 See Figure 55

Figure 5. Noninverting Pulse Response

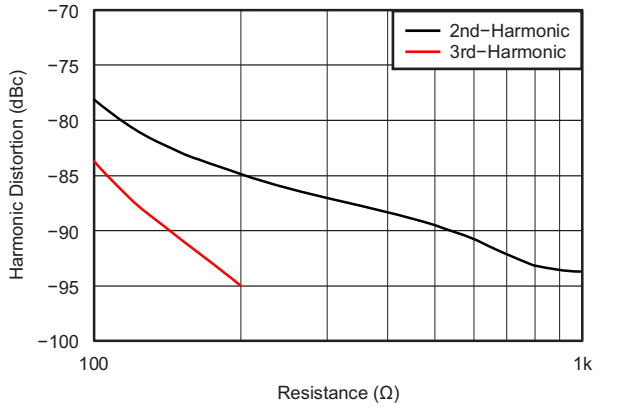


G = –1 See Figure 56

Figure 6. Inverting Pulse Response

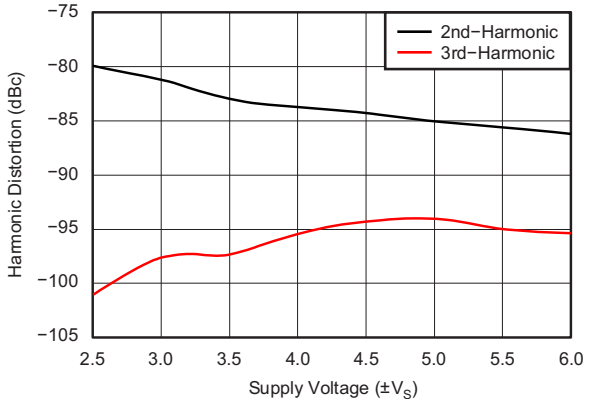
±5-V Supply Voltage (continued)

V_S = ±5 V, R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)



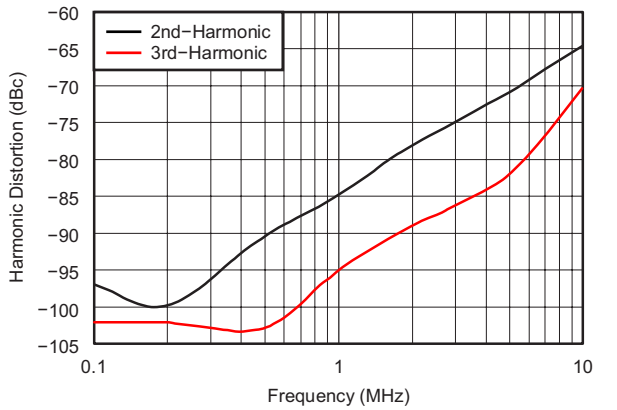
f = 1 MHz V_O = 2 V_{PP} G = 2 V/V
See Figure 55

Figure 7. Harmonic Distortion vs Load Resistance



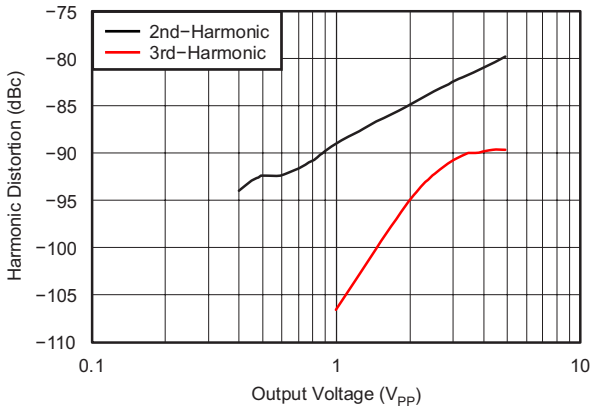
V_O = 2 V_{PP} R_L = 200 Ω G = 2 V/V
See Figure 55

Figure 8. 1-MHz Harmonic Distortion vs Supply Voltage



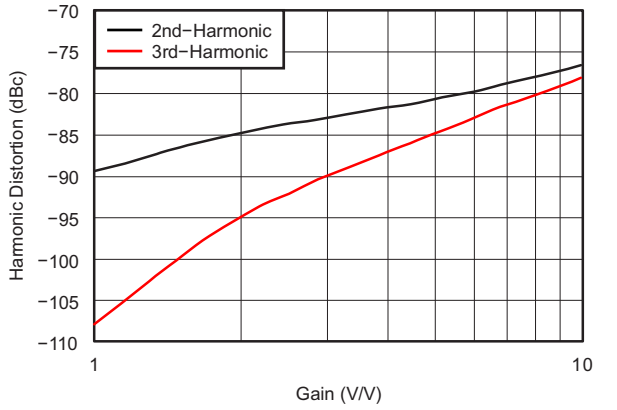
V_O = 2 V_{PP} G = 2 V/V
See Figure 55

Figure 9. Harmonic Distortion vs Frequency



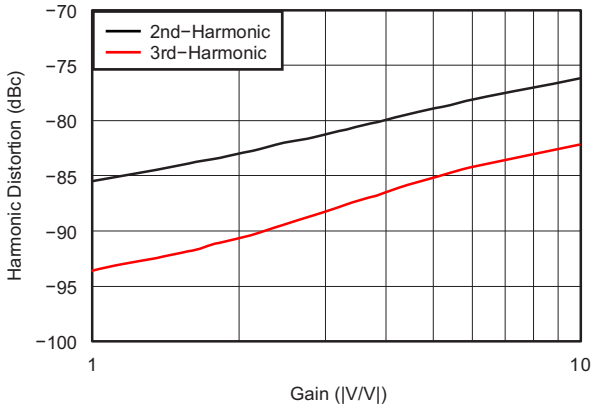
f = 1 MHz R_L = 200 Ω G = 2 V/V
See Figure 55

Figure 10. Harmonic Distortion vs Output Voltage



f = 1 MHz R_L = 200 Ω V_O = 2 V_{PP}
See Figure 55

Figure 11. Harmonic Distortion vs Noninverting Gain



f = 1 MHz R_L = 200 Ω V_O = 2 V_{PP}
See Figure 56

Figure 12. Harmonic Distortion vs Inverting Gain

±5-V Supply Voltage (continued)

V_S = ±5 V, R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)

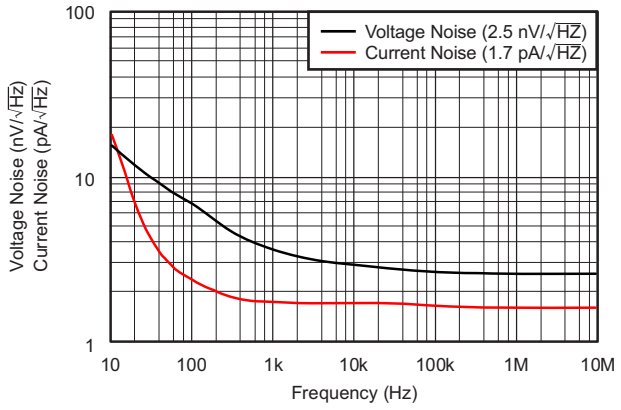
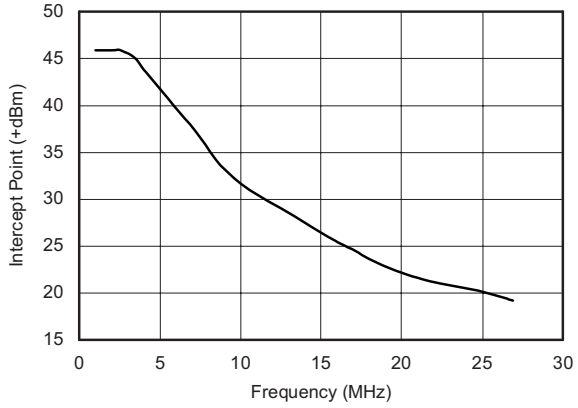
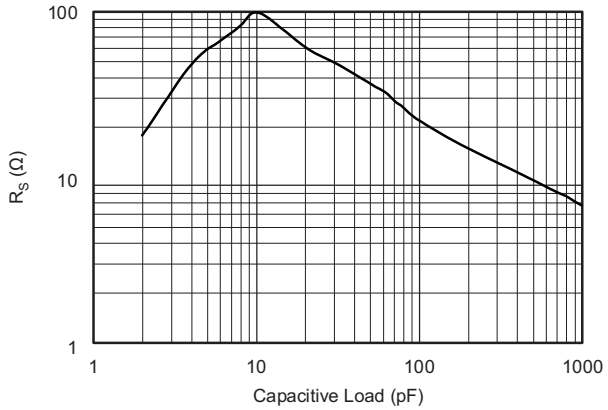


Figure 13. Input Voltage and Current Noise



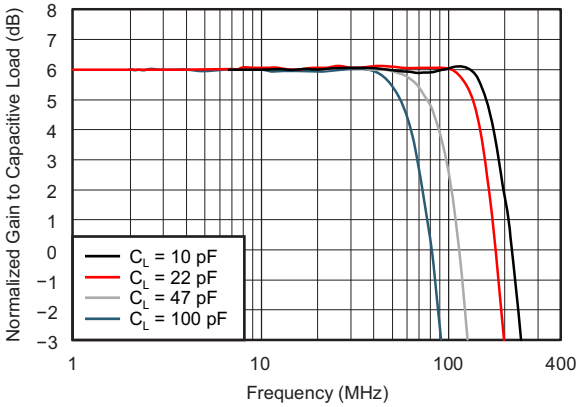
See Figure 48

Figure 14. Two-Tone, 3rd-Order Intermodulation Intercept



0-dB peaking targeted

Figure 15. Recommended R_S vs Capacitive Load



See Figure 49

Figure 16. Frequency Response vs Capacitive Load

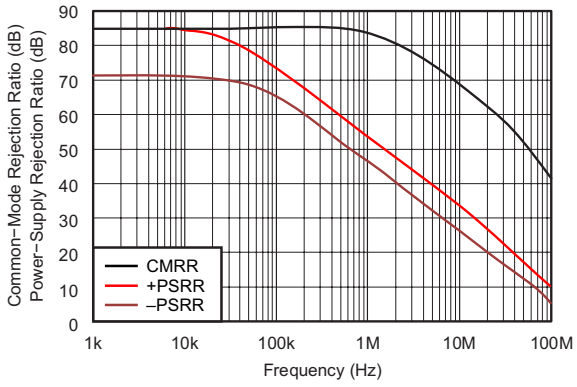


Figure 17. CMRR and PSRR vs Frequency

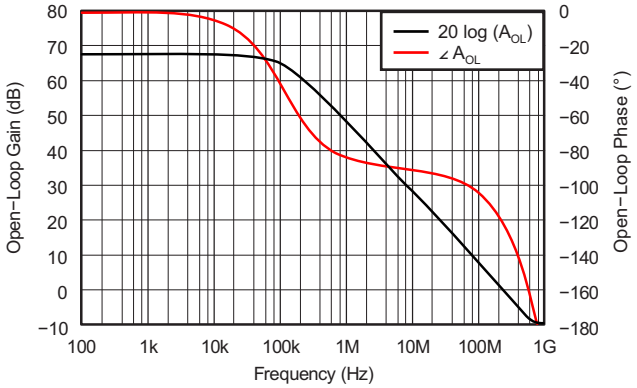


Figure 18. Open-Loop Gain and Phase

±5-V Supply Voltage (continued)

V_S = ±5 V, R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)

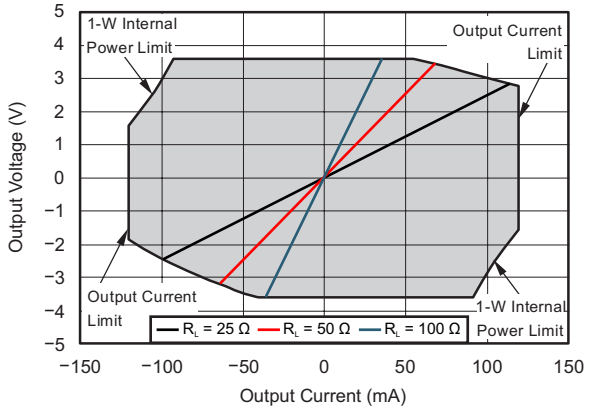


Figure 19. Output Voltage and Current Limitations

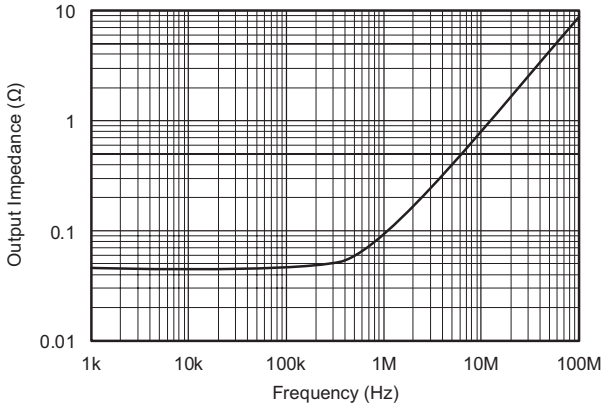
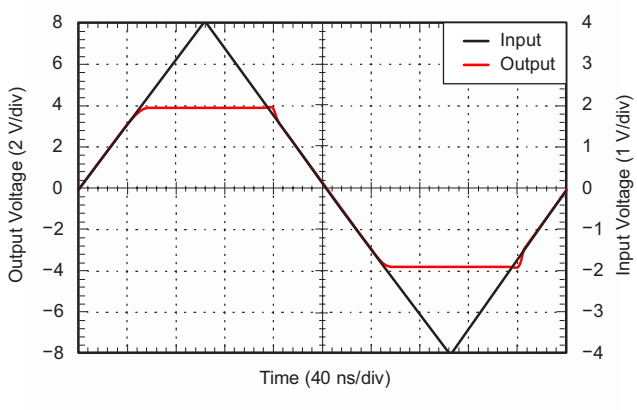
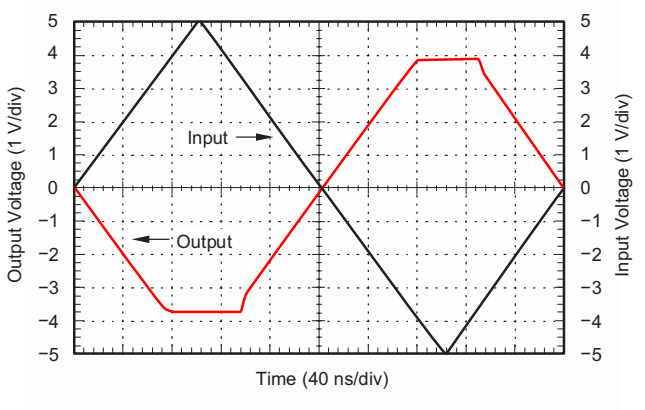


Figure 20. Closed-Loop Output Impedance vs Frequency



G = 2 V/V See Figure 55

Figure 21. Noninverting Overdrive Recovery



G = 2 V/V See Figure 56

Figure 22. Inverting Overdrive Recovery

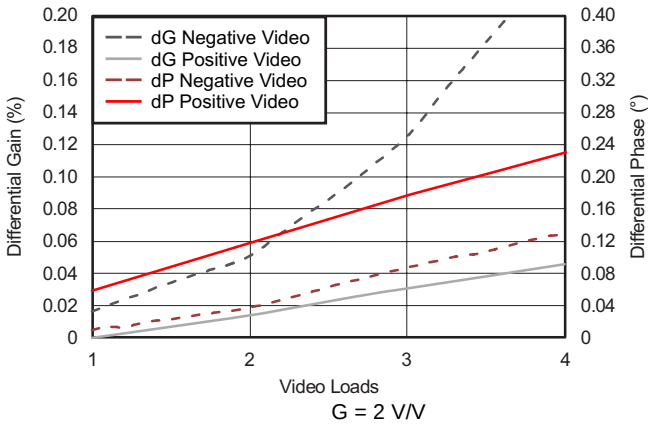


Figure 23. Composite Video dG/dP

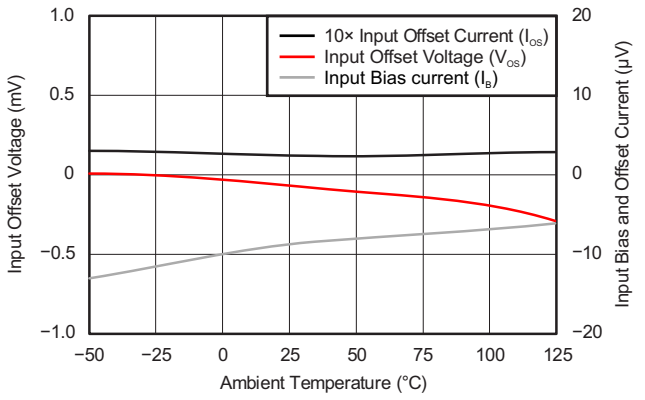


Figure 24. Typical DC Drift Over Temperature

±5-V Supply Voltage (continued)

V_S = ±5 V, R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)

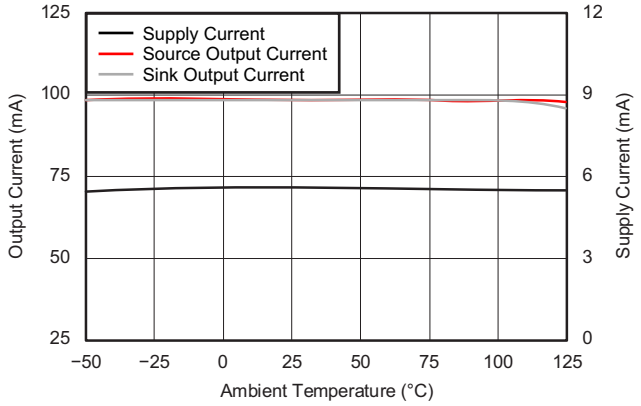


Figure 25. Supply and Output Current vs Temperature

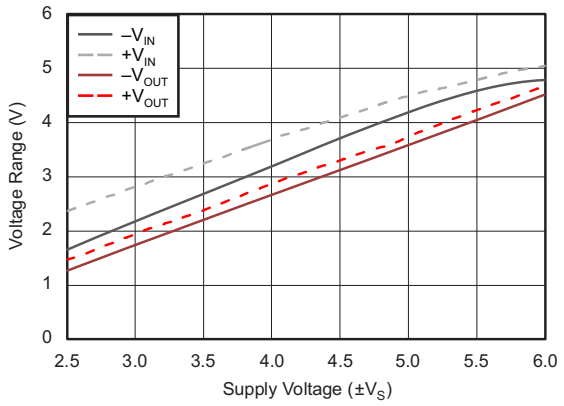


Figure 26. Common-Mode Input Range and Output Swing vs Supply Voltage

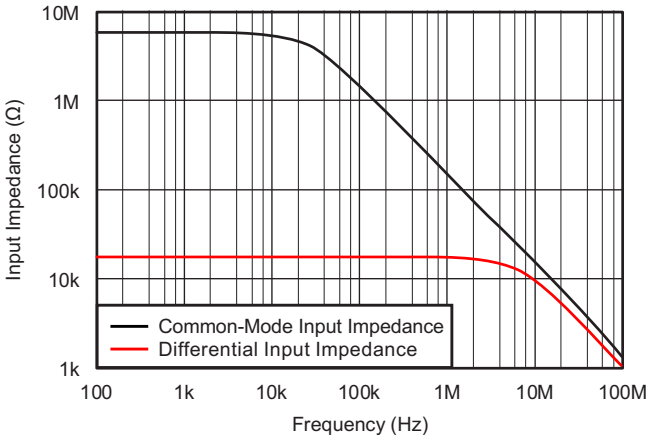
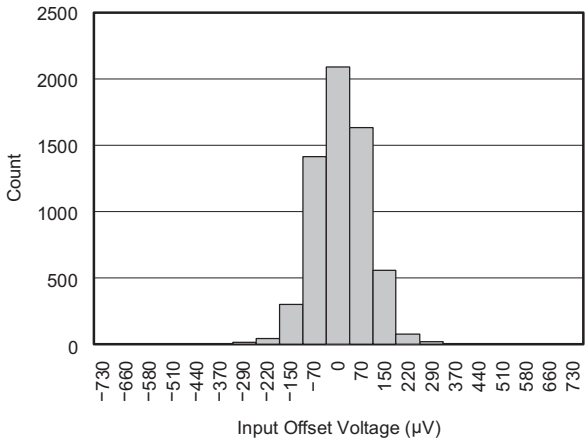
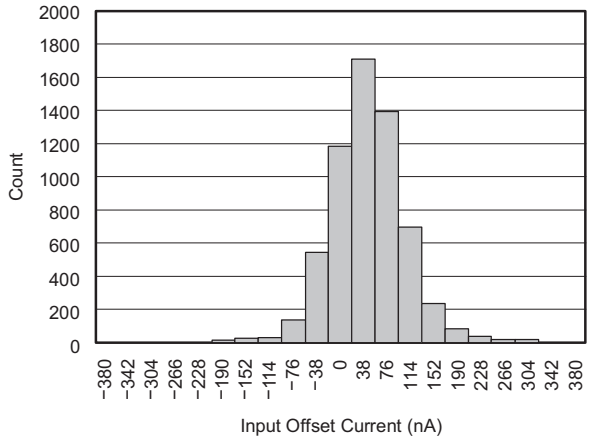


Figure 27. Common-Mode and Differential Input Impedance



Mean = –30 µV Total count = 6115
Standard deviation = 80 µV

Figure 28. Typical Input Offset Voltage Distribution

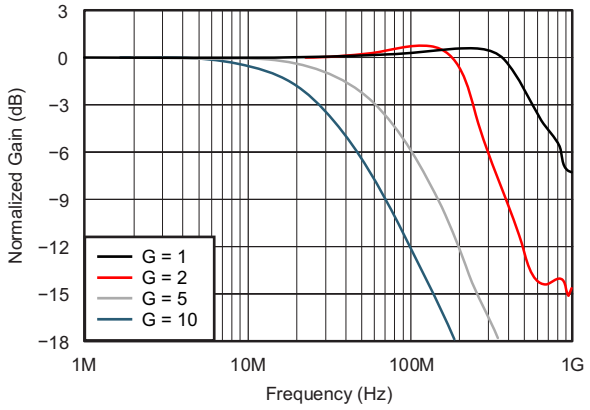


Mean = 26 nA Standard deviation = 57 nA Total count = 6115

Figure 29. Typical Input Offset Current Distribution

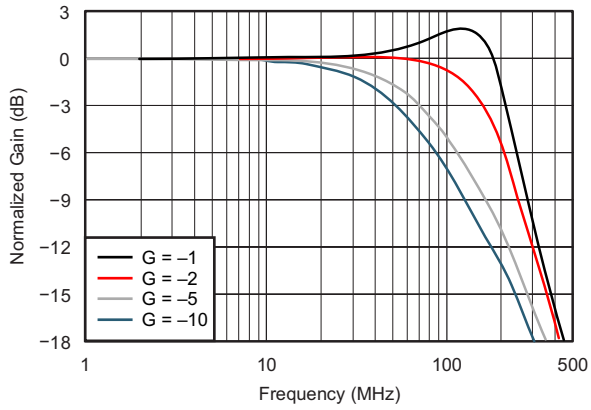
7.7.2 5-V Supply Voltage

V_S = 5 V, R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)



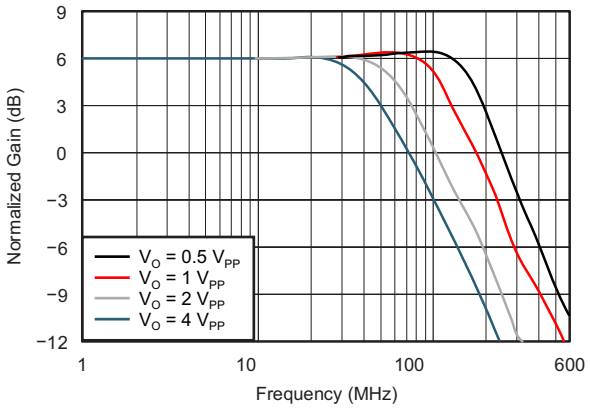
V_O = 0.1 V_{PP} See Figure 57

Figure 30. Noninverting Small-Signal Frequency Response



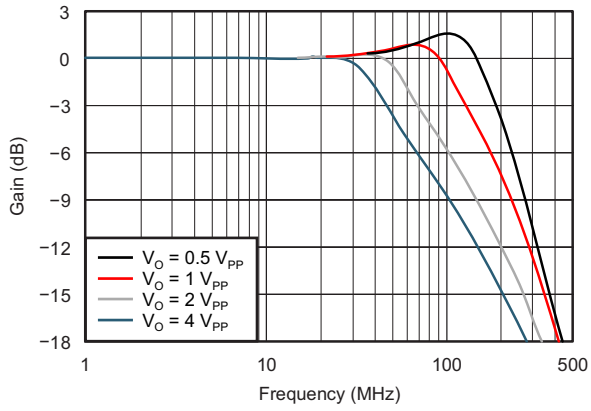
V_O = 0.1 V_{PP} See Figure 58

Figure 31. Inverting Small-Signal Frequency Response



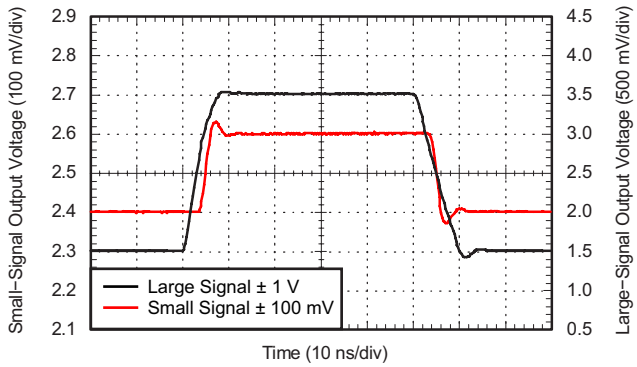
G = 2 V/V See Figure 57

Figure 32. Noninverting Large-Signal Frequency Response



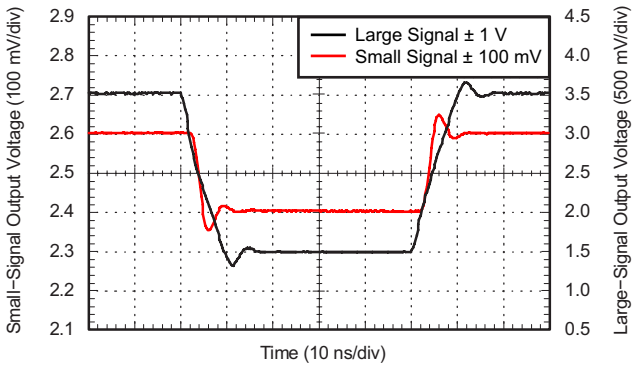
G = –1 See Figure 58

Figure 33. Inverting Large-Signal Frequency Response



G = 2 See Figure 57

Figure 34. Noninverting Pulse Response

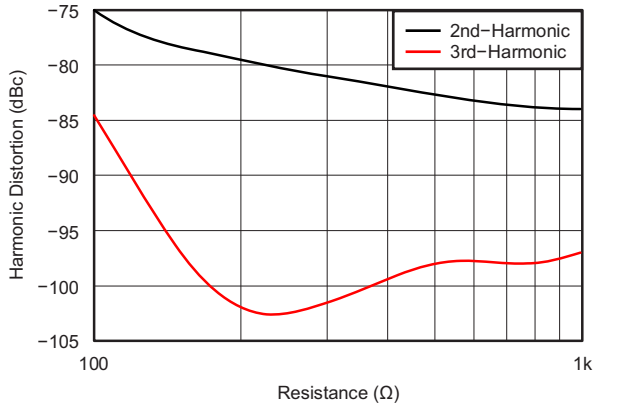


G = –1 See Figure 58

Figure 35. Inverting Pulse Response

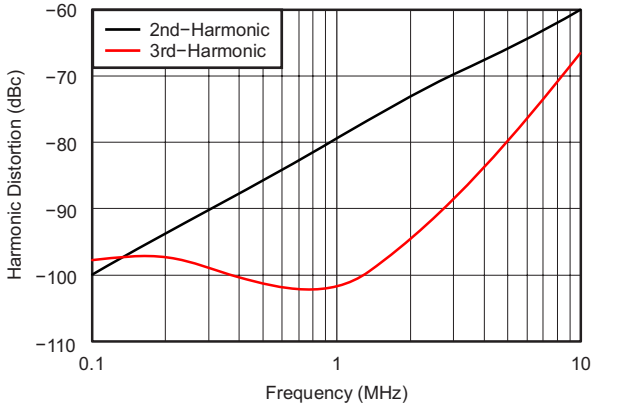
5-V Supply Voltage (continued)

V_S = 5 V, R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)



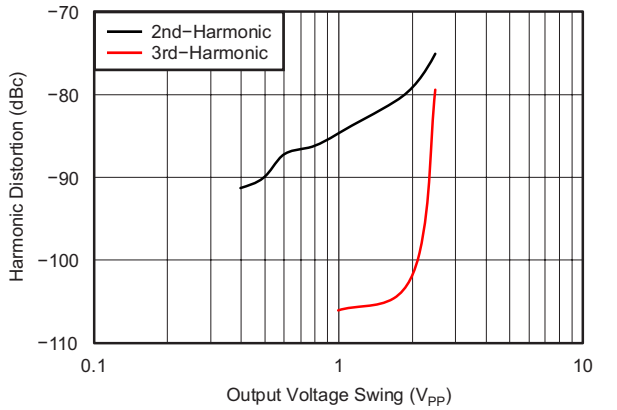
G = 2 V/V f = 1 MHz V_O = 2 V_{PP}
See Figure 57

Figure 36. Harmonic Distortion vs Load Resistance



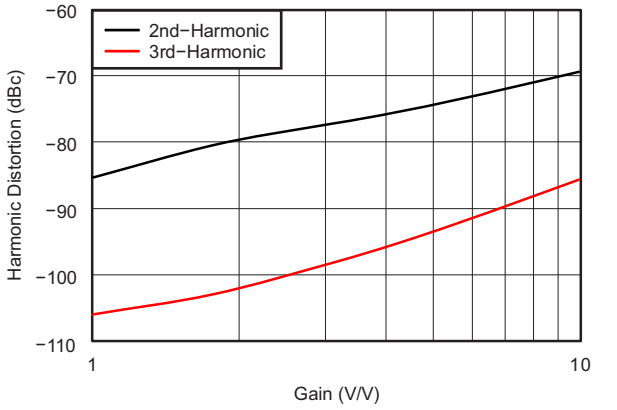
G = 2 V/V R_L = 200 Ω V_O = 2 V_{PP}
See Figure 57

Figure 37. Harmonic Distortion vs Frequency



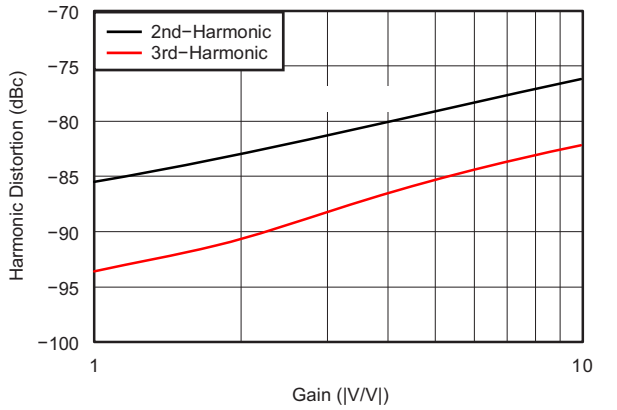
f = 1 MHz R_L = 200 Ω V_O = 2 V_{PP}
G = 2 V/V

Figure 38. Harmonic Distortion vs Output Voltage



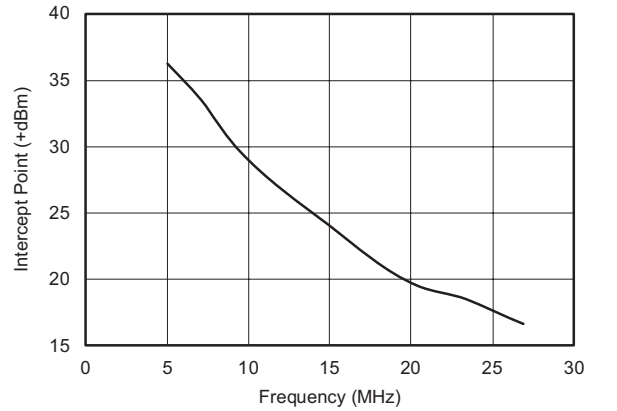
f = 1 MHz R_L = 200 Ω V_O = 2 V_{PP}

Figure 39. Harmonic Distortion vs Noninverting Gain



f = 1 MHz R_L = 200 Ω V_O = 2 V_{PP}

Figure 40. Harmonic Distortion vs Inverting Gain

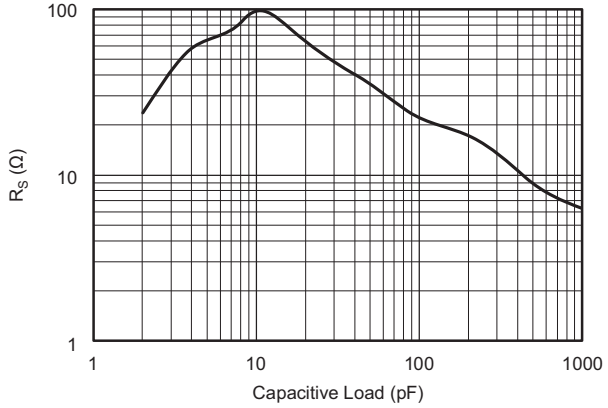


See Figure 50

Figure 41. Two-Tone, 3rd-Order Intermodulation Intercept

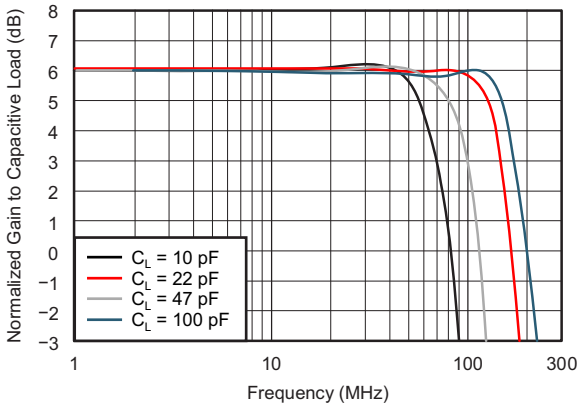
5-V Supply Voltage (continued)

V_S = 5 V, R_F = 402 Ω, R_L = 100 Ω, G = 2, and T_A = 25°C (unless otherwise noted)



0-dB peaking targeted

Figure 42. Recommended R_S vs Capacitive Load



See Figure 51

Figure 43. Frequency Response vs Capacitive Load

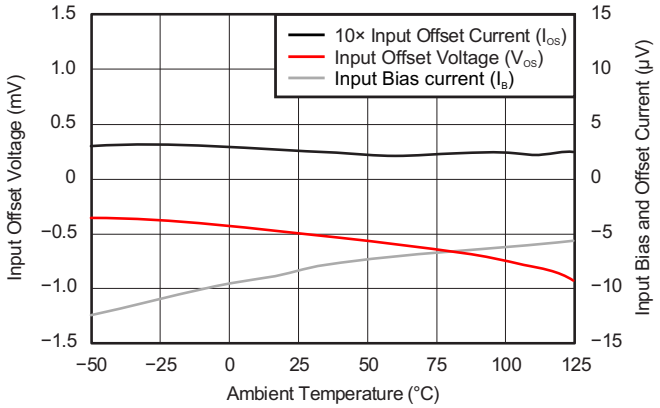


Figure 44. Typical DC Drift Over Temperature

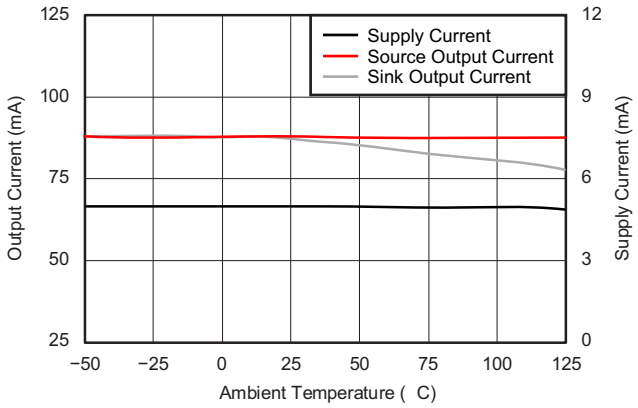
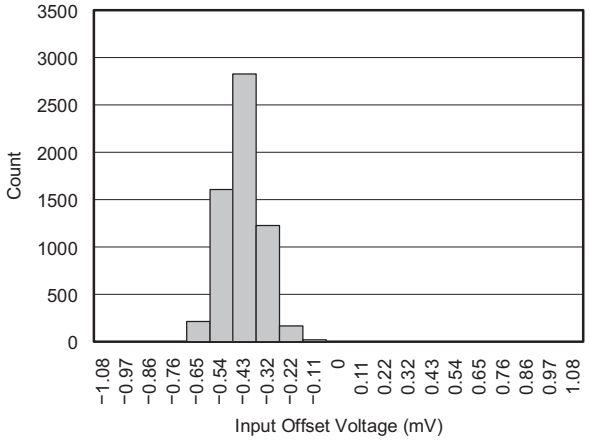
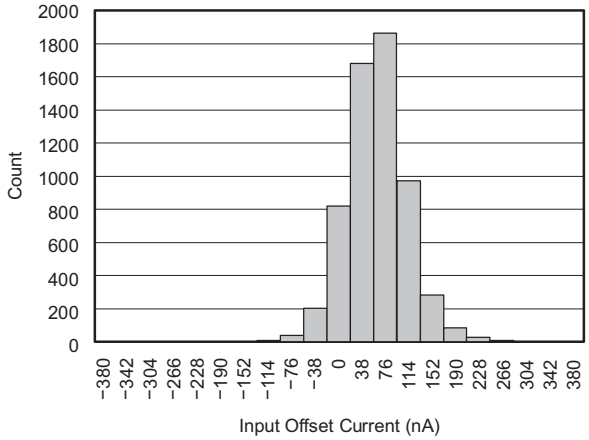


Figure 45. Supply and Output Current vs Temperature



Mean = 490 µV Total count = 6115
Standard deviation = 90 µV

Figure 46. Typical Input Offset Voltage Distribution



Mean = 43 nA Total count = 6115
Standard deviation = 50 nA

Figure 47. Typical Input Offset Current Distribution

8 Parameter Measurement Information

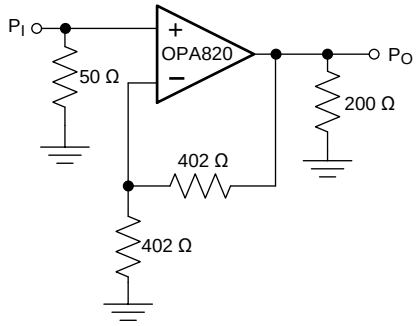
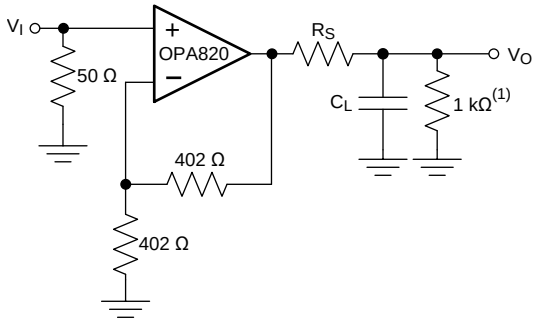


Figure 48. Circuit for ±5-V Two-Tone, 3rd-Order Intermodulation Intercept (Figure 14)



(1) 1 kΩ is optional.

Figure 49. Circuit for ±5-V Frequency Response vs Capacitive Load (Figure 55)

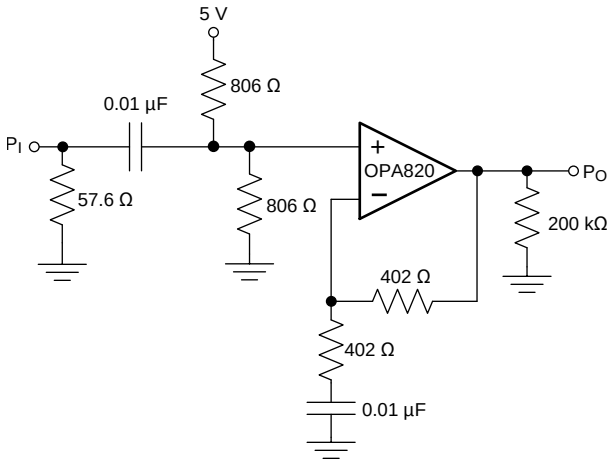
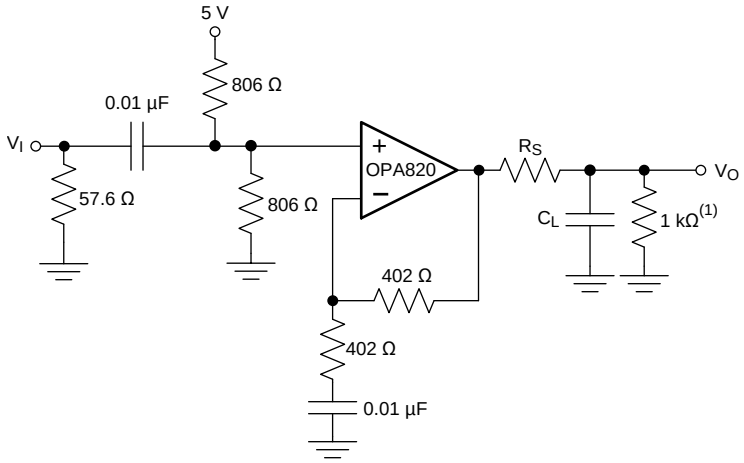


Figure 50. Circuit for 5-V Two-Tone, 3rd-Order Intermodulation Intercept (Figure 41)

Parameter Measurement Information (continued)



(1) This resistor is optional.

Figure 51. Circuit for 5-V Frequency Response vs Capacitive Load (Figure 43)

9 Detailed Description

9.1 Overview

The OPA820 provides an exceptional combination of DC precision, wide bandwidth, and low noise while consuming 5.6 mA of quiescent current. With excellent performance extending from DC to high frequencies, the OPA820 can be used in a variety of applications ranging from driving the inputs of high-precision SAR ADCs to video distributions systems.

9.2 Feature Description

9.2.1 Input and ESD Protection

The OPA820 device is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in *Absolute Maximum Ratings*. All device pins are protected with internal ESD-protection diodes to the power supplies, as shown in Figure 52.

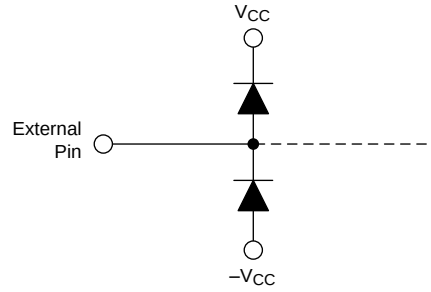
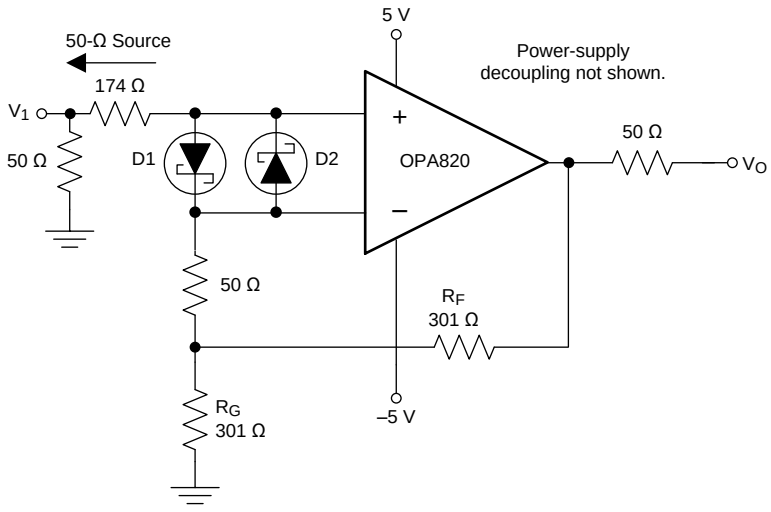


Figure 52. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30-mA continuous current. Where higher currents are possible (for example, in systems with ±15-V supply parts driving into the OPA820 device), add current-limiting series resistors into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response. Figure 53 shows an example protection circuit for I/O voltages that may exceed the supplies.



D1 = D2; IN5911 (or equivalent)

Figure 53. Gain of 2 With Input Protection

Feature Description (continued)

9.2.2 Bandwidth versus Gain

Voltage-feedback op amps exhibit decreasing closed-loop bandwidth as the signal gain is increased. In theory, this relationship is described by the GBP listed in *Specifications*. Ideally, dividing GBP by the noninverting signal gain (also called the noise gain, or NG) predicts the closed-loop bandwidth. In practice, this prediction only holds true when the phase margin approaches 90°, as it does in high-gain configurations. At low signal gains, most amplifiers exhibit a more complex response with lower phase margin. The OPA820 device is optimized to give a maximally-flat, 2nd-order Butterworth response in a gain of 2. In this configuration, the OPA820 device has approximately 64° of phase margin and shows a typical –3-dB bandwidth of 240 MHz. When the phase margin is 64°, the closed-loop bandwidth is approximately $\sqrt{2}$ greater than the value predicted by dividing GBP by the noise gain.

Increasing the gain causes the phase margin to approach 90° and the bandwidth to more closely approach the predicted value of GBP / NG. At a gain of 10, the 30-MHz bandwidth shown in *Electrical Characteristics: V_S = ±5 V* matches the prediction of the simple formula using the typical GBP of 280 MHz.

9.2.3 Output Drive Capability

The OPA820 device has been optimized to drive the demanding load of a doubly-terminated transmission line. When a 50-Ω line is driven, a series 50-Ω source resistor leading into the cable and a terminating 50-Ω load resistor at the end of the cable are used. Under these conditions, the cable impedance seems resistive over a wide frequency range, and the total effective load on the OPA820 device is 100 Ω in parallel with the resistance of the feedback network. *Specifications* lists a ±3.6-V swing into this load—which is then reduced to a ±1.8-V swing at the termination resistor. The ±75-mA output drive over temperature provides adequate current-drive margin for this load. Higher voltage swings (and lower distortion) are achievable when driving higher impedance loads.

A single video load typically appears as a 150-Ω load (using standard 75-Ω cables) to the driving amplifier. The OPA820 device provides adequate voltage and current drive to support up to three parallel video loads (50-Ω total load) for an NTSC signal. With only one load, the OPA820 device achieves an exceptionally low 0.01% or 0.03° dG/dP error.

9.2.4 Driving Capacitive Loads

One of the most demanding, and yet very common, load conditions for an op amp is capacitive loading. A high-speed, high open-loop gain amplifier like the OPA820 device can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. In simple terms, the capacitive load reacts with the open-loop output resistance of the amplifier to introduce an additional pole into the loop and thereby decrease the phase margin. This issue has become a popular topic of application notes and articles, and several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, distortion, or a combination, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This solution does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

Figure 15 (±5 V) and Figure 42 (5 V) show the recommended R_S versus capacitive load and the resulting frequency response at the load. The criterion for setting the recommended resistor is the maximum-bandwidth, flat-frequency response at the load. Because a passive low-pass filter is now between the output pin and the load capacitance, the response at the output pin is typically somewhat peaked, and becomes flat after the roll-off action of the RC network. This response is not a concern in most applications, but can cause clipping if the desired signal swing at the load is very close to the swing limit of the amplifier. Such clipping most likely to occurs in pulse response applications where the frequency peaking is manifested as an overshoot in the step response.

Parasitic capacitive loads greater than 2 pF can begin to degrade the performance of the OPA820 device. Long printed-circuit board traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA820 output pin (see *Layout Guidelines*).

Feature Description (continued)

9.2.5 Distortion Performance

The OPA820 device is capable of delivering an exceptionally-low distortion signal at high frequencies and low gains. The distortion plots in *Typical Characteristics* show the typical distortion under a wide variety of conditions. Most of these plots are limited to 100-dB dynamic range. The OPA820 distortion does not rise above –90 dBc until either the signal level exceeds 0.9 V, the fundamental frequency exceeds 500 kHz, or both occur. Distortion in the audio band is less than or equal to –100 dBc.

Generally, until the fundamental signal reaches very high frequencies or powers, the 2nd-harmonic dominates the distortion with a negligible 3rd-harmonic component. Focusing then on the 2nd-harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting configuration this is the sum of $R_F + R_G$, whereas in the inverting configuration this is just R_F (see Figure 55). Increasing the output voltage swing directly increases harmonic distortion. Increasing the signal gain also increases the 2nd-harmonic distortion. Again, a 6-dB increase in gain increases the 2nd and 3rd-harmonic by 6 dB even with a constant output power and frequency. Finally, the distortion increases as the fundamental frequency increases because of the roll-off in the loop gain with frequency. Conversely, the distortion improves going to lower frequencies down to the dominant open-loop pole at approximately 100 kHz. Starting from the –85-dBc 2nd-harmonic for 2 V_{PP} into 200 Ω, G = 2 distortion at 1 MHz (from *Typical Characteristics*), the 2nd-harmonic distortion does not show any improvement below 100 kHz and then becomes Equation 1.

$$–100\ dB – 20log\ (1\ MHz / 100\ kHz) = –105\ dBc \quad (1)$$

9.2.6 Noise Performance

The OPA820 device complements low harmonic distortion with low input-noise terms. Both the input-referred voltage noise and the two input-referred current noise terms combine to give a low output noise under a wide variety of operating conditions. Figure 54 shows the op amp noise analysis model with all the noise terms included. In this model, all the noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

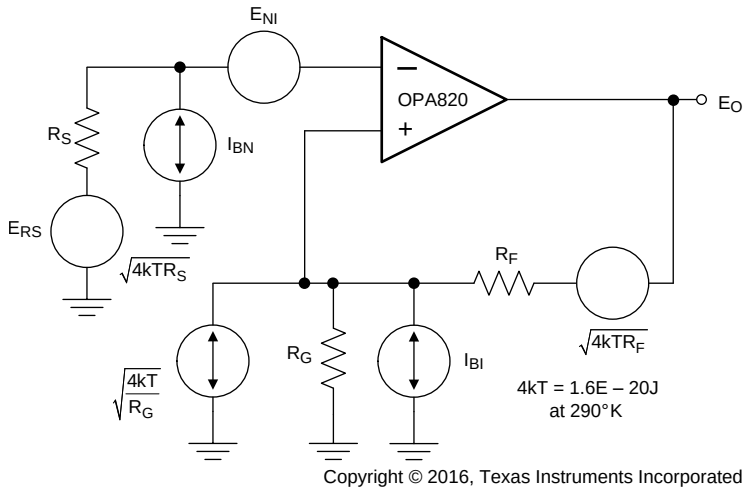


Figure 54. Op Amp Noise Analysis Model

The total output spot noise voltage is computed as the square root of the squared contributing terms to the output noise voltage. This computation is adding all the contributing noise powers at the output by superposition, then taking the square root to get back to a spot noise voltage. Equation 2 shows the general form for this output noise voltage using the terms presented in Figure 54.

$$E_O = \sqrt{\left[E_{NI}^2 + \left(I_{BN}R_S\right) + 4kTR_S\right]NG^2 + \left(I_{BI}R_F\right)^2 + 4kTR_FNG} \quad (2)$$

Feature Description (continued)

Dividing this expression by the noise gain (NG = 1 + R_F / R_G) gives the equivalent input referred spot noise voltage at the noninverting input, as shown in Equation 3.

$$E_N = \sqrt{E_{NI}^2 + \left(I_{BN}R_S\right)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \quad (3)$$

Evaluating these two equations for the OPA820 circuit shown in Figure 55 gives a total output spot noise voltage of 6.44 nV/√Hz and an equivalent input spot noise voltage of 3.22 nV/√Hz.

9.2.7 DC Offset Control

The OPA820 device can provide excellent DC-signal accuracy because of high open-loop gain, high common-mode rejection, high power-supply rejection, low input-offset voltage, and low bias-current offset errors. To take full advantage of this low input-offset voltage, careful attention to input bias-current cancellation is also required. The high-speed input stage for the OPA820 device has a moderately high input bias current (9 µA typical into the pins) but with a very close match between the two input currents—typically 100-nA input offset current. The total output-offset voltage can be considerably reduced by matching the source impedances looking out of the two inputs. For example, one way to add bias current cancellation to the circuit of Figure 55 is to insert a 175-Ω series resistor into the noninverting input from the 50-Ω terminating resistor. When the 50-Ω source resistor is DC-coupled, the source impedance for the noninverting input bias current increases to 200 Ω. Because this value is now equal to the impedance looking out of the inverting input (R_F || R_G), the circuit cancels the gains for the bias currents to the output leaving only the offset current times the feedback resistor as a residual DC error term at the output. Using a 402-Ω feedback resistor, this output error is now less than ±0.4 µA × 402 Ω = ±160 µV at 25°C.

9.2.8 Thermal Analysis

The OPA820 device does not require heat sinking or airflow in most applications. The maximum desired junction temperature sets the maximum allowed internal power dissipation as described in this section. Make sure that the maximum junction temperature does not exceed 150°C.

Use Equation 4 to calculate the operating junction temperature (T_J).

$$T_A + P_D \times R_{\theta JA} \quad (4)$$

The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load but, for a grounded resistive load, is at a maximum when the output is fixed at a voltage equal to ½ of either supply voltage (for equal bipolar supplies). Under this worst-case condition, use Equation 5 to calculate P_{DL}.

$$P_{DL} = V_S^2 / (4 \times R_L)$$

where

- R_L includes feedback network loading. (5)

NOTE

The power in the output stage and not in the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA820IDBV (SOT23-5 package) in the circuit of Figure 55 operating at the maximum specified ambient temperature of 85°C.

$$P_D = 10\ V\ (6.4\ mA) + 52 / (4 \times (100\ \Omega \parallel 800\ \Omega)) = 134\ mW \quad (6)$$

$$\text{Maximum } T_J = 85°C + (134\ mW \times 150°C/W) = 105°C \quad (7)$$

9.3 Device Functional Modes

9.3.1 Wideband Noninverting Operation

The combination of speed and dynamic range offered by the OPA820 device is easily achieved in a wide variety of application circuits, providing that simple principles of good design practice are observed. For example, good power-supply decoupling, as shown in Figure 55, is essential to achieve the lowest-possible harmonic distortion and smooth frequency response.

Proper PCB layout and careful component selection maximize the performance of the OPA820 device in all applications, as discussed in the following sections of this data sheet.

Figure 55 shows the gain of 2 configuration used as the basis for most of the typical characteristics. Most of the curves in *Typical Characteristics* were characterized using signal sources with a 50-Ω driving impedance and with measurement equipment presenting 50-Ω load impedance. In Figure 55, the 50-Ω shunt resistor at the V_I terminal matches the source impedance of the test generator while, the 50-Ω series resistor at the V_O terminal provides a matching resistor for the measurement equipment load. Generally, data sheet specifications refer to the voltage swings at the output pin (V_O in Figure 55). The 100-Ω load, combined with the 804-Ω total feedback network load, presents the OPA820 device with an effective load of approximately 90 Ω in Figure 55.

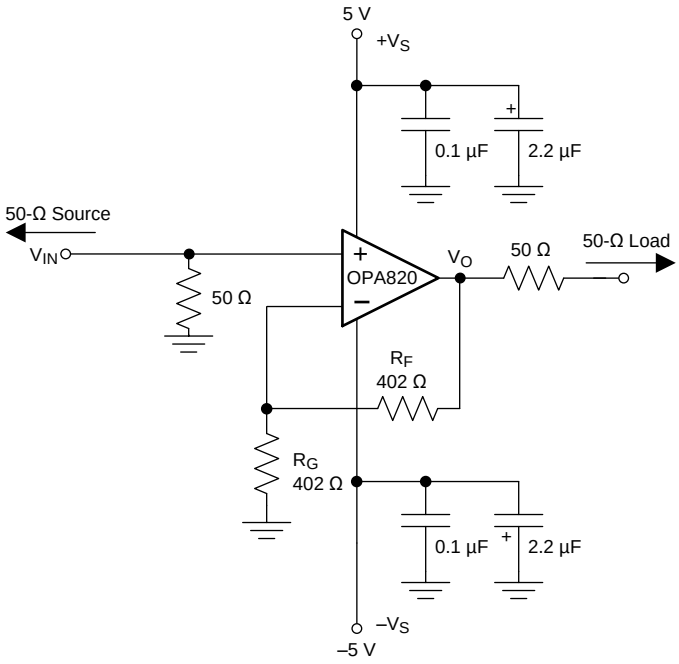


Figure 55. Gain of 2, High-Frequency Application and Characterization Circuit

9.3.2 Wideband Inverting Operation

Operating the OPA820 device as an inverting amplifier has several benefits and is particularly useful when a matched 50-Ω source and input impedance is required. Figure 56 shows the inverting gain of –1 circuit used as the basis of the inverting mode curves in *Typical Characteristics*.

Device Functional Modes (continued)

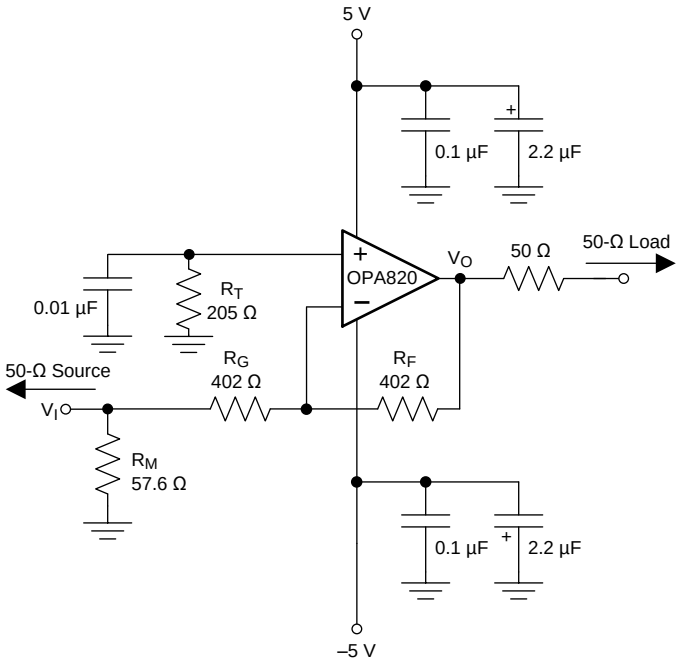


Figure 56. Inverting G = –1 Specifications and Test Circuit

In the inverting case, only the feedback resistor appears as part of the total output load in parallel with the actual load. For the 100-Ω load used in the curves in *Typical Characteristics*, this results in a total load of 80 Ω in this inverting configuration. The gain resistor is set to get the desired gain (in this case 402 Ω for a gain of –1) while an additional input-matching resistor (R_M) can be used to set the total input impedance equal to the source if desired. In this case, R_M is 57.6 Ω in parallel with the 402-Ω gain setting resistor results in a matched input impedance of 50 Ω. This matching is only required when the input must be matched to a source impedance, as in the characterization testing done using the circuit of Figure 56.

The OPA820 device offers extremely good DC accuracy as well as low noise and distortion. To take full advantage of that DC precision, the total DC impedance at each of the input nodes must be matched to get bias current cancellation. For the circuit of Figure 56, this matching requires the 205-Ω resistor to ground on the noninverting input. The calculation for this resistor includes a DC-coupled 50-Ω source impedance along with R_G and R_M. Although this resistor provides cancellation for the bias current, it must be well decoupled (0.01 µF in Figure 56) to filter the noise contribution of the resistor and the input current noise.

As the required R_G resistor approaches 50 Ω at higher gains, the bandwidth for the circuit in Figure 56 exceeds the bandwidth at that same gain magnitude for the noninverting circuit of Figure 55 which occurs because of the lower noise gain for the circuit of Figure 56 when the 50-Ω source impedance is included in the analysis. For instance, at a signal gain of –10 (R_G = 50 Ω, R_M = open, R_F = 499 Ω) the noise gain for the circuit of Figure 56 is shown in Equation 8.

$$1 + 499\ \Omega / (50\ \Omega + 50\ \Omega) = 6 \quad (8)$$

Equation 8 is a result of adding the 50-Ω source in the noise gain equation which results in a considerably higher bandwidth than the noninverting gain of 10. Using the 240-MHz gain bandwidth product for the OPA820 device, an inverting gain of –10 from a 50-Ω source to a 50-Ω R_G gives 55-MHz bandwidth, whereas the noninverting gain of 10 gives 30 MHz.

Device Functional Modes (continued)

9.3.3 Wideband Single-Supply Operation

Figure 57 shows the AC-coupled, single 5-V supply, gain of 2-V/V circuit configuration used as a basis only for the 5-V specifications in *Specifications*. The most important requirement for single-supply operation is to maintain input and output-signal swings within the useable voltage ranges at both the input and the output. The circuit of Figure 57 establishes an input midpoint bias using a simple resistive divider from the 5-V supply (two 806-Ω resistors) to the noninverting input. The input signal is then AC-coupled into this midpoint voltage bias. The input voltage can swing to within 0.9 V of the negative supply and 0.5 V of the positive supply, giving a 3.6-V_{PP} input-signal range. The input impedance-matching resistor (57.6 Ω) used in Figure 57 is adjusted to give a 50-Ω input match when the parallel combination of the biasing divider network is included. The gain resistor (R_G) is AC-coupled, giving the circuit a DC gain of 1 which puts the input DC bias voltage (2.5 V) on the output as well. On a single 5-V supply, the output voltage can swing to within 1.3 V of either supply pin while delivering more than 80-mA output current giving 2.4-V output swing into 100 Ω (5.6 dBm maximum at the matched load).

Figure 58 shows the AC-coupled, single 5-V supply, gain of –1-V/V circuit configuration used as a basis only for the 5-V specifications in *Specifications*. In this case, the midpoint DC bias on the noninverting input is also decoupled with an additional 0.01-µF decoupling capacitor which reduces the source impedance at higher frequencies for the noninverting-input bias-current noise. This 2.5-V bias on the noninverting input pin appears on the inverting input pin and, because R_G is DC blocked by the input capacitor, also appears at the output pin.

The single-supply test circuits of Figure 57 and Figure 58 show 5-V operation. These same circuits can be used with a single-supply of 5 V to 12 V. Operating on a single 12-V supply, with the absolute-maximum supply-voltage specification of 13 V, gives adequate design margin for the typical ±5% supply tolerance.

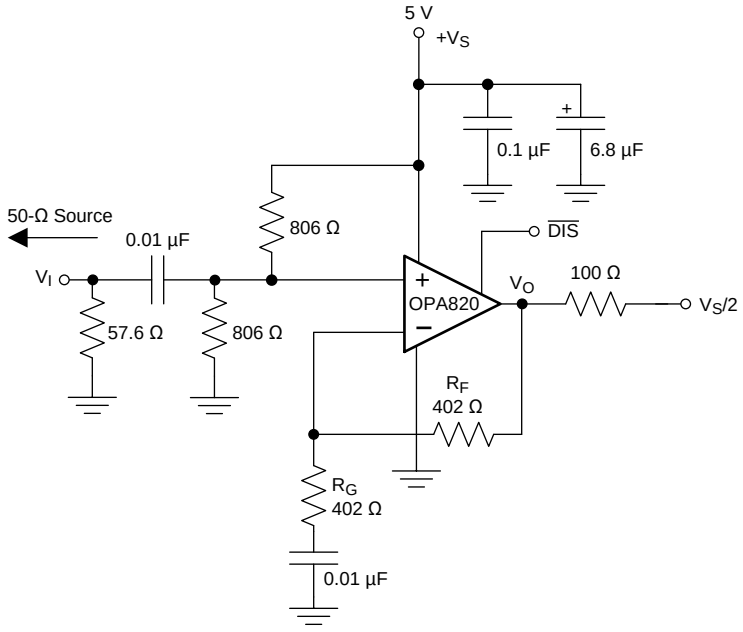


Figure 57. AC-Coupled, G = 2 V/V, Single-Supply Specifications and Test Circuit

Device Functional Modes (continued)

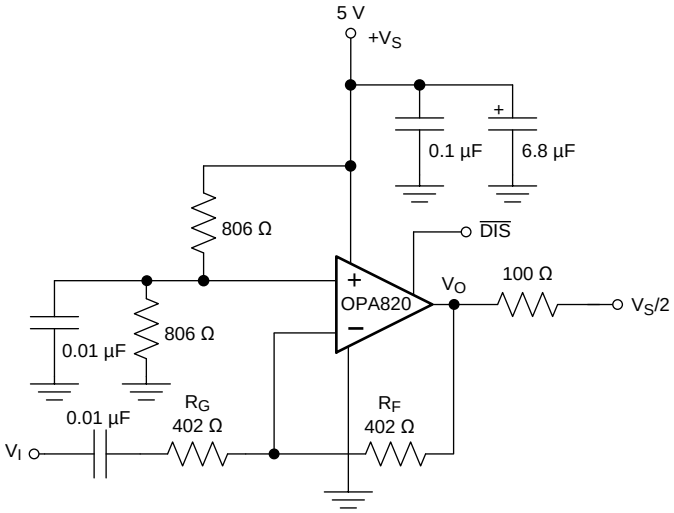


Figure 58. AC-Coupled, G = –1 V/V, Single-Supply Specifications and Test Circuit

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Optimizing Resistor Values

Because the OPA820 device is a unity-gain stable, voltage-feedback op amp, a wide range of resistor values can be used for the feedback and gain-setting resistors. The primary limits on these values are set by dynamic range (noise and distortion) and parasitic capacitance considerations. Usually, the feedback resistor value is from 200 Ω to 1 kΩ. At less than 200 Ω, the feedback network presents additional output loading which can degrade the harmonic distortion performance of the OPA820 device. At greater than 1 kΩ, the typical parasitic capacitance (approximately 0.2 pF) across the feedback resistor can cause unintentional band limiting in the amplifier response. A direct short is suggested as a feedback for AV = 1 V/V.

A good design practice is to target the parallel combination of R_F and R_G (see Figure 55) to be less than approximately 200 Ω. The combined impedance $R_F \parallel R_G$ interacts with the inverting input capacitance, placing an additional pole in the feedback network, and thus a zero in the forward response. Assuming a total parasitic of 2 pF on the inverting node, holding $R_F \parallel R_G < 200\ \Omega$ keeps this pole above 400 MHz. This constraint implies that the feedback resistor R_F can increase to several kΩ at high gains which is acceptable as long as the pole formed by R_F and any parasitic capacitance appearing in parallel is kept out of the frequency range of interest.

In the inverting configuration, an additional design consideration must be considered. R_G becomes the input resistor and therefore the load impedance to the driving source. If impedance matching is desired, R_G can be set equal to the required termination value. However, at low inverting gains, the resulting feedback resistor value can present a significant load to the amplifier output. For example, an inverting gain of 2 with a 50-Ω input matching resistor (R_G) requires a 100-Ω feedback resistor, which contributes to output loading in parallel with the external load. In such a case, increasing both the R_F and R_G values is preferable, and then achieve the input matching impedance with a third resistor to ground (see Figure 56). The total input impedance becomes the parallel combination of R_G and the additional shunt resistor.

10.2 Typical Applications

10.2.1 Active Filter Design

Most active filter topologies have exceptional performance using the broad bandwidth and unity-gain stability of the OPA820 device. Topologies employing capacitive feedback require a unity-gain stable, voltage-feedback op amp. Sallen-Key filters simply use the op amp as a noninverting gain stage inside an RC network. Either current feedback or voltage-feedback op amps can be used in Sallen-Key implementations.

Typical Applications (continued)

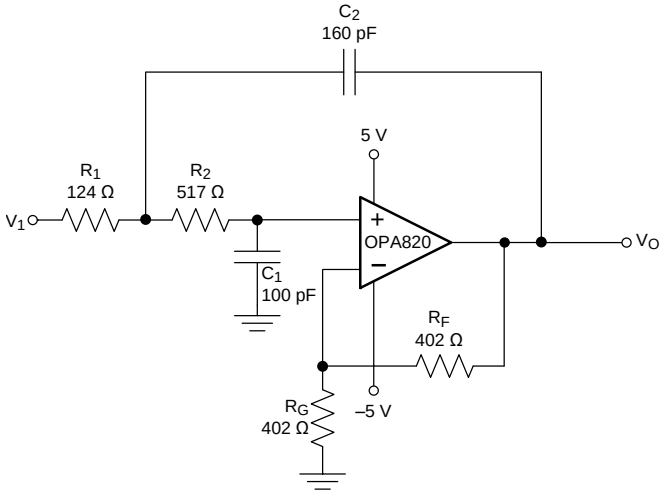


Figure 59. 5-MHz Butterworth Low-Pass Active Filter

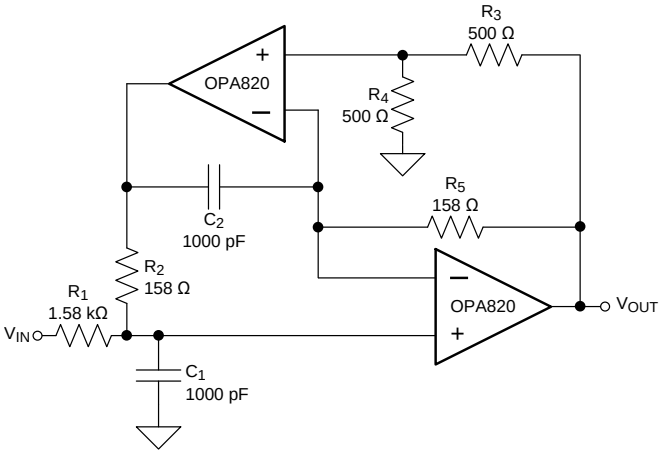


Figure 60. High-Q 1-MHz Bandpass Filter

10.2.1.1 Design Requirements

The design requirements for the active filters are given in Table 2:

Table 2. Design Requirements

FILTER TYPE	Q	FILTER CUTOFF FREQUENCY f_{-3dB} (MHz)	DC GAIN (dB)
Second order Butterworth, low-pass filter	0.707	5	6
High-Q, bandpass filter	10	1	—

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 High-Q Bandpass Filter Design Procedure

The transfer function of a high-Q bandpass filter shown in Figure 64 is given by Equation 9.

$$\frac{V_{OUT}}{V_{IN}} = \frac{S\frac{R_3 + R_4}{R_1 R_4 C_1}}{S^2 + S\frac{1}{R_1 C_1} + \frac{R_3}{R_2 R_4 R_5 C_1 C_2}} \quad (9)$$

$$\omega_O{}^2 = \frac{R3}{R_2 R_4 R_5 C_1 C_2} \quad (10)$$

$$\frac{\omega_O}{Q} = \frac{1}{R_1 C_1} \quad (11)$$

$$f_O = \frac{\omega_O}{2\pi} \simeq 1\,\text{MHz} \quad (12)$$

Use Equation 11 and Equation 12, along with the filter specifications in table to find the relationship between ω_0, Q, R_1, and C_1. Set C_1 = 1000 pF, which results in R_1= 1.5915 kΩ. The closest E96 standard value resistor value is 1.58 kΩ.

Notice that the DC load driven by the OPA820 driving the output V_{OUT} = R_3 + R_4. Select the total load to be 1 kΩ and R_3 = R_4, which results in a value of 500 Ω.

To simplify the filter design, set C_1 = C_2 = 1000 pF.

Plugging the values of R_3, R_4, C_1, and C_2 into Equation 10 and assuming $R_2 = R_5$ results in a value of 159.15 Ω. The closest standard E96 value is 158 Ω.

See Figure 61 for the frequency response of the filter shown in Figure 60.

10.2.1.2.2 Low-Pass Butterworth Filter Design Procedure

The transfer function of a low-pass Butterworth filter shown in Figure 59 is given by Equation 13.

$$\frac{V_{OUT}}{V_{IN}} = \frac{K}{s^2\left(R_1R_2C_1C_2\right) + s\left(R_1C_1 + R_2C_1 + R_1C_2\left(1-K\right)\right) + 1}$$

where

- $K = \left(1 + \frac{R_F}{R_G}\right)$ is the low-frequency DC gain (13)

The values for R_F and R_G are the standard recommended values in the data sheet.

The cutoff frequency is in Equation 14.

$$\omega_0 = \frac{1}{\left(R_1C_1R_2C_2\right)} \quad (14)$$

The Q of the filter is given by Equation 15.

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_1 + R_1C_2\left(1-K\right)} \quad (15)$$

From Table 1, Q = 0.707 and $\omega_0 = 2\pi \times 5$ MHz. To aid in solving this circuit, assume C_1 = 100 pF and R_1 = 124 Ω. Plugging these values into Equation 14 and Equation 15 and finding the closest standard value components results in R_2 = 517 Ω and C_2 = 160 pF. See Figure 62 for the frequency response of the filter shown in Figure 59.

10.2.1.3 Application Curves

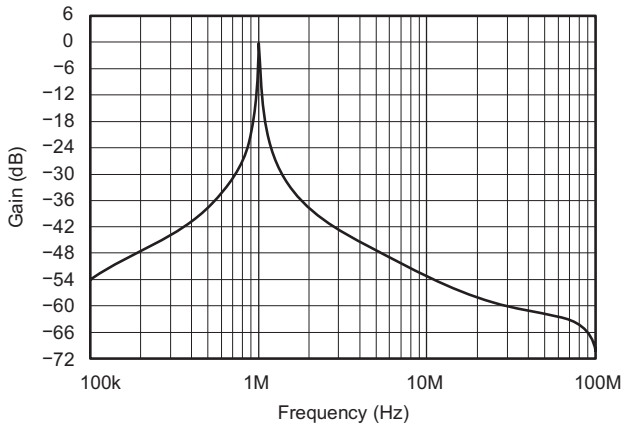


Figure 61. High-Q 1-MHz Bandpass Filter Frequency Response

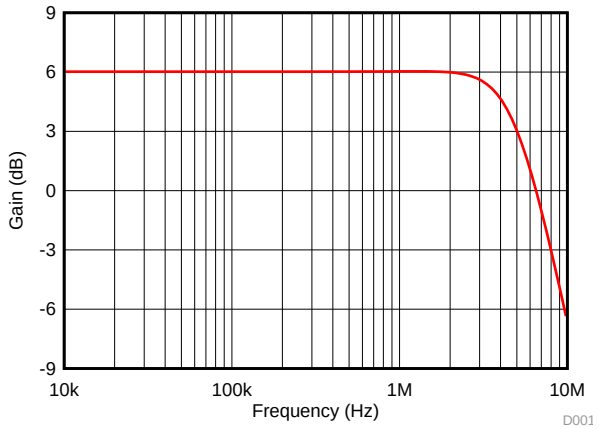


Figure 62. Frequency Response

10.2.2 Buffering High-Performance ADCs

To achieve full performance from a high-dynamic range ADC, take considerable care in the design of the input-amplifier interface circuit. The example circuit in Figure 63 shows a typical AC-coupled interface to a very-high dynamic-range converter. This AC-coupled example allows the OPA820 device to operate using a signal range that swings symmetrically around ground (0 V). The 2-V_{PP} swing is then level-shifted through the blocking capacitor to a midscale reference level, which is created by a well-decoupled resistive divider off the internal reference voltages of the converter. To have a negligible effect (1 dB) on the rated spurious-free dynamic range

(SFDR) of the converter, the SFDR of the amplifier must be at least 18 dB greater than the converter. The OPA820 device has a minimal effect on the rated distortion of the ADS850 device, given the 79-dB SFDR at 2 V_{PP}, 1 MHz of the ADS850 device. The greater than 90-dB (<1 MHz) SFDR for the OPA820 device in this configuration implies a less than 3-dB degradation (for the system) from the specification of the converter. For additional SFDR improvement with the OPA820 device, use a differential configuration.

Successful application of the OPA820 device for ADC driving requires careful selection of the series resistor at the amplifier output and the additional shunt capacitor at the ADC input. To some extent, the selection of this RC network is determined empirically for each converter. Many high-performance CMOS ADCs, such as the ADS850, perform better with the shunt capacitor at the input pin. This capacitor provides low source impedance for the transient currents produced by the sampling process. Improved SFDR is often obtained by adding this external capacitor, whose value is often recommended in the data sheet of the converter. The external capacitor, in combination with the built-in capacitance of the ADC input, presents a significant capacitive load to the OPA820 device. Without a series isolation resistor, an undesirable peaking or loss of stability in the amplifier can occur.

Because the DC bias current of the CMOS ADC input is negligible, the resistor has no effect on overall gain or offset accuracy. See Figure 15 (±5 V) and Figure 42 (5 V) to obtain a good starting value for the series resistor which ensures a flat-frequency response to the ADC input. Increasing the external capacitor value allows the series resistor to be reduced. Intentionally band limiting using this RC network can also be used to limit noise at the converter input.

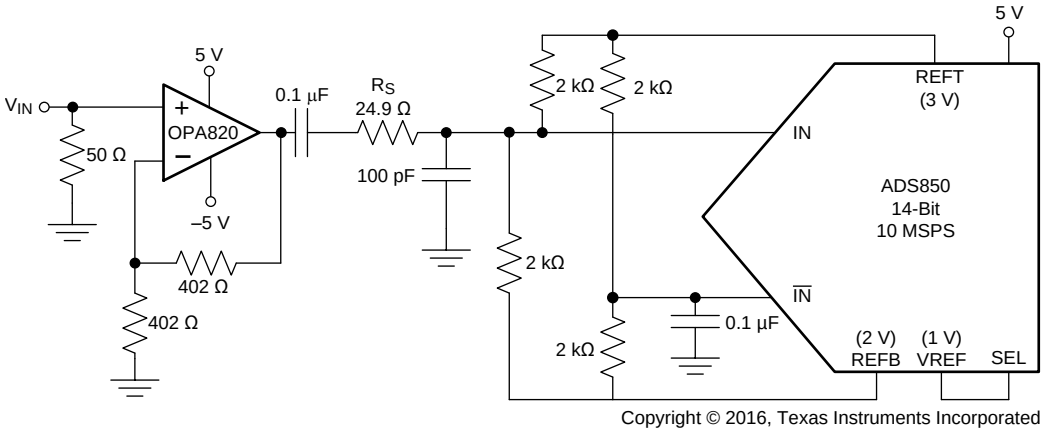
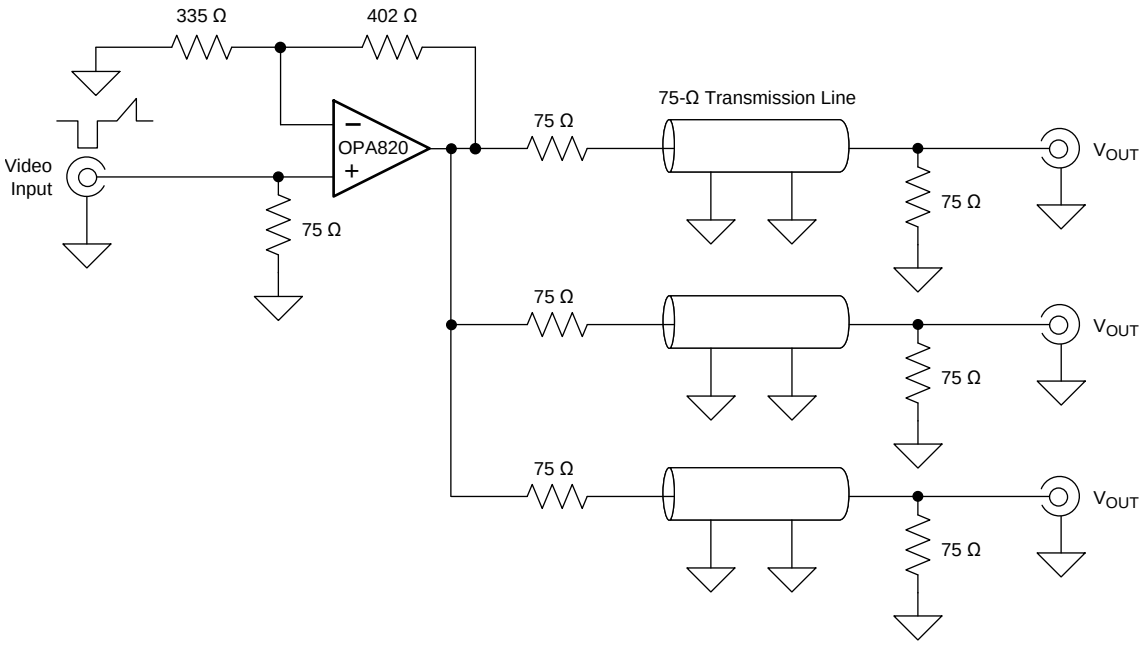


Figure 63. High Dynamic-Range Converter

10.2.3 Video Line Driving

Most video distribution systems are designed with 75-Ω series resistors to drive a matched 75-Ω cable. To deliver a net gain of 1 to the 75-Ω matched load, the amplifier is typically set up for a voltage gain of 2, compensating for the 6-dB attenuation of the voltage divider formed by the series and shunt 75-Ω resistors at either end of the cable.

The circuit of Figure 55 applies to this requirement if all references to 50-Ω resistors are replaced by 75-Ω values. Often, the amplifier gain is further increased to 2.2, which recovers the additional DC loss of a typical long cable run. This change would require the gain resistor (R_G) in Figure 55 to be reduced from 402 Ω to 335 Ω. In either case, both the gain flatness and the differential gain and phase performance of the OPA820 device provides exceptional results in video-distribution applications. Differential gain and phase measure the change in overall small-signal gain and phase for the color sub-carrier frequency (3.58 MHz in NTSC systems) versus changes in the large-signal output level (which represents luminance information in a composite video signal). The OPA820 device, with the typical 150-Ω load of a single-matched video cable, shows less than 0.01% differential gain and 0.01° phase errors over the standard luminance range for a positive video (negative sync) signal. Similar performance can be observed for multiple video signals, as shown in Figure 64.



High output current drive capability allows three back-terminated 75-Ω transmission lines to be simultaneously driven.

Figure 64. Video Distribution Amplifier

10.2.4 Single Differential Op Amp

The voltage-feedback architecture of the OPA820 device, with the high common-mode rejection ratio (CMRR), provides exceptional performance in differential amplifier configurations. Figure 65 shows a typical configuration. The starting point for this design is the selection of the R_F value from 200 Ω to 2 kΩ. Lower values reduce the required R_G, increasing the load on the V_2 source and on the OPA820 output. Higher values increase output noise as well as the effects of parasitic board and device capacitances. Following the selection of R_F, R_G must be set to achieve the desired inverting gain for V_2. Remember that the bandwidth is set approximately by the gain bandwidth product (GBP) divided by the noise gain ($1 + R_F / R_G$). For accurate differential operation (that is, good CMRR), the ratio R_2 / R_1 must be set equal to R_F / R_G.

Usually, setting the absolute values of R_2 and R_1 equal to R_F and R_G (respectively) is best. This setting equalizes the divider resistances and cancels the effect of input bias currents. However, scaling the values of R_2 and R_1 to adjust the loading on the driving source, V_1, can be useful. In most cases, the achievable low-frequency CMRR is limited by the accuracy of the resistor values. The 85-dB CMRR of the OPA820 device does not determine the overall circuit CMRR unless the resistor ratios are matched to better than 0.003%. If trimming the CMRR is required, R_2 is the suggested adjustment point.

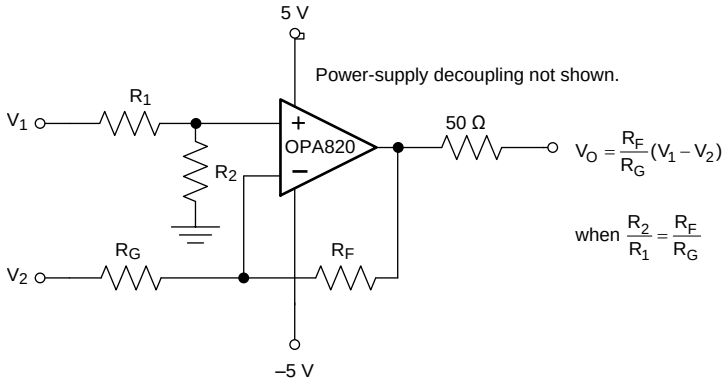


Figure 65. High-Speed, Single Differential Amplifier

10.2.5 Triple Differencing Op Amp (Instrumentation Topology)

The primary drawback of the single differential amplifier is the relatively low input impedances of the topology. Where high impedance is required at the differential input, a standard instrumentation amplifier (INA) topology can be built using the OPA820 device as the differencing stage. Figure 66 shows an example of this, in which the two input amplifiers are packaged together as a dual voltage-feedback op amp, the OPA2822 device.

This approach saves board space, cost, and power compared to using two additional OPA820 devices, and still achieves very good noise and distortion performance as a result of the moderate loading on the input amplifiers.

In this circuit, the common-mode gain to the output is always 1, because of the four matched 500-Ω resistors, whereas the differential gain is set by Equation 16 which is equal to 2 using the values in Figure 66.

$$1 + 2R_{F1} / R_G \quad (16)$$

The differential to single-ended conversion is still performed by the OPA820 output stage. The high-impedance inputs allow the V_1 and V_2 sources to be terminated or impedance-matched as required. If the V_1 and V_2 inputs are already truly differential, such as the output from a signal transformer, then a single-matching termination resistor can be used between them. Remember, however, that a defined DC signal path must always exist for the V_1 and V_2 inputs; for the transformer case, a center-tapped secondary connected to ground would provide an optimum DC operating point.

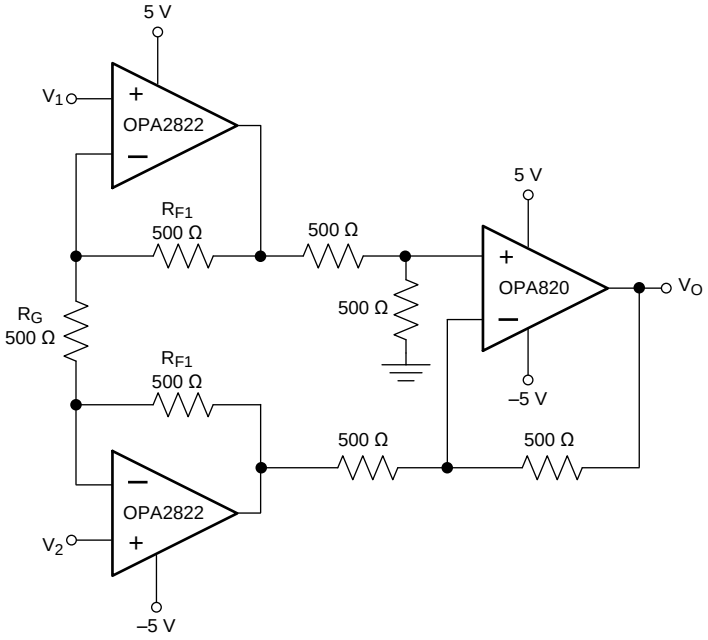


Figure 66. Wideband 3-Differencing Amplifier

10.2.6 DAC Transimpedance Amplifier

High-frequency digital-to-analog converters (DACs) require a low-distortion output amplifier to retain the SFDR performance into practical loads. Figure 67 shows a single-ended output-drive implementation. In this circuit, only one side of the complementary output drive signal is used. Figure 67 shows the signal output current connected into the virtual ground-summing junction of the OPA820 device, which is set up as a transimpedance stage or I-V converter. The unused current output of the DAC is connected to ground. If the DAC requires the outputs to be terminated to a compliance voltage other than ground for operation, then the appropriate voltage level can be applied to the noninverting input of the OPA820 device.

The DC gain for this circuit is equal to R_F. At high frequencies, the DAC output capacitance (C_D) produces a zero in the noise gain for the OPA820 device that can cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise-gain peaking. To achieve a flat transimpedance-frequency response, this pole in the feedback network must be set to the value shown in Equation 17 which gives a corner frequency $f_{-3\ dB}$ of approximately as shown in Equation 18.

$$\frac{1}{2\pi R_F C_F} = \sqrt{\frac{GBP}{4\pi R_F C_D}} \quad (17)$$

$$f_{-3\ dB} = \sqrt{\frac{GBP}{2\pi R_F C_D}} \quad (18)$$

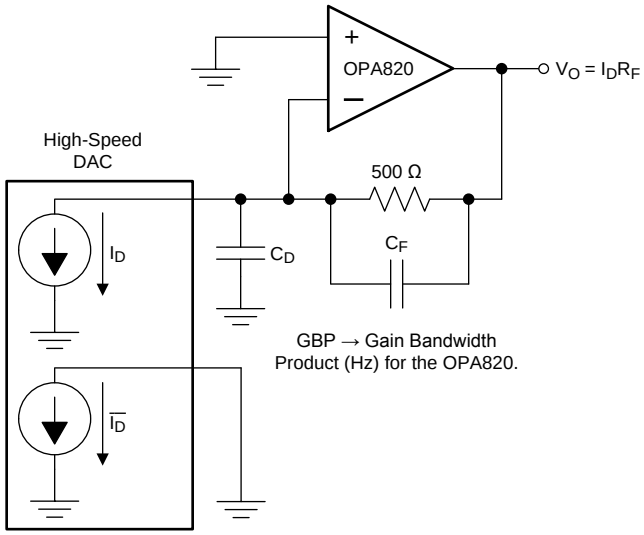


Figure 67. Wideband, Low-Distortion DAC Transimpedance Amplifier

11 Power Supply Recommendations

High-speed amplifiers require low-inductance power supply traces and low-ESR bypass capacitors. When possible both power and ground planes must be used in the printed-circuit board design and the power plane must be adjacent to the ground plane in the board stack-up. The power supply voltage must be centered on the desired amplifier output voltage; so for ground referenced output signals, split supplies are required. The power supply voltage must be from 5 V to 12 V.

12 Layout

12.1 Layout Guidelines

Achieving optimum performance with a high-frequency amplifier such as the OPA820 device requires careful attention to board layout parasitics and external component types. This section lists recommendations to optimize performance.

12.1.1 Minimizing Parasitic Capacitance

Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability. On the noninverting input, parasitic capacitance can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins must be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes must be unbroken elsewhere on the board.

12.1.2 Minimizing Distance from Power Supply to Decoupling Capacitors

Minimize the distance, less than 0.25 inches, from the power-supply pins to high-frequency 0.1-µF decoupling capacitors. At the device pins, the ground and power-plane layout must not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections must always be decoupled with these capacitors. Larger (2.2-µF to 6.8-µF) decoupling capacitors, effective at lower frequency, must also be used on the main supply pins. Place these capacitors somewhat farther from the device. These capacitors can be shared among several devices in the same area of the PCB.

12.1.3 Selecting and Placing External Components

Careful selection and placement of external components preserves the high-frequency performance of the OPA820 device. Resistors must be a very-low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially leaded resistors can also provide good high-frequency performance. Again, keep the leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Because the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, must also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values greater than 1.5 kΩ, this parasitic capacitance can add a pole, a zero, or both below 500 MHz that can effect circuit operation. Keep resistor values as low as possible consistent with load-driving considerations. A good starting point for design is to set $R_G \parallel R_F = 200\ \Omega$. Using this setting automatically keeps the resistor noise terms low, and minimizes the effect of the parasitic capacitance.

12.1.4 Connecting Other Wideband Devices

Connections to other wideband devices on the board can be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) must be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of Figure 15 (±5 V) and Figure 42 (5 V). Low parasitic capacitive loads (<5 pF) may not require an R_S because the OPA820 device is nominally compensated to operate with a 2-pF parasitic load. Higher parasitic capacitive loads without an R_S are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact, a higher impedance environment improves distortion as shown in Figure 7 and Figure 36. With a characteristic board-trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA820 device is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt

Layout Guidelines (continued)

resistor and input impedance of the destination device; this total effective impedance must be set to match the trace impedance. If the 6-dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of Figure 15 (±5 V) and Figure 42 (5 V) which does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, some signal attenuation occurs because of the voltage divider formed by the series output into the terminating impedance.

12.1.5 Socketing

TI does not recommend socketing a high-speed part like the OPA820 device. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make achieving a smooth, stable frequency response almost impossible. The best results are obtained by soldering the OPA820 device onto the board.

12.2 Layout Example

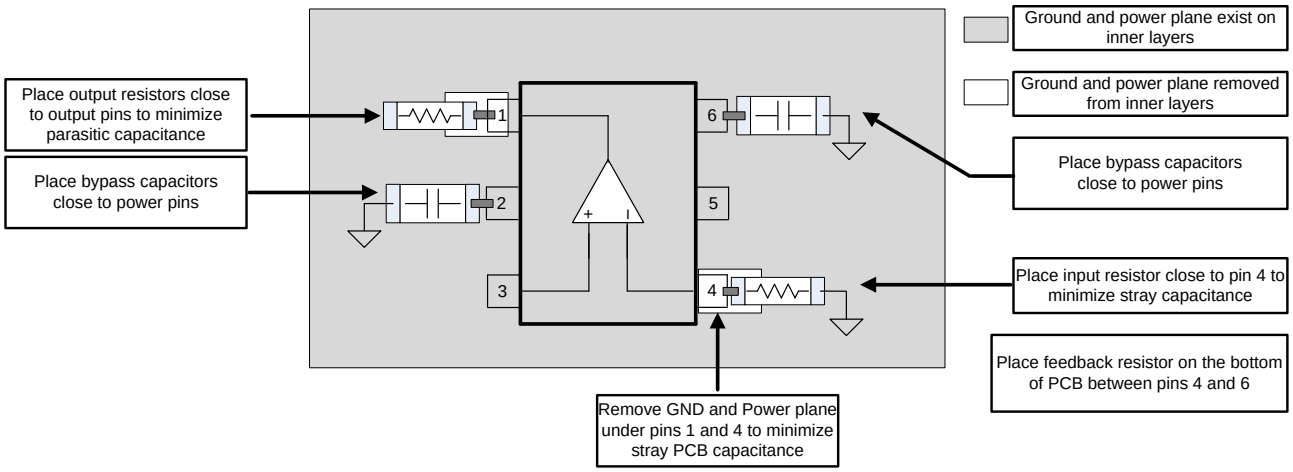


Figure 68. OPA820 Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Design-In Tools

13.1.1.1 Demonstration Fixtures

Two printed-circuit boards (PCBs) are available to assist in the initial evaluation of circuit performance using the OPA820 device in the two package options. Both of these boards are offered free of charge as unpopulated PCBs, delivered with a user's guide. Table 3 lists a summary information for these fixtures.

Table 3. Demonstration Fixtures

DEVICE NUMBER	PACKAGE	ORDERING NUMBER	USER'S GUIDE
OPA820	SOIC (8)	DEM-OPA-SO-1A	*DEM-OPA-SO-1A Demonstration Fixture*
OPA820	SOT-23 (5)	DEM-OPA-SOT-1A	*DEM-OPA-SOT-1A Demonstration Fixture*

The demonstration fixtures can be requested through the OPA820 product folder.

13.1.1.2 Macromodels and Applications Support

Computer simulation of circuit performance using SPICE is often a quick way to analyze the performance of the OPA820 device and the device circuit designs. This is particularly true for video and R_F amplifier circuits where parasitic capacitance and inductance can play a major role on circuit performance. A SPICE model for the OPA820 device is available through www.ti.com. The applications department is also available for design assistance. These models predict typical small-signal AC, transient steps, DC performance, and noise under a wide variety of operating conditions. The models include the noise terms found in the electrical specifications of the data sheet. These models do not attempt to distinguish between the package types in their small-signal AC performance.

13.1.2 Development Support

For the OPA820 PSpice Model, see SBOC048.

For the OPA820 TINA-TI Reference Design, see SBOC094.

For the OPA820 TINA-TI Spice Model, see SBOM176.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

- *ADS850 14-Bit, 10MSPS Self-Calibrating Analog-to-Digital Converter* (SBAS154)
- *DEM-OPA-SO-1A Demonstration Fixture* (SBOU009)
- *DEM-OPA-SOT-1A Demonstration Fixture* (SBOU010)
- *Measuring Board Parasitics in High-Speed Analog Design* (SBOA094)
- *Noise Analysis for High-Speed Op Amps* (SBOA066)
- *OPA2822 Dual, Wideband, Low-Noise Operational Amplifier* (SBOS188)
- *RLC Filter Design for ADC Interface Applications* (SBAA108)
- *Wideband Complementary Current Output DAC to Single-Ended Interface: Improved Matching for the Gain and Compliance Voltage Swing* (SBAA135)

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA820ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 820	Samples
OPA820IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSO	Samples
OPA820IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSO	Samples
OPA820IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSO	Samples
OPA820IDBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NSO	Samples
OPA820IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA 820	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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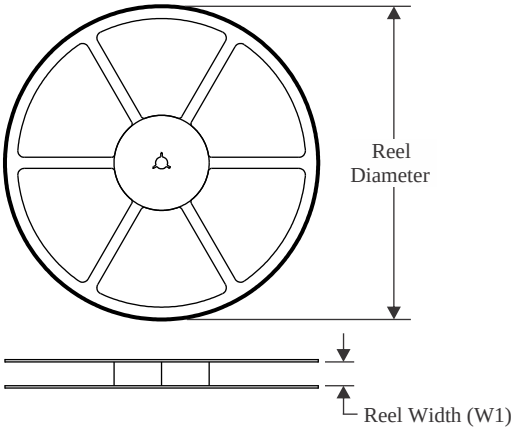
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPA820 :

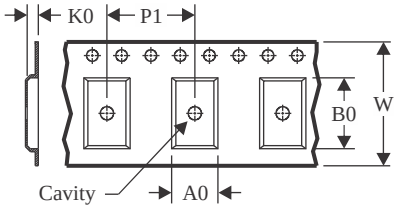
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

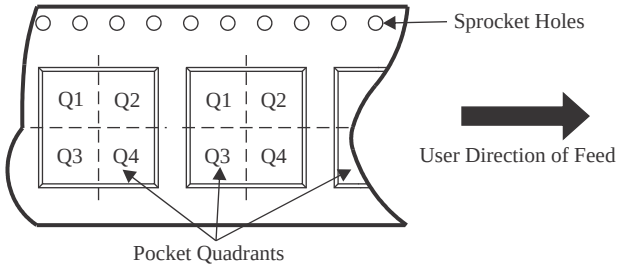


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

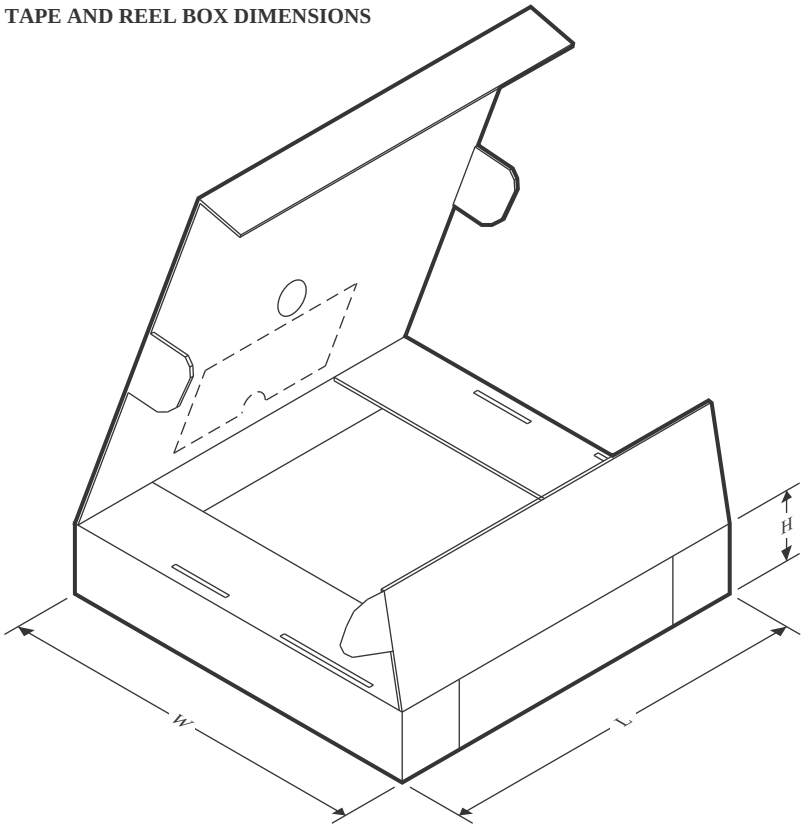
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA820IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA820IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.15	3.1	1.55	4.0	8.0	Q3
OPA820IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

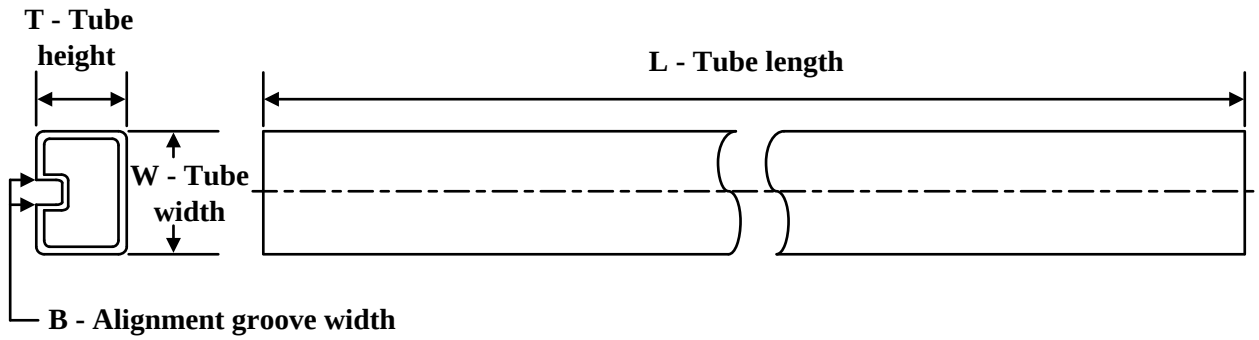
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA820IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
OPA820IDBVT	SOT-23	DBV	5	250	210.0	185.0	35.0
OPA820IDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

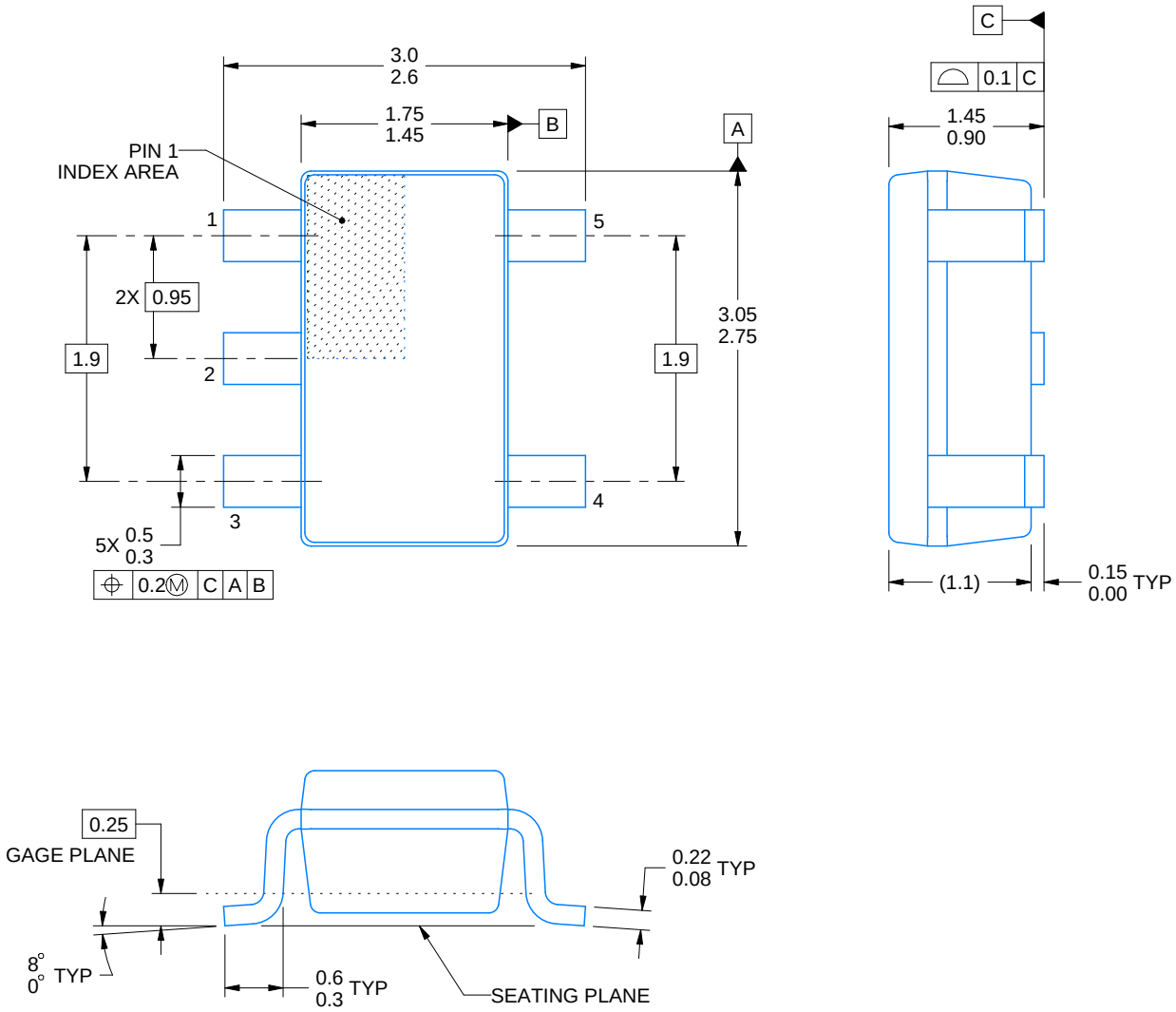
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA820ID	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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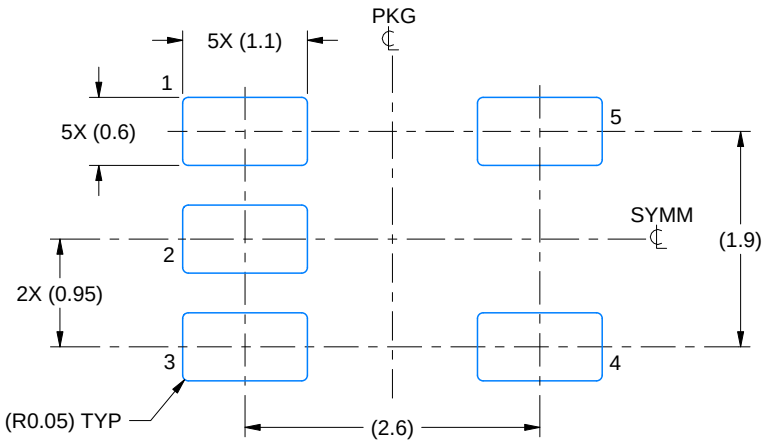
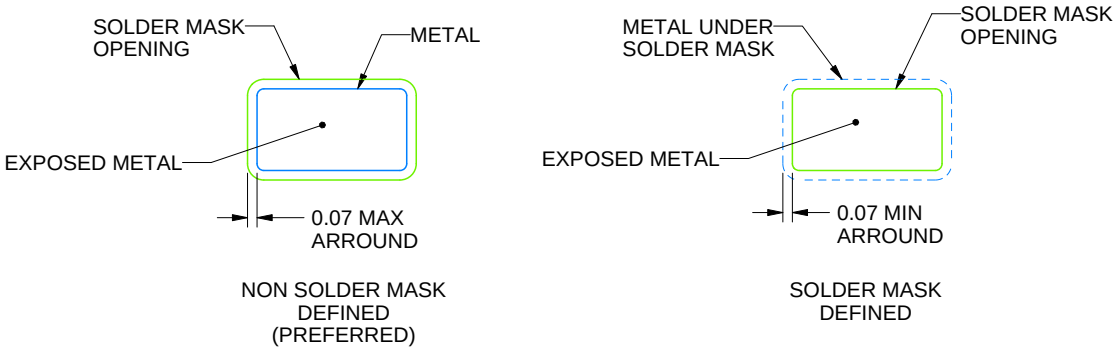
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

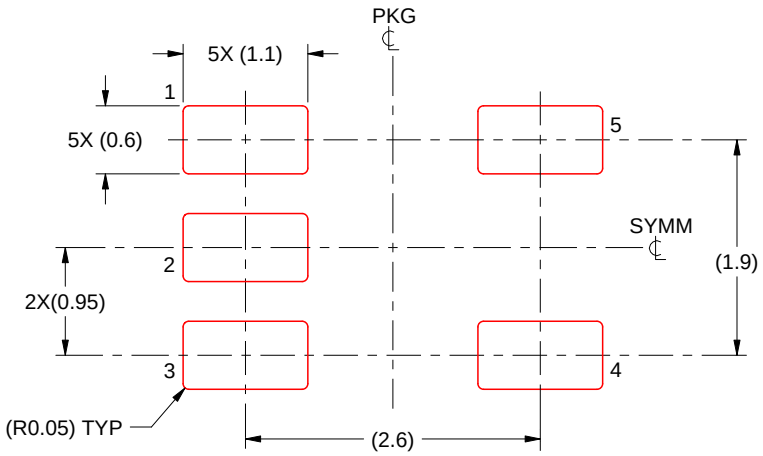


SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

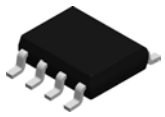


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

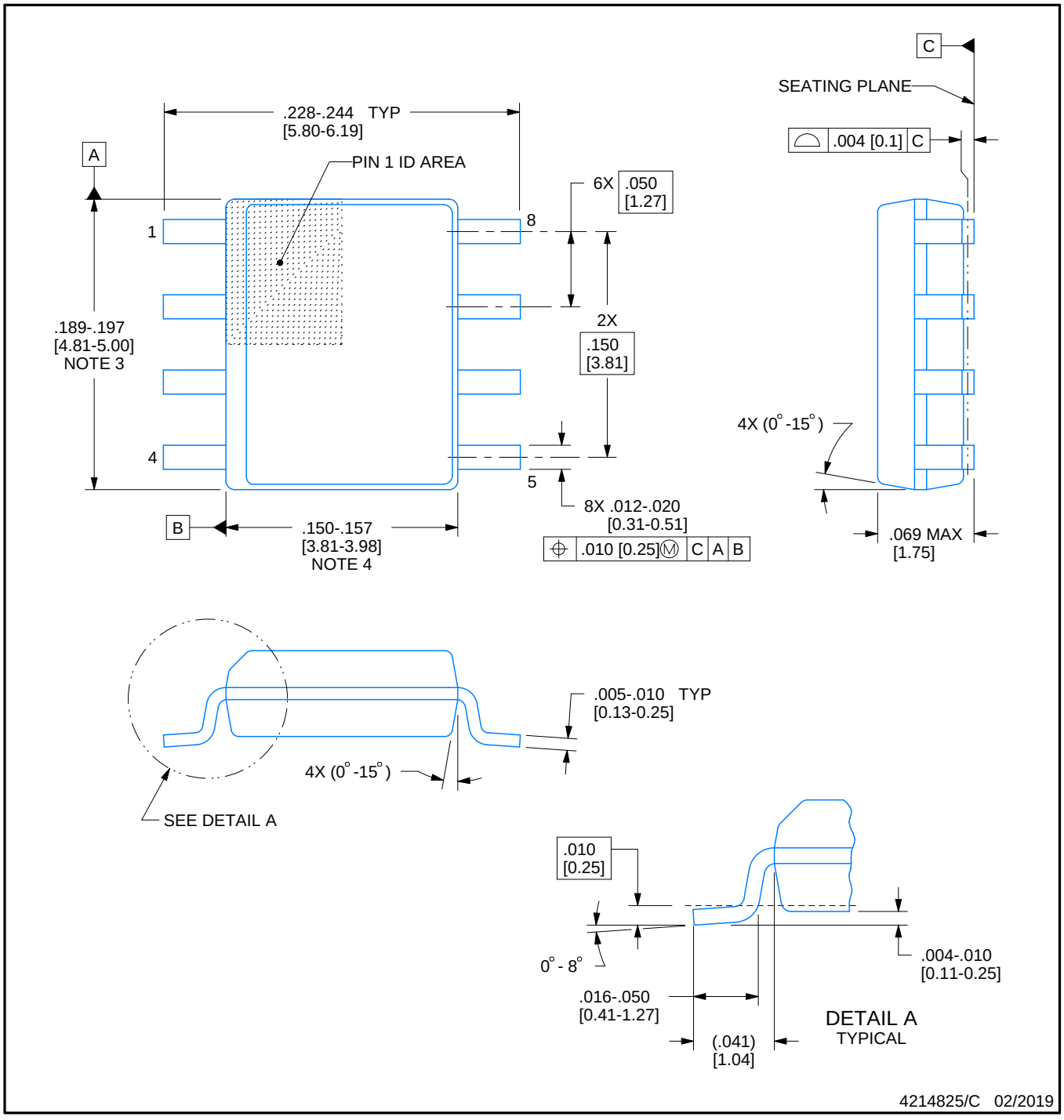


PACKAGE OUTLINE

D0008A

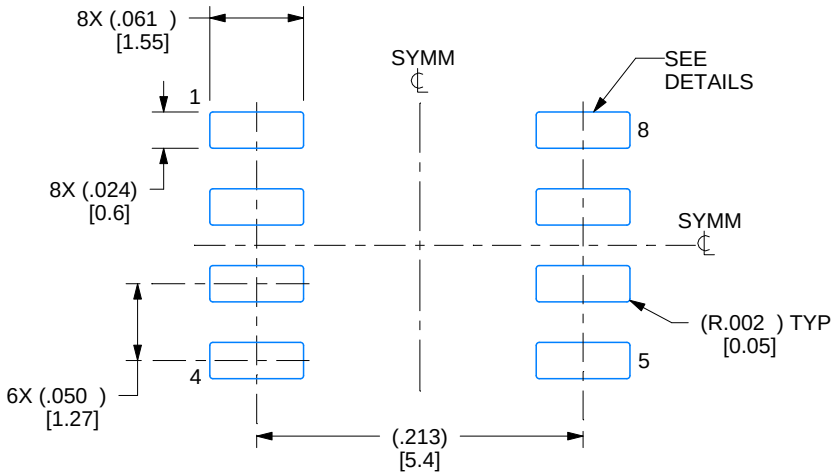
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

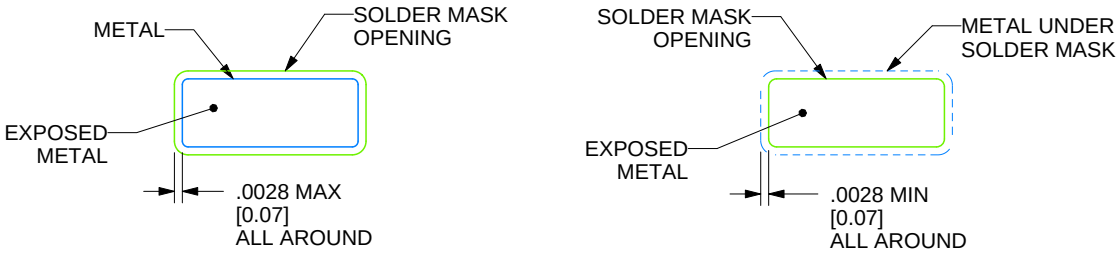


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

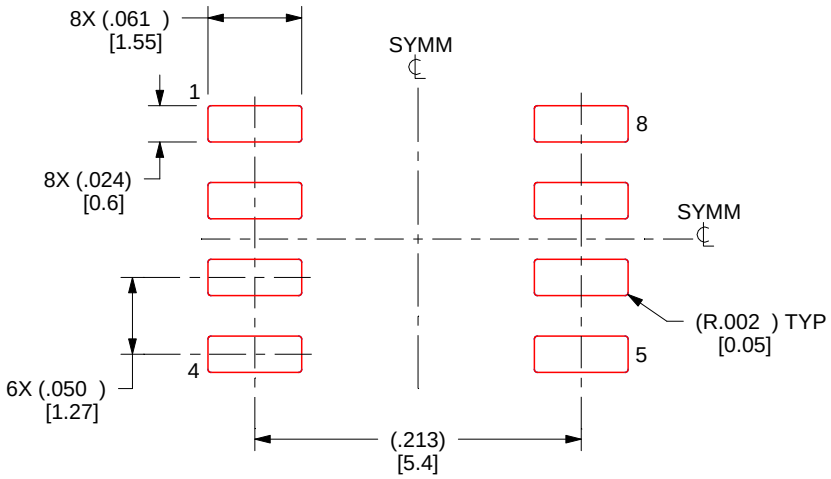
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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