LMH6881 直流至 2.4GHz、高线性度、可编程差分放大器

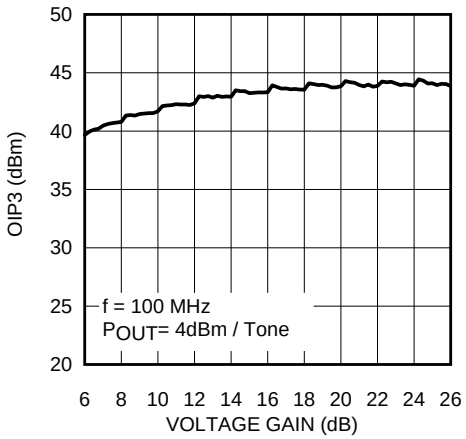
1 特性

- 小信号带宽：2400MHz
- 100MHz 时的 OIP3：44dBm
- 100MHz 时的 HD3：-100dBc
- 噪声系数：9.7dB
- 电压增益范围：6dB 至 26dB
- 电压增益步长：0.25dB
- 输入阻抗：100Ω
- 并行和串行增益控制
- 断电功能

2 应用

- 示波器前端
- 频谱分析仪增益块
- 差分模数转换器 (ADC) 驱动器
- 差分电缆驱动器
- 中频 (IF)/射频 (RF) 和基带增益块
- 医疗成像

OIP3 与电压增益间的关系



3 说明

LMH6881 是一款高速、高性能、可编程的差分放大器。 该器件具有 2.4GHz 的带宽和 44dBm OIP3 的高线性度，适合各类信号调节应用。

LMH6881 可编程差分放大器完美结合了全差分放大器和可变增益放大器的优点。 此器件无需外部电阻即可在整个增益范围内提供优异的抗噪声和失真性能，因此只需使用一个器件和一种设计就能满足需要不同增益设置的多种应用的要求。

LMH6881 是一款易于使用的放大器，既可以替代全差分、固定增益放大器，也可以替代可变增益放大器。 LMH6881 无需任何外部增益设置元件，并且支持在 6dB 到 26dB 范围内进行增益设置（增益步长为 0.25dB，小而精确）。 LMH6881 的输入阻抗为 100Ω，可轻松驱动混频器或滤波器等各类源。 LMH6881 还支持 50Ω 单端信号源，并且支持直流和交流耦合应用。

凭借并行增益控制，可将 LMH6881 以固定增益进行焊接，因此无需任何控制电路。 如果需要进行动态增益控制，则可以通过 串行外设接口 (SPI)™ 串行命令或并行引脚来更改 LMH6881。

LMH6881 由德州仪器 (TI) 的 CBiCMOS8 专有硅锗互补工艺制成，并且采用节省空间的散热增强型 24 引脚超薄型四方扁平无引线 (WQFN) 封装。 此放大器还提供了双路封装型号 LMH6882。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMH6881	WQFN (24)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

目录

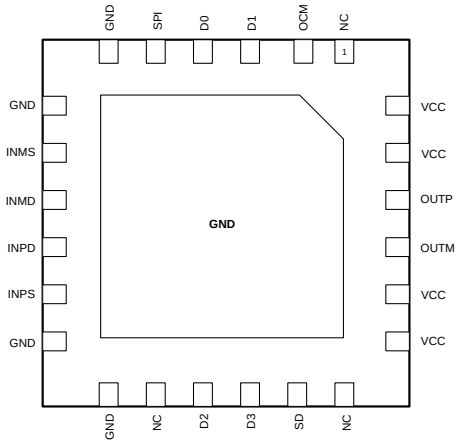
4 修订历史记录

Changes from Revision E (March 2013) to Revision F **Page**

- 已添加 *引脚配置和功能*部分，*ESD 额定值*表，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

5 Pin Configuration and Functions

RTW Package
24-Pins WQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	NC	—	
2	OCM	I	Output Common Mode, gain of 2
3	D1, SDI	I	Parallel mode = Logic control signal, position 1 or weight 2^1 SPI mode = serial data in (SDI)
4	D0, SDO	I/O	Parallel mode = Logic control signal, position 0 or weight 2^0 SPI mode = serial data out (SDO)
5	SPI	I	Serial mode control
6	GND	I/O	Ground
7	GND	I/O	Ground
8	INMS	I	Amplifier single-ended input minus swing (negative)
9	INMD	I	Amplifier differential input minus swing (negative)
10	INPD	I	Amplifier differential input plus swing (positive)
11	INPS	I	Amplifier single-ended input plus swing (positive)
12	GND	I/O	Ground
13	GND	I/O	Ground
14	NC	—	
15	D2	I	Parallel mode = Logic control signal, position 2 or weight 2^2 SPI mode = serial clock (CLK)
16	D3	I	Parallel mode = Logic control signal, position 3 or weight 2^3 SPI mode = chip select (CS)
17	SD	I	Device Shutdown
18	NC	—	
19	VCC	I/O	Power supply nominal value of 5 V
20	VCC	I/O	Power supply nominal value of 5 V
21	OUTM	O	Amplifier output minus (negative)
22	OUTP	O	Amplifier output plus (positive)
23	VCC	I/O	Power supply nominal value of 5 V
24	VCC	I/O	Power supply nominal value of 5 V

Pin Descriptions

NO.	SYMBOL	PIN CATEGORY	DESCRIPTION
ANALOG I/O			
9,10	INPD, INMD	Analog Input	Differential inputs 100 Ω
8, 11	INPS, INMS	Analog Input	Single-ended inputs 50 Ω
21, 22	OUTP, OUTM	Analog Output	Differential outputs, low impedance
POWER			
6, 7, 12, 13	GND	Ground	Ground pins. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is internally bonded to the ground pins.
19, 20, 23, 24	VCC	Power	Power supply pins. Valid power supply range is 4.75 V to 5.25 V.
Exposed Center Pad		Thermal/ Ground	Thermal management/ Ground
DIGITAL INPUTS			
5	SPI	Digital Input	0 = Parallel Mode, 1 = Serial Mode
PARALLEL MODE DIGITAL PINS, SPI = LOGIC LOW			
3, 4, 15, 16	D0, D1, D2, D3	Digital Input	Attenuator control
17	SD	Digital Input	Shutdown 0 = amp on, 1 = amp off
SERIAL MODE DIGITAL PINS, SPI= LOGIC HIGH, SPI COMPATIBLE			
4	SDO	Digital Output - Open Emitter	Serial Data Output (Requires external bias.)
3	SDI	Digital Input	Serial Data In
16	CS	Digital Input	Chip Select (active low)
15	CLK	Digital Input	Clock

6 Specifications

6.1 Absolute Maximum Ratings(1)(2)

		MIN	MAX	UNIT
Positive Supply Voltage (VCC)		−0.6	5.5	V
Differential Voltage between Any Two Grounds			< 200	mV
Analog Input Voltage Range		−0.6	5.5	V
Digital Input Voltage Range		−0.6	5.5	V
Output Short Circuit Duration (one pin to ground)			Infinite	
Junction Temperature			150	°C
Soldering Information	Infrared or Convection (30 sec)		260	°C
Storage temperature range, T_{stg}		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (VCC)	4.75	5.25	V
Differential Voltage Between Any Two Grounds		< 10	mV
Analog Input Voltage Range, AC Coupled	0	VCC	V
Temperature Range (1)	−40	85	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

6.4 Thermal Information

THERMAL METRIC (1)		LMH6881 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	16.7	
ψ_{JT}	Junction-to-top characterization parameter	0.5	
ψ_{JB}	Junction-to-board characterization parameter	16.8	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics (1)(2)(3)

The following specifications apply for single supply with VCC = 5 V, Maximum Gain (26 dB), R_L = 200 Ω, fin = 100 MHz.

		TEST CONDITIONS	MIN (4)	TYP (5)	MAX (4)	UNIT
DYNAMIC PERFORMANCE						
3 dBBW	−3-dB Bandwidth	V_{OUT}= 2 V_{PPD}		2.4		GHz
NF	Noise Figure	Source Resistance (Rs) = 100 Ω		9.7		dB
OIP3	Output Third Order Intercept Point (6)	f = 100 MHz, P_{OUT} = 4 dBm per tone, tone spacing = 1 MHz		44		dBm
		f = 200 MHz, P_{OUT} = 4 dBm per tone, tone spacing = 2 MHz		42		
OIP2	Output Second Order Intercept Point	P_{OUT}= 4 dBm per Tone, f1 =112.5 MHz, f2 = 187.5 MHz		76		dBm
IMD3	Third Order Intermodulation Products	f = 100 MHz, P_{OUT} = 4 dBm per tone, tone spacing = 1 MHz		−80		dBc
		f = 200 MHz, P_{OUT} = 4 dBm per tone, tone spacing =2 MHz		−76		
P1dB	1dB Compression Point	Output Power		17		dBm
HD2	Second Order Harmonic Distortion	f = 200 MHz, P_{OUT} = 4 dBm		−70		dBc
HD3	Third Order Harmonic Distortion	f = 200 MHz, P_{OUT} = 4 dBm		−76		dBc

(1) Electrical Table values apply only for factory testing conditions at the temperature indicated. No verification of parametric performance is indicated in the electrical tables under conditions different than those tested
(2) Negative input current implies current flowing out of the device.
(3) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(4) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(5) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(6) OIP3 is the third order intermodulation intercept point. In this data sheet OIP3 numbers are single power measurements where OIP3 = IMD3 / 2 + POUT (per tone). OIP2 is the second order intercept point where OIP2 = IMD2 + POUT (per tone). HD2 is the second order harmonic distortion and is a single tone measurement. HD3 is the third order harmonic distortion and is a single tone measurement. Power measurements are made at the amplifier output pins.

Electrical Characteristics[1][2][3] (continued)

The following specifications apply for single supply with VCC = 5 V, Maximum Gain (26 dB), R_L = 200 Ω, fin = 100 MHz.

		TEST CONDITIONS	MIN[4]	TYP[5]	MAX[4]	UNIT
CMRR	Common Mode Rejection Ratio[7]	Pin = −15 dBm, f = 100 MHz		−40		dBc
SR	Slew Rate			6000		V/us
	Output Voltage Noise	Maximum Gain f > 1 MHz		47		nV/√Hz
	Input Referred Voltage Noise	Maximum Gain f > 1 MHz		2.3		nV/√Hz
ANALOG I/O						
R_{IN}	Input Resistance	Differential, INPD to INMD		100		Ω
R_{IN}	Input Resistance	Single Ended, INPS or INPD, 50-Ω termination on unused input		50		Ω
V_{ICM}	Input Common Mode Voltage	Self Biased		2.5		V
	Maximum Input Voltage Swing	Volts peak to peak, differential		2.85		V_{PPD}
	Maximum Differential Output Voltage Swing	Differential, f < 10 MHz		6		V_{PPD}
R_{OUT}	Output Resistance	Differential, f = 100 MHz		0.4		Ω
GAIN PARAMETERS						
	Maximum Voltage Gain	Parallel Inputs (INPD and INMD), Rs = 100 Ω		26		dB
		Single-ended input (INMS or INPS), 50-Ω Rs and 50-Ω termination on unused input.		26.6		
	Minimum Gain	Parallel Inputs, Rs = 100 Ω		6		dB
	Gain Steps	Available using SPI interface		80		
		Available using parallel interface		10		
	Gain Step Size	Available using SPI interface		0.25		dB
		Available using parallel interface		2		
	Gain Step Error	Any two adjacent steps over entire range		±0.125		dB
	Gain Step Phase Shift	Any two adjacent steps over entire range		±3		Degrees
	Gain Step Switching Time			20		ns
	Enable/ Disable Time	Settled to 90% level		15		ns
POWER REQUIREMENTS						
ICC	Supply Current			100	135	mA
P	Power			0.5		W
ICCD	Disabled Supply Current			15		mA
ALL DIGITAL INPUTS						
	Logic Compatibility	TTL, 2.5-V CMOS, 3.3-V CMOS, 5-V CMOS				
VIL	Logic Input Low Voltage			0.4		V
VIH	Logic Input High Voltage			2.0 - 5.0		V
IIH	Logic Input High Input Current			−9		µA
IIL	Logic Input Low Input Current			−47		µA
PARALLEL MODE TIMING						
t_{GS}	Setup Time			3		ns
t_{GH}	Hold Time			3		ns
SERIAL MODE						
f_{CLK}	SPI Clock Frequency	50% duty cycle	10	50		MHz

(7) CMRR is defined as the differential response at the output in response to a common mode signal at the input.

6.6 Typical Characteristics

(Unless otherwise specified, the following conditions apply: T_A = 25°C, VCC = 5 V, R_L = 200 Ω, Maximum Gain, Differential Input). LMH6882 devices have been used for some typical performance plots.

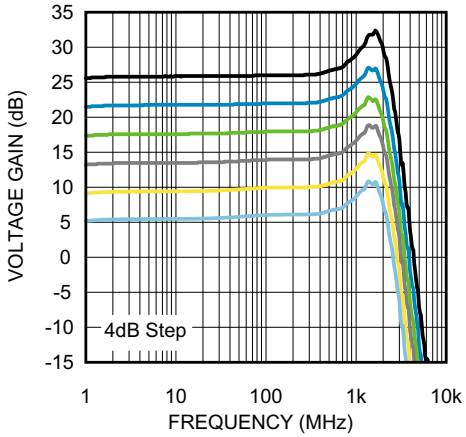


Figure 1. Frequency Response over Gain Range, 4-dB Steps

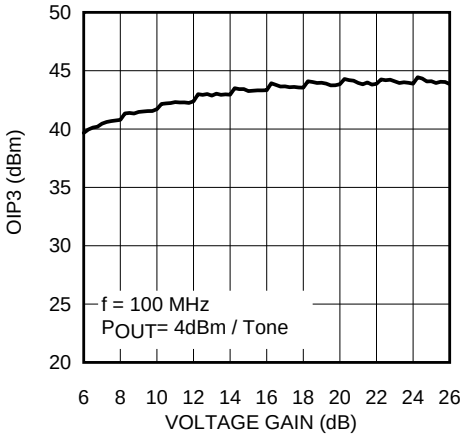


Figure 2. OIP3 vs Voltage Gain

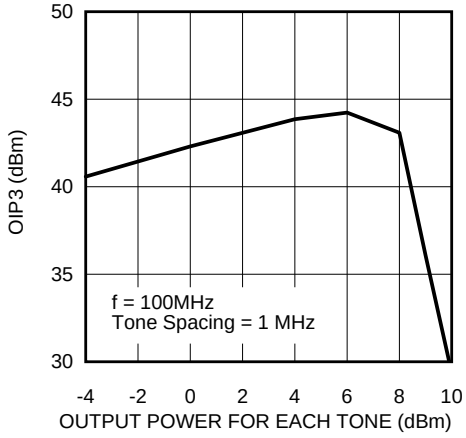


Figure 3. OIP3 vs Output Power

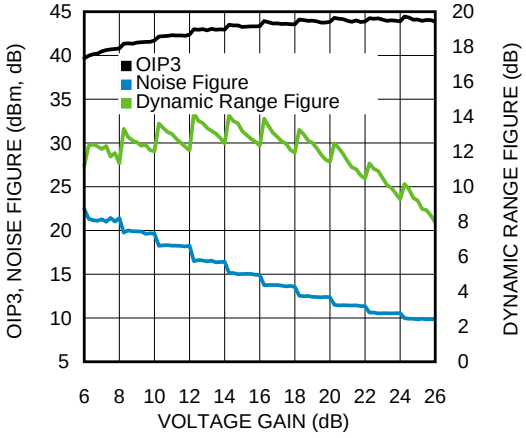


Figure 4. Dynamic Range Figure vs Voltage Gain

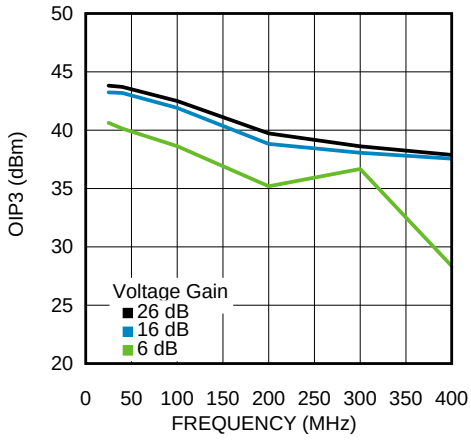


Figure 5. OIP3 vs Frequency

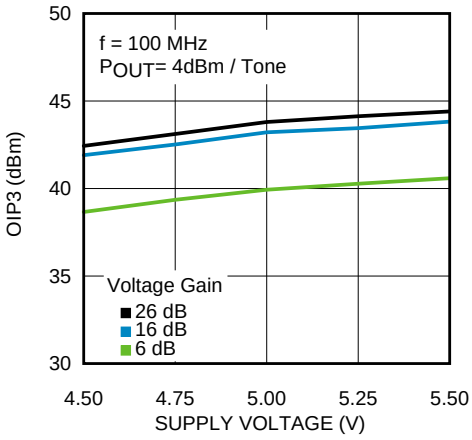


Figure 6. OIP3 vs Supply Voltage

Typical Characteristics (continued)

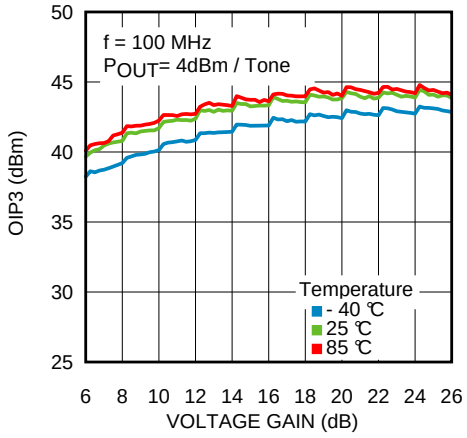


Figure 7. OIP3 vs Temperature

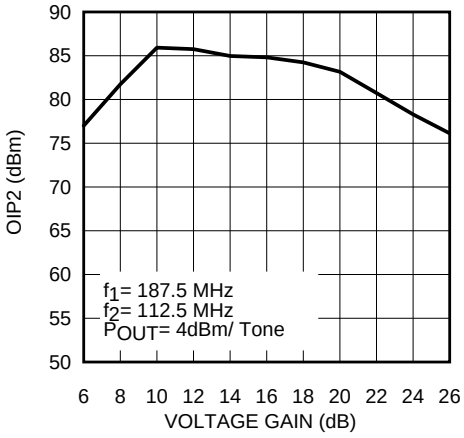


Figure 8. OIP2 vs Voltage Gain

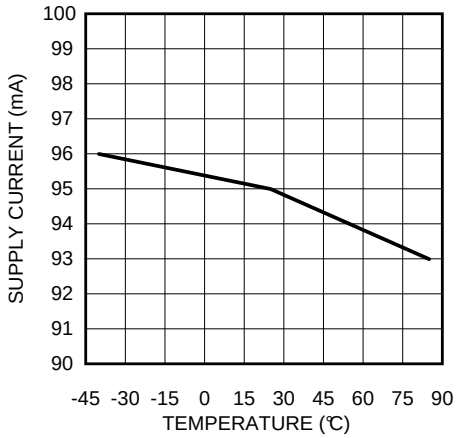


Figure 9. Supply Current vs Temperature

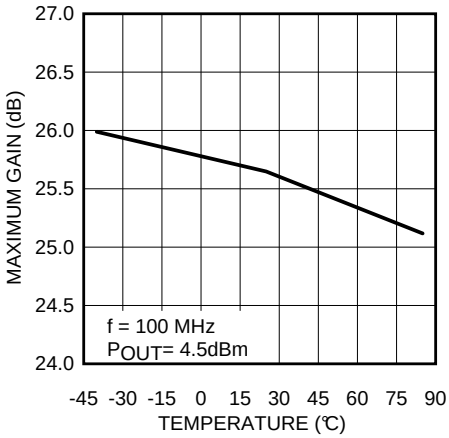


Figure 10. Maximum Voltage Gain vs Temperature

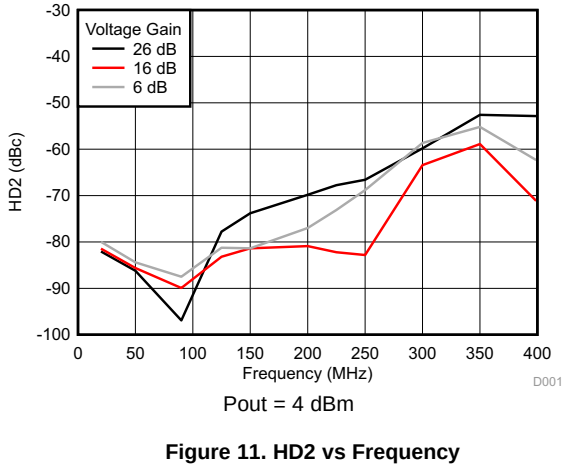


Figure 11. HD2 vs Frequency

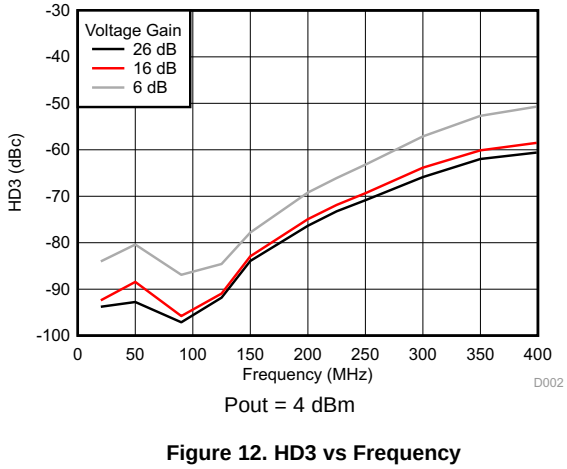


Figure 12. HD3 vs Frequency

Typical Characteristics (continued)

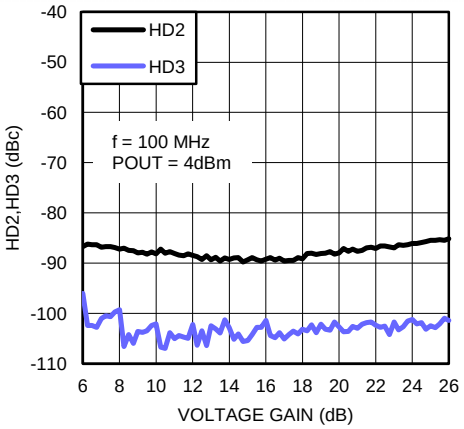


Figure 13. HD2 and HD3 vs Voltage Gain

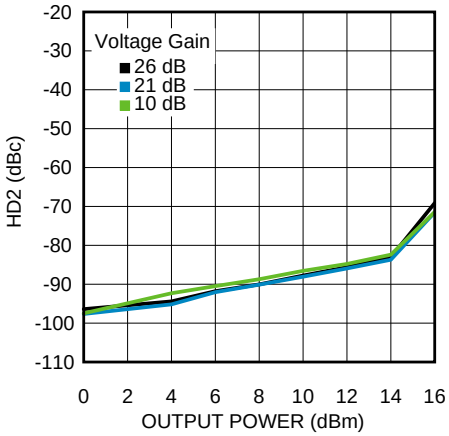


Figure 14. HD2 vs Output Power

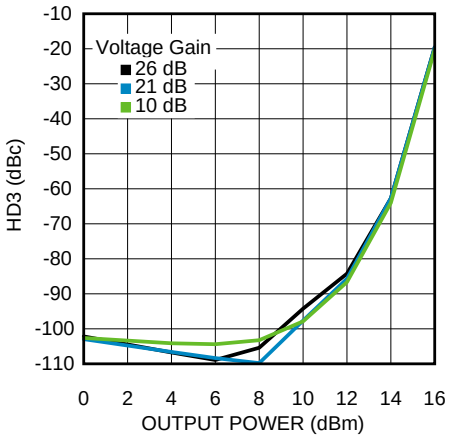


Figure 15. HD3 vs Output Power

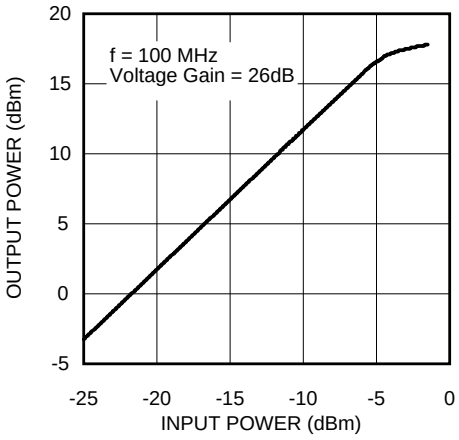


Figure 16. Output Power vs Input Power

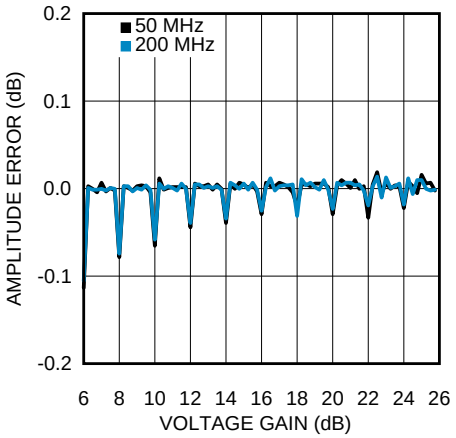


Figure 17. Gain Step Amplitude Error

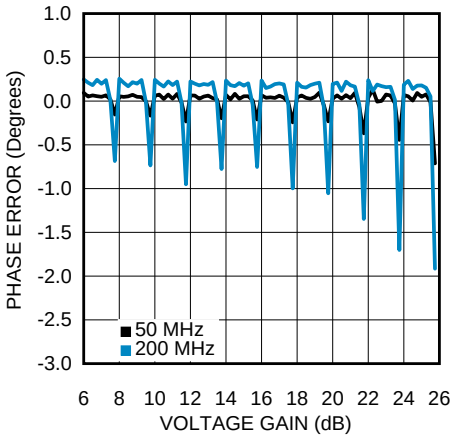


Figure 18. Gain Step Phase Error

Typical Characteristics (continued)

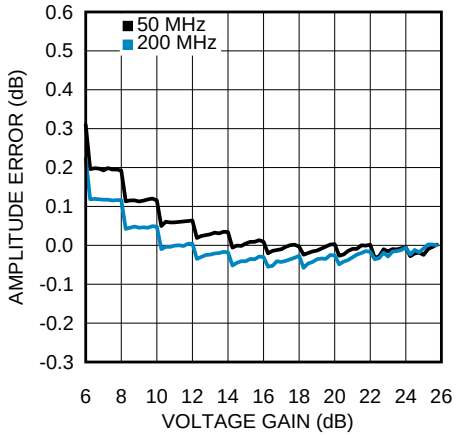


Figure 19. Cumulative Amplitude Error

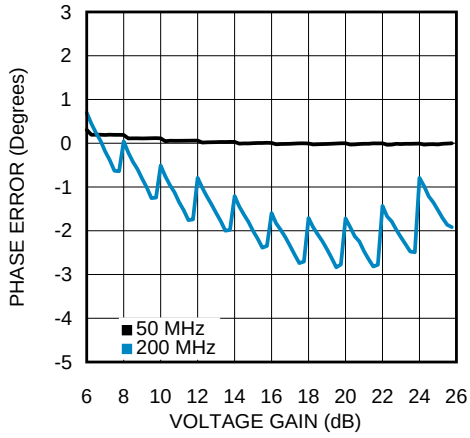


Figure 20. Cumulative Phase Error

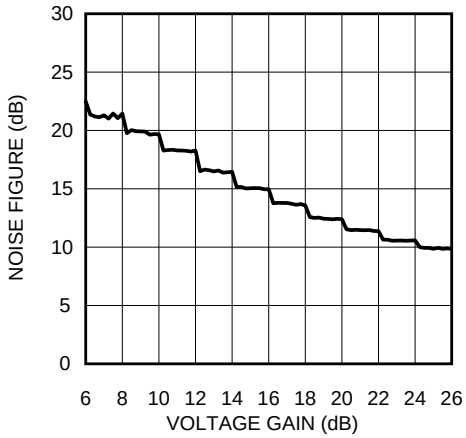


Figure 21. Noise Figure vs Voltage Gain

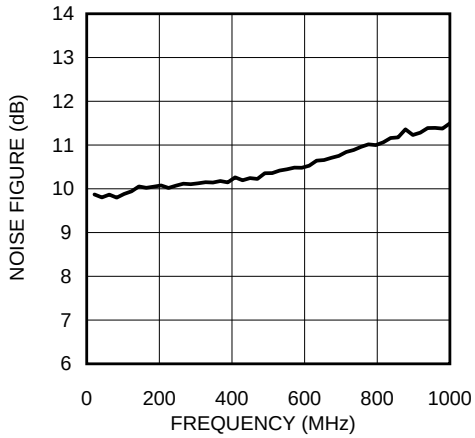


Figure 22. Noise Figure vs Frequency

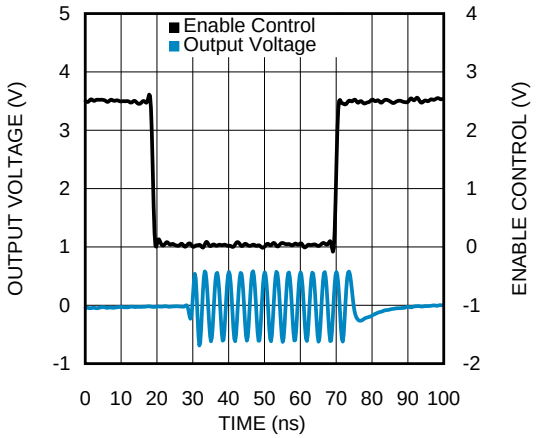


Figure 23. Channel Enable Control Timing Behavior

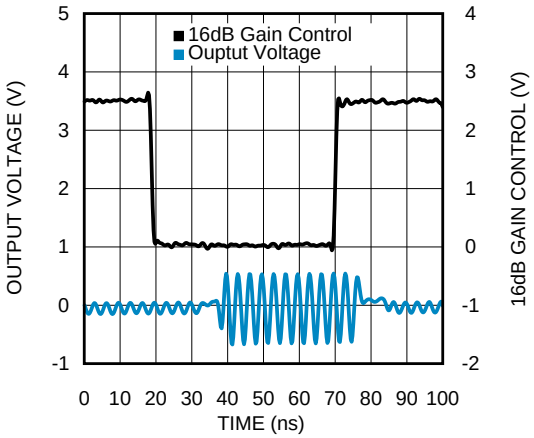


Figure 24. 16-dB Gain Control Timing Behavior

Typical Characteristics (continued)

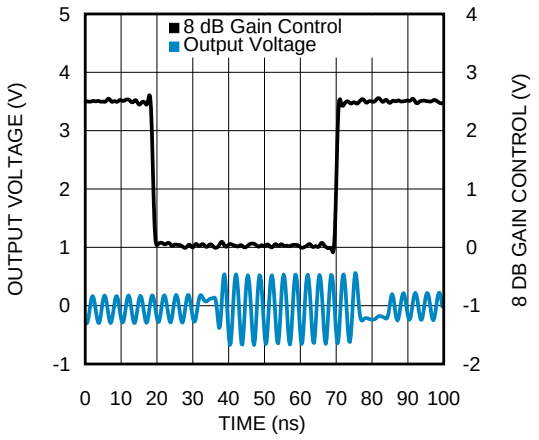


Figure 25. 8-dB Step Control Timing Behavior

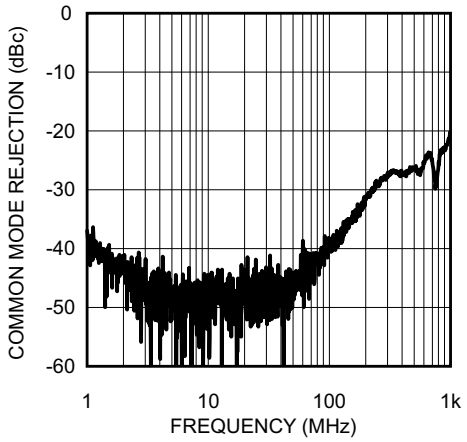


Figure 26. Common Mode Rejection (Sdc21) vs Frequency

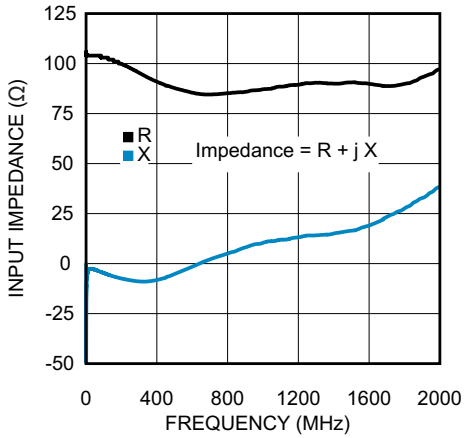


Figure 27. Input Impedance

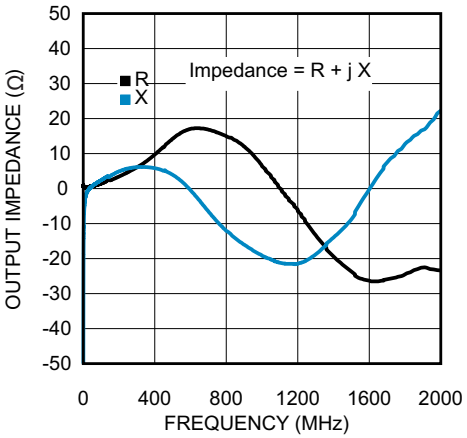


Figure 28. Output Impedance

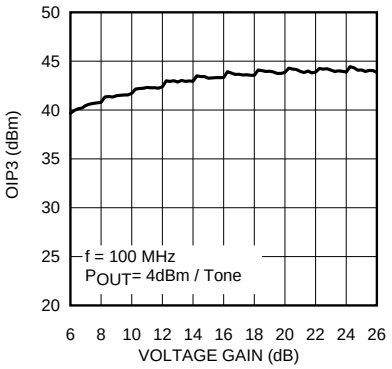


Figure 29. OIP3 Overvoltage Gain Range

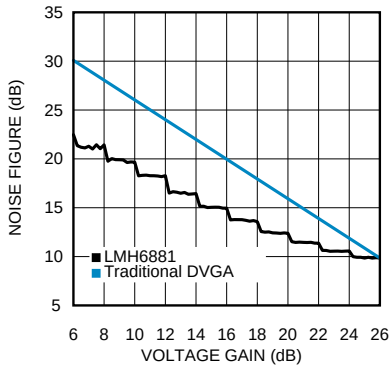


Figure 30. Noise Figure Overvoltage Gain Range DVGA Response Shown for Comparison

6.6.1 Single-Ended Input

(Unless otherwise specified, the following conditions apply: T_A = 25°C, VCC = 5 V, R_L = 200 Ω, Maximum Gain.)

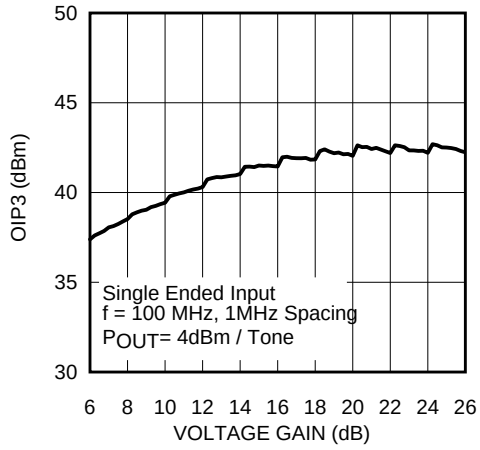


Figure 31. OIP3 vs Voltage Gain

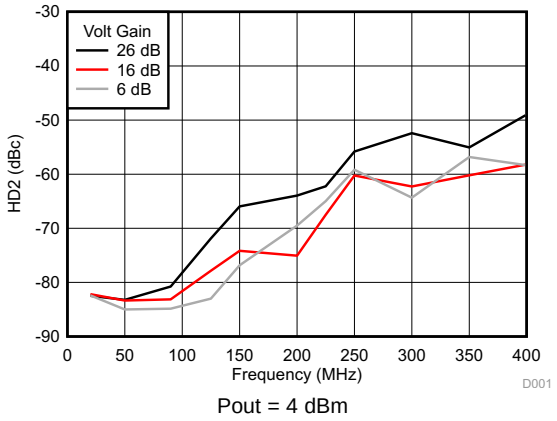


Figure 32. HD2 vs Frequency

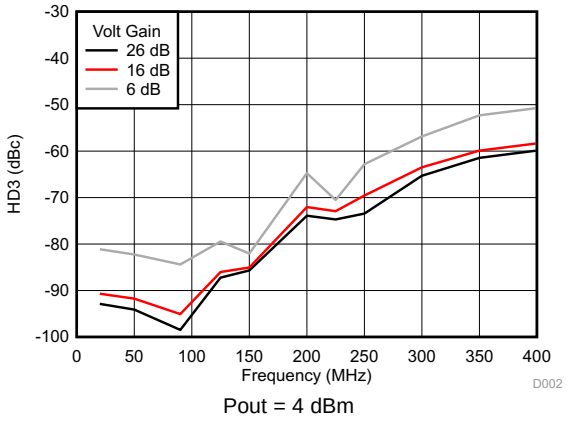


Figure 33. HD3 vs Frequency

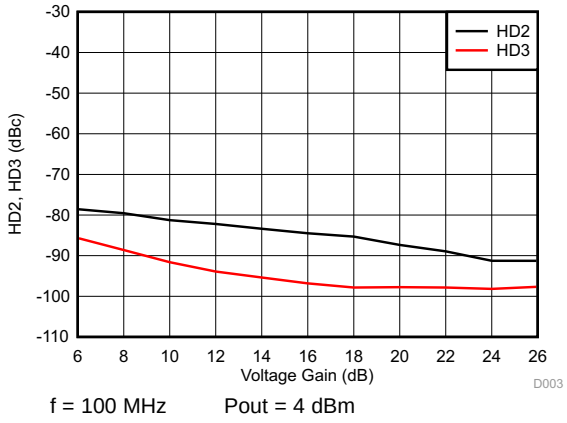


Figure 34. HD2 and HD3 vs Voltage Gain

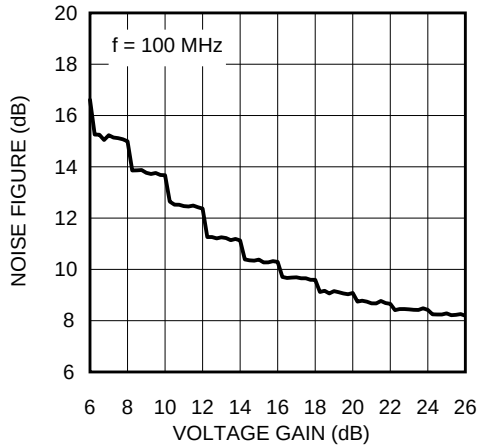


Figure 35. Noise Figure vs Voltage Gain

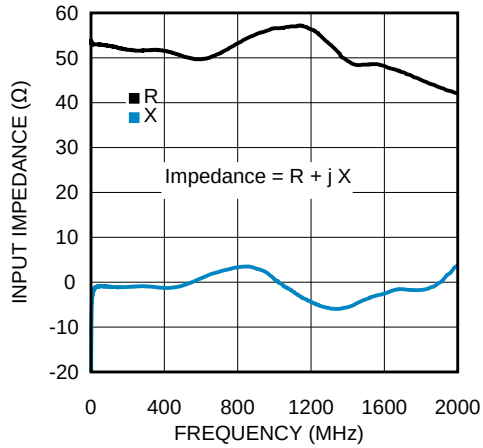


Figure 36. Single-Ended Input Impedance

7 Detailed Description

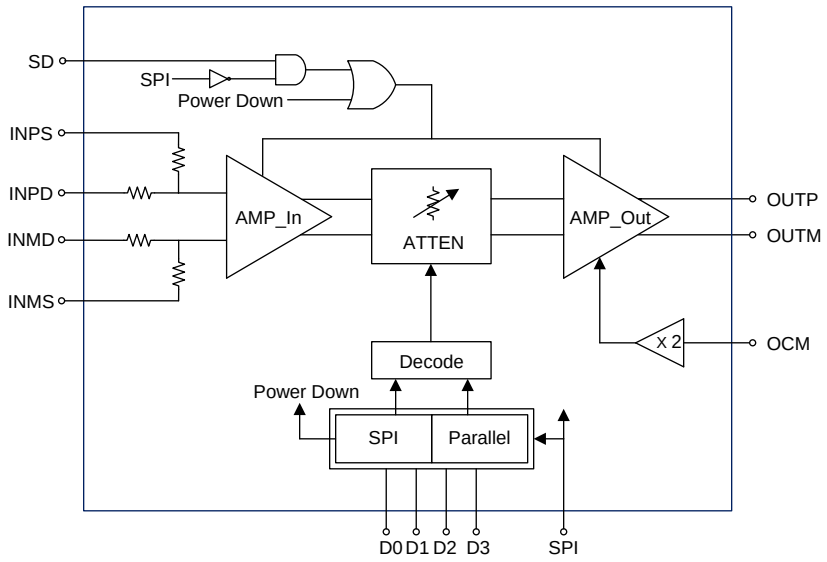
7.1 Overview

The LMH6881 has been designed to replace traditional, fixed-gain amplifiers, as well as variable-gain amplifiers, with an easy-to-use device which can be flexibly configured to many different gain settings while maintaining excellent performance over the entire gain range. Many systems can benefit from this programmable-gain, DC-capable, differential amplifier. Last-minute design changes can be implemented immediately, and external resistors are not required to set the gain.

The LMH6881 is a fully differential amplifier optimized for signal-path applications up to 1000 MHz. The LMH6881 has a 100-Ω input impedance and a low (less than 0.5 Ω) impedance output. The gain is digitally controlled over a 20-dB range from 26 dB to 6 dB. The LMH6881 is designed to replace fixed-gain differential amplifiers with a single, flexible-gain device. It has been designed to provide good noise figure and OIP3 over the entire gain range. This design feature is highlighted by the DRF of merit. Traditional variable gain amplifiers generally have the best OIP3 and NF performance at maximum gain only.

Gain control is enabled with a parallel or a serial-control interface, and as a result, the amplifier can also serve as a digitally controlled variable-gain amplifier (DVGA) for automatic gain-control applications. Figure 37 and Figure 38 show typical implementations of the amplifier.

7.2 Functional Block Diagram



7.3 Feature Description

The LMH6881 has three functional stages, a low-noise amplifier, followed by a digital attenuator, and a low-distortion, low-impedance output amplifier. The amplifier has four signal-input pins, to accommodate both differential signals and single-ended signals. The amplifier has an OCM pin used to set the output common mode voltage. There is a gain of 2 on this pin so that 1.25 V applied on that pin will place the output common mode at 2.5 V.

Feature Description (continued)

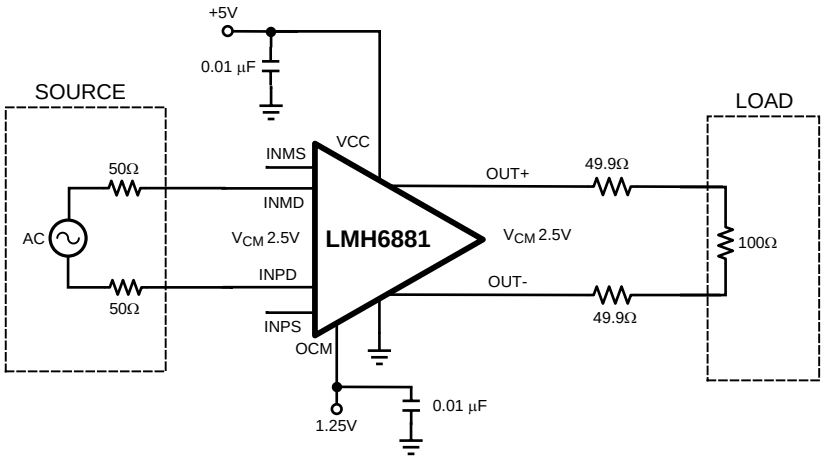


Figure 37. Typical Implementation With a Differential Input Signal

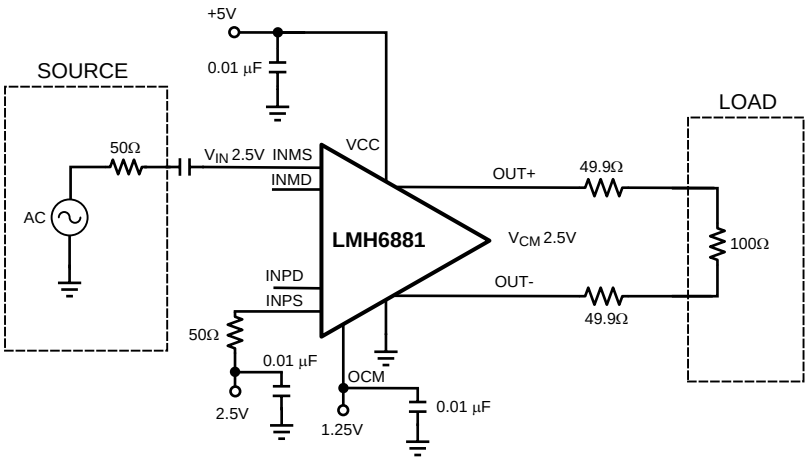


Figure 38. Typical Implementation With a Single-Ended Input Signal

7.4 Device Functional Modes

The LMH6881 will support two modes of control for its gain: a parallel mode and a serial mode (SPI compatible). Parallel mode is fastest and requires the most board space for logic line routing. Serial mode is compatible with existing SPI-compatible systems. The device has gain settings covering a range of 20 dB. In parallel mode, only 2-dB steps are available. The serial interface should be used for finer gain control of 0.25 dB for a gain between 6 dB and 26 dB of voltage gain. If fixed gain is desired, the digital pins can be strapped to ground or VCC, as required.

The device also supports two modes of power down control to enable power savings when the amplifier is not being used: using the SD pin (when SPI pin = Logic 0) and the power-down register (when SPI pin = Logic 1).

7.5 Programming

7.5.1 Digital Control of the Gain and Power-Down Pins

The LMH6881 was designed to interface with 2.5-V to 5-V CMOS logic circuits. If operation with 5-V logic is required, care should be taken to avoid signal transients exceeding the supply voltage of the amplifier. Long, unterminated digital signal traces should be avoided. Signal voltages on the logic pins that exceed the device power supply voltage may trigger ESD protection circuits and cause unreliable operation. Some digital input-output pins have different functions depending on the digital control mode. Table 1 shows the mapping of the digital pins. These functions for each pin will be described in the sections *Parallel Interface* and *SPI-Compatible Serial Interface*.

Table 1. Pins With Dual Functions

Pin	SPI = 0	SPI = 1
3	D1	SDI
4	D0	SDO(1)
15	D2	CLK
16	D3	CS (active low)

(1) Pin 4 requires external bias. See *SPI-Compatible Serial Interface* section for Details.

7.5.1.1 Parallel Interface

Parallel mode offers the fastest gain update capability with the drawback of requiring the most board space dedicated to control lines. To place the LMH6881 into parallel mode the SPI pin (pin 5) is set to the logical zero state. Alternately the SPI pin can be connected directly to ground. The SPI pin has a weak internal resistor to ground. If left unconnected, the amplifier will operate in parallel mode.

In parallel mode the gain can be changed in 2-dB steps with a 4-bit gain control bus. The attenuator control pins are internally biased to logic high state with weak pull-up resistors, with the exception of D0 which is biased low due to the shared SDO function. If the control bus is left unconnected, the amplifier gain will be set to 6 dB. Table 2 shows the gain of the amplifier when controlled in parallel mode.

Table 2. Amplifier Gain for All Control Pin Combinations

CONTROL PINS LOGICAL LEVEL IN PARALLEL MODE					
D3	D2	D1	D0	DECIMAL VALUE	AMPLIFIER VOLTAGE GAIN [dB]
1	X	1	X	10 - 15	6
1	0	0	1	9	8
1	0	0	0	8	10
0	1	1	1	7	12
0	1	1	0	6	14
0	1	0	1	5	16
0	1	0	0	4	18
0	0	1	1	3	20
0	0	1	0	2	22
0	0	0	1	1	24
0	0	0	0	0	26

For fixed-gain applications the attenuator-control pins should be connected to the desired logic state instead of relying on the weak internal bias. Data from the gain-control pins directly drive the amplifier gain circuits. To minimize gain change glitches all gain pins should be driven with minimal skew. If gain-pin timing is uncertain, undesirable transients can be avoided by using the shutdown pin to disable the amplifier while the gain is changed. Gain glitches are most likely to occur when multiple bits change value for a small gain change, such as the gain change from 10 dB to 12 dB which requires changing all 4 gain-control pins.

A shutdown pin (SD == 0, amplifier on, SD == 1, amplifier off) is provided to reduce power consumption by disabling the highest power portions of the amplifier. The digital control circuit is not shut down and will preserve the last active gain setting during the disabled state. See the *Typical Characteristics* section for disable and enable timing information. The SD pin is functional in parallel mode only and disabled in serial mode.

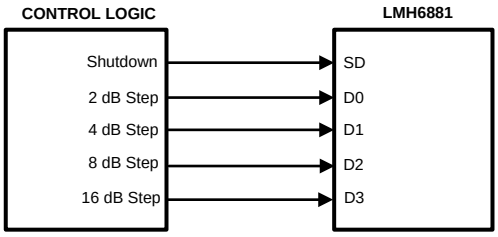


Figure 39. Parallel Mode Connection

7.5.1.2 SPI-Compatible Serial Interface

The serial interface allows a great deal of flexibility in gain programming and reduced board complexity. The LMH6881 serial interface is a generic 4-wire synchronous interface that is compatible with SPI-type interfaces that are used on many microcontrollers and DSP controllers. Using only four wires, the SPI mode offers access to the 0.25-dB gain steps of the amplifier.

For systems where gain is changed only infrequently, or where only slower gain changes are required, serial mode is the best choice. To place the LMH6881 into serial mode the SPI pin (Pin 5) should be put into the logic high state. Alternatively the SPI pin can be connected directly to the 5-V supply bus. In this configuration the pins function as shown in Table 1. The SPI interface uses the following signals: clock input (CLK), serial data in (SDI), serial data out (SDO), and serial chip select (CS). The chip-select pin is active low meaning the device is selected when the pin is low.

The SD pin is inactive in the serial mode. This pin can be left disconnected for serial mode. The SPI interface has the ability to shut down the amplifier without using the SD pin.

The CLK pin is the serial clock pin. It is used to register the input data that is presented on the SDI pin on the rising edge and to source the output data on the SDO pin on the falling edge. The user may disable clock and hold it in the low state, as long as the clock pulse-width minimum specification is not violated when the clock is enabled or disabled. The clock pulse-width minimum is equal to one setup plus one hold time, or 6 ns.

The CS pin is the chip-select pin. This pin is active low; the chip is selected in the logic low state. Each assertion starts a new register access - that is, the SDATA field protocol is required. The user is required to deassert this signal after the 16th clock. If the CS pin is deasserted before the 16th clock, no address or data write will occur. The rising edge captures the address just shifted in and, in the case of a write operation, writes the addressed register. There is a minimum pulse-width requirement for the de-asserted pulse, which is specified in the *Specifications* section.

The SDI pin is the input pin for the serial data. Each write cycle is 16-bits long.

The SDO pin is the data output pin. This output is normally at a high impedance state, and is driven only when CS is asserted. Upon CS assertion, contents of the register addressed during the first byte are shifted out with the second 8 SCLK falling edges. The SDO pin is a current output and requires external bias resistor to develop the correct logic voltage. See Figure 41 for details on sizing the external bias resistor. Resistor values of 180 Ω to 400 Ω are recommended. The SDO pin can source 10 mA in the logic high state. With a bias resistor of 250 Ω the logic 1 voltage would be 2.5 V. In the logic 0 state, the SDO output is off and no current flows, so the bias resistor will pull the voltage to 0 V.

Each serial interface write access cycle is exactly 16 bits long as shown in Figure 40.

The external bias resistor means that in the high-impedance state the SDO pin impedance is equal to the external bias resistor value. If busing multiple SPI devices make sure that the SDO pins of the other devices can drive the bias resistor.

The serial interface has four registers with address [0] to address [3]. Table 3 shows the content of each SPI register. Registers 0 and 1 are read only. Registers 2 and 3 are read/write and control the gain and power of the amplifier. Table 4 shows the data format of register 2 and Table 5 shows the data format of register 3.

Table 3. SPI Registers

Address	Read/Write	Name	Description	Default value [Hex]
0	R	Revision ID	Revision of the product	1 (first revision)
1	R	Product ID	Identification of the product	20
2	R/W	Power down	Power up/down of the amplifier	0
3	R/W	Attenuation	Attenuation control	50

Table 4. Register 2 Definition

7	6	5	4	3	2	1	0
Reserved					OFF = 1,1: ON = 0,0		Reserved

Table 5. Register 3 Definition

7	6	5	4	3	2	1	0
Reserved	16dB	8dB	4dB	2dB	1dB	0.5dB	0.25dB
	Gain [dB] = 26- (Register3 * 0.25); valid range is 0 to 80 in decimal.						

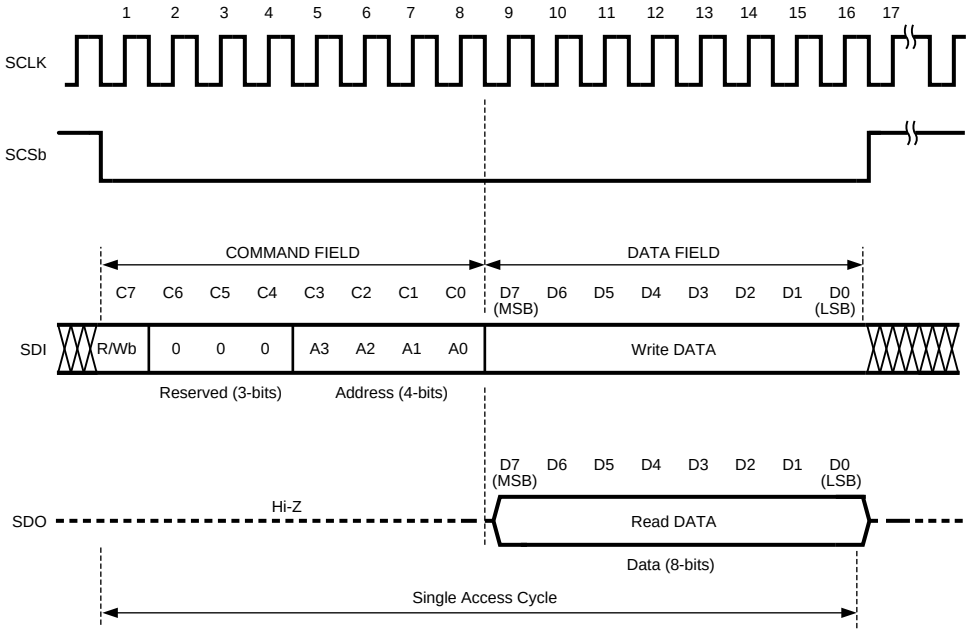


Figure 40. Serial Interface Protocol (SPI Compatible)

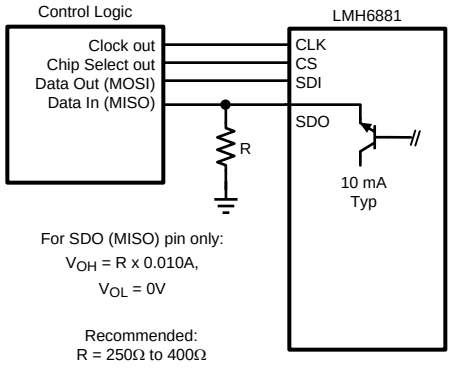


Figure 41. Internal Operation of the SDO Pin

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input Characteristics

The LMH6881 has internally terminated inputs. The INMD and INPD pins are intended to be the differential input pins and have an internal 100-Ω resistive termination. An example differential circuit is shown in Figure 37. When using the differential inputs, the single-ended inputs should be left disconnected.

The INMS and INPS pins are intended to be used for single-ended inputs and have been designed to support single-ended termination of 50 Ω working as an active termination. For single-ended signals an external 50-Ω resistor is required as shown in Figure 38. When using the single-ended inputs, the differential inputs should be left disconnected.

All of the input pins are self biased to 2.5 V. When using the LMH6881 for DC-coupled applications it is possible to externally bias the input pins to voltages from 1.5 V to 3.5 V. Performance is best at the 2.5-V level specified. Performance will degrade slightly as the common mode shifts away from 2.5 V.

The first stage of the LMH6881 is a low-noise amplifier that can accommodate a maximum input signal of 2 V_{ppd} on the differential input pins and 1 V_{pp} on either of the single-ended pins. Signals larger than this will cause severe distortion. Although the inputs are protected against ESD, sustained electrical overstress will damage the part. Signal power over 13 dBm should not be applied to the amplifier differential inputs continuously. On the single-ended pins the power limit is 10 dBm for each pin.

8.1.2 Output Characteristics

The LMH6881 has a low-impedance output very similar to a traditional Op-amp output. This means that a wide range of loads can be driven with good performance. Matching load impedance for proper termination of filters is as easy as inserting the proper value of resistor between the filter and the amplifier (See Figure 47 for example.) This flexibility makes system design and gain calculations very easy. By using a differential output stage the LMH6881 can achieve large voltage swings on a single 5-V supply. This is illustrated in Figure 42. This figure shows how a voltage swing of 4 V_{PPD} is realized while only swinging 2 V_{PP} on each output. A 1-V_P signal on one branch corresponds to 2 V_{PP} on that branch and 4 V_{PPD} when looking at both branches (positive and negative).

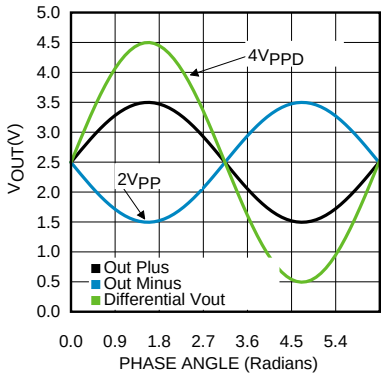


Figure 42. Differential Output Voltage

Application Information (continued)

The LMH6881 has been designed for both AC-coupled and DC-coupled applications. To give more flexibility in DC-coupled applications, the common mode voltage of the output pins is set by the OCM pin. The OCM pin needs to be driven from an external low-noise source. If the OCM pin is left floating, the output common mode is undefined, and the amplifier will not operate properly.

There is a DC gain of 2 between the OCM pin and the output pins so that the OCM voltage should be from 1 V to 1.5 V. This will set the output common mode voltage from 2 V to 3 V. Output common mode voltages outside the recommended range will exhibit poor voltage swing and distortion performance. The amplifier will give optimum performance when the output common mode is set to half of the supply voltage (2.5 V or 1.25 V at the OCM pin).

The ability of the LMH6881 to drive low-impedance loads while maintaining excellent OIP3 performance creates an opportunity to greatly increase power gain and drive low-impedance filters. This gives the system designer much needed flexibility in filter design. In many cases using a lower impedance filter will provide better component values for the filter. Another benefit of low-impedance filters is that they are less likely to be influenced by circuit board parasitic reactances such as pad capacitance or trace inductance. The output stage is a low-impedance voltage amplifier, so voltage gain is constant over different load conditions. Power gain will change based on load conditions. See Figure 43 for details on power gain with respect to different load conditions. The graph was prepared for the 26-dB voltage gain. Other gain settings will behave similarly.

All measurements in this data sheet, unless specified otherwise, refer to voltage or power at the device output pins. For instance, in an OIP3 measurement the power out will be equal to the output voltage at the device pins squared, divided by the total load voltage. In back terminated applications, power to the load would be 3 dB less. Common back terminated applications include driving a matched filter or driving a transmission line.

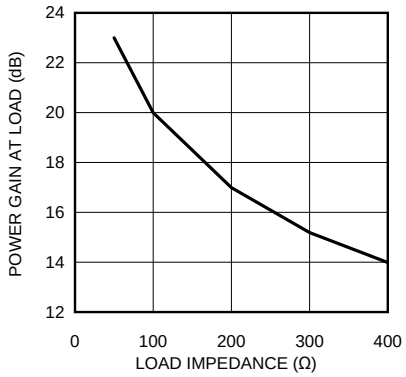


Figure 43. Power Gain as a Function of the Load

Printed-circuit-board (PCB) design is critical to high-frequency performance. To ensure output stability the load-matching resistors should be placed as close to the amplifier output pins as possible. This allows the matching resistors to mask the board parasitics from the amplifier output circuit. An example of this is shown in Figure 47. Also note that the low-pass filters in Figure 45 and Figure 46 use center-tapped capacitors. Having capacitors to ground provides a path for high-frequency, common-mode energy to dissipate. This is equally valuable for the ADC, so there are also capacitors to ground on the ADC side of the filter. The LMH6881EVAL evaluation board is available to serve as a guide for system board layout. See SNOA869 for more details.

8.1.3 Interfacing to an ADC

The LMH6881 is an excellent choice for driving high-speed ADCs such as the ADC12D1800RF, ADC12D1600RF or the ADS5400. The following sections will detail several elements of ADC system design, including noise filters, and AC- and DC-coupling options.

Application Information (continued)

8.1.3.1 ADC Noise Filter

When connecting a broadband amplifier to an analog-to-digital converter, it is nearly always necessary to filter the signal before sampling it with the ADC. Figure 44 shows a schematic of a second order Butterworth filter, and Table 6 shows component values for some common IF frequencies. These filters offer a good compromise between bandwidth, noise rejection and cost. This filter topology is the same as is used on the ADC14V155KDRB High IF Receiver reference design board. This filter topology is adequate for reducing aliasing of broadband noise and will also provide rejection of harmonic distortion and many of the images that are commonly created by mixers.

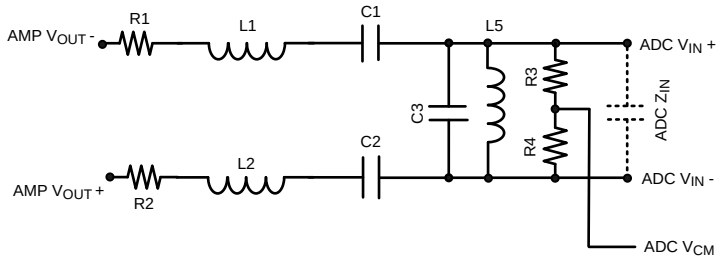


Figure 44. ADC Noise Filter Schematic

Table 6. Filter Component Values(1)

CENTER FREQUENCY	BANDWIDTH	R1, R2	L1, L2	C1, C2	C3	L5	R3, R4
75 MHz	40 MHz	90 Ω	390 nH	10 pF	22 pF	220 nH	100 Ω
150 MHz	60 MHz	90 Ω	370 nH	3 pF	19 pF	62 nH	100 Ω
180 MHz	75 MHz	90 Ω	300 nH	2.7 pF	15 pF	54 nH	100 Ω
250 MHz	100 MHz	90 Ω	225 nH	1.9 pF	11 pF	36 nH	100 Ω

(1) Resistor values are approximate, but have been reduced due to the internal 10 Ω of output resistance per pin.

8.1.3.2 AC Coupling to ADC

AC coupling is an effective method for interfacing to an ADC for many communications systems. In many applications this will be the best choice. The LMH6881 evaluation board is configured for AC coupling as shipped from the factory. Coupling with capacitors is usually the most cost-effective method. Transformers can provide both AC coupling and impedance transformation as well as single-ended to differential conversion. One of the key benefits to AC coupling is that each stage of the system can be biased to the ideal DC operating point. Many systems operate with lower overall power dissipation when DC bias currents are eliminated between stages.

8.1.3.3 DC Coupling to ADC

The LMH6881 supports DC-coupled signals. In order to successfully implement a DC-coupled signal chain the common-mode voltage requirements of every stage need to be met. This will require careful planning, and in some cases there will be signal level, gain or termination compromises required to meet the requirements of every part. Figure 45 and Figure 46 show a method using resistors to change the 2.5-V common mode of the amplifier output to a common mode compatible for the input of a low-input-voltage ADC such as the ADC12D1800RF. This DC level shift is achieved while maintaining an AC impedance match with the filter in Figure 45, while in Figure 46 there is a small mismatch between the amplifier termination resistors and the ADC input. Because there is no universal ADC input common mode and some ADCs have impedance controlled input, each design will require a different resistor ratio. For high-speed data conversion systems it is very important to keep the physical distance between the amplifier and the ADC electrically short. When connections between the amplifier and the ADC are electrically short, termination mismatches are not critical.

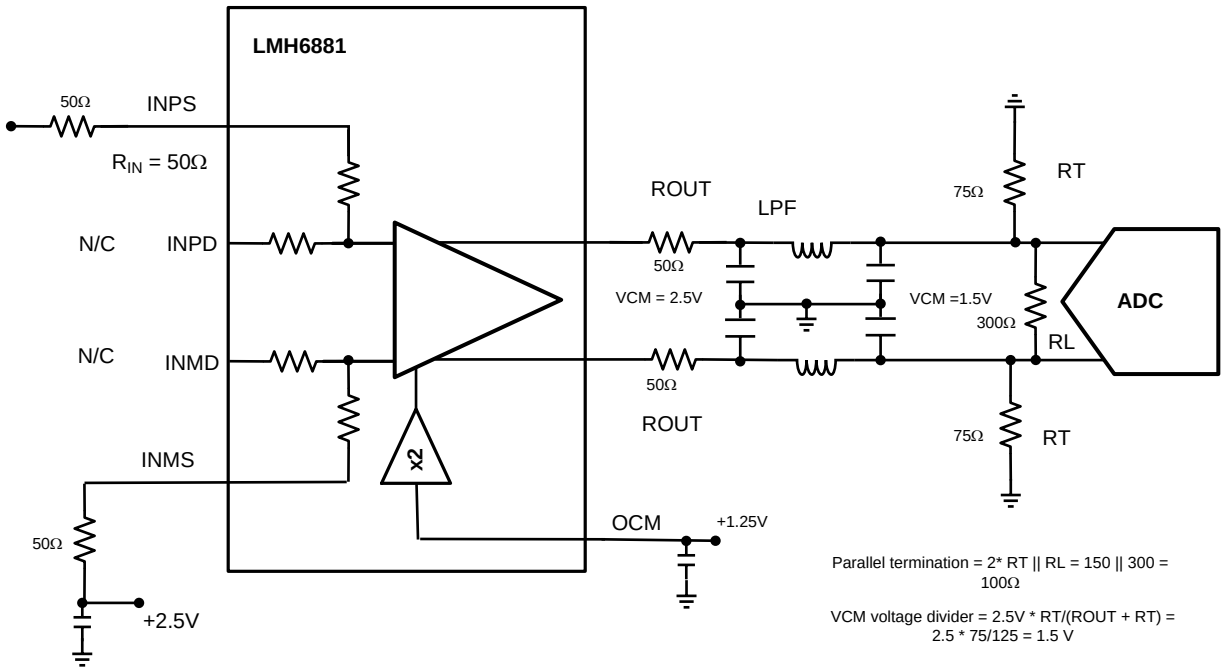


Figure 45. DC-Coupled ADC Driver Example 1, High-Input Impedance ADC

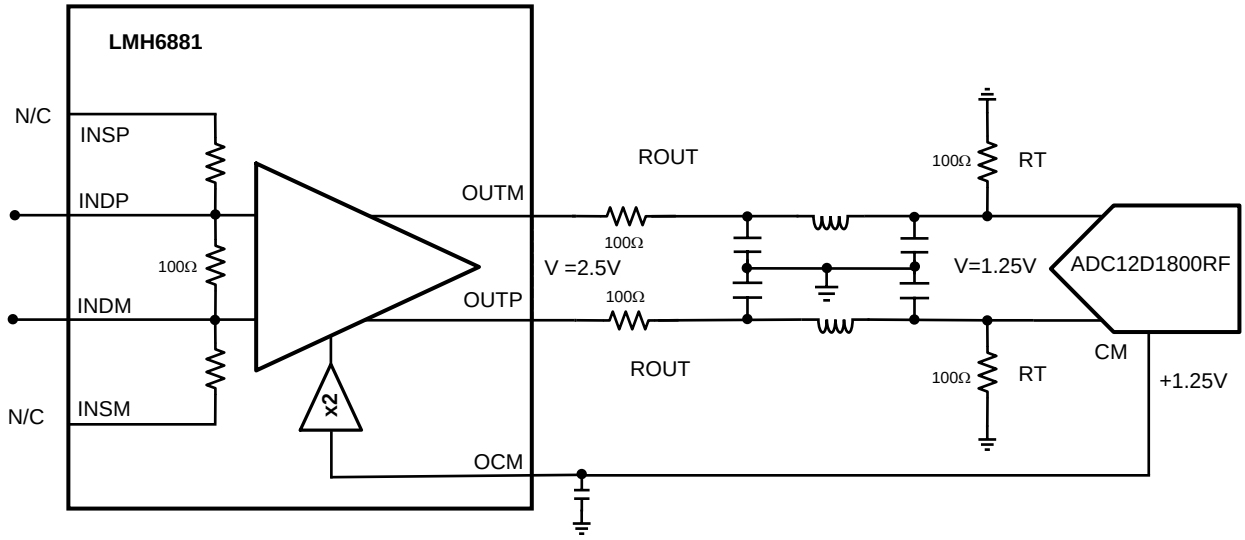


Figure 46. DC-Coupled ADC Driver Example 2, Terminated Input ADC

8.1.4 Figure of Merit: Dynamic Range Figure

The dynamic range figure (DRF) as illustrated in Figure 4, is defined as the input third order intercept point (IIP3) minus the noise figure (NF). The combination of noise figure and linearity gives a good proxy for the total dynamic range of an amplifier. In some ways this figure is similar to the SFDR of an analog-to-digital converter. In contrast to an ADC, though, an amplifier will not have a full-scale input to use as a reference point. With amplifiers, there is no one point where signal amplitude hits “full scale”. Yet, there are real limitations to how large of a signal the amplifier can handle. Normally, the distortion products produced by the amplifier will

determine the upper limit to signal amplitude. The intermodulation intercept point is an imaginary point that gives a well understood figure of merit for the maximum signal an amplifier can handle. For low-amplitude signals the noise figure gives a threshold of the lowest signal that the amplifier can reproduce. By combining the third-order input intercepts point and the noise figure the DRF gives a very good indication of the available dynamic range offered.

Table 7. Compatible High Speed ADCs

PRODUCT NUMBER	MAX SAMPLING RATE (MSPS)	RESOLUTION	CHANNELS
ADC12D1800RF	1800	12	DUAL
ADC12D1600RF	1600	12	DUAL
12D1000 RF	1000	12	DUAL
ADC12D800RF	800	12	DUAL
ADS5400	1000	12	SINGLE
ADC12C105	105	12	SINGLE
ADC10D1500	1500	10	DUAL
ADC12C170	170	12	SINGLE
ADC12V170	170	12	SINGLE
ADC14C105	105	14	SINGLE
ADC14DS105	105	14	DUAL
ADC14155	155	14	SINGLE
ADC14V155	155	14	SINGLE
ADC16V130	130	16	SINGLE
ADC16DV160	160	16	DUAL
ADC08D500	500	8	DUAL
ADC08500	500	8	SINGLE
ADC08D1000	1000	8	DUAL
ADC081000	1000	8	SINGLE
ADC08D1500	1500	8	DUAL
ADC081500	1500	8	SINGLE
ADC08(B)3000	3000	8	SINGLE
ADC08100	100	8	SINGLE
ADCS9888	170	8	SINGLE
ADC08(B)200	200	8	SINGLE
ADC11C125	125	11	SINGLE
ADC11C170	170	11	SINGLE

8.2 Typical Applications

8.2.1 LMH6881 Typical Application

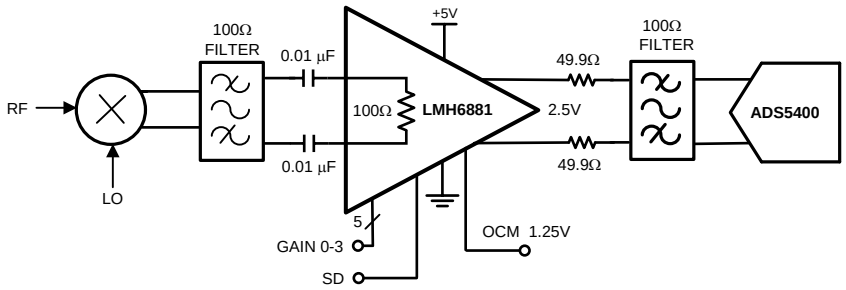


Figure 47. LMH6881 Typical Application

8.2.1.1 Design Requirements

Table 8 shows a design example for an IF amplifier in a typical direct-IF receiver application and LMH6882 meets these requirements.

Table 8. Example Design Requirement for an IF Receiver Application

SPECIFICATION	EXAMPLE DESIGN REQUIREMENT
Supply Voltage and Current	4.75 V to 5.25 V, with a minimum 150-mA supply current
Input structure and Impedance	DC-coupled Single-ended or Differential with 100-Ω input differential impedance
Output control	DC coupled with output common mode control capability
RF input frequency range	DC to 250 MHz
Voltage Gain Range	26 dB to 6 dB
OIP3 in RF input frequency range for Pout = 4 dBm/tone with RL = 200 Ω	> 38 dBm at 200 MHz for Max Gain
Noise Figure	< 12 dB at Max Gain across RF input frequency
Attenuation Control	Parallel control as well as SPI control

8.2.1.2 Detailed Design Procedure

The LMH6881 device can be included in most receiver applications by following these basic procedures:

- Select an appropriate input drive circuitry to the LMH6881 by frequency planning the signal chain properly such that the down-converted input signal is within the input frequency specifications of the device. Identify whether dc-or ac-coupling is required or filtering is needed to optimize the system. Follow the guidelines mentioned in *Input Characteristics* for interfacing the LMH6881 inputs.
- Choose the right speed grade ADC that meets the signal bandwidth application. Based upon the noise filtering and anti-aliasing requirement , determine the right order and type for the anti-aliasing filter. Follow the guidelines mentioned in *Output Characteristics* and *Interfacing to an ADC* when interfacing the device to an anti-aliasing filter.
- Optimize the signal chain gain leading up to the ADC for best SNR and SFDR performance by employing the device in automatic gain control (AGC) loop using serial or parallel digital interface.
- While interfacing the digital inputs, verify the electrical and functional compatibility of the LMH6881 digital input pins with the external microcontroller (µC).
- Choose the appropriate power-supply architecture and supply bypass filtering devices to provide stable, low noise supplies as mentioned in the *Power Supply Recommendations*.

8.2.1.3 Application Curves

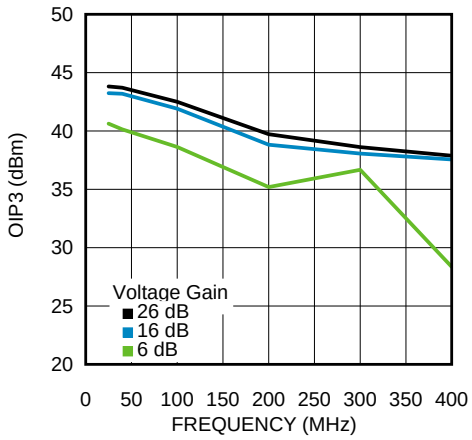


Figure 48. OIP3 vs Frequency

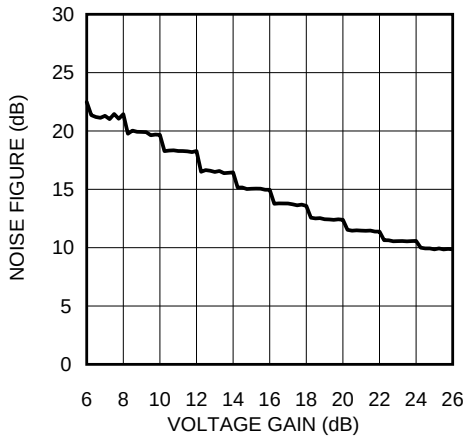


Figure 49. Noise Figure vs Voltage Gain

8.2.2 LMH6881 Used as Twisted-Pair Cable Driver

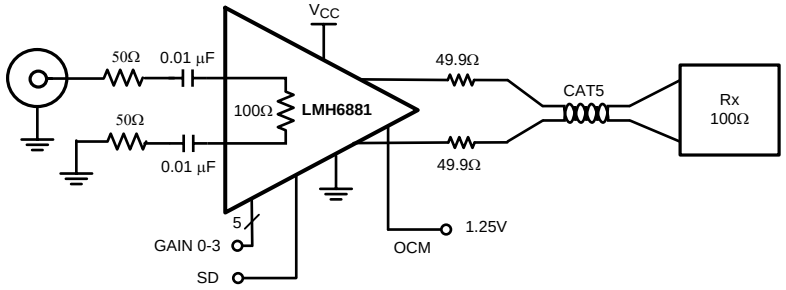


Figure 50. LMH6881 Used as Twisted-Pair Cable Driver

8.2.2.1 Design Requirements

Table 9 shows a design example for LMH6881 used as cable driver for driving unshielded twisted-pair (UTP) CAT-5 cables.

Table 9. Example Design Requirement for a Cable Driver

SPECIFICATION	EXAMPLE DESIGN REQUIREMENT
Supply Voltage and Current	4.75 V to 5.25 V, with a minimum 150-mA supply current
Input to Output Device Configuration	Single-ended input to differential output
Input frequency range	0.1 to 100 MHz
Voltage Gain Range	26-dB to 6-dB gain range
Output voltage swing	4 Vppdiff into a 200-Ω load at the output
Cable length to be driven	300 to 400 feet

8.2.2.2 Detailed Design Procedure

The LMH6881 device can be used as a cable driver to drive (UTP) CAT-5 cable by following these basic procedures:

- Select an appropriate input buffer or drive circuitry to the LMH6881 that provides pre-equalization in the frequency range of interest that needs to be driven down the CAT-5 cable. The cable usually presents attenuation of the signal at the receive end which is proportional to the length of the cable and the frequency being transmitted. In some cases, use of the pre-equalization buffer is not possible which mandates the use of a post-equalizer at the receive end to gain up the received signal.

- Determine the maximum output swing required to be transmitted in-order to receive the signal with good signal integrity. When driving long cable lengths, there is a possibility of corruption of differential signals due to common mode signals which requires the use of devices that offer good common mode rejection. Also, care must be taken to match the source impedance with the characteristic impedance of the CAT-5 cable to minimize signal reflections at higher frequencies. The LMH6881 offers low differential output resistance that makes source matching of driven cable very convenient.
- Verify the electrical and functional compatibility when interfacing LMH6881 digital input pins with the external microcontroller (µC).
- Also, use appropriate power-supply architecture and supply bypass filtering devices to provide stable, low noise supplies as mentioned in the *Power Supply Recommendations*.

8.2.2.3 Application Curves

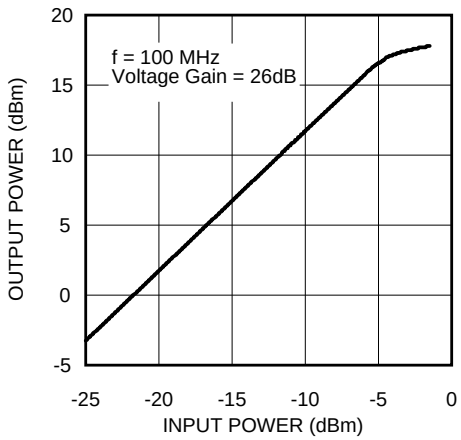


Figure 51. Output Power vs Input Power

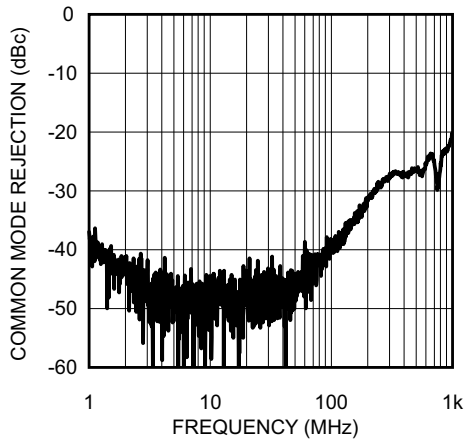


Figure 52. Common Mode Rejection (Sdc21) vs Frequency

9 Power Supply Recommendations

The LMH6881 was designed to be operated on 5-V power supplies. The voltage range for VCC is from 4.75 V to 5.25 V. Power-supply accuracy of 5% or better is advised. When operated on a board with high-speed digital signals it is important to provide isolation between digital signal noise and the analog input pins. The SP16160CH1RB reference board provides an example of good board layout.

The power supply pins are 19, 20, 23 and 24. Each supply pin should be decoupled with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF as close to the device as possible. When vias are used to connect the bypass capacitors to a ground plane the vias should be configured for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems two capacitors per supply pin are advised.

To avoid undesirable signal transients the LMH6881 should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

10 Layout

10.1 Layout Guidelines

It is very important to employ good high-speed layout techniques when dealing with devices having relatively high gain bandwidth in excess of 1 GHz to ensure stability and optimum performance. The LMH6881 evaluation board provides a good reference for suggested layout techniques. The LMH6881 evaluation board was designed for both good signal integrity and thermal dissipation using higher performance (Rogers) dielectric on the top layer. The high performance dielectric provides well matched impedance and low loss to frequencies beyond 1 GHz.

TI recommends that the LMH6881 board be multi-layered to improve thermal performance, grounding and power-supply decoupling. The LMH6881 evaluation board is an 8-layered board with the supply sandwiched in-between the GND layers for decoupling and having the stack up as Top layer - GND - GND - GND - Supply - GND - GND - Bottom layer. All signal paths are routed on the top layer on the higher performance (Rogers) dielectric, while the remainder signal layers are conventional FR4.

10.1.1 Uncontrolled Impedance Traces

It is important to pay careful attention while routing high-frequency signal traces on the PCB to maintain signal integrity. A good board layout software package can simplify the trace thickness design to maintain controlled characteristic impedances for high-frequency signals. Eliminating copper (the ground and power plane) from underneath the input and output pins of the device also helps in minimizing parasitic capacitance affecting the high-frequency signals near the PCB and package junctions. The LMH6881 evaluation board has copper keep-out areas under both the input and the output traces for this purpose. It is recommended that the application board also follow these keep-out areas to avoid any performance degradation.

10.2 Layout Example

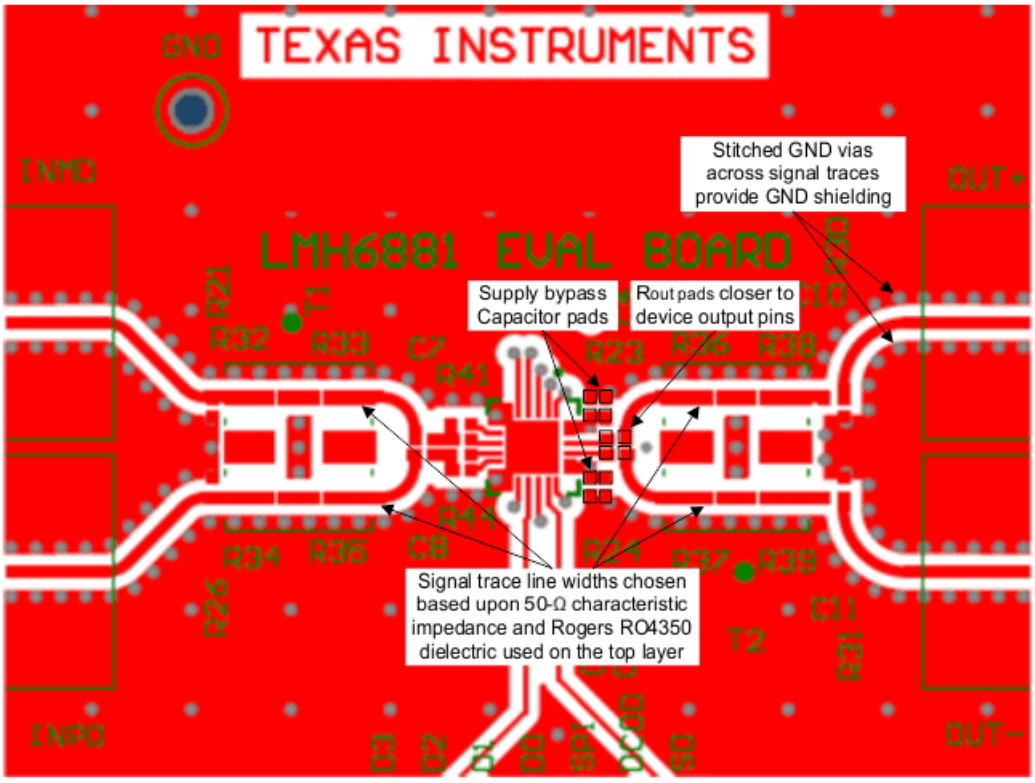


Figure 53. Top Layer

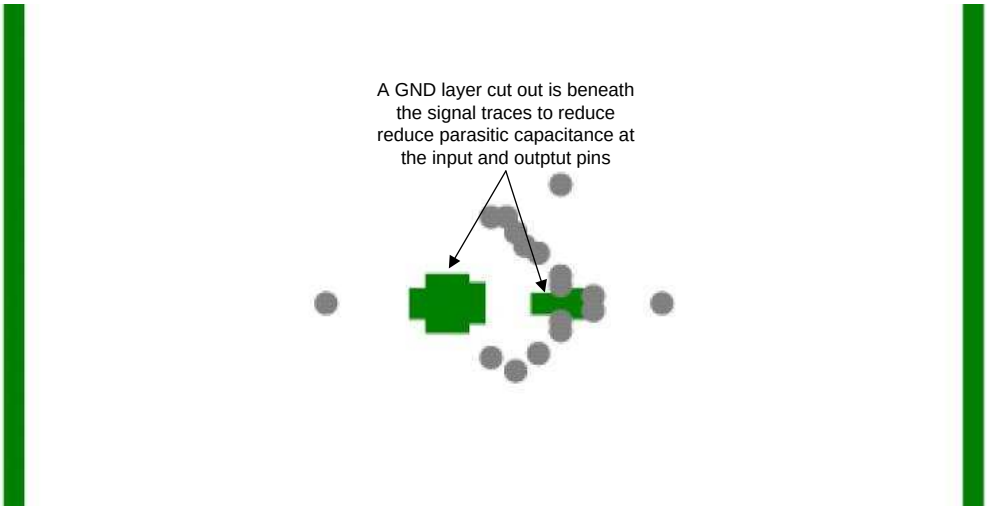


Figure 54. GND Layer

10.3 Thermal Considerations

The LMH6881 is packaged in a thermally enhanced package. The exposed pad on the bottom of the package is the primary means of removing heat from the package. It is recommended, but not necessary, that the exposed pad be connected to the supply ground plane. In any case, the thermal dissipation of the device is largely dependent on the attachment of the exposed pad to the system printed circuit board (PCB). The exposed pad should be attached to as much copper on the PCB as possible, preferably external layers of copper.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

《AN-2235 LMH6517/21/22 和其它高速 IF/RF 反馈放大器的电路板设计》，SNOA869

11.2 商标

串行外设接口 (SPI) is a trademark of Motorola, Inc.
All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6881SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L6881SQ	Samples
LMH6881SQE/NOPB	ACTIVE	WQFN	RTW	24	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L6881SQ	Samples
LMH6881SQX/NOPB	ACTIVE	WQFN	RTW	24	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	L6881SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

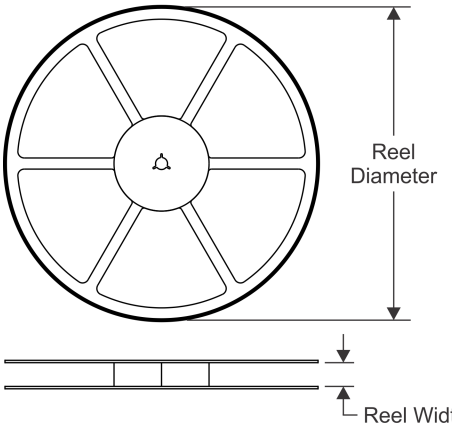
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

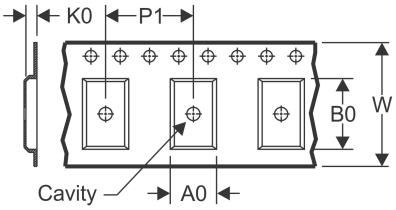
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

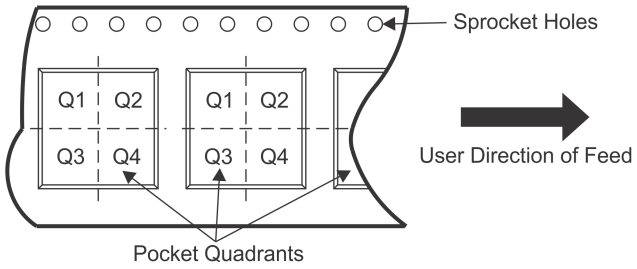


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

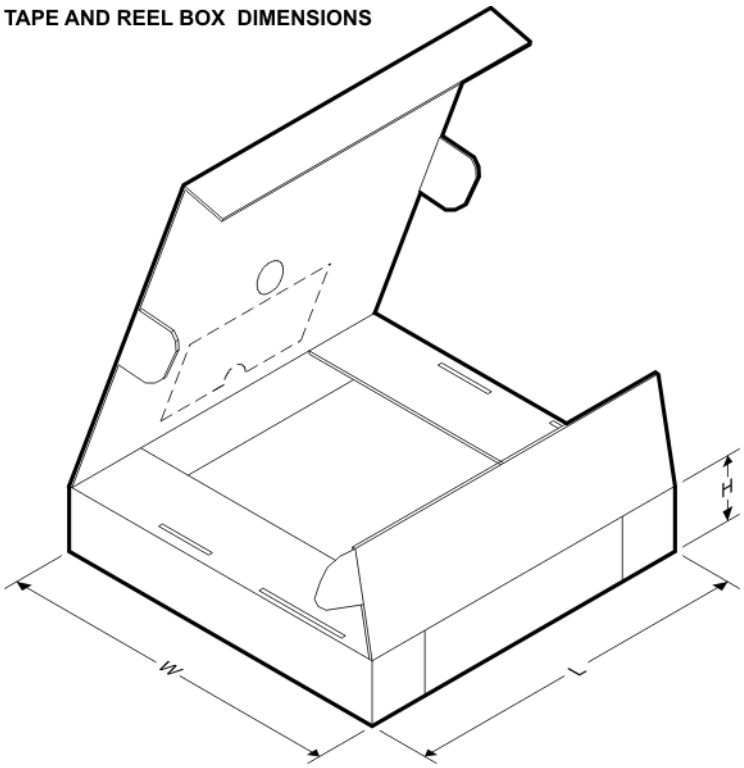
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6881SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6881SQE/NOPB	WQFN	RTW	24	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6881SQX/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

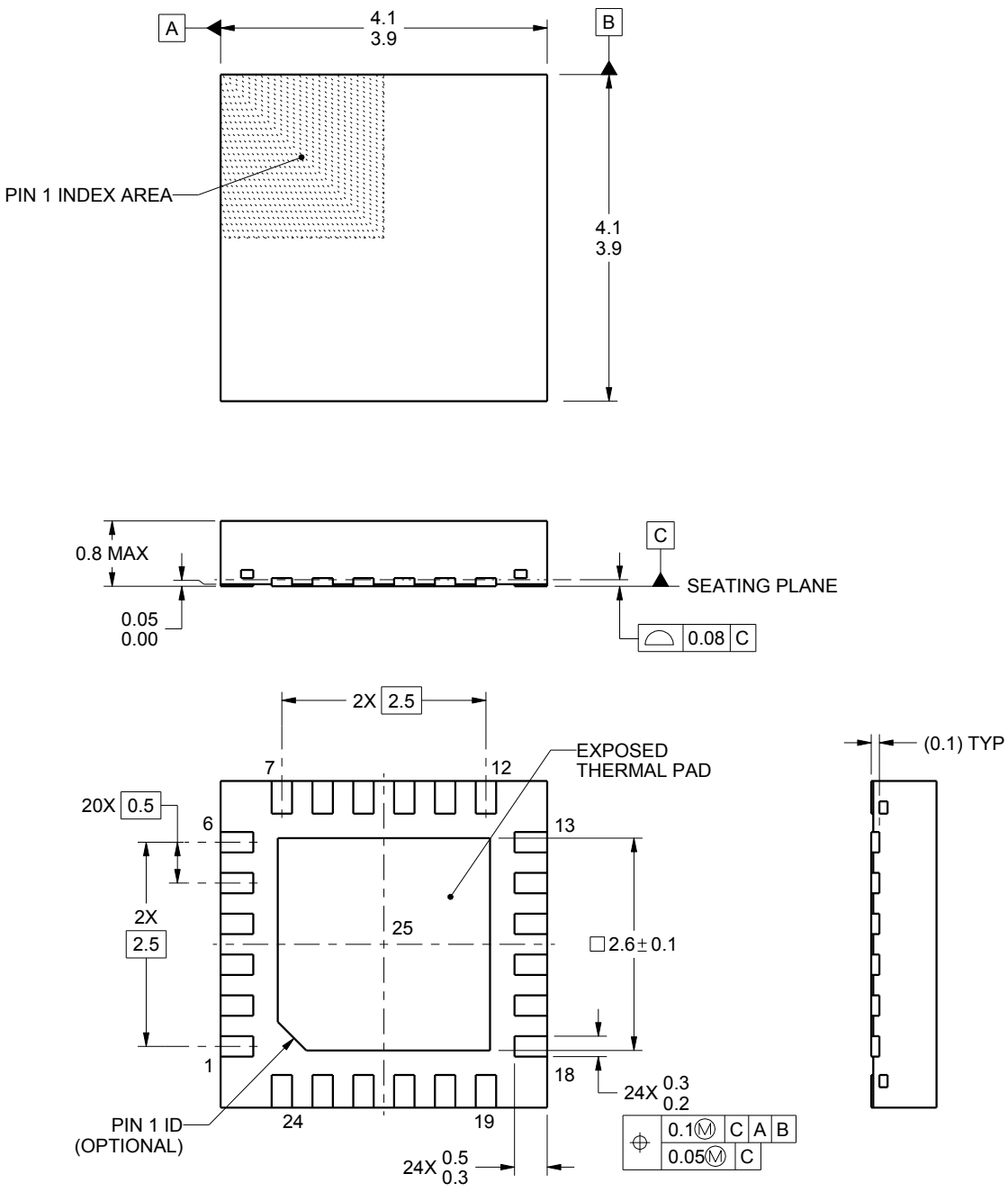
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6881SQ/NOPB	WQFN	RTW	24	1000	208.0	191.0	35.0
LMH6881SQE/NOPB	WQFN	RTW	24	250	208.0	191.0	35.0
LMH6881SQX/NOPB	WQFN	RTW	24	4500	356.0	356.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

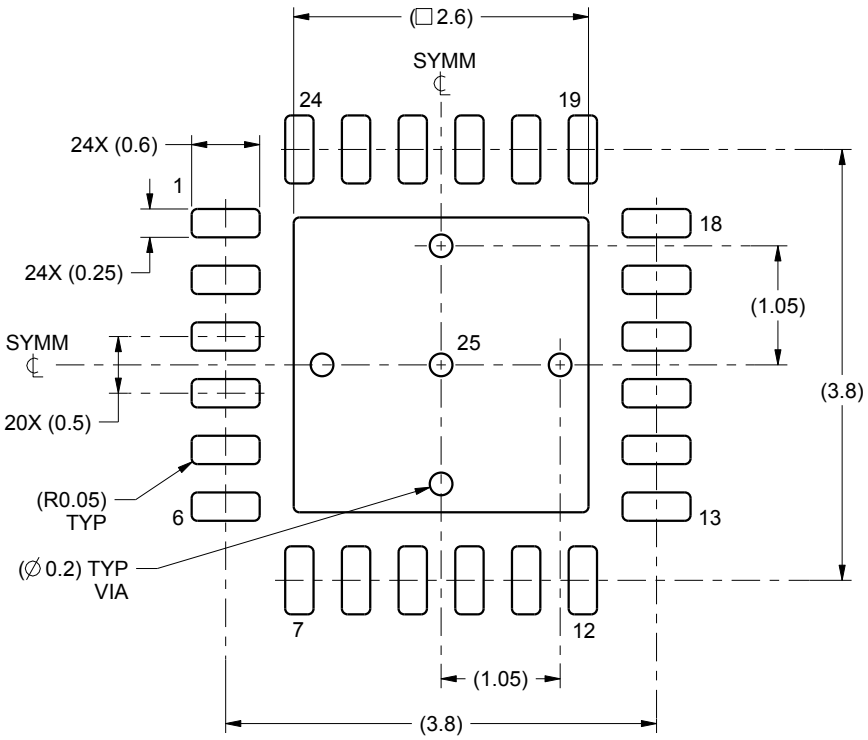
PLASTIC QUAD FLATPACK - NO LEAD



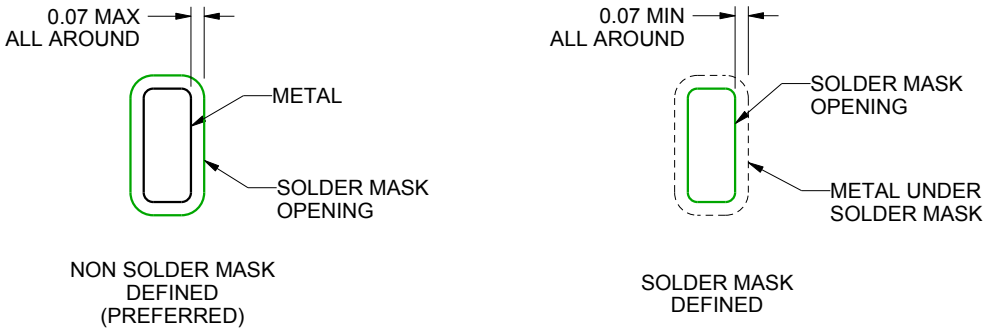
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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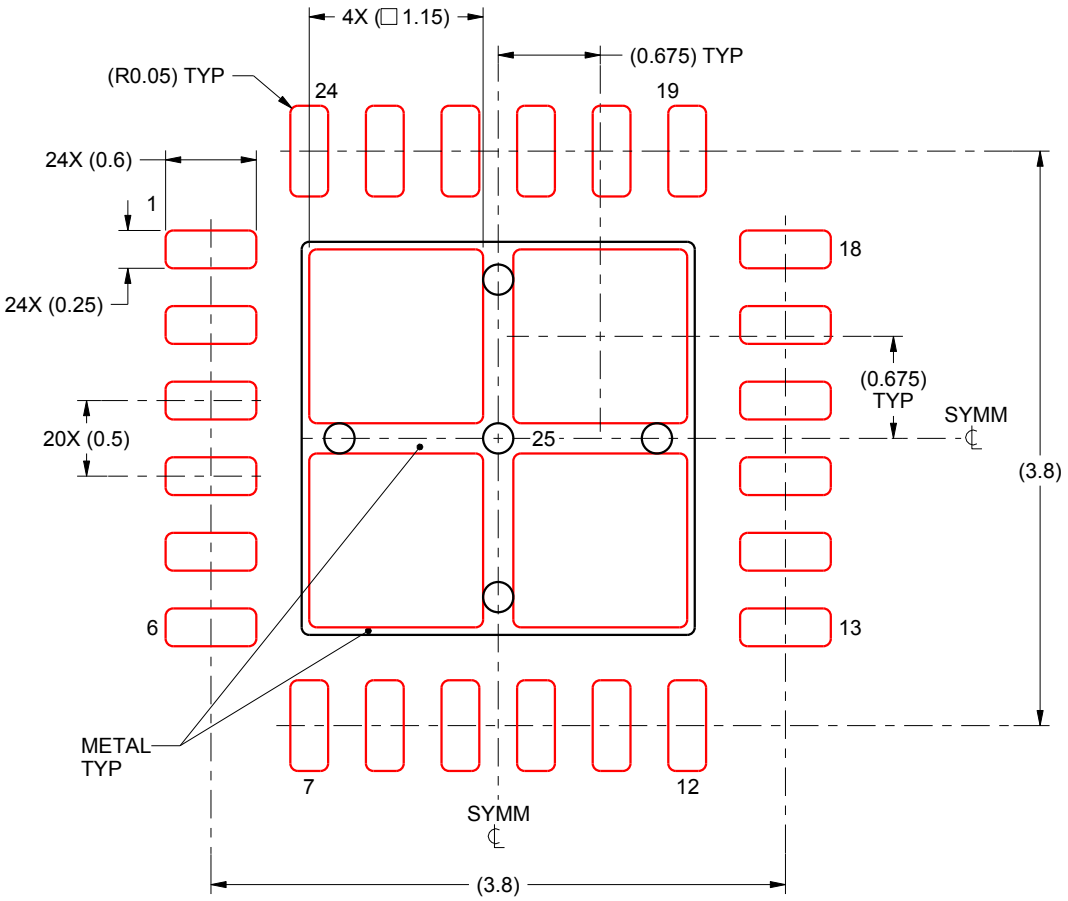
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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