具有稳定可靠的 IEC ESD 性能的 ESD401 1 通道 ESD 保护二极管

1 特性

- 稳定可靠的 IEC 61000-4-2 4 级 ESD 保护
  - ±24kV 接触放电
  - ±30kV 气隙放电
- IEC 61000-4-5 浪涌保护
  - 4.5A (8/20μs)
  - 1.8A I_{PP} (8/20μs) 时，具有 12V 的低 V_{clamp}
- IEC 61000-4-4 瞬态放电 (EFT) 保护
  - 80A (5/50ns)
- 具有可在高达 ± 5.5V 的电压下保护接口的双向 ESD 二极管
- IO 电容：0.77pF（典型值）
- 高直流击穿电压：8.3V（典型值）
- 超低泄漏电流：30pA（典型值）
- 低动态电阻：0.7Ω（典型值）
- 工业温度范围：-40°C 至 +125°C
- 行业标准的 0402 封装

2 应用

- 终端设备
  - 可穿戴产品
  - 便携式计算机和台式机
  - 手机和平板电脑
  - 机顶盒
  - 数字视频录像机 (DVR) 和网络视频录像机 (NVR)
  - 电视和监视器
  - EPOS（电子销售终端）
- 接口
  - 1Gbps 以太网
  - USB 2.0/1.1（5.5V 容差）
  - 通用输入/输出 (GPIO)
  - 按钮/键盘
  - 音频

3 说明

ESD401 是一种双向 TVS ESD 保护二极管，具有低 R_{DYN} 和低钳位电压。ESD401 旨在消除超出 IEC 61000-4-2（4 级）国际标准所规定的最高限量水平的 ESD 冲击。低动态电阻 (0.7Ω) 可确保系统级抗瞬变事件保护。该器件 采用 0.77pF IO 电容，非常适合用于保护 USB 2.0 之类的接口。该器件可在高达 ±5.5V 的电压运行，具有超低泄漏电流，并能承受高达 8.3V 的直流故障。

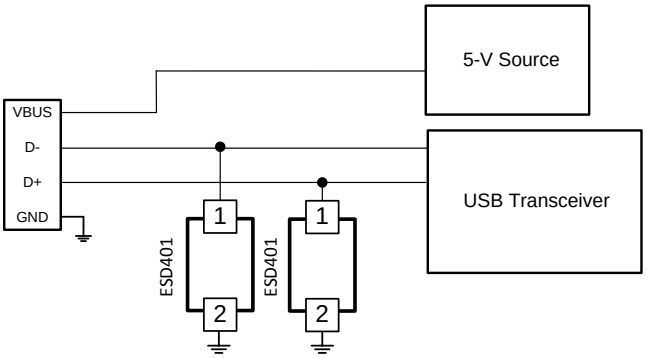
ESD401 采用符合行业标准的 0402 (DPY) 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ESD401DPY	X1SON (2)	0.60mm x 1.00mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型的 **USB 2.0** 应用原理图



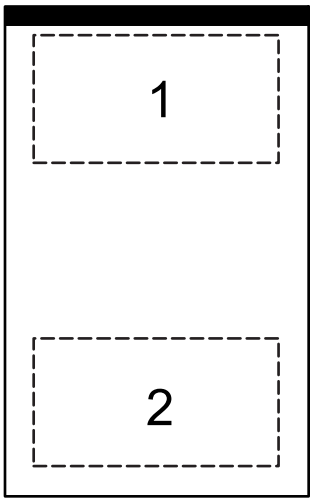
目录

4 修订历史记录

Changes from Original (July 2017) to Revision A	**Page**
• Updated 图 9 and图 13	6

5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
2	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs) at 25°C		67	W
	IEC 61000-4-5 current (t_p - 8/20 µs) at 25°C		4.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings — JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±24000	V
		IEC 61000-4-2 air-gap discharge	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–5.5	5.5	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD401 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	420	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	169.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	276.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	122.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	157.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–5.5		5.5	V
V_{BRF}	Breakdown voltage, Pin 1 to Pin 2 (1)	I_{IO} =1 mA, at T_A = 25°C	7.5		9.1	V
V_{BRR}	Breakdown voltage, Pin 2 to Pin 1 (1)	I_{IO} =1 mA, at T_A = 25°C	7.5		9.1	V
V_{HOLD}	Holding voltage (2)	I_{IO} =1 mA		8.3		V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		11		V
		I_{PP} = 5 A, TLP, from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		16		
		I_{PP} = 16 A, TLP, from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		24		
		I_{PP} = 1.8 A, IEC-61000-4-5 (t_p - 8/20 µs) from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		12		
		I_{PP} = 4.5 A, IEC-61000-4-5 (t_p - 8/20 µs) from Pin 1 to Pin 2 and Pin 2 to Pin 1, T_A = 25°C		15		
I_{LEAK}	Leakage current, Pin 1 to Pin2 and PIn2 to Pin 1	V_{IO} = ±2.5 V		0.03	10	nA
R_{DYN}	Dynamic resistance	Measured between TLP I_{PP} of 10 A and 20 A, Pin 2 to Pin 1 and Pin 1 to Pin2, T_A = 25°C		0.7		Ω
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, Pin 1 to Pin 2 and Pin2 to Pin1, T_A = 25°C		0.77	0.95	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state.
(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics

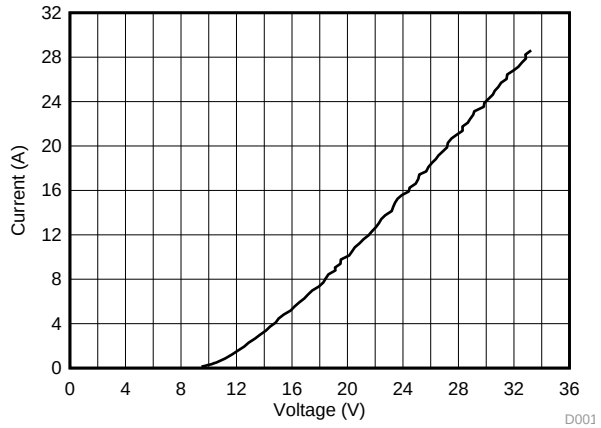


图 1. Positive TLP Curve, Pin 1 to Pin 2

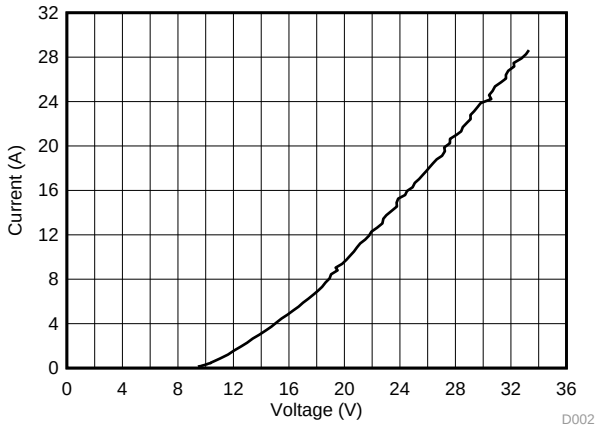


图 2. Negative TLP Curve, Pin 1 to Pin 2 (Plotted as Positive TLP Curve Pin 2 to Pin 1

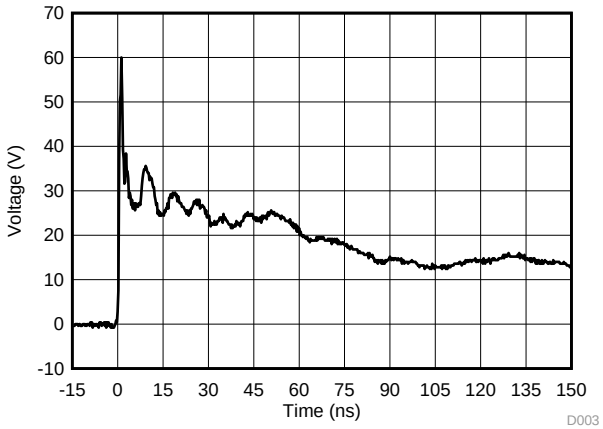


图 3. 8-kV IEC 61000-4-2 Waveform, Pin1 to Pin 2

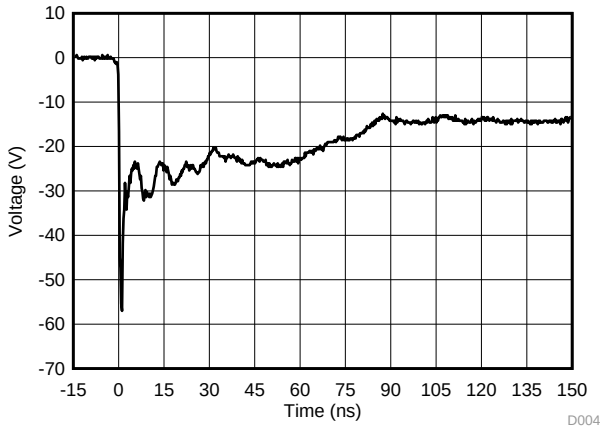


图 4. –8-kV IEC 61000-4-2 Waveform, Pin 1 to Pin 2

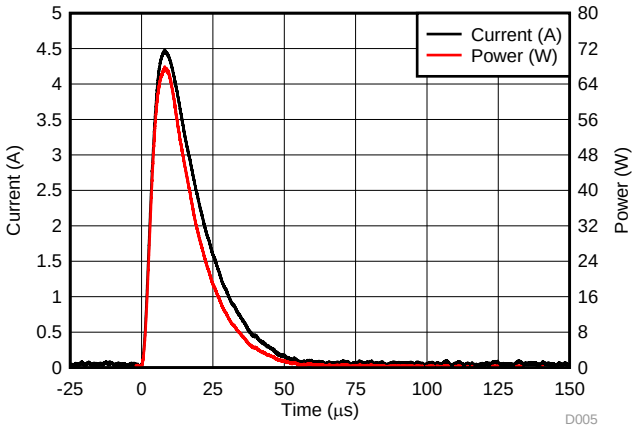


图 5. Surge (IEC 61000-4-5) Curve (tp = 8/20 µs), Pin 1 to Pin 2

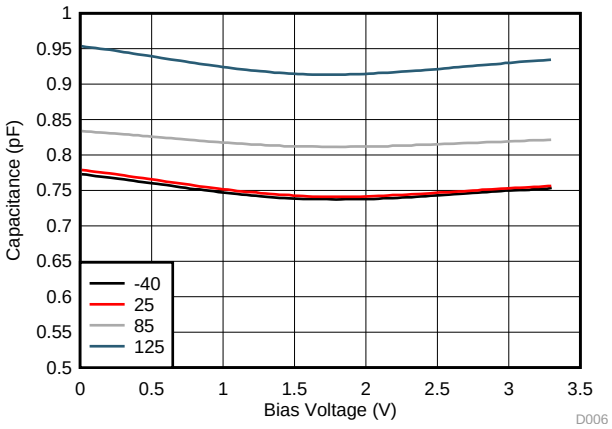


图 6. Capacitance vs Bias Voltage, Pin 1 to Pin 2

Typical Characteristics (接下页)

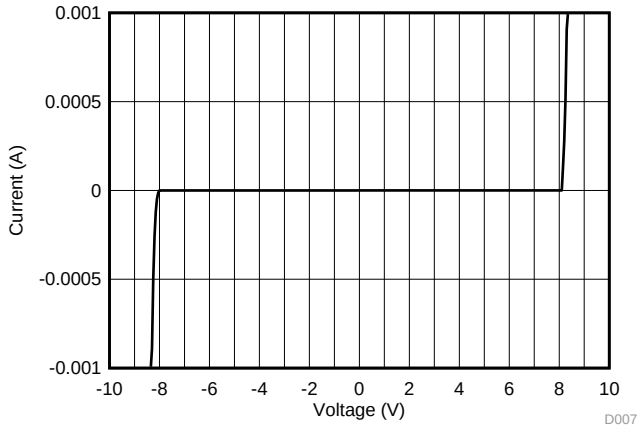


图 7. DC Voltage Sweep I-V Curve, Pin 1 to Pin 2

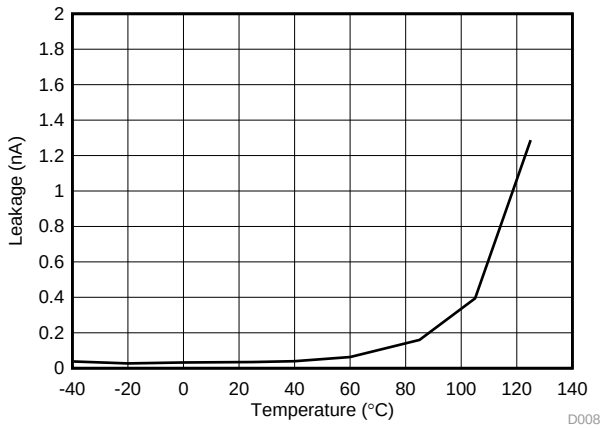


图 8. Leakage Current vs. Temperature, Pin 1 to Pin 2

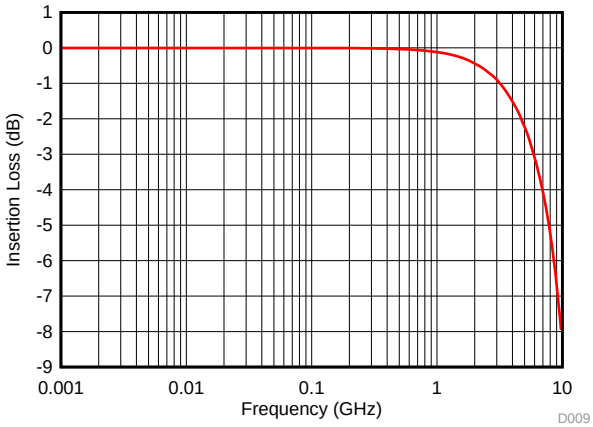


图 9. Insertion Loss

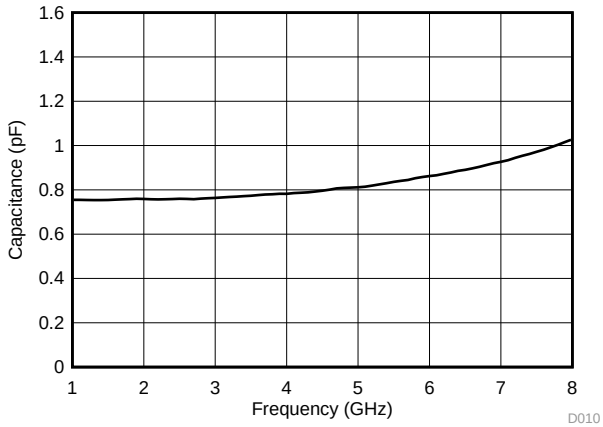


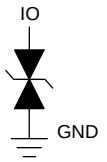
图 10. Capacitance vs. Frequency, Pin 1 to Pin 2

7 Detailed Description

7.1 Overview

The ESD401 is a bidirectional ESD Protection Diode with ultra-low clamping voltage. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low clamping makes this device ideal for protecting any sensitive signal pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±24-kV contact and ±30-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 4.5 A and 67W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 0.77 pF (typical) and 0.95 pF (maximum).

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±8.3 V typical. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±5.5 V.

7.3.6 Low Leakage Current

The I/O pins feature an low leakage current of 10 nA (maximum) with a bias of ±2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 24 V (TLP I_{PP} = 16 A).

7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.9 Industry Standard Footprint

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The ESD401 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±24 kV (contact) or ±30 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD401 (usually within 10s of nano-seconds) the device reverts to passive.

图 11 shows typical TLP behavior of bi-directional ESD device that does not exhibit snapback.

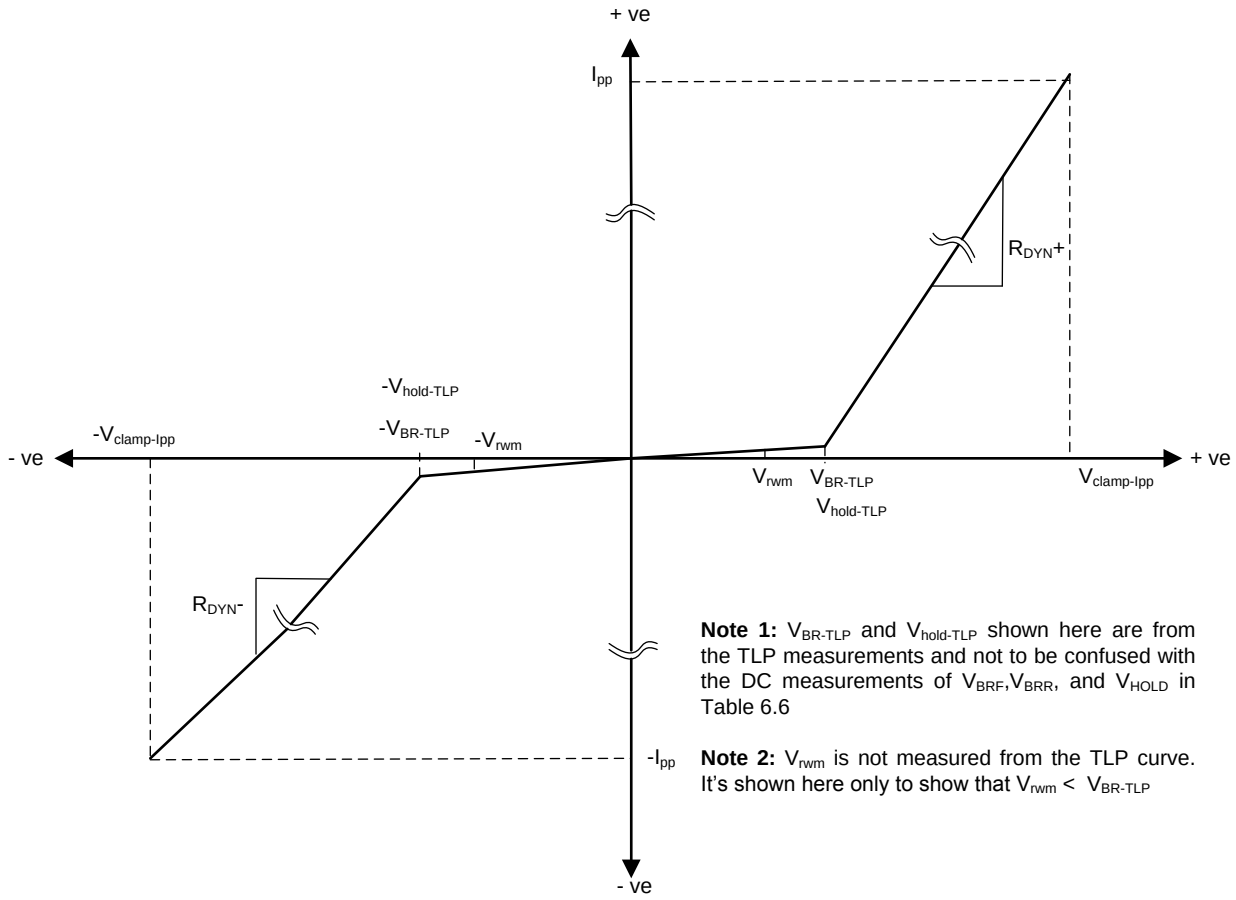


图 11. Typical TlpLP Behavior Of Bi-directional ESD Device that Does Not Exhibit Snapback

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ESD401 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

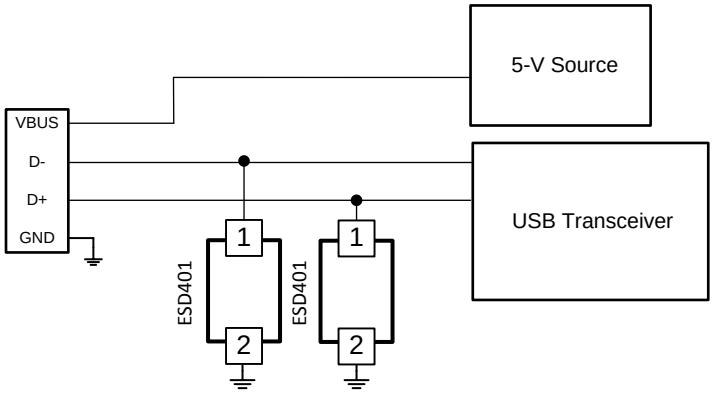


图 12. USB 2.0 ESD Schematic

8.2.1 Design Requirements

For this design example, two ESD401 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0 V to 3.6 V
Operating frequency on DP-DM lines	up to 240 MHz or 480 Mbps

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The ESD401 supports signal ranges between –5.5 V and 5.5 V, which supports the USB 2.0 signal range of 0 to 3.6 V on the DM/DP lines..

8.2.2.2 Operating Frequency

The ESD401 has a 0.85 pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

8.2.3 Application Curves

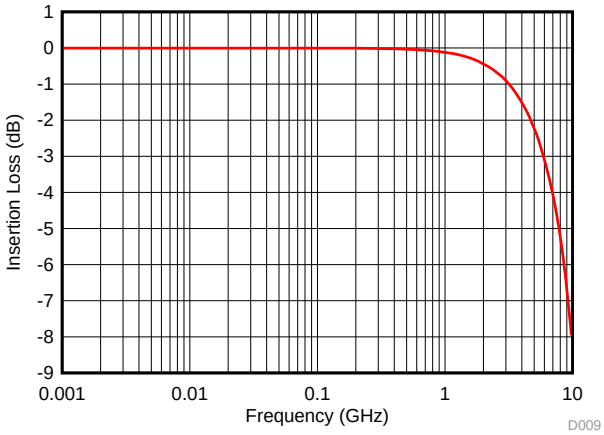


图 13. Insertion Loss

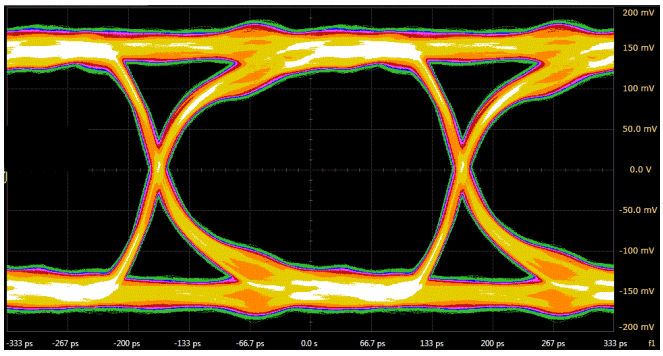


图 14. Eye Diagram - 3-Gbps Signal No Device

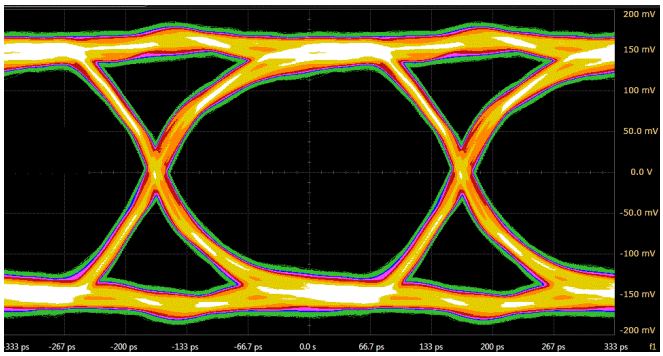


图 15. Eye Diagram - 3-Gbps Signal With ESD401

9 Power Supply Recommendations

The ESD401 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–5.5 V to 5.5 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

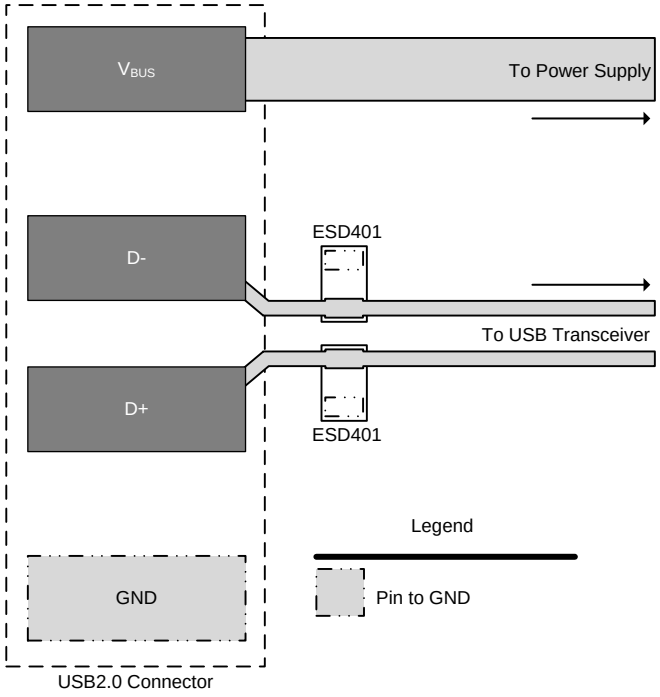


图 16. USB 2.0 ESD Layout

11 器件和文档支持

11.1 文档支持

相关文档请参见以下部分：

《ESD401DPY 评估模块》

11.2 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

E2E is a trademark of Texas Instruments.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD401DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

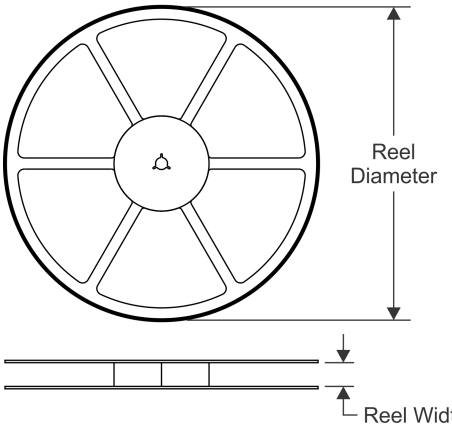
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

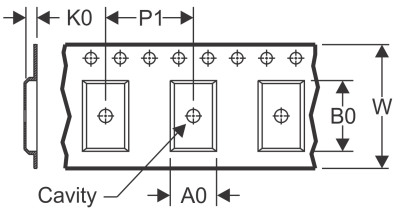
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

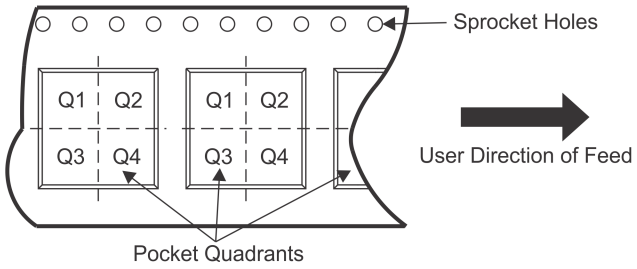


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

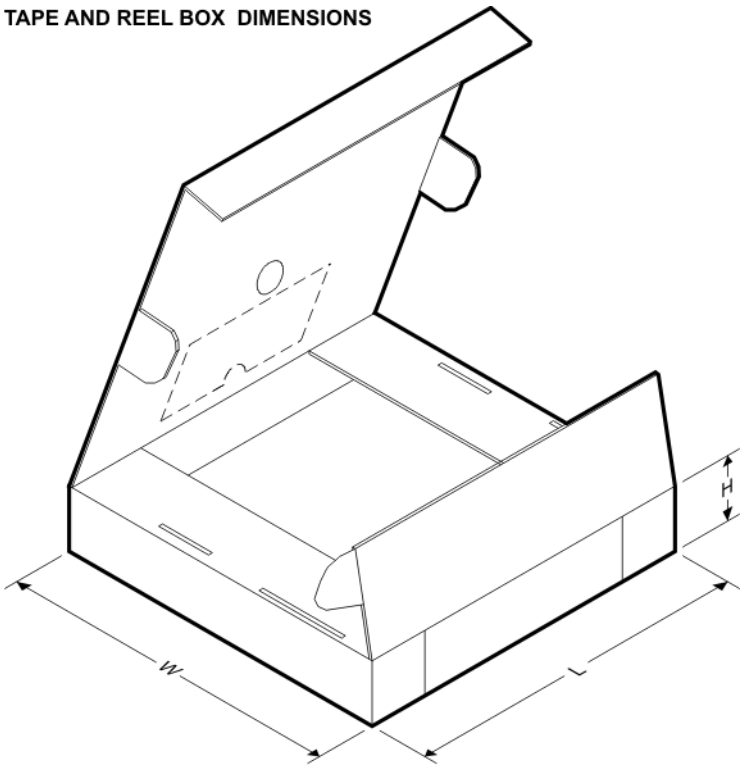
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD401DPYR	X1SON	DPY	2	10000	180.0	9.5	0.73	1.13	0.5	2.0	8.0	Q1
ESD401DPYR	X1SON	DPY	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

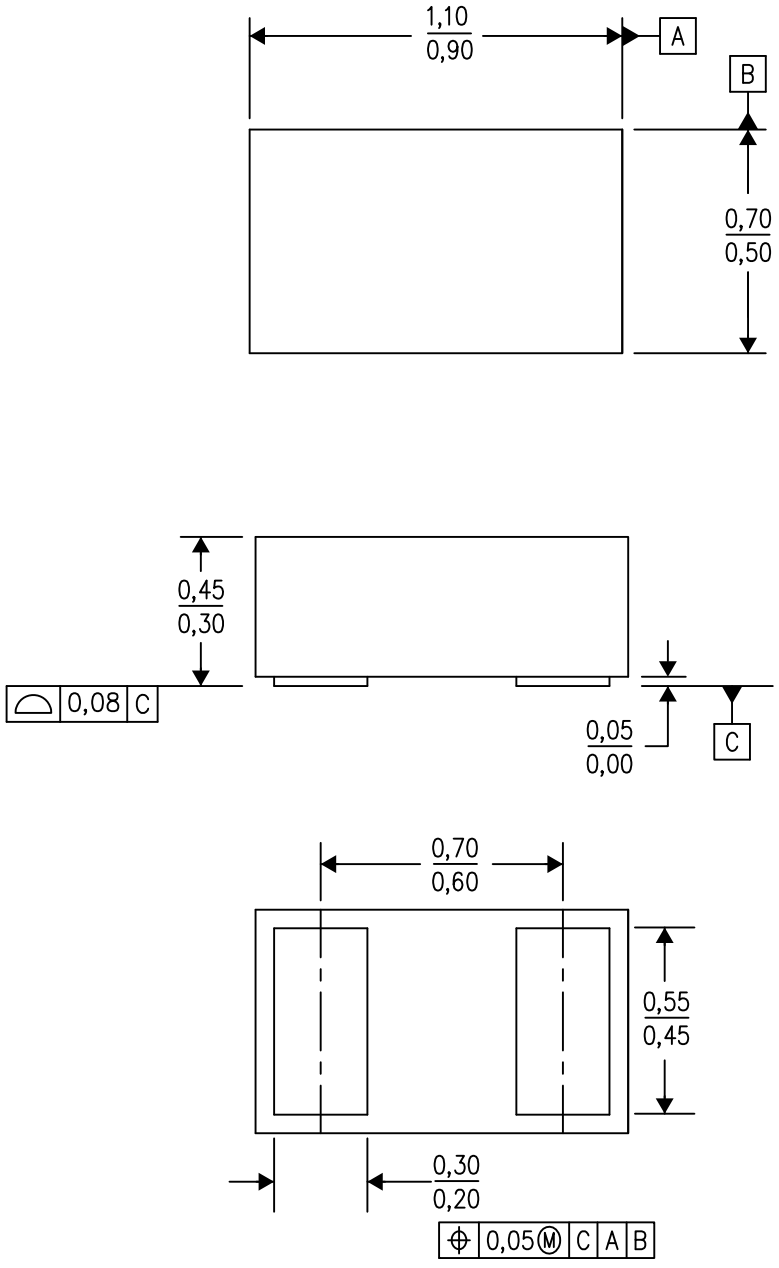
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD401DPYR	X1SON	DPY	2	10000	189.0	185.0	36.0
ESD401DPYR	X1SON	DPY	2	10000	205.0	200.0	33.0

DPY (R–PX1SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



4211012/D 08/14

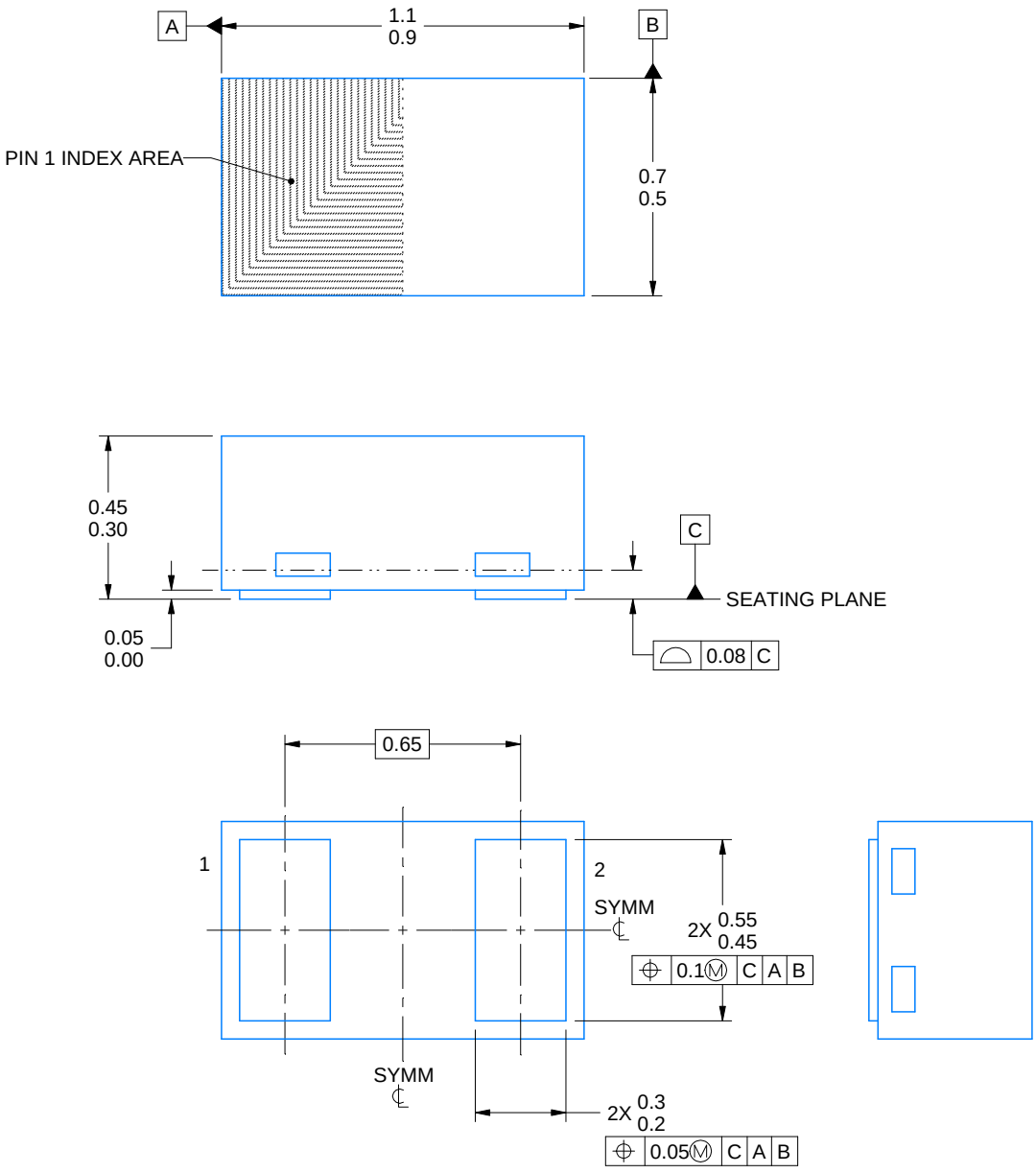
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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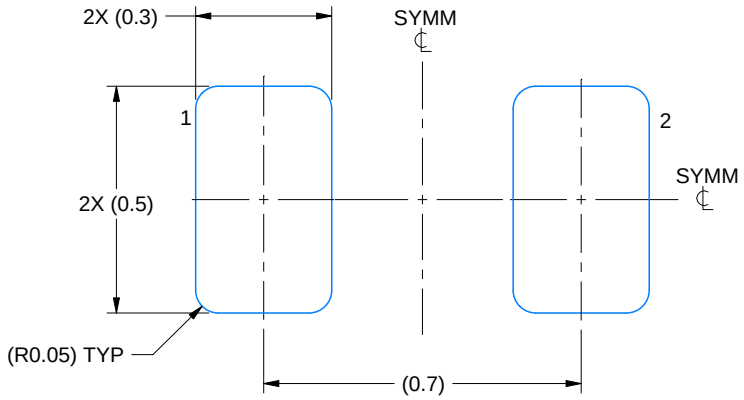
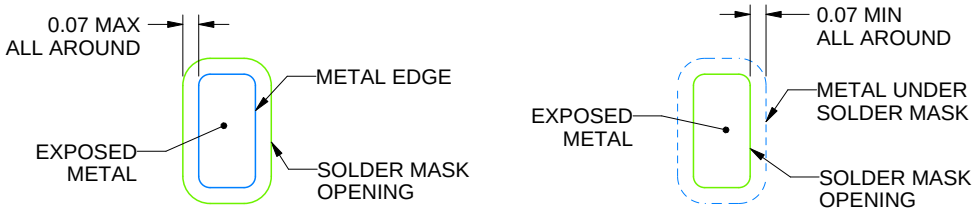
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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NOTES: (continued)

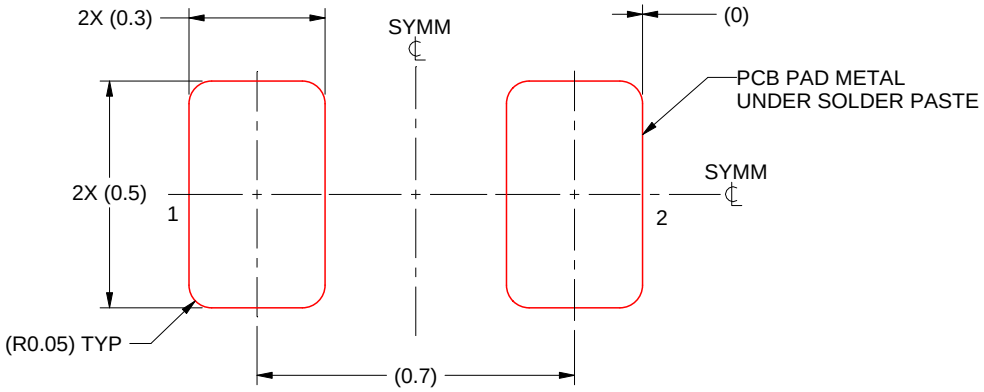
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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