采用芯片级封装的500mA / 600 mA, 4 MHz 高效率降压转换器

查询样品: TPS62690, TPS62691, TPS62697

特性

- 工作频率为 **4 MHz** 时，效率高达 **95%**
- **19 µA** 静态电流
- **4 MHz** 稳定频率工作
- 高占空比工作
- 总体 **DC** 电压误差精度：**±2%**
- 业界最佳的负载与线路瞬态
- 优异的 **AC** 负载稳压
- 低纹波轻负载 **PFM** 模式
- **≥40 dB V_{IN} PSRR**（**1kHz** 至 **10kHz**）
- 内部软启动，**250µs** 启动时间
- 集成型有源断电排序控制（可选）
- 电流过载和热关断保护
- 需要三个表面贴装外部组件（一个 **2012 MLCC** 电感器、两个 **0402** 陶瓷电容器）
- 完整的 **1** 毫米以下组件外形解决方案
- 总体解决方案尺寸不足 **12** 毫米^2
- 采用 **6** 引脚 **NanoFree™ (CSP)**

应用范围

- **LDO** 替代产品
- 手机、智能电话
- 便携式音频、便携式媒体
- **DC/DC** 微小型模块

说明

TPS6269x 器件是一款针对电池供电便携式应用优化的高频率同步降压 DC/DC 转换器。 TPS6269x 不但支持高达 600 mA 的负载电流，而且还允许使用低成本芯片电感器与电容器，从而可满足低功耗应用的需求。

该器件是移动电话以及类似单节锂离子电池供电应用的理想选择。 不同固定电压输出版本支持介于 2.2 V 至 2.9 V 之间的电压。

TPS6269x 不但可在稳定的 4 MHz 开关频率下工作，而且还可在轻负载电流时进入节电模式，以维持整个负载电流范围内的高效率。

PFM 模式可在轻负载工作时将静态电流降至 19 µA（典型值），从而可延长电池使用寿命。 对于低噪声应用，该器件可通过拉高该模式引脚强制进入固定频率 PWM 模式。 该特性结合高 PSRR 与 AC 负载调节性能，可使该器理想地替代线性稳压器，获得更高的电源转换效率。

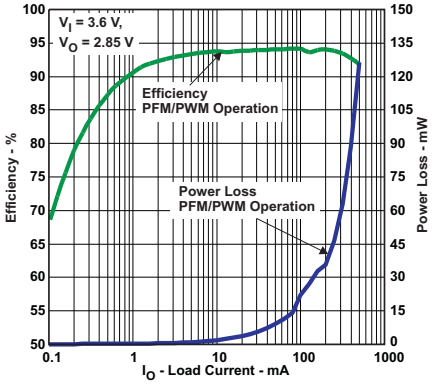


图 **1.** 效率对 负载电流

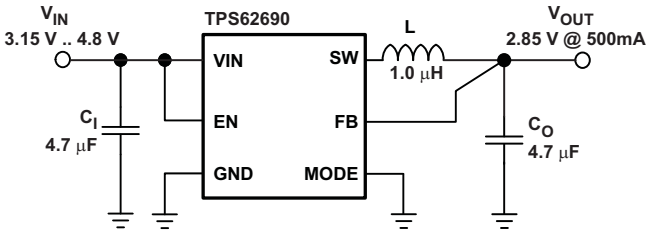


图 **2.** 最小解决方案尺寸应用

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER	OUTPUT VOLTAGE(2)	DEVICE SPECIFIC FEATURE	ORDERING(3)	PACKAGE MARKING CHIP CODE
-40°C to 85°C	TPS62690	2.85V	500mA peak output current	TPS62690YFF	PB
	TPS62691(4)	2.2V	600mA peak output current	TPS62691YFF	SU
	TPS62697	2.8V	500mA peak output current	TPS62697YFF	WA

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Internal tap points are available to facilitate output voltages in 25mV increments.
(3) The YFF package is available in tape and reel. Add a R suffix (e.g. TPS62690YFFR) to order quantities of 3000 parts. Add a T suffix (e.g. TPS62690YFFT) to order quantities of 250 parts.
(4) Product preview. Contact TI factory for more information.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Input Voltage	Voltage at VIN(2)(3), SW(3)		–0.3	6	V
	Voltage at FB(3)		–0.3	3.6	V
	Voltage at EN, MODE (3)		–0.3	V_I + 0.3	V
Peak output current, I_O		TPS62690, TPS62697		500	mA
		TPS62691		600	mA
Power dissipation			Internally limited		
Operating temperature range, T_A (4)			–40	85	°C
Operating junction temperature, T_J				150	°C
Storage temperature range, T_{stg}			–65	150	°C
ESD(5)	Human body model			2	kV
	Charge device model			1	kV
	Machine model			200	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Operation above 4.8V input voltage is not recommended over an extended period of time.
(3) All voltage values are with respect to network ground terminal.
(4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.
(5) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS62690 YFF (6 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	133.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	1.4	
θ_{JB}	Junction-to-board thermal resistance	22.5	
ψ_{JT}	Junction-to-top characterization parameter	5.5	
ψ_{JB}	Junction-to-board characterization parameter	22.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	-	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range		2.3		4.8 (1)	V
I_O	Output current range	TPS62690, TPS62697	0		500	mA
		TPS62691	0		600	mA
L	Inductance		0.5		1.8	µH
C_O	Output capacitance		1	5	10	µF
T_A	Ambient temperature		–40		+85	°C
T_J	Operating junction temperature		–40		+125	°C

(1) Operation above 4.8V input voltage is not recommended over an extended period of time.

ELECTRICAL CHARACTERISTICS

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 2.85V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 2.85V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current	TPS6269x	I_O = 0mA. Device not switching		19	50	µA
		TPS6269x	I_O = 0mA, PWM mode		4.2		mA
$I_{(SD)}$	Shutdown current	TPS6269x	EN = GND		0.2	5	µA
UVLO	Undervoltage lockout threshold	TPS6269x			2.05	2.1	V
ENABLE, MODE							
V_{IH}	High-level input voltage	TPS6269x		1			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN		0.01	1.5	µA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on resistance	TPS6269x	V_{IN} = $V_{(GS)}$ = 3.6V. PWM mode		160	280 (1)	mΩ
			V_{IN} = $V_{(GS)}$ = 2.9V. PWM mode		190	350 (1)	mΩ
I_{lkg}	P-channel leakage current, PMOS	TPS6269x	$V_{(DS)}$ = 5.5V, -40°C ≤ T_J ≤ 85°C			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance	TPS6269x	V_{IN} = $V_{(GS)}$ = 3.6V. PWM mode		110		mΩ
			V_{IN} = $V_{(GS)}$ = 2.9V. PWM mode		140		mΩ
I_{lkg}	N-channel leakage current, NMOS	TPS6269x	$V_{(DS)}$ = 5.5V, -40°C ≤ T_J ≤ 85°C			2	µA
r_{DIS}	Discharge resistor for power-down sequence				100	150	Ω
	P-MOS current limit	TPS62690 TPS62697	2.3V ≤ V_{IN} ≤ 4.8V. Open loop	900	1100	1250	mA
			V_{IN} = 3.6V. Closed loop		830		mA
		TPS62691	2.3V ≤ V_{IN} ≤ 4.8V. Open loop	1050	1250	1400	mA
	Input current limit under short-circuit conditions	TPS6269x	V_O shorted to ground		15		mA
	Thermal shutdown	TPS6269x			140		°C
	Thermal shutdown hysteresis				10		°C

(1) Verified by characterization. Not tested in production.

ELECTRICAL CHARACTERISTICS (continued)

Minimum and maximum values are at V_{IN} = 2.3V to 5.5V, V_{OUT} = 2.85V, EN = 1.8V, AUTO mode and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 2.85V, EN = 1.8V, AUTO mode and T_A = 25°C (unless otherwise noted).

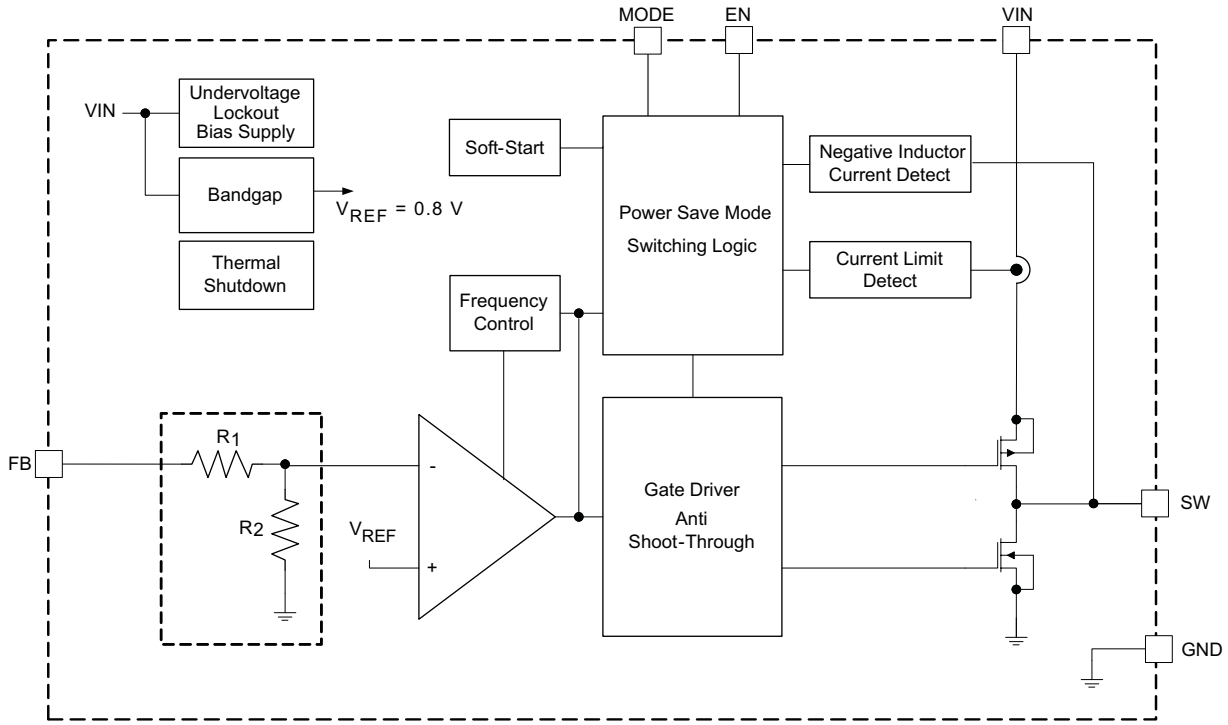
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR							
f_{SW}	Oscillator frequency	TPS6269x	I_O = 0mA, PWM mode. T_A = 25°C	3.6	4	4.4	MHz
OUTPUT							
V_{OUT}	Regulated DC output voltage	TPS62690 TPS62697	3.15V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			3.15V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.04×V_{NOM}	V
			3.15V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 500 mA PWM operation	0.98×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
	Line regulation		V_{IN} = V_O + 0.5V (min 3.15V) to 5.5V I_O = 200 mA		0.18		%/V
	Load regulation		I_O = 0mA to 500 mA		–0.0002		%/mA
	Load regulation		I_O = 0mA to 500 mA		–0.0002		%/mA
V_{OUT}	Regulated DC output voltage	TPS62691	2.9 V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.98×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			2.65V ≤ V_{IN} ≤ 4.8V, 0mA ≤ I_O ≤ 600 mA PFM/PWM operation	0.97×V_{NOM}	V_{NOM}	1.03×V_{NOM}	V
			2.65V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_O ≤ 600 mA PWM operation	0.97×V_{NOM}	V_{NOM}	1.02×V_{NOM}	V
	Line regulation		V_{IN} = V_O + 0.5V (min 2.5V) to 5.5V I_O = 200 mA		0.12		%/V
	Load regulation		I_O = 0mA to 600 mA		–0.0003		%/mA
	Feedback input resistance	TPS6269x			480		kΩ
ΔV_O	Power-save mode ripple voltage	TPS62690 TPS62697	I_O = 1mA C_O = 4.7µF X5R 6.3V 0402		65		mV_{PP}
			I_O = 1mA C_O = 10µF X5R 6.3V 0603		25		mV_{PP}
		TPS62691	I_O = 1mA C_O = 10µF X5R 6.3V 0603		22		mV_{PP}
	Start-up time	TPS62690 TPS62697	I_O = 0mA, Time from active EN to V_O		250		µs
		TPS62691	I_O = 0mA, Time from active EN to V_O		205		µs

PIN ASSIGNMENTS TPS6269X

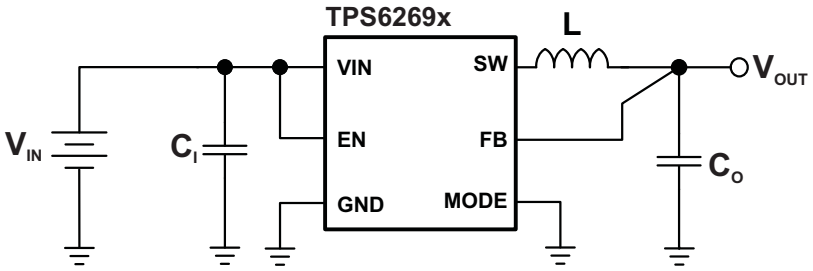
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	C1	I	Output feedback sense input. Connect FB to the converter's output.
VIN	A2	I	Power supply input.
SW	B1	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
EN	B2	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin to V_I enables the device. This pin must not be left floating and must be terminated.
MODE	A1	I	This is the mode selection pin of the device. This pin must not be left floating and must be terminated. MODE = LOW: The device is operating in regulated frequency pulse width modulation mode (PWM) at high-load currents and in pulse frequency modulation mode (PFM) at light load currents. MODE = HIGH: Low-noise mode enabled, regulated frequency PWM operation forced.
GND	C2	–	Ground pin.

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION



List of components:

- L = MURATA LQM21PN1R0NGC
- C_I = MURATA GRM155R60J475M (4.7µF, 6.3V, 0402, X5R)
- C_O = MURATA GRM188R60J106ME84 (10µF, 6.3V, 0603, X5R)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Load current	3, 4, 5
		vs Input voltage	6
	Peak-to-peak output ripple voltage	vs Load current	7, 8
	Combined line/load transient response		9, 10
	Load transient response		11, 12, 13, 14
	AC load transient response		15, 16, 17, 18
V_O	DC output voltage	vs Load current	19, 20
	PFM/PWM boundaries	vs Input voltage	21
I_Q	Quiescent current	vs Input voltage	22
f_s	PWM switching frequency	vs Input voltage	23
	PFM switching frequency	vs Load current	24
$r_{DS(on)}$	P-channel MOSFET $r_{DS(on)}$	vs Input voltage	25
	N-channel MOSFET $r_{DS(on)}$	vs Input voltage	26
	PWM operation		27
	Power-save mode operation		28
	Start-up		29, 30
PSRR	Power supply rejection ratio	vs. Frequency	31
	Spurious output noise (PFM mode)	vs. Frequency	32
	Spurious output noise (PWM mode)	vs. Frequency	33
	Output spectral noise density	vs. Frequency	34

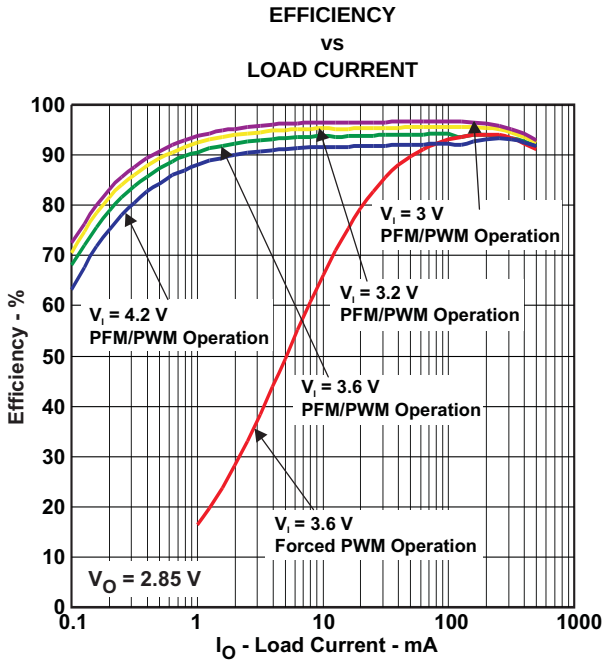


Figure 3.

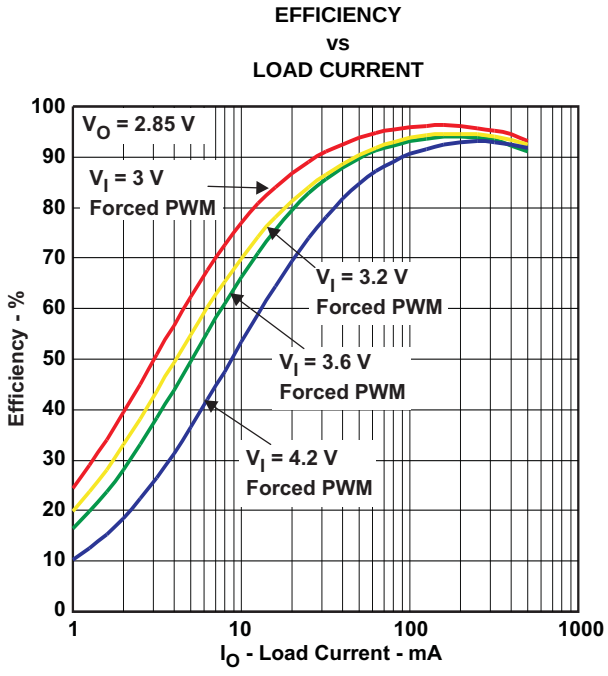


Figure 4.

TYPICAL CHARACTERISTICS (continued)

EFFICIENCY
vs
LOAD CURRENT

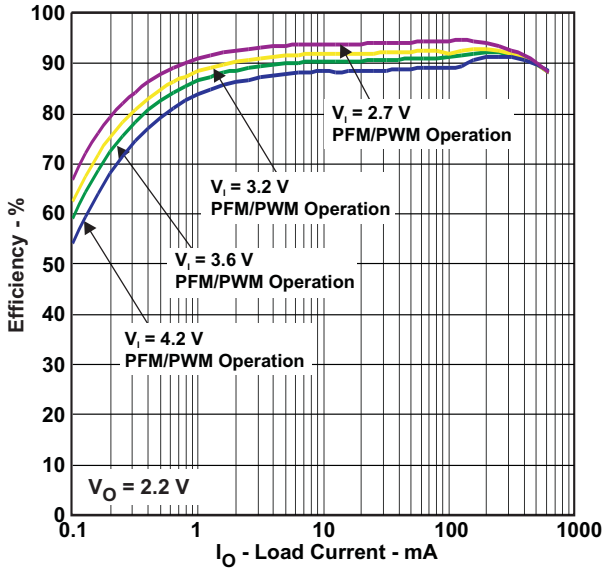


Figure 5.

EFFICIENCY
vs
INPUT VOLTAGE

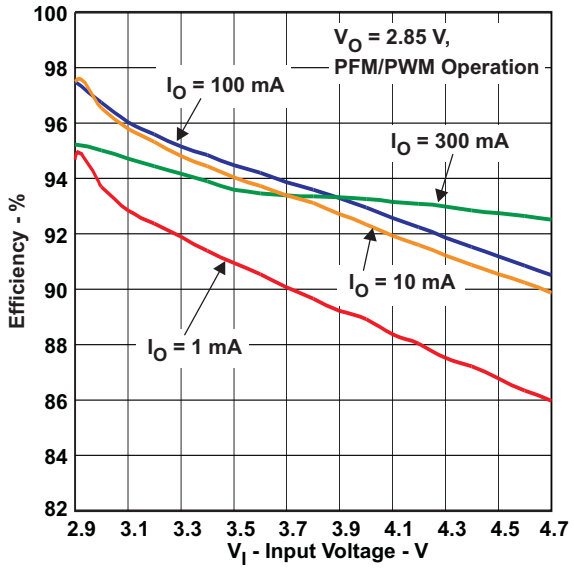


Figure 6.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
LOAD CURRENT

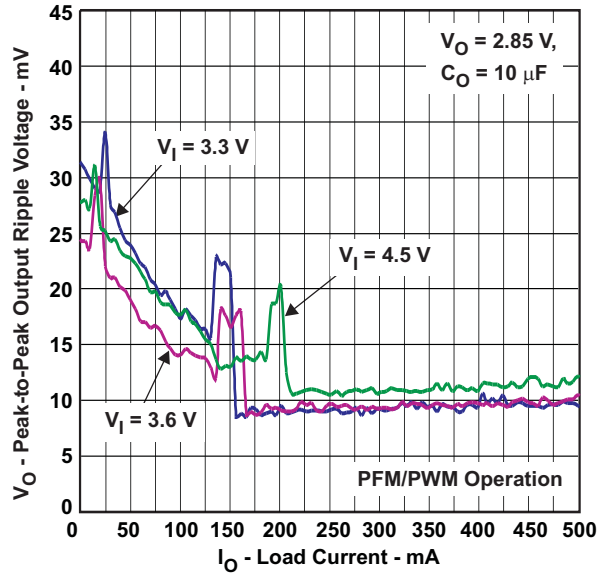


Figure 7.

PEAK-TO-PEAK OUTPUT RIPPLE VOLTAGE
vs
LOAD CURRENT

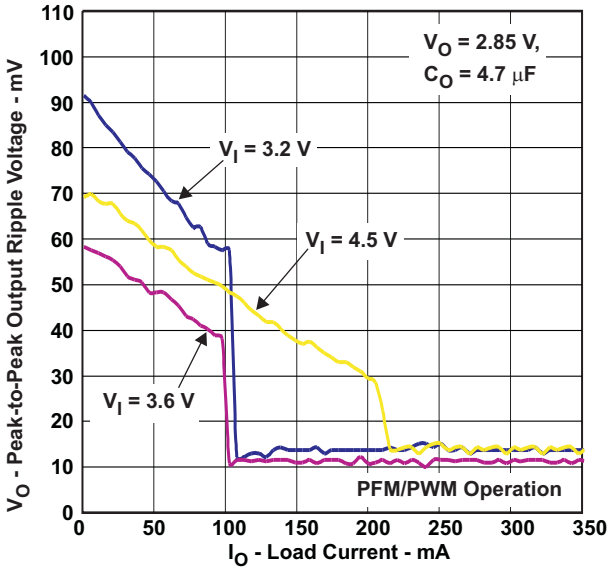


Figure 8.

TYPICAL CHARACTERISTICS (continued)

COMBINED LINE/LOAD TRANSIENT RESPONSE

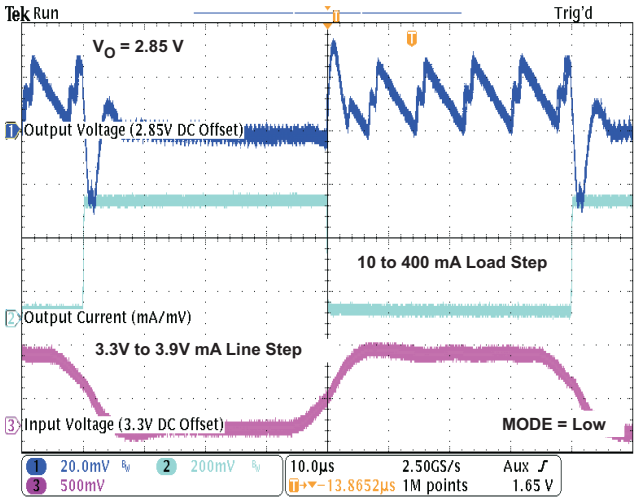


Figure 9.

COMBINED LINE/LOAD TRANSIENT RESPONSE

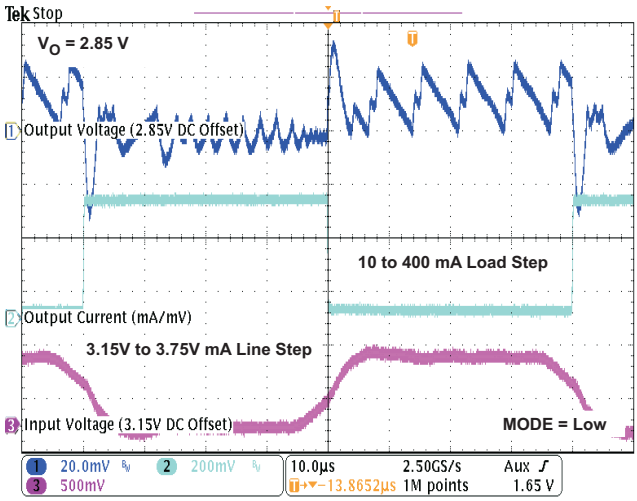


Figure 10.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

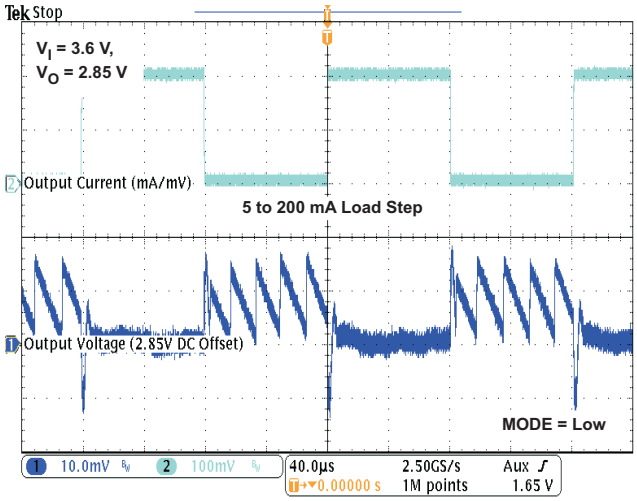


Figure 11.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

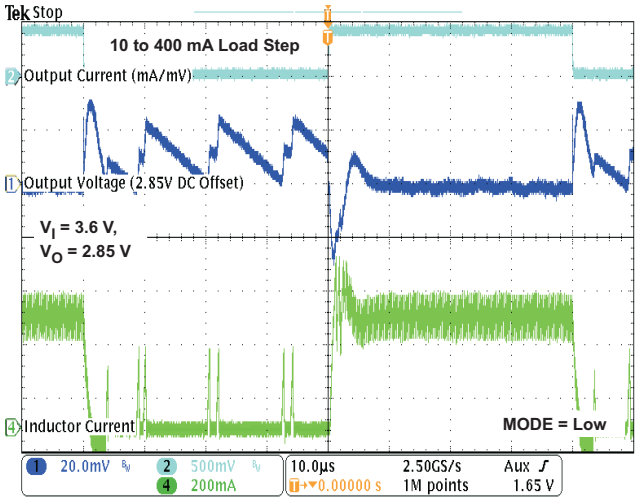


Figure 12.

TYPICAL CHARACTERISTICS (continued)

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

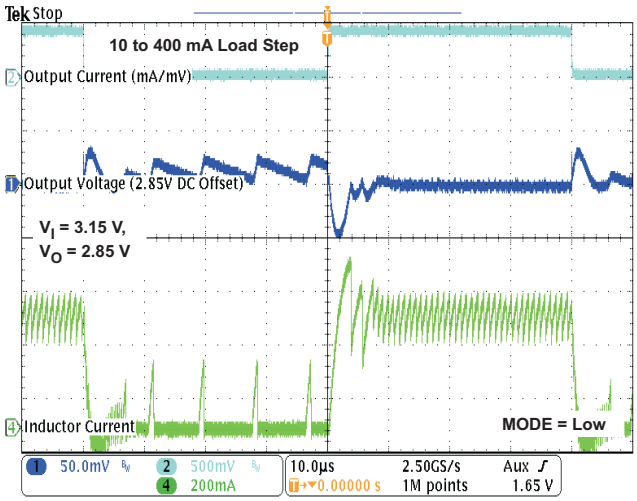


Figure 13.

LOAD TRANSIENT RESPONSE IN PFM/PWM OPERATION

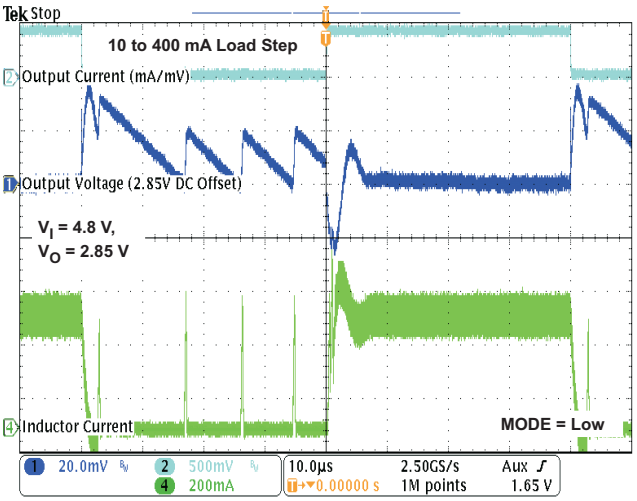


Figure 14.

AC LOAD TRANSIENT RESPONSE

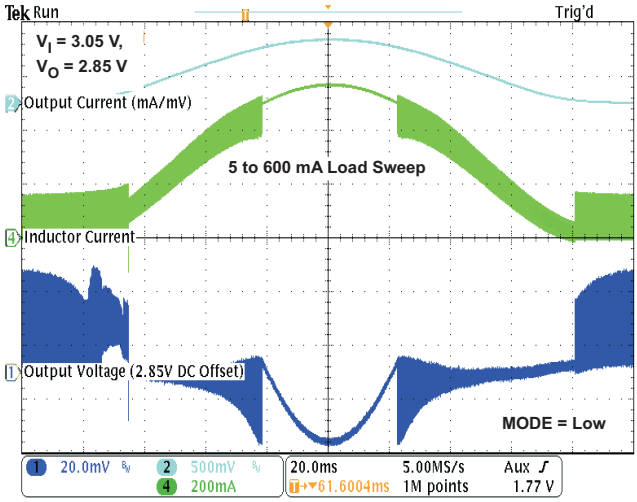


Figure 15.

AC LOAD TRANSIENT RESPONSE

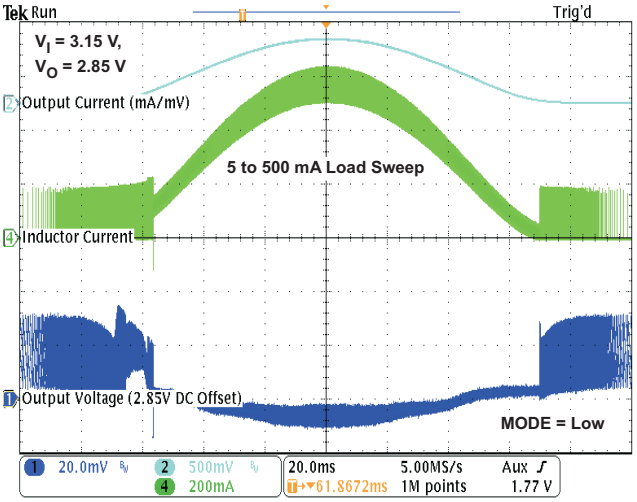


Figure 16.

TYPICAL CHARACTERISTICS (continued)

AC LOAD TRANSIENT RESPONSE

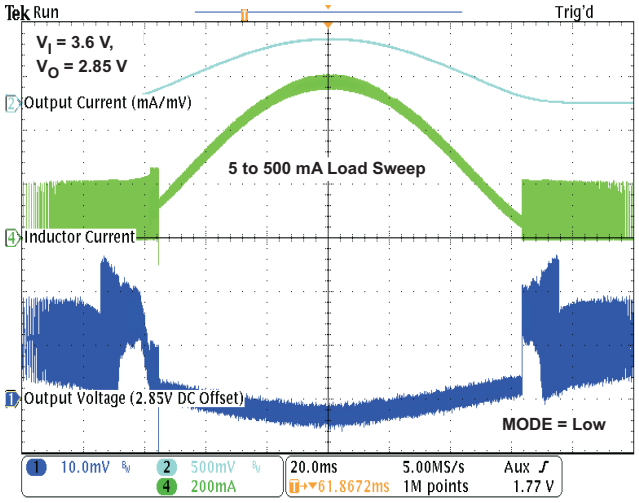


Figure 17.

AC LOAD TRANSIENT RESPONSE

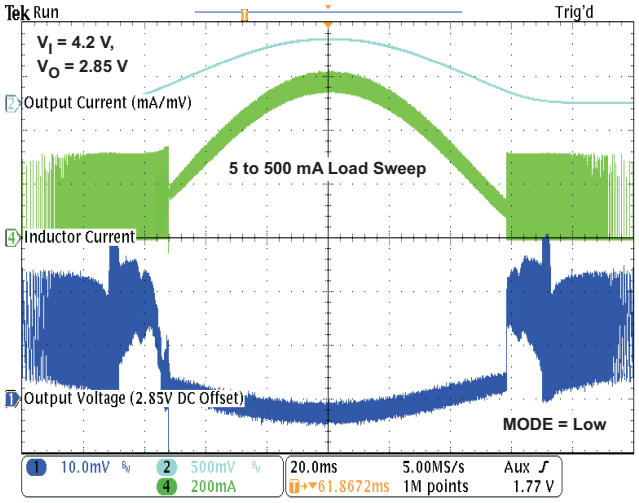


Figure 18.

DC OUTPUT VOLTAGE vs LOAD CURRENT

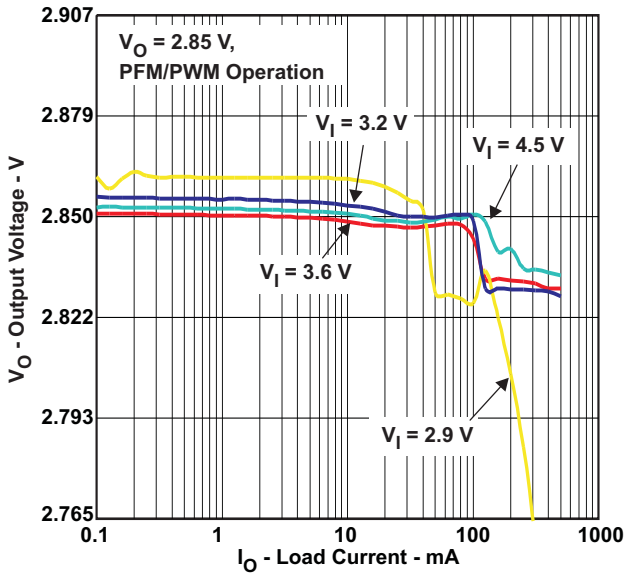


Figure 19.

DC OUTPUT VOLTAGE vs LOAD CURRENT

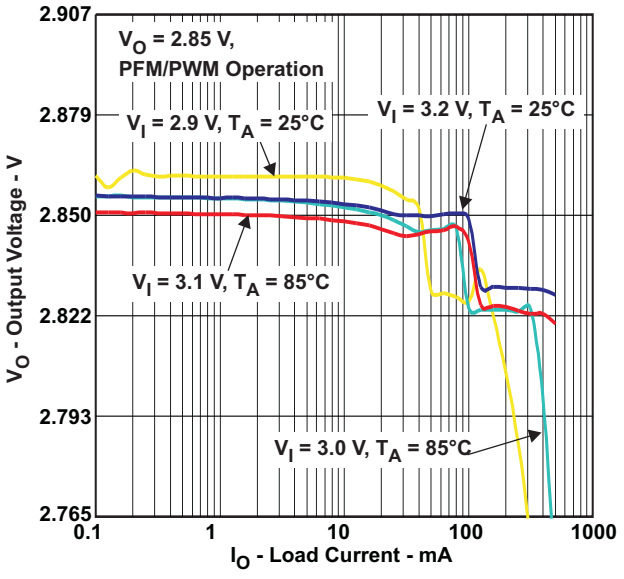


Figure 20.

TYPICAL CHARACTERISTICS (continued)

PFM/PWM BOUNDARIES

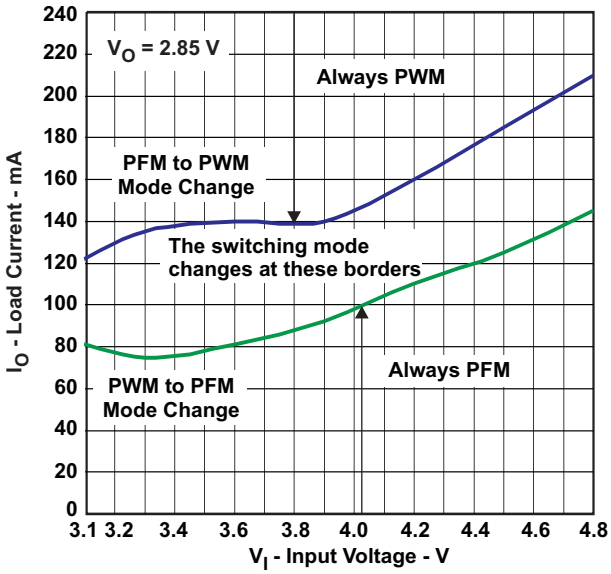


Figure 21.

QUIESCENT CURRENT
vs
INPUT VOLTAGE

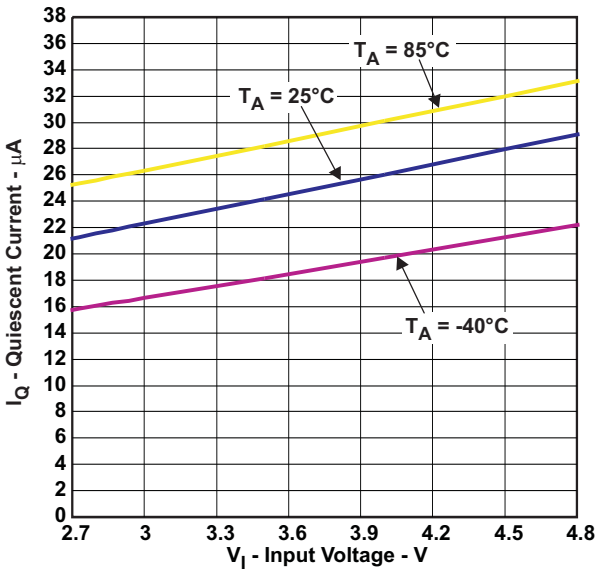


Figure 22.

PWM SWITCHING FREQUENCY
vs
INPUT VOLTAGE

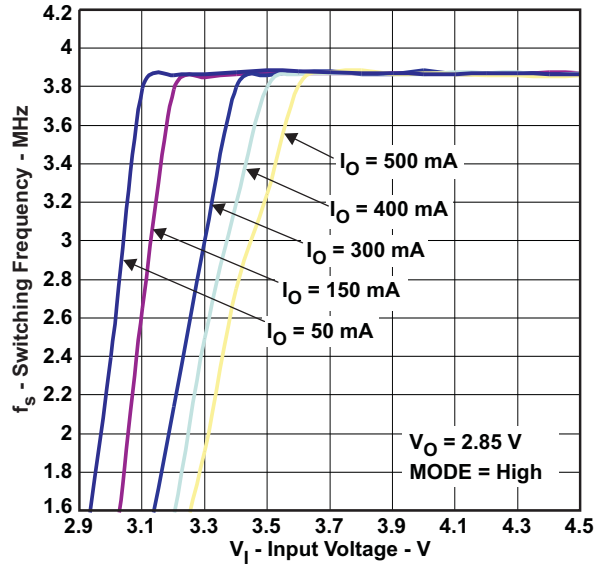


Figure 23.

PFM SWITCHING FREQUENCY
vs
INPUT VOLTAGE

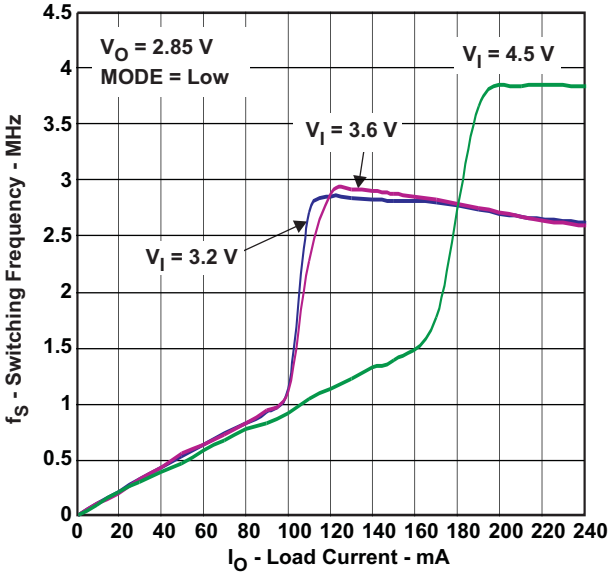


Figure 24.

TYPICAL CHARACTERISTICS (continued)

P-CHANNEL $r_{DS(ON)}$ vs INPUT VOLTAGE

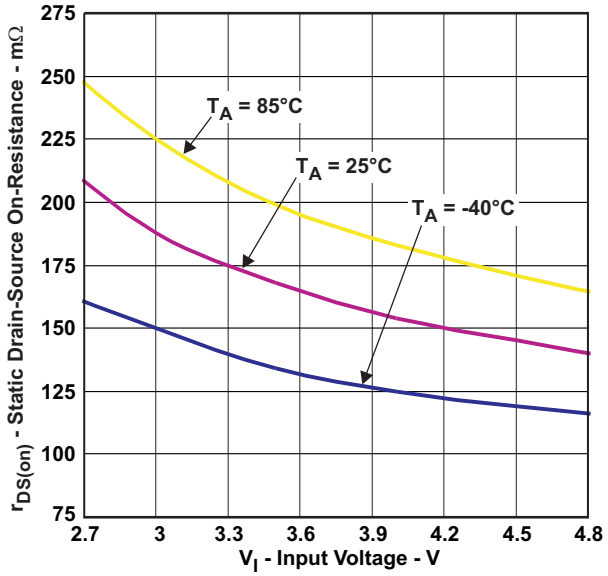


Figure 25.

N-CHANNEL $r_{DS(ON)}$ vs INPUT VOLTAGE

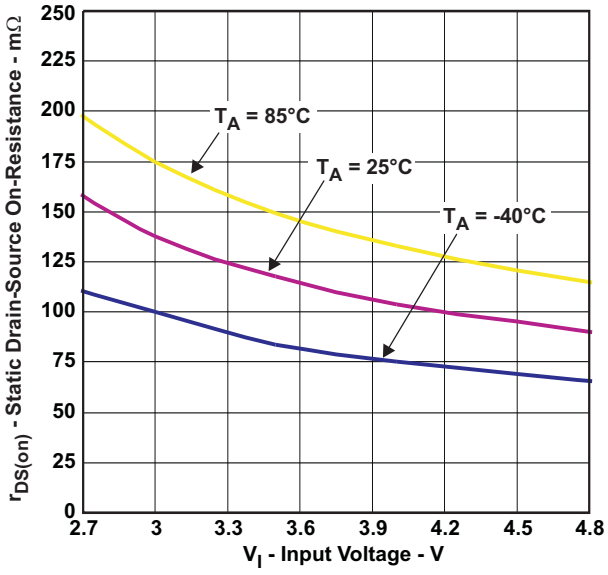


Figure 26.

PWM OPERATION

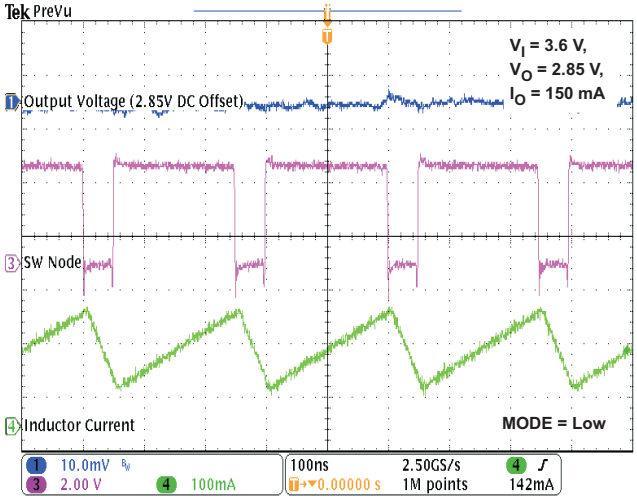


Figure 27.

POWER-SAVE MODE OPERATION

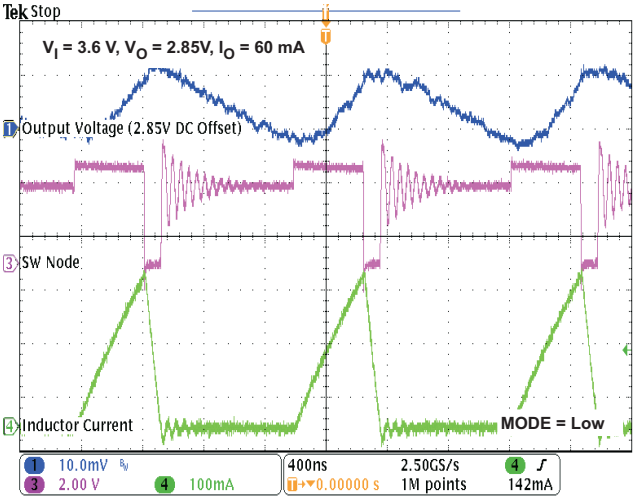


Figure 28.

TYPICAL CHARACTERISTICS (continued)

START-UP

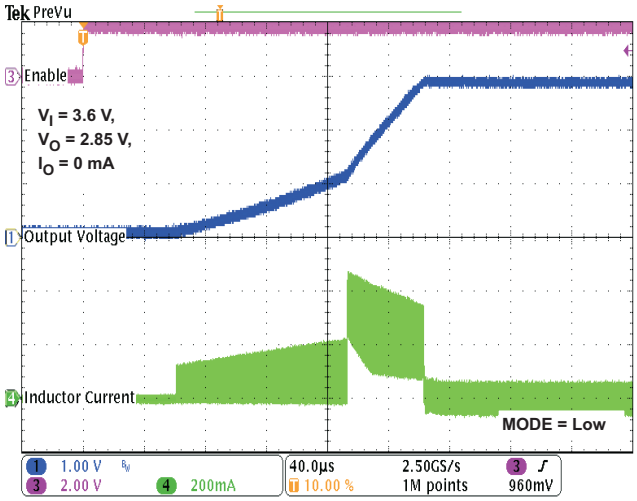


Figure 29.

START-UP

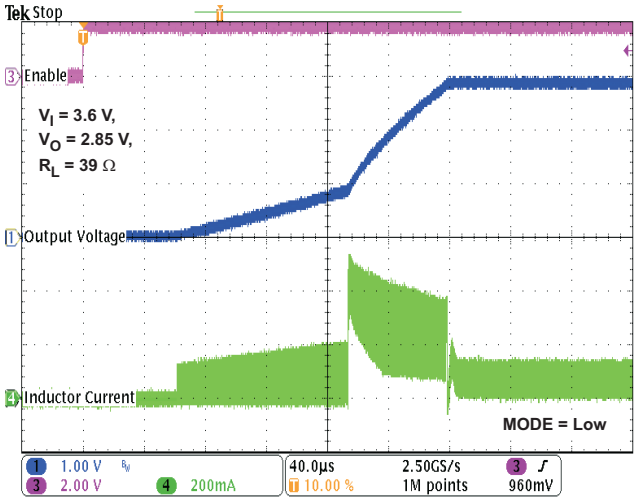


Figure 30.

POWER SUPPLY REJECTION RATIO vs FREQUENCY

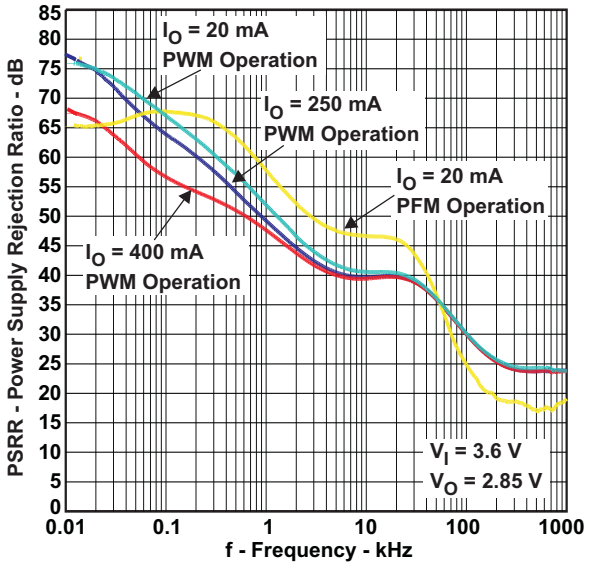


Figure 31.

SPURIOUS OUTPUT NOISE (PFM MODE) vs FREQUENCY

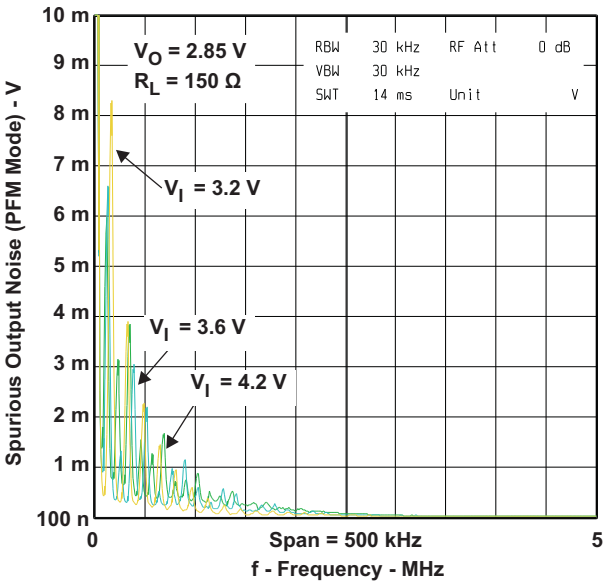


Figure 32.

TYPICAL CHARACTERISTICS (continued)

SPURIOUS OUTPUT NOISE (PWM MODE) vs FREQUENCY

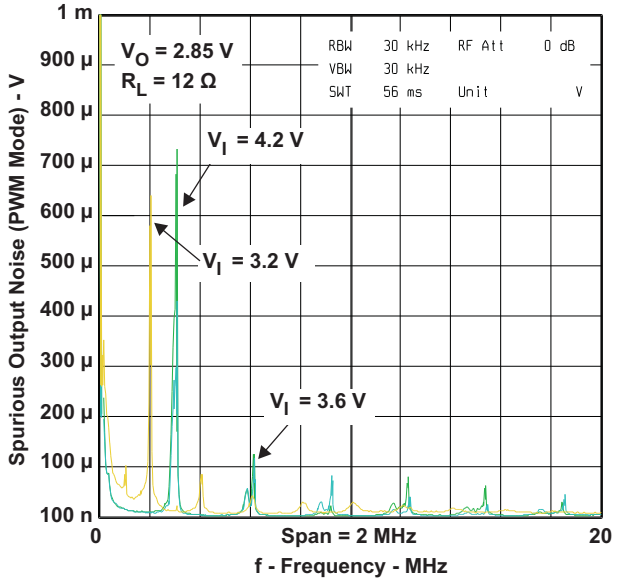


Figure 33.

OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

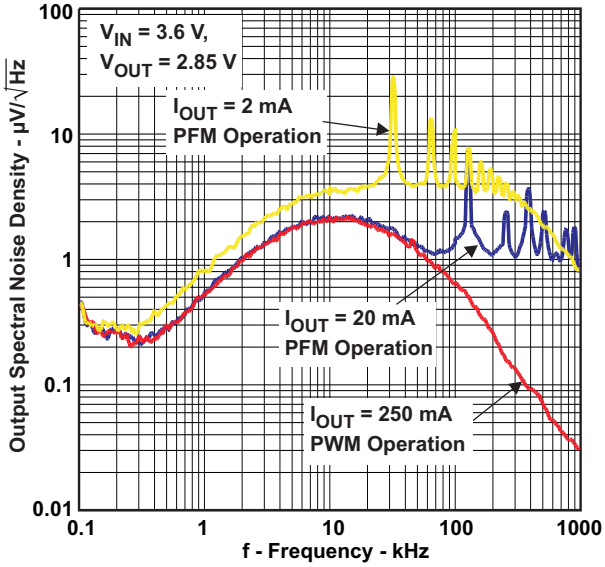


Figure 34.

DETAILED DESCRIPTION

OPERATION

The TPS6269x is a synchronous step-down converter typically operates at a regulated 4-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS6269x converter operates in power-save mode with pulse frequency modulation (PFM).

The converter uses a unique frequency locked ring oscillating modulator to achieve *best-in-class* load and line response and allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the P-channel MOSFET switch is turned on and the inductor current ramps up rising the output voltage until the main comparator trips, then the control logic turns off the switch.

One key advantage of the non-linear architecture is that there is no traditional feed-back loop. The loop response to change in V_O is essentially instantaneous, which explains the transient response. The absence of a traditional, high-gain compensated linear loop means that the TPS6269x is inherently stable over a range of L and C_O.

Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency lock loop (FLL) holds the switching frequency constant over a large range of operating conditions.

Combined with *best in class* load and line transient response characteristics, the low quiescent current of the device (ca. 19µA) allows to maintain high efficiency at light load, while preserving fast transient response for applications requiring tight output regulation.

SWITCHING FREQUENCY

The magnitude of the internal ramp, which is generated from the duty cycle, reduces for duty cycles either set of 50%. Thus, there is less overdrive on the main comparator inputs which tends to slow the conversion down. The intrinsic maximum operating frequency of the converter is about 5MHz to 7MHz, which is controlled to circa. 4MHz by a frequency locked loop.

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 4MHz. The tendency is for the converter to operate more towards a "constant inductor peak current" rather than a "constant frequency". In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the 4MHz nominal at extreme duty cycles, the application can be assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent serial inductance (ESL). This increases the *ESL step* seen at the main comparator's feed-back input thus decreasing its propagation delay, hence increasing the switching frequency.

POWER-SAVE MODE

If the load current decreases, the converter will enter Power Save Mode operation automatically. During power-save mode the converter operates in discontinuous current (DCM) single-pulse PFM mode, which produces low output ripple compared with other PFM architectures.

When in power-save mode, the converter resumes its operation when the output voltage trips below the nominal voltage. It ramps up the output voltage with a minimum of one pulse and goes into power-save mode when the inductor current has returned to a zero steady state. The PFM on-time varies inversely proportional to the input voltage and proportional to the output voltage giving the regulated switching frequency when in steady-state.

PFM mode is left and PWM operation is entered as the output current can no longer be supported in PFM mode. As a consequence, the DC output voltage is typically positioned ca. 0.5% above the nominal output voltage and the transition between PFM and PWM is seamless.

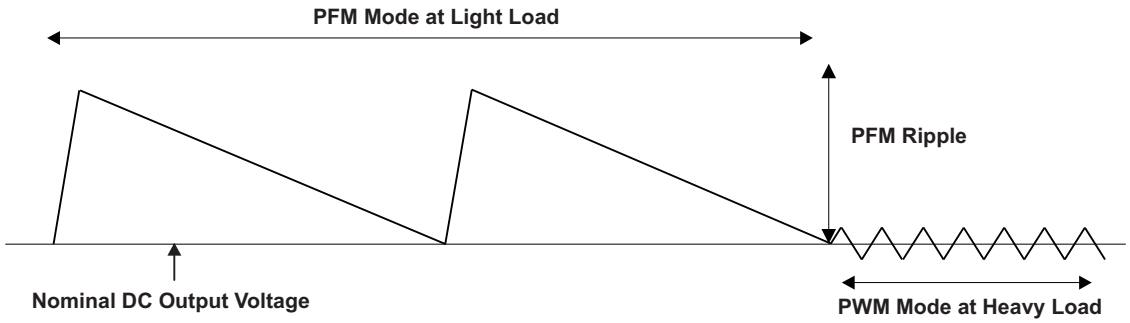


Figure 35. Operation in PFM Mode and Transfer to PWM Mode

MODE SELECTION

The MODE pin allows to select the operating mode of the device. Connecting this pin to GND enables the automatic PWM and power-save mode operation. The converter operates in regulated frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, which maintains high efficiency over a wide load current range.

Pulling the MODE pin high forces the converter to operate in the PWM mode even at light load currents. The advantage is that the converter modulates its switching frequency according to a spread spectrum PWM modulation technique allowing simple filtering of the switching harmonics in noise-sensitive applications. In this mode, the efficiency is lower compared to the power-save mode during light loads.

For additional flexibility, it is possible to switch from power-save mode to PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

LOW DROPOUT, 100% DUTY CYCLE OPERATION

The device starts to enter 100% duty cycle mode once input and output voltage come close together. In order to maintain the output voltage, the P-channel MOSFET is turned on 100% for one or more cycles.

With further decreasing V_{IN} the high-side switch is constantly turned on, thereby providing a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}\text{min} = V_{OUT}\text{max} + I_{OUT}\text{max} \times \left(R_{DS(on)}\text{max} + R_L\right) \quad (1)$$

With:

I_{OUT}max = Maximum output current, plus inductor ripple current.
$R_{DS(on)}$max = Maximum P-channel MOSFET $R_{DS(on)}$.
R_L = Inductor DC resistance.
V_{OUT}max = Nominal output voltage, plus maximum output voltage tolerance.

ENABLE

The TPS6269x device starts operation when EN is set high and starts up with the soft start as previously described. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown, with a shutdown quiescent current of typically 0.2μA. In this mode, the P and N-channel MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal-control circuitry is switched off.

The TPS6269x device can actively discharge the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 100 Ω. The required time to discharge the output capacitor at the output node depends on load current and the output capacitance value.

SOFT START

The TPS6269x has an internal soft-start circuit that limits the inrush current during start-up. This limits input voltage drops when a battery or a high-impedance power source is connected to the input of the converter.

The soft-start system progressively increases the on-time from a minimum pulse-width of 35ns as a function of the output voltage. This mode of operation continues for c.a. 150μs after enable. Should the output voltage not have reached its target value by this time, such as a heavy load, the soft-start transitions to a second mode of operation.

The converter then operates in a current limit mode, specifically the P-MOS current limit is set to half the nominal limit, and the N-channel MOSFET remains on until the inductor current has reset. After a further 150 μs, the device ramps up to the full current limit operation if the output voltage has risen above 0.5V (approximately). Therefore, the start-up time mainly depends on the output capacitor and load current.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on the switch or rectifier MOSFET under undefined conditions. The TPS6269x device have a UVLO threshold set to 2.05V (typical). Fully functional operation is permitted down to 2.1V input voltage.

SHORT-CIRCUIT PROTECTION

The TPS6269x integrates a P-channel MOSFET current limit to protect the device against heavy load or short circuits. When the current in the P-channel MOSFET reaches its current limit, the P-channel MOSFET is turned off and the N-channel MOSFET is turned on. The regulator continues to limit the current on a cycle-by-cycle basis.

As soon as the output voltage falls below ca. 0.4V, the converter current limit is reduced to half of the nominal value. Because the short-circuit protection is enabled during start-up, the device does not deliver more than half of its nominal current limit until the output voltage exceeds approximately 0.5V. This needs to be considered when a load acting as a current sink is connected to the output of the converter.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the P- and N-channel MOSFETs are turned off. The device continues its operation when the junction temperature again falls below typically 130°C.

APPLICATION INFORMATION

INDUCTOR SELECTION

The TPS6269x series of step-down converters have been optimized to operate with an effective inductance value in the range of 0.5µH to 1.8µH and with output capacitors in the range of 4.7µF to 10µF. The internal compensation is optimized to operate with an output filter of L = 1µH and C_O = 4.7µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For more details, see the *CHECKING LOOP STABILITY* section.

The inductor value affects its peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its dc resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

$$\Delta I_L = \frac{V_O}{V_I} \times \frac{V_I - V_O}{L \times f_{SW}} \qquad \Delta I_{L(MAX)} = I_{O(MAX)} + \frac{\Delta I_L}{2}$$

with: f_{SW} = switching frequency (4 MHz typical)

L = inductor value

ΔI_L = peak-to-peak inductor ripple current

$I_{L(MAX)}$ = maximum inductor current (2)

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance $_{(DC)}$) and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6269x converters.

Table 1. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS (in mm)
MURATA	LQM21PN1R0NGC	2.0 x 1.2 x 1.0 max. height
	LQM21PN1R5MC0	2.0 x 1.2 x 0.55 max. height
FDK	MIPS2012D1R0-X2	2.0 x 1.2 x 1.0 max. height
TAIYO YUDEN	NM2012N1R0M	2.0 x 1.2 x 1.0 max. height
TOKO	MDT2012-CH1R0A	2.0 x 1.2 x 1.0 max. height

OUTPUT CAPACITOR SELECTION

The advanced fast-response voltage mode control scheme of the TPS6269x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For best performance, the device should be operated with a minimum effective output capacitance of 1µF. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At nominal load current, the device operates in PWM mode and the overall output voltage ripple is the sum of the voltage step caused by the output capacitor ESL and the ripple current flowing through the output capacitor impedance.

At light loads, the output capacitor limits the output ripple voltage and provides holdup during large load transitions. A 4.7µF or 10µF ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions. The typical output voltage ripple is ca. 0.5% to 1.5% of the nominal output voltage V_O.

The output voltage ripple during PFM mode operation can be kept small. The PFM pulse is time controlled, which allows to modify the charge transferred to the output capacitor by the value of the inductor. The resulting PFM output voltage ripple and PFM frequency depend in first order on the size of the output capacitor and the inductor value. The PFM frequency decreases with smaller inductor values and increases with larger once. Increasing the output capacitor value and the effective inductance will minimize the output ripple voltage.

INPUT CAPACITOR SELECTION

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required to prevent large voltage transients that can cause misbehavior of the device or interferences with other circuits in the system. For most applications, a 2.2 or 4.7-µF capacitor is sufficient. If the application exhibits a noisy or erratic switching frequency, the remedy should be found by experimenting with the value of the input capacitor.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_I and the power source lead to reduce ringing than can occur between the inductance of the power source leads and C_I.

CHECKING LOOP STABILITY

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin.

Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

LAYOUT CONSIDERATIONS

As for all switching power supplies, the layout is an important step in the design. High-speed operation of the TPS6269x devices demand careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulator could show poor line and/or load regulation, stability and switching frequency issues as well as EMI problems. It is critical to provide a low inductance, impedance ground path. Therefore, use wide and short traces for the main current paths.

The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. In order to get an optimum *ESL step*, the output voltage feedback point (FB) should be taken in the output capacitor path, approximately 1mm away for it. The feed-back line should be routed away from noisy components and traces (e.g. SW line).

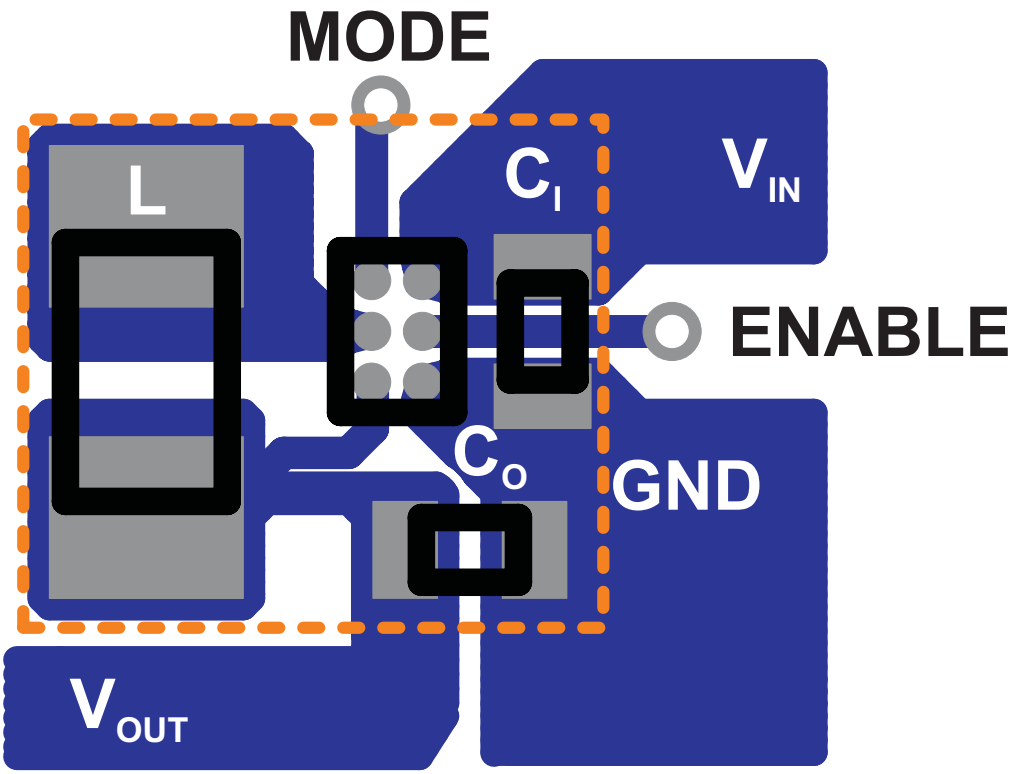


Figure 36. Suggested Layout (Top)

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

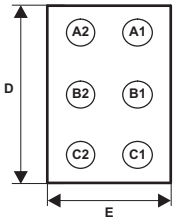
- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow into the system

The maximum recommended junction temperature (T_J) of the TPS6269x devices is 105°C. The thermal resistance of the 6-pin CSP package (YFF-6) is $R_{\theta JA}$ = 125°C/W. Regulator operation is specified to a maximum steady-state ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 160 mW.

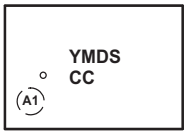
$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{105°C - 85°C}{125°C/W} = 160mW \quad (3)$$

PACKAGE SUMMARY

CHIP SCALE PACKAGE (BOTTOM VIEW)



CHIP SCALE PACKAGE (TOP VIEW)



Code:

- YM — Year Month date Code
- D — Day of laser mark
- S — Assembly site code
- CC— Chip code

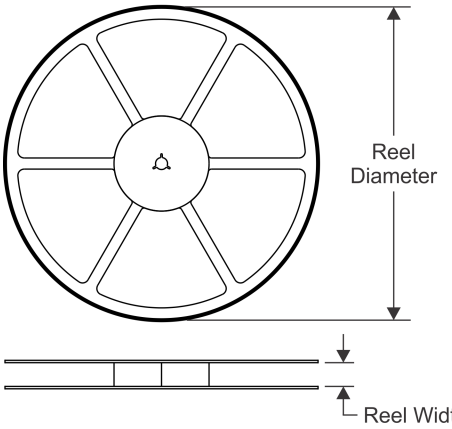
CHIP SCALE PACKAGE DIMENSIONS

The TPS6269x device is available in an 6-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

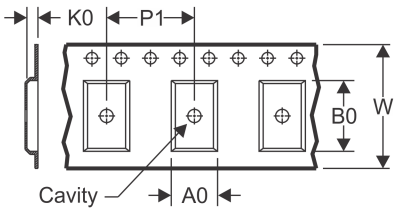
D	E
Max = 1.33 mm	Max = 0.956 mm
Min = 1.27 mm	Min = 0.896 mm

TAPE AND REEL INFORMATION

REEL DIMENSIONS

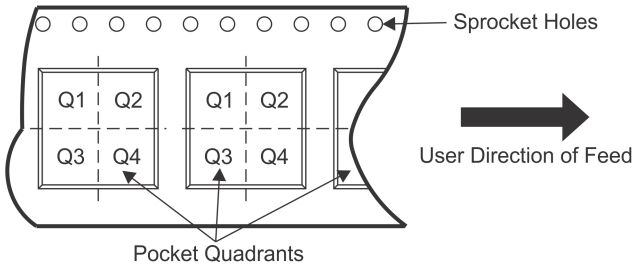


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

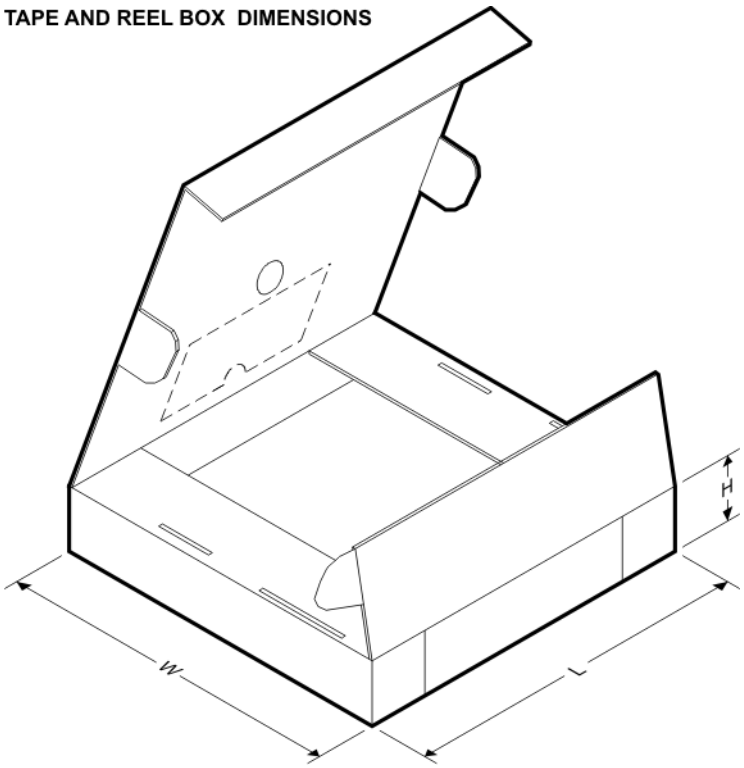
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62690YFFR	DSBGA	YFF	6	3000	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1
TPS62690YFFT	DSBGA	YFF	6	250	180.0	8.4	1.07	1.42	0.74	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

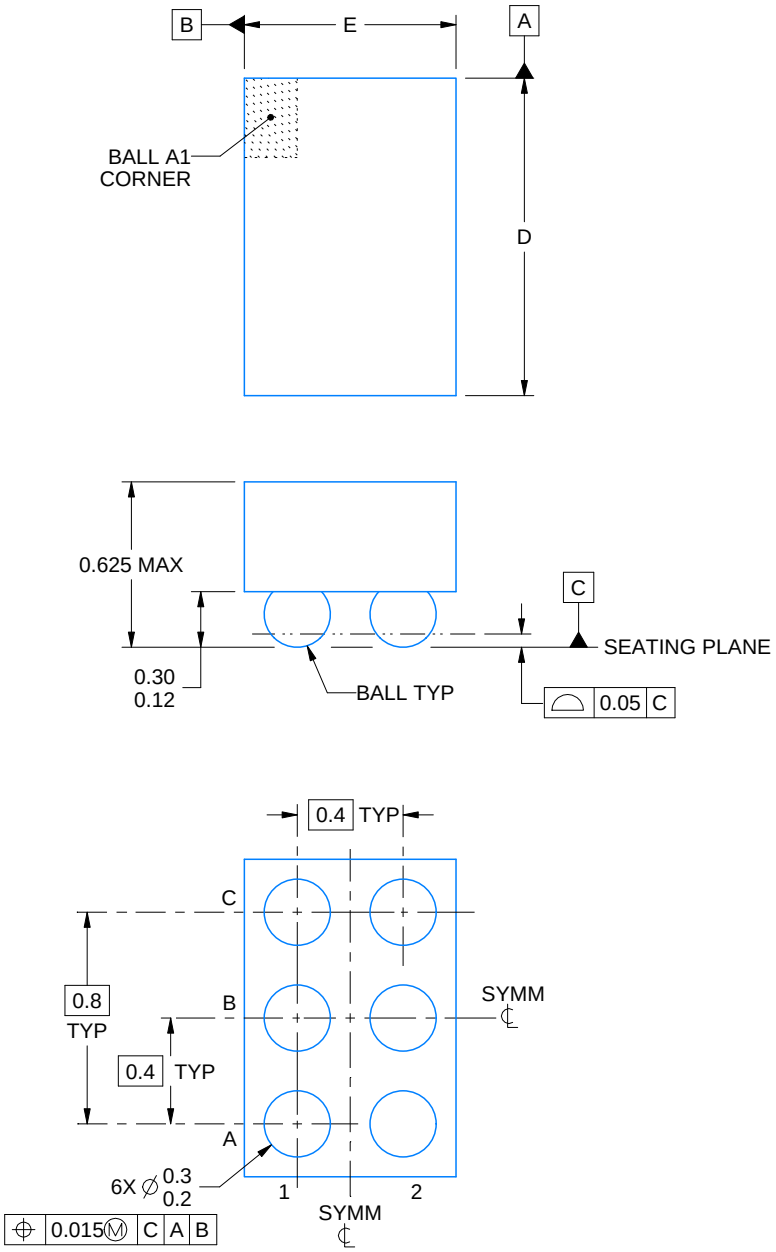
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62690YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS62690YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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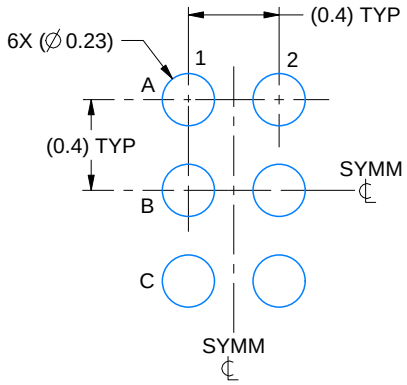
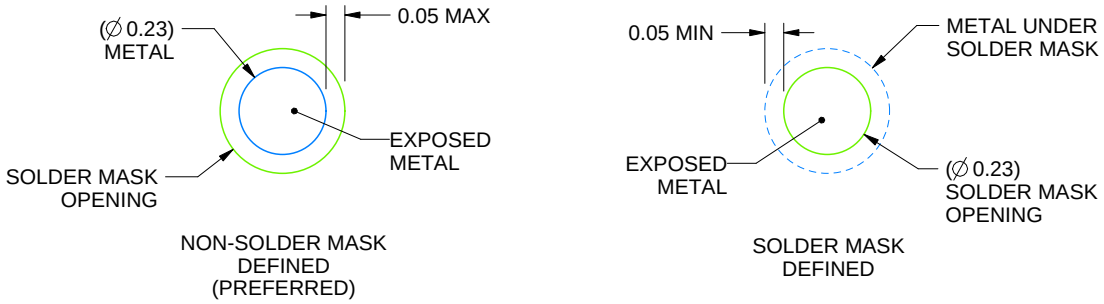
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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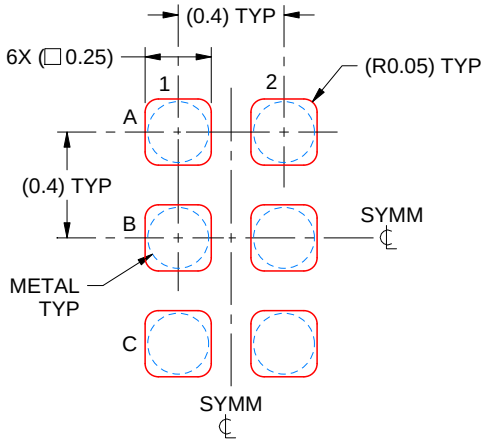
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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