TPS75003 可配置多轨 PMIC

1 特性

- 两个效率为 95% 的 3A 降压控制器和一个 300mA LDO
- 经过了 Xilinx 的测试和认可，可为 Spartan™-3、Spartan-3E 和 Spartan-3L FPGA 供电
- 在所有通道上具有可调（降压控制器为 1.2V 至 6.5V，LDO 为 1.0V 至 6.5V）输出电压
- 输入电压范围：2.2V 至 6.5V
- 每个电源的独立软启动
- 每个电源的独立使能，支持灵活定序
- LDO 与 2.2µF 陶瓷输出电容器一起工作，可保持稳定
- 小型低厚度 4.5mm × 3.5mm × 0.9mm VQFN 封装

2 应用

- FPGA、DSP 和 ASIC 电源
- 机顶盒
- DSL 调制解调器
- 等离子电视显示面板

3 说明

TPS75003 是一个面向 FPGA、DSP 和其他多电源应用的完整电源管理解决 方案。该器件已经过测试，符合所有 Xilinx Spartan-3、Spartan-3E 和 Spartan-3L 启动曲线要求，包括单调电压斜坡和最小电压轨上升时间。每个输出均具有独立的使能，因此可进行排序，以最大限度地减少启动时对电源的需求。各个电源上的软启动会限制启动期间的浪涌电流。两个集成式降压控制器支持为低电流和高电流电源（如内核和 I/O）进行具有成本效益的高效电压转换。该器件还集成了一个 300mA LDO，可在 Xilinx Spartan-3 FPGA 上提供辅助电源轨，例如 V_{CCAUX}。三个输出电压均支持外部配置，可实现最大灵活性。

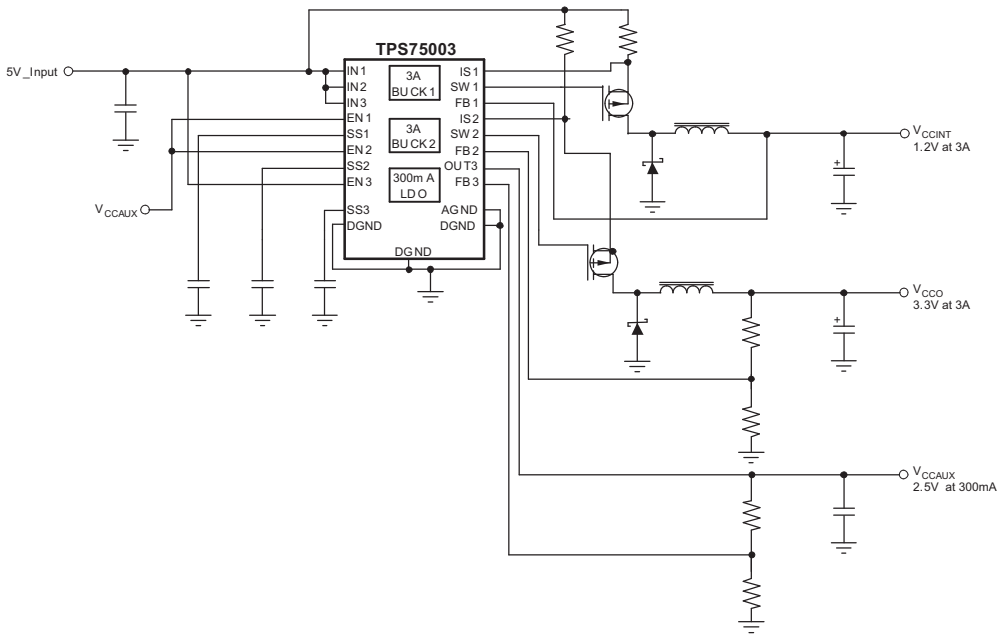
TPS75003 的额定温度范围为 –40°C 至 +85°C，采用了 VQFN 封装，可实现高度紧凑的整体解决方案尺寸，同时获得高功耗能力。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS75003	VQFN (20)	4.50mm x 3.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用原理图



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision I (August 2010) to Revision J **Page**

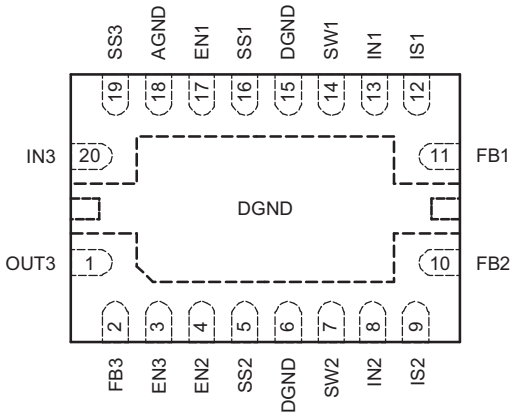
- 已更改 数据表的标题并将格式更新至最新的 TI 数据表格式 ... 1
- Moved the ESD rating parameters for HBM and CDM from the *Absolute Maximum Ratings* table to the *ESD Ratings* table ... 4
- Added the *Recommended Operating Conditions* table, *Overview* section, *Feature Description* section, *Design Requirements* section, *Power Supply Recommendations* section, and *Device and Documentation Support* section ... 4
- Updated the symbols for the thermal resistance parameters in the *Thermal Information* table ... 5

Changes from Revision H (August 2008) to Revision I **Page**

- Replaced the *Dissipation Ratings* table with the *Thermal Information* table ... 5

5 Pin Configuration and Functions

RHL Package
20-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	18	GND	Ground connection for LDO.
DGND	6, 15, PAD	GND	Ground connection for BUCK1 and BUCK2 converters. Pins 6 and 15 should be connected to the back side exposed pad by a short metal trace as shown in the *PCB Layout Considerations* section of this data sheet.
EN1	17	I	Driving the enable pin (ENx) high turns on BUCK1 regulator. Driving this pin low puts it into shutdown mode, reducing operating current. The enable pin does not trigger on fast negative going transients.
EN2	4	I	Same as EN1 but for BUCK2 controller.
EN3	3	I	Same as EN1 but for LDO.
FB1	11	I (Analog)	Feedback pin. Used to set the output voltage of BUCK1 regulator.
FB2	10	I (Analog)	Same as FB1 but for BUCK2 controller.
FB3	2	I (Analog)	Same as FB1 but for LDO.
IN1	13	I (Analog)	Input supply to BUCK1.
IN2	8	I (Analog)	Input supply to BUCK2.
IN3	20	I (Power)	Input supply to LDO.
IS1	12	I (Analog)	Current sense input for BUCK1 regulator. The voltage difference between this pin and IN1 is compared to an internal reference to set current limit. For a robust output start-up ramp, careful layout and bypassing are required. See the *Application Information* section for details.
IS2	9	I (Analog)	Same as IS1 but compared to IN2 and used for BUCK2 controller.
OUT3	1	O (Power)	Regulated LDO output. A small ceramic capacitor (≥ 2.2μF) is needed from this pin to ground to ensure stability.
SS1	16	I (Analog)	Connecting a capacitor between this pin and ground increases start-up time of the BUCK1 regulator by slowing the ramp-up of current limit. This high-impedance pin is noise-sensitive; careful layout is important. See the *Typical Characteristics*, *Application Information* , and *PCB Layout Considerations* sections for details.
SS2	5	I (Analog)	Same as SS1 but for BUCK2 regulator.
SS3	19	I (Analog)	Connecting a capacitor from this pin to ground slows the start-up time of the LDO reference, thereby slowing output voltage ramp-up. See the *Application Information* section for details.
SW1	14	O (Analog)	Gate drive pin for external BUCK1 P-channel MOSFET.
SW2	7	O (Analog)	Same as SW1 but for BUCK2 controller.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{INX}	IN1, IN2, IN3 voltage	–0.3	7	V
V_{ENX}	EN1, EN2, EN3 voltage	–0.3	V_{INX} + 0.3	V
V_{SWX}	SW1, SW2, SW3 voltage	–0.3	V_{INX} + 0.3	V
V_{ISX}	IS1, IS2, IS3 voltage	–0.3	V_{INX} + 0.3	V
V_{OUT3}	OUT3 voltage	–0.3	7	V
V_{SSX}	SS1, SS2, SS3 voltage	–0.3	V_{INX} + 0.3	V
V_{FBX}	FB1, FB2, FB3 voltage	–0.3	3.3	V
I_{OUT3}	Peak LDO output current	Internally limited		
	Continuous total power dissipation	See *Thermal Information* Table		
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN1}	Input voltage at IN1 pin	2.2		6.5	V
V_{OUT1}	Output voltage of BUCK1	1.2		V_{IN1}	V
I_{OUT1}	Maximum output current of BUCK1			3	A
V_{IN2}	Input voltage at IN2 pin	2.2		6.5	V
V_{OUT2}	Output voltage of BUCK1	1.2		V_{IN2}	V
I_{OUT2}	Maximum output current of BUCK2			3	A
V_{IN3}	Input voltage at IN3 pin	2.2		6.5	V
V_{OUT3}	Output voltage of LDO	1		$V_{IN3} – V_{DO}$	V
I_{OUT3}	Maximum output current of LDO			300	mA

6.4 Thermal Information

THERMAL METRIC[1]		TPS75003 RHL (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

$V_{EN1} = V_{IN1}$, $V_{EN2} = V_{IN2}$, $V_{EN3} = V_{IN3}$, $V_{IN1} = V_{IN2} = 2.2V$, $V_{IN3} = 3.0V$, $V_{OUT3} = 2.5V$, $C_{OUT1} = C_{OUT2} = 47\mu F$, $C_{OUT3} = 2.2\mu F$, T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply and Logic						
V_{INX}	Input Voltage Range (IN1, IN2, IN3)[1]		2.2		6.5	V
I_Q	Quiescent Current, $I_Q = I_{DGND} + I_{AGND}$	$I_{OUT1} = I_{OUT2} = 0mA$, $I_{OUT3} = 1mA$		75	150	µA
I_{SHDN}	Shutdown Supply Current	$V_{EN1} = V_{EN2} = V_{EN3} = 0V$		0.05	3	µA
$V_{IH1, 2}$	Enable High, enabled (EN1, EN2)		1.4		V_{INX}	V
V_{IH3}	Enable High, enabled (EN3)		1.14		V_{IN3}	V
V_{ILX}	Enable Low, shutdown (EN1, EN2, EN3)		0		0.3	V
I_{ENX}	Enable pin current (EN1, EN2, EN3)			0.01	0.5	µA
Buck Controllers 1 and 2						
$V_{OUT1,2}$	Adjustable Output Voltage Range[2]		V_{FBX}		V_{INX}	V
$V_{FB1,2}$	Feedback Voltage (FB1, FB2)			1.220		V
	Feedback Voltage Accuracy[1] (FB1, FB2)		–2%		2%	
$I_{FB1,2}$	Current into FB1, FB2 pins			0.01	0.5	µA
$V_{IS1,2}$	Reference Voltage for Current Sense		80	100	120	mV
$I_{IS1,2}$	Current into IS1, IS2 Pins			0.01	0.5	µA
$\Delta V_{OUT\%}/\Delta V_{IN}$	Line Regulation[1]	Measured with the circuit in Figure 18, $V_{OUT} + 0.5V \le V_{IN} \le 6.5V$		0.1		%/V
$\Delta V_{OUT\%}/\Delta I_{OUT}$	Load Regulation	Measured with the circuit in Figure 18, $30mA \le I_{OUT} \le 2A$		0.6		%/A
$n_{1,2}$	Efficiency[3]	Measured with the circuit in Figure 18, $I_{OUT} = 1A$		94%		
$t_{STR1,2}$	Startup Time[3]	Measured with the circuit in Figure 18, $R_L = 6\Omega$, $C_{OUT} = 100\mu F$, $C_{SS} = 2.2nF$		5		ms

(1) To be in regulation, minimum V_{IN1} (or V_{IN2}) must be greater than $V_{OUT1,NOM}$ (or $V_{OUT2,NOM}$) by an amount determined by external components. Minimum $V_{IN3} = V_{OUT3} + V_{DO}$ or 2.2V, whichever is greater.
(2) Maximum V_{OUT} depends on external components and will be less than V_{IN}.
(3) Depends on external components.

Electrical Characteristics (continued)

$V_{EN1} = V_{IN1}$, $V_{EN2} = V_{IN2}$, $V_{EN3} = V_{IN3}$, $V_{IN1} = V_{IN2} = 2.2V$, $V_{IN3} = 3.0V$, $V_{OUT3} = 2.5V$, $C_{OUT1} = C_{OUT2} = 47\mu F$, $C_{OUT3} = 2.2\mu F$, T_A = –40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

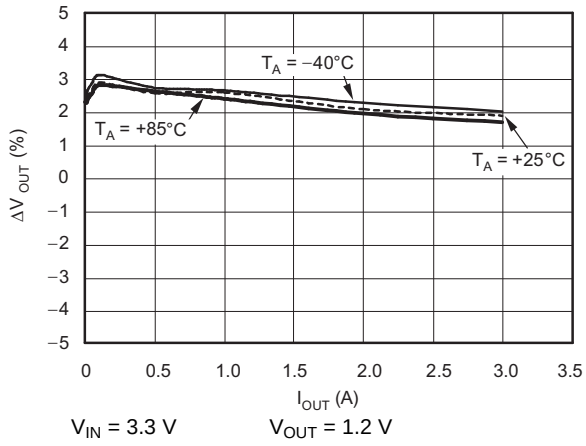
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS,ON1,2}$	Gate Driver P-Channel and N-Channel MOSFET On-Resistance	$V_{IN1,2} > 2.5V$		4		Ω
		$V_{IN1,2} = 2.2V$		6		
$I_{SW1,2}$	Gate Driver P-Channel and N-Channel MOSFET Drive Current			100		mA
t_{ON}	Minimum On Time		1.36	1.55	1.84	µs
t_{OFF}	Minimum Off Time		0.44	0.65	0.86	µs
LDO						
V_{OUT3}	Output Voltage Range		1		6.5 – V_{DO}	V
V_{FB3}	Feedback Pin Voltage			0.507		V
	Feedback Pin Voltage Accuracy(1)	2.95V ≤ V_{IN3} ≤ 6.5V 1mA ≤ I_{OUT3} ≤ 300mA	–4%		4%	
$\Delta V_{OUT\%}/\Delta V_{IN}$	Line Regulation(1)	V_{OUT3} + 0.5V ≤ V_{IN3} ≤ 6.5V		0.075		%/V
$\Delta V_{OUT\%}/\Delta I_{OUT}$	Load Regulation	10mA ≤ I_{OUT3} ≤ 300mA		0.01		%/mA
V_{DO}	Dropout Voltage (V_{IN} = $V_{OUT(NOM)}$ – 0.1)(4)	I_{OUT3} = 300mA		250	350	mV
I_{CL3}	Current Limit	V_{OUT} = 0.9 x $V_{OUT(NOM)}$	375	600	1000	mA
I_{FB3}	Current into FB3 pin			0.03	0.1	µA
V_n	Output Noise	BW = 100Hz – 100kHz, I_{OUT3} = 300mA		400		μV_{RMS}
t_{SD}	Thermal Shutdown Temperature for LDO	Shutdown, Temp Increasing		175		°C
		Reset, Temp Decreasing		160		
UVLO	Under-Voltage Lockout Threshold	V_{IN} Rising		1.80		V
	Under-Voltage Lockout Hysteresis	V_{IN} Falling		100		mV

(4) V_{DO} does not apply when $V_{OUT} + V_{DO} < 2.2V$.

6.6 Typical Characteristics

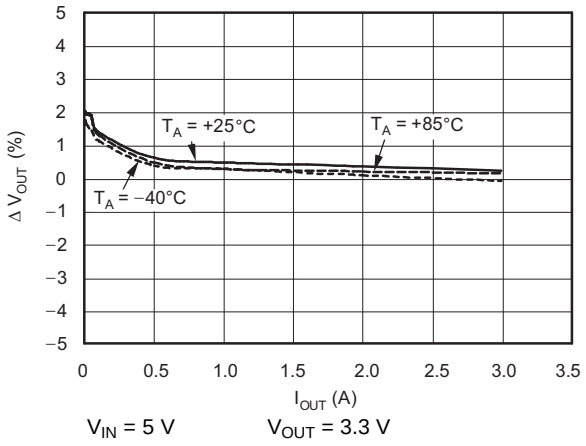
Measured using circuit in Figure 18.

6.6.1 Buck Converter



V_{IN} = 3.3 V V_{OUT} = 1.2 V

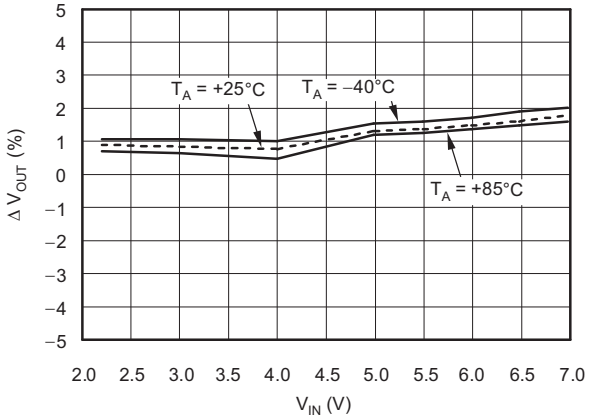
Figure 1. Buck Load Regulation



V_{IN} = 5 V V_{OUT} = 3.3 V

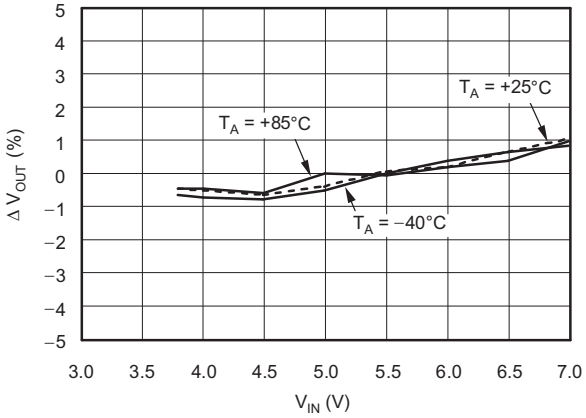
Figure 2. Buck Load Regulation

Buck Converter (continued)



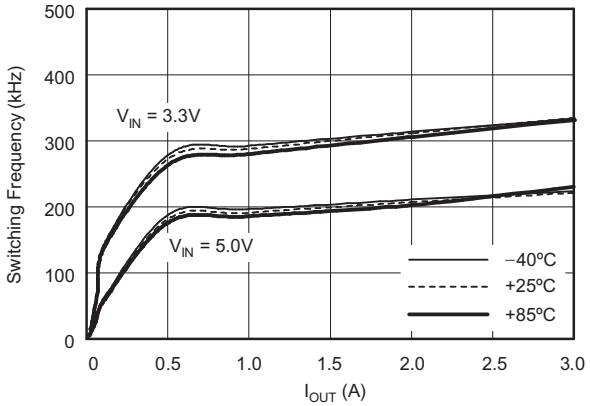
V_{OUT} = 1.2 V I_{OUT} = 2 A

Figure 3. Buck Line Regulation



V_{OUT} = 3.3 V I_{OUT} = 2 A

Figure 4. Buck Line Regulation



V_{OUT} = 1.2 V

Figure 5. Buck Switching Frequency vs I_{OUT}, T_A

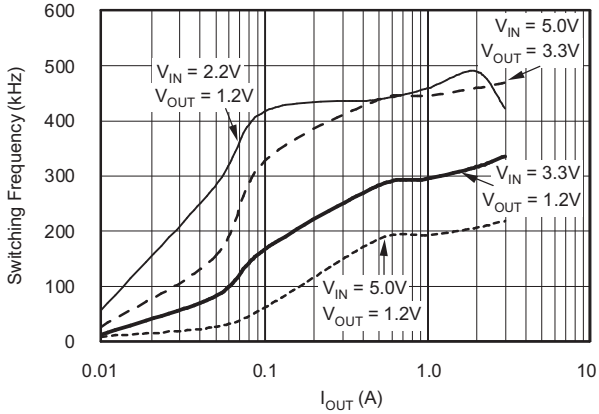


Figure 6. Buck Switching Frequency vs I_{OUT}

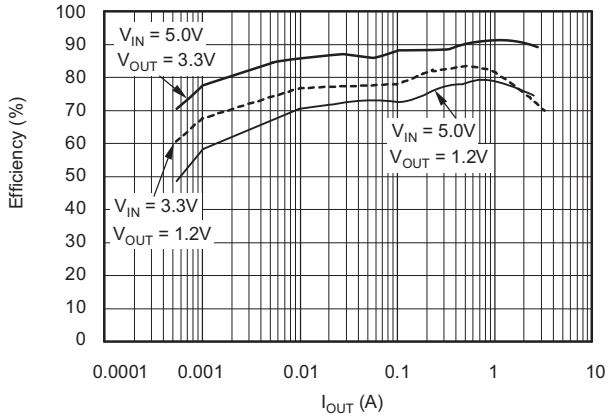
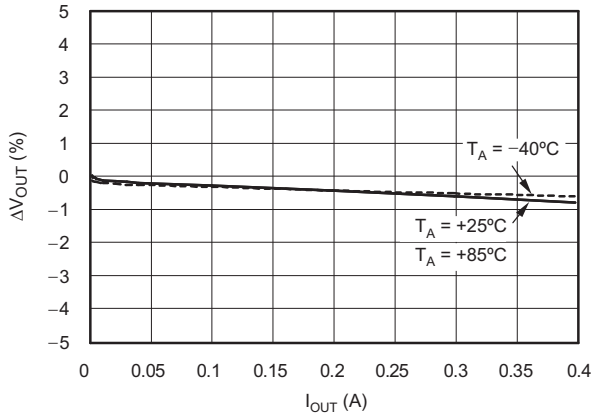


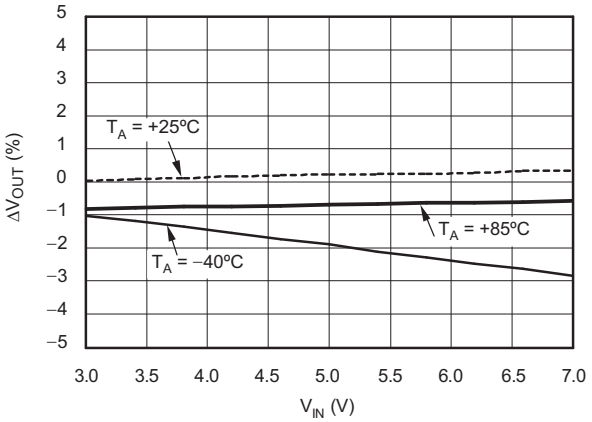
Figure 7. Efficiency vs I_{OUT}

6.6.2 LDO Converter



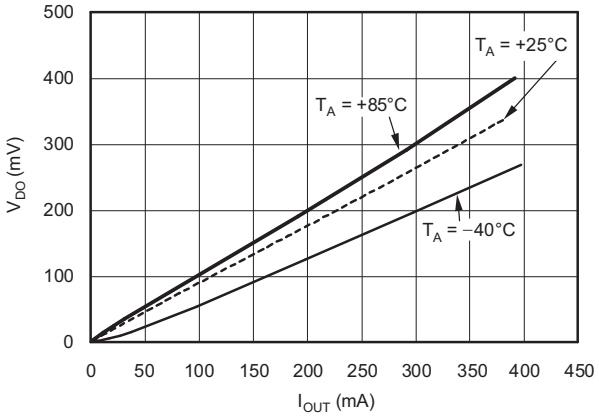
V_{IN} = 3.3 V V_{OUT} = 2.5 V

Figure 8. LDO Load Regulation



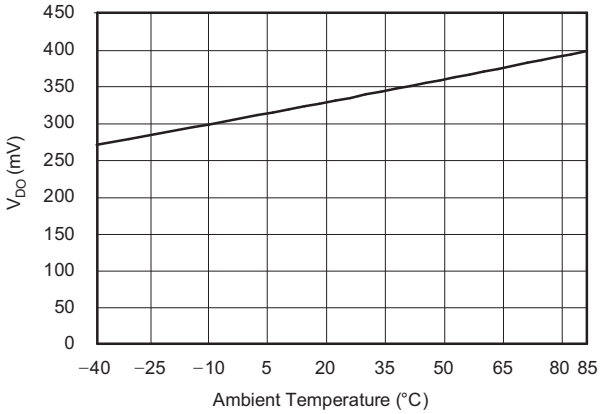
V_{OUT} = 2.5 V I_{OUT} = 1 mA

Figure 9. LDO Line Regulation



V_{IN} = 3.3 V V_{OUT} = 2.5 V

Figure 10. LDO Dropout vs I_{OUT}



V_{OUT} = 2.5 V I_{OUT} = 300 mA

Figure 11. LDO Dropout vs T_A

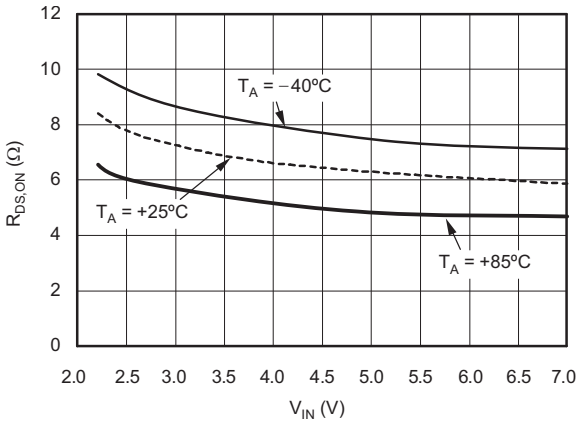


Figure 12. $R_{DS,ON}$ PMOS vs V_{IN}

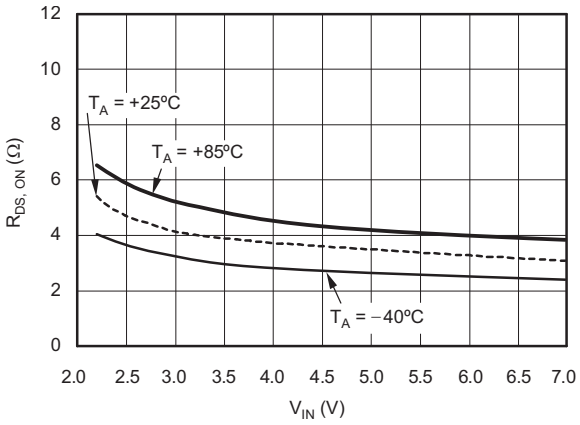
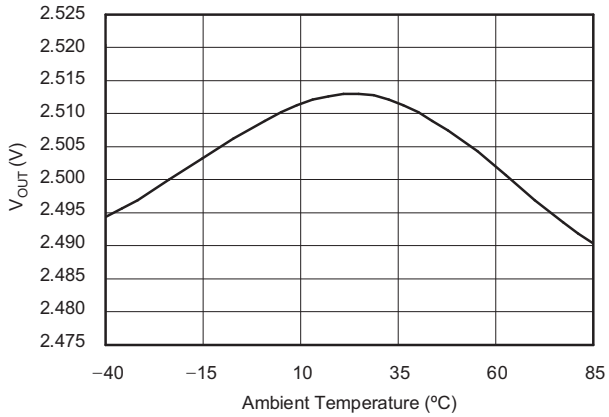


Figure 13. $R_{DS,ON}$ NMOS vs V_{IN}

LDO Converter (continued)



V_{IN} = 3.3 V

Figure 14. LDO V_{OUT} vs T_A

7 Detailed Description

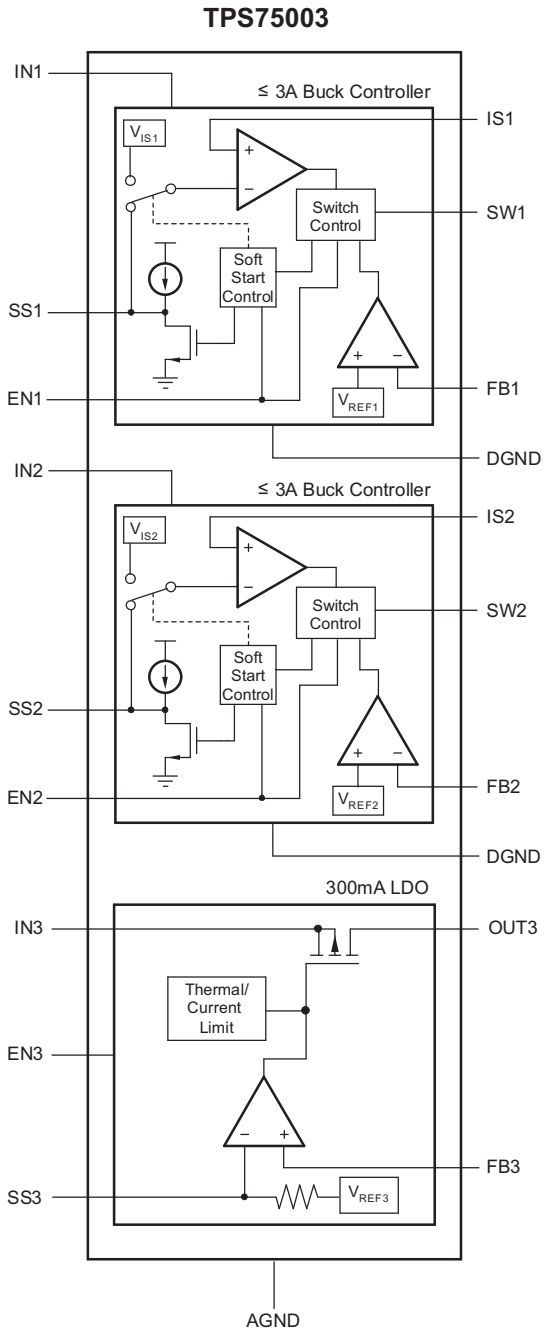
7.1 Overview

The TPS75003 device is a power management IC (PMIC) with two buck controllers and one integrated LDO regulator. The three voltage regulators have independent enable pins for flexible power sequence timing, and all of the output voltages are set by external feedback resistor dividers. The independent power regulators can be wired in parallel, in series, or connected to separate input voltages as needed to meet the requirements of the application.

The two buck controllers are identical and operate over a input voltage range of 2.2 V to 6.5 V to supply a load with an externally configurable output voltage with up to 3-A of current. The buck controllers drive the gate of a single PMOS FET in an asynchronous buck regulator architecture. The use of a PMOS FET lets the buck regulator operate with 100% duty cycle when the input voltage is approximately equal to or less than the desired output voltage. The buck controllers have an eternally configurable current sense feature to limit the output current and protect the PMOS FET. The buck controllers have an externally configurable soft-start feature that ramps the voltage and meet the timing requirements of the load.

The LDO regulator integrates the FET and operates over the same input voltage range of 2.2 V to 6.5 V to supply a load with an externally configurable output voltage with up to 300-mA of current. The LDO regulator includes integrated current limiting and thermal protection features. The LDO regulator also has an externally configurable soft-start feature to ramp the voltage to meet desired timing requirements.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operation (Buck Controllers)

Channels 1 and 2 have two identical non-synchronous buck controllers that use minimum on-time and minimum off-time hysteretic control (see Figure 18. For clarity, BUCK1 is used throughout the discussion of device operation. When V_{OUT1} is less than its target, an external PMOS (Q1) is turned on for at least the minimum on-time, increasing current through the inductor (L1) until V_{OUT1} reaches its target value or the current limit (set by R1) is reached. When either of these conditions is met, the PMOS is switched off for at least the minimum off-time of the device. After the minimum off-time has passed, the output voltage is monitored and the switch is turned on again when necessary.

Feature Description (continued)

When output current is low, the buck controllers operate in discontinuous mode. In this mode, each switching cycle begins at zero inductor current, rises to a maximum value, then falls back to zero current. When current reaches zero on the falling edge, ringing occurs at the resonant frequency of the inductor and stray switch node capacitance. This operation is normal; it does not affect circuit performance, and can be minimized if desired by using an RC snubber, a resistor in series with the gate of the PMOS, or both as shown in Figure 15.

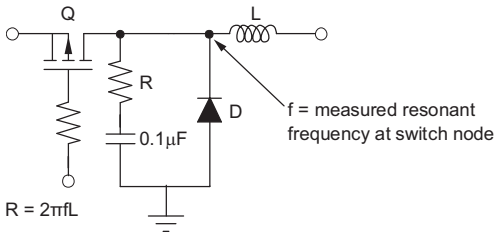


Figure 15. RC Snubber and Series Gate Resistor Used to Minimize Ringing

At higher output currents, the TPS75003 device operates in continuous mode. In continuous mode, there is no ringing at the switch node and V_{OUT} is equal to V_{IN} times the duty cycle of the switching waveform.

When V_{IN} approaches or falls to less than V_{OUT}, the buck controllers operate in 100% duty cycle mode, fully turning on the external PMOS to let regulation occur at a lower dropout than would otherwise be possible.

7.3.2 Enable (Buck Controllers)

The enable pins (EN1 and EN2) for the buck controllers are active high. When the enable pin is driven low and input voltage is present at IN1 or IN2, an on-chip FET is turned on to discharge the soft-start pin SS1 or SS2, respectively. If the soft-start feature is being used, enable should be driven high at least 10µs after V_{IN} is applied to make sure that this discharge cycle occurs.

7.3.3 UVLO (Buck Controllers)

The device has an undervoltage lockout circuit to prevent the turnon of the external PMOS (Q1 or Q2) until a reliable operating voltage is reached on the appropriate regulator (IN1 or IN2). This prevents the buck controllers from misoperation at low input voltages.

7.3.4 Current Limit (Buck Controllers)

An external resistor (R1 or R2) is used to set the current limit for the external PMOS transistor (Q1 or Q2). These resistors are connected between IN1 and IS1 (or IN2 and IS2) to provide a reference voltage across these pins that is proportional to the current flowing through the PMOS transistor. This reference voltage is compared to an internal reference to determine if an overcurrent condition exists. When current limit is exceeded, the external PMOS is turned off for the minimum off-time. Current limit detection is disabled for 10ns any time the PMOS is turned on to avoid triggering on switching noise. In 100% duty cycle mode, current limit is always enabled. Current limit is calculated using the V_{IS1} or V_{IS2} specification in the *Electrical Characteristics* section as shown in Equation 1.

$$I_{LIMIT} = \frac{V_{IS1,2}}{R_{1,2}} \tag{1}$$

The current limit resistor must be appropriately rated for the dissipated power determined by its RMS current calculated by Equation 2.

$$I_{RMS} \approx I_{OUT}\sqrt{D} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}}$$

$$P_{DISS} = (I_{RMS})^2 \times R \tag{2}$$

Feature Description (continued)

For low-cost applications the $I_{S1,2}$ pin can be connected to the drain of the PMOS, using $R_{DS,ON}$ instead of R1 or R2 to set current limit. Variations in the PMOS $R_{DS,ON}$ must be considered to make sure that current limit will protect external components such as the inductor, the diode, and the switch itself from damage as a result of overcurrent.

7.3.5 Short-Circuit Protection (Buck Controllers)

In an overload condition, the current rating of the external components (PMOS, diode, and inductor) can be exceeded. To help guard against this, the TPS75003 device increases its minimum off-time when the voltage at the feedback pin is less than the reference voltage. When the output is shorted (V_{FB} is zero), the minimum off-time is increased to approximately 4μs. The increase in off-time is proportional to the difference between the voltage at the feedback pin and the internal reference.

7.3.6 Soft-Start (Buck Controllers)

The buck controllers each have independent soft-start capability to limit inrush during start-up and to meet timing requirements of the Xilinx Spartan-3 FPGA. Limiting inrush current by using soft-start, or by staggering the turnon of power rails, also guards against voltage drops at the input source due to its output impedance. Refer to the soft-start circuitry shown in Figure 16 and the soft-start timing diagram shown in Figure 17. The BUCK1 controller is discussed in this section; it is identical to BUCK2. Note that pins SS1 and SS2 are very high-impedance and cannot be probed using a typical oscilloscope setup. When input voltage is applied at IN1 and EN1 is driven low, any charge on the SS pin is discharged by an on-chip pulldown transistor. When EN1 is driven high, an on-chip current source starts charging the external soft-start capacitor C_{SS1}. The voltage on the capacitor is compared to the voltage across the current sense resistor R1 to determine if an overcurrent condition exists. If the voltage drop across the sense resistor becomes greater than the reference voltage, then the external PMOS is shut off for the minimum off-time. This implementation provides a cycle-by-cycle current limit and lets the user configure the soft-start time over a wide range for most applications. For detailed information on selecting C_{SS1} and C_{SS2}, see the *Soft-Start Capacitor Selection (Buck Controllers)* section.

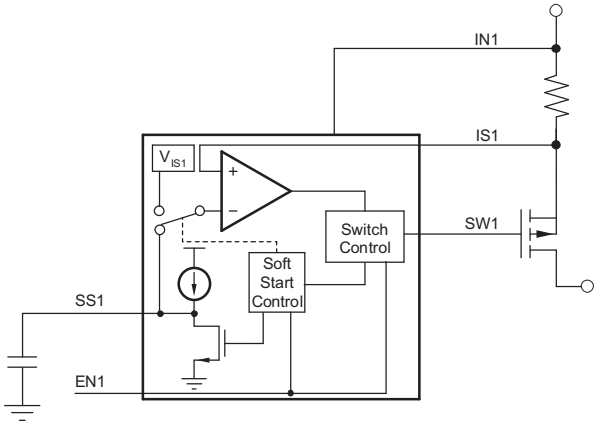


Figure 16. Soft-Start Circuitry

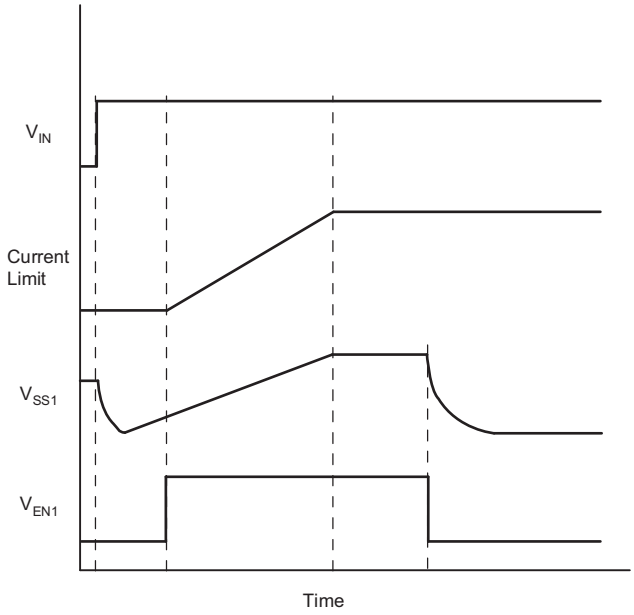


Figure 17. Soft-Start Timing Diagram

7.3.7 LDO Operation

The TPS75003 LDO regulator uses a PMOS pass transistor and is offered in an adjustable version to easily configure any output voltage. When used to power $V_{CC,AUX}$ the LDO regulator output voltage is set to 2.5V; the LDO regulator can optionally be set to other output voltages to power other circuitry. The LDO regulator has integrated soft-start, independent enable, and short-circuit and thermal protection. The LDO regulator can be used to power $V_{CC,AUX}$ on the Xilinx Spartan-3 FPGA when 3.3V JTAG signals are used as described in the *Using 3.3-V Signals for Spartan-3 Configuration and JTAG Ports* application note.

7.3.8 Internal Current Limit (LDO)

The internal current limit of the LDO regulator helps protect the regulator during fault conditions. When an overcurrent condition is detected, the output voltage is decreased until the current falls to a level that will not damage the device. For good device reliability, the LDO regulator should not operate at the current limit.

7.3.9 Enable Pin (LDO)

The active high enable pin (EN3) can be used to put the device into shutdown mode. If shutdown and soft-start capability are not required, EN3 can be tied to IN3.

7.3.10 Dropout Voltage (LDO)

The LDO regulator uses a PMOS transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the pass transistor is in its linear region of operation, and the input-output resistance is the $R_{DS,ON}$ of the pass transistor. In this region, the LDO regulator is said to be out of regulation; ripple rejection, line regulation, and load regulation degrade as (V_{IN} – V_{OUT}) decreases to much lower than 0.5V.

7.3.11 Transient Response (LDO)

The LDO regulator does not have an on-chip pulldown circuit for output is overvoltage conditions. This feature lets the device be used in applications that connect higher voltage sources such as an alternate power supply to the output. This design also results in an output overshoot of several percent if the load current quickly drops to zero. The amplitude of overshoot can be reduced by increasing C_{OUT}; the duration of overshoot can be decreased by adding a load resistor.

7.3.12 Thermal Protection (LDO)

Thermal protection disables the output when the junction temperature, T_J, reaches unsafe levels. When the junction temperature cools, the output is enabled again. The thermal protection circuit may cycle on and off depending on the power dissipation, thermal resistance, and ambient temperature. This cycling limits the dissipation of the regulator, protecting it from damage. For good long term reliability, the device should not be continuously operated at or near thermal shutdown.

7.3.13 Power Dissipation (LDO)

The TPS75003 device is available in a QFN-style package with an exposed lead frame on the package underside. The exposed lead frame is the primary path for removing heat and should be soldered to a PC board that is configured to remove the amount of power dissipated by the LDO regulator, as calculated by Equation 3.

$$P_D = (V_{IN3} - V_{OUT3}) \times I_{OUT3} \tag{3}$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to ensure the required output voltage. The two buck converters do not contribute a significant amount of dissipated power. Using heavier copper will increase the overall effectiveness of removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heatsink effectiveness.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS75003 is an integrated power management IC designed specifically to power DSPs and FPGAs such as the Xilinx Spartan-3, Spartan-3E and Spartan-3L. Two non-synchronous buck controllers can be configured to supply up to 3A for both CORE and I/O rails. A low dropout linear regulator powers auxiliary rails up to 300mA. All channels have independent enable and soft-start, allowing control of inrush current and output voltage ramp time as required by the application.

Table 1 through Table 4 show component values that have been tested for use with up to 3A load currents. Inductors in Table 1 are tested up to the respective saturation currents. Other similar external components can be substituted as desired; however, in all cases the circuits that are used should be tested for compliance to application requirements.

Table 1. Inductors Tested with the TPS75003

PART NUMBER	MANUFACTURER	INDUCTANCE	DC RESISTANCE	SATURATION CURRENT
SLF7032T−100M1R4	TDK	10μH ±20%	53mΩ ±20%	1.4A
SLF6025−150MR88	TDK	15μH ±20%	85mΩ ±20%	0.88A
CDRH6D28−5R0	Sumida	5μH	23mΩ	2.4A
CDRH6D38-5R0	Sumida	5μH	18mΩ	2.9A
CDRH103R−100	Sumida	10μH	45mΩ	2.4A
CDRH4D28−100	Sumida	10μH	96mΩ	1.0A
CDRH8D43-150	Sumida	15μH	42mΩ	2.9A
CDRH5D18−6R2	Sumida	6.2μH	71mΩ	1.4A
DO3316P−472	Coilcraft	4.7μH	18mΩ	5.4A
MSS7341-153	Coilcraft	15μH	55mΩ	1.6A
MSS7341-223	Coilcraft	22μH	82mΩ	1.26A
744052006	Wurth	6.2μH	80mΩ	1.45A
74451115	Wurth	15μH	90mΩ	0.8A

Table 2. PMOS Transistors Tested with the TPS75003

PART NUMBER	MANUFACTURER	$R_{DS,ON}$ (TYP)	V_{DS}	I_D	PACKAGE
SI5457DC-T1-GE3	Vishay	0.056Ω at VGS = –2.5V	–20V	–6A at +25°C	1206-8
SI2301BDS-T1-E3	Vishay	0.15Ω at VGS = –2.5V	–20V	–2.0A at +25°C	SOT-23
SI2323DS-T1-E3	Vishay	0.052Ω at VGS = –2.5V	–20V	–4.1A at +25°C	SOT-23
FDG328P	Fairchild	0.12Ω at VGS = –2.5V	–20V	–1.5A	SC70-6

Table 3. Diodes Tested with the TPS75003

PART NUMBER	MANUFACTURER	V_R	I_F	PACKAGE
FSV240AF	ON Semiconductor / Fairchild	40V	2.0A	DO-214-2
FSV340FP	ON Semiconductor / Fairchild	40V	3.0A	SOD-123-2
SS32	ON Semiconductor / Fairchild	20V	3.0A	DO-214AB
ZHCS2000TA	Zetex	40V	2.0A	SOT-23−6
B320AE-13	Diodes Inc.	20V	3.0A	SMA

Table 4. Capacitors Tested with the TPS75003

PART NUMBER	MANUFACTURER	CAPACITANCE	ESR	VOLTAGE RATING
10TPB47M (PosCap)	Panasonic	47µF	0.07Ω	10V
T491D476M010AT	Kemet	47µF	0.8Ω	10V
T495D476K016ATE180	Kemet	47µF	0.18Ω	16V
TR3C476K016C0300	Vishay	47µF	0.3Ω	16V
T495D107M006ATE050	Kemet	100µF	0.05Ω	6.3V
TPSC107M006R0075	AVX	100µF	0.075Ω	6.3V
6TPE100MPB (PosCap)	Panasonic	100µF	0.025Ω	6.3V
TR3C107K6R3C0125	Vishay	100µF	0.25Ω	6.3V

8.2 Typical Application

Figure 18 shows a typical application circuit for powering the Xilinx Spartan-3 FPGA.

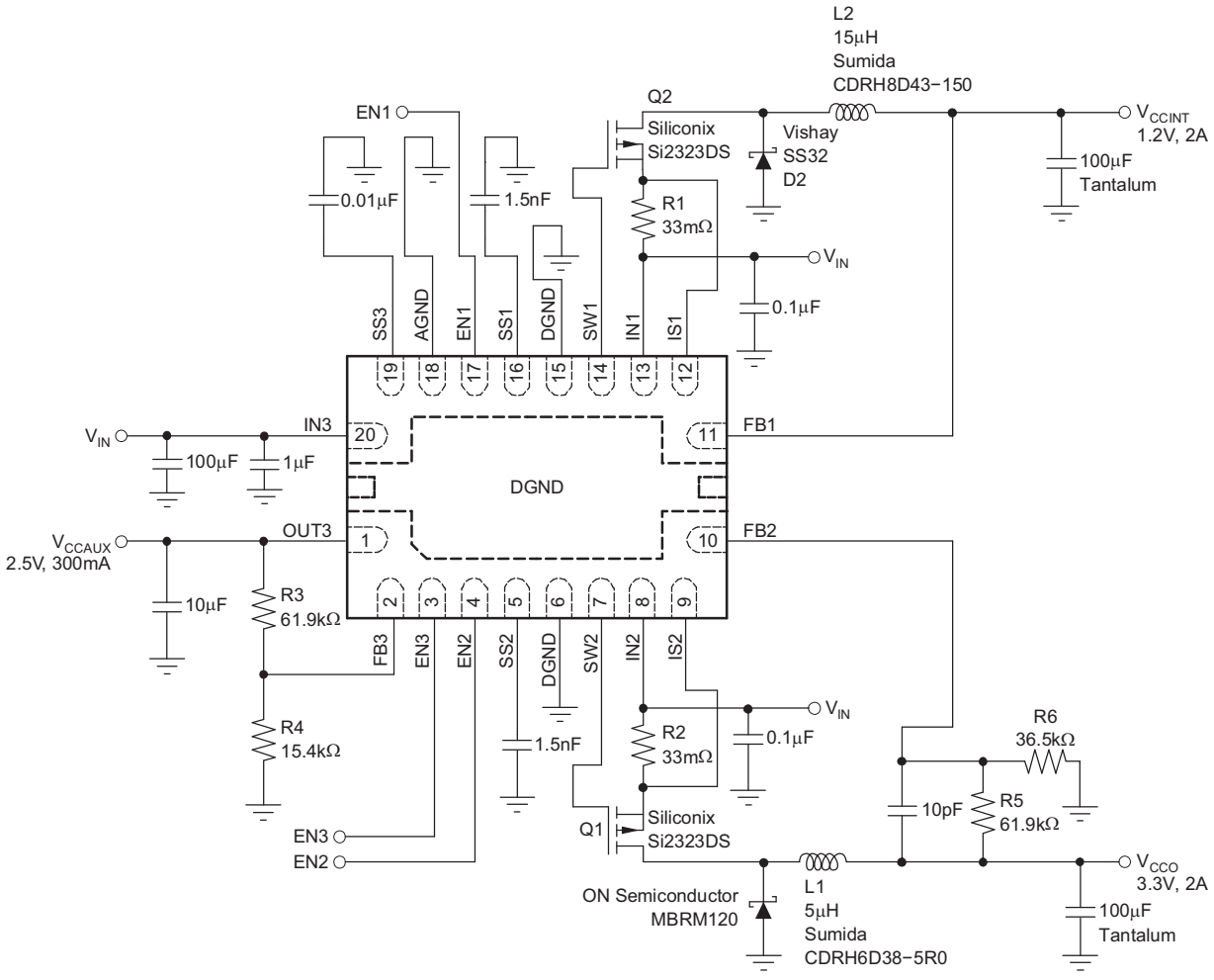


Figure 18. Typical Application Circuit for Powering the Xilinx Spartan-3 FPGA

Typical Application (continued)

8.2.1 Design Requirements

Table 5 lists the design requirements that are met by the application shown in Figure 18

Table 5. Design Parameters for Xilinx Spartan-3 FPGA Design

PARAMETER	DESCRIPTION	VALUE	UNIT
V_{IN}	Input power supply to all regulators: BUCK1 (IN1), BUCK2 (IN2), and LDO (IN3)	3.3 to 6.5	V
V_{OUT1}	Output of BUCK1 regulator V_{CCINT}, core rail power for the FPGA	1.2	V
I_{OUT1}	Load current of FPGA for V_{CCINT} rail	2	A
V_{OUT2}	Output of BUCK2 regulator V_{CCO}, I/O rail power for the FPGA	3.3	V
I_{OUT2}	Load current of FPGA for V_{CCO} rail	2	A
V_{OUT3}	Output of LDO regulator V_{CCAUX}, auxiliary rail power for the FPGA	2.5	V
I_{OUT3}	Load current of FPGA for V_{CCAUX} rail	300	mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor C_{IN1}, C_{IN2} Selection (Buck Controllers)

It is good analog design practice to place input capacitors near the inputs of the device in order to ensure a low impedance input supply. 10µF to 22µF of capacitance for each buck converter is adequate for most applications, and should be placed within 100mils (0.01in, or 2.54mm) of the IN1 and IN2 pins to minimize the effects of pulsed current switching noise on the soft-start circuitry during the first ~1V of output voltage ramp. Low ESR capacitors also help to minimize noise on the supply line. The minimum value of capacitance can be estimated using Equation 4:

$$C_{IN,\ MIN} + \frac{(1/2)L \times (\Delta I_L)^2}{V_{(RIPPLE)} \times V_{IN}} \approx \frac{(1/2)L \times (0.3 \times I_{OUT})^2}{V_{(RIPPLE)} \times V_{IN}} \tag{4}$$

Note that the capacitors must be able to handle the RMS current in continuous conduction mode, which can be calculated using Equation 5:

$$I_{C,IN(RMS)} \approx I_{OUT} \sqrt{\left(\frac{V_{OUT}}{V_{IN,MIN}} \right)} \tag{5}$$

8.2.2.2 Inductor Value Selection (Buck Controllers)

The inductor is chosen based on inductance value and maximum current rating. Larger inductors reduce current ripple (and therefore, output voltage ripple) but are physically larger and more expensive. Inductors with lower DC resistance typically improve efficiency, but also have higher cost and larger physical size. The buck converters work well with inductor values between 4.7µH and 47µH in most applications. When selecting an inductor, the current rating should exceed the current limit set by R_{IS} or $R_{DS,ON}$ (see the *Current Limit (Buck Controllers)* section). To determine the minimum inductor size, first determine if the device will operate in minimum on-time or minimum off-time mode. The device will operate in minimum on-time mode if Equation 6 is satisfied:

$$V_{IN} - V_{OUT} - I_{OUT} \times R_{DS,ON} - R_L \times I_{OUT} \geq \frac{t_{OFF,MIN} \times (V_{OUT} + V_{SCHOTTKY} + R_L \times I_{OUT})}{t_{ON,MIN}} \tag{6}$$

where

- R_L = the inductor DC resistance

Minimum inductor size needed when operating in minimum on-time mode is given by Equation 7:

$$L_{MIN} = \frac{\left(V_{IN} - V_{OUT} - I_{OUT} \times R_{DS,ON} - R_L \times I_{OUT}\right) \times t_{ON,}MIN}{\Delta I_L} \quad (7)$$

Minimum inductor size needed when operating in minimum off-time mode is given by Equation 8:

$$L_{MIN} = \frac{\left(V_{OUT} + V_{SCHOTTKY} + R_L \times I_{OUT}\right) \times t_{OFF,}MIN}{\Delta I_L}$$

where

- ΔI_L = (20%–30%) × $I_{OUT\text{-}MAX}$ (8)

8.2.2.3 External PMOS Transistor Selection (Buck Controllers)

The external PMOS transistor is selected based on threshold voltage (V_T), on-resistance ($R_{DS,ON}$), gate capacitance (C_G) and voltage rating. The PMOS V_T magnitude must be much lower than the lowest voltage at IN1 or IN2 that will be used. A V_T magnitude that is 0.5V less than the lowest input voltage is normally sufficient. The PMOS gate will see voltages from 0V to the maximum input voltage, so gate-to-source breakdown should be a few volts higher than the maximum input supply. The drain-to-source of the device will also see this full voltage swing, and should therefore be a few volts higher than the maximum input supply. The RMS current in the PMOS can be estimated by using Equation 9:

$$I_{PMOS(RMS)} \approx I_{OUT}\sqrt{D} = I_{OUT}\sqrt{\frac{V_{OUT}}{V_{IN}}} \quad (9)$$

The power dissipated in the PMOS is comprised of both conduction and switching losses. Switching losses are typically insignificant. The conduction losses are a function of the RMS current and the $R_{DS,ON}$ of the PMOS, and are calculated by Equation 10:

$$P_{(cond)} = \left(I_{OUT}\sqrt{D}\right)^2 \times R_{DS,ON} \times \left(1 + TC \times \left[T_J - 25°C\right]\right) \approx \left(I_{OUT}\sqrt{D}\right) \times R_{DS,ON} \quad (10)$$

8.2.2.4 Diode Selection (Buck Controllers)

The diode is off when the PMOS is on, and on when the PMOS is off. Since it will be turned on and off at a relatively high frequency, a Schottky diode is recommended for good performance. The peak current rating of the diode should exceed the peak current limit set by the sense resistor $R_{IS1,2}$. A diode with low reverse leakage current and low forward voltage at operating current will optimize efficiency. Equation 11 calculates the estimated average power dissipation:

$$I_{(diode)(RMS)} \approx I_{OUT}\left(1 - D\right) = I_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (11)$$

8.2.2.5 Output Capacitor Selection (Buck Controllers)

The output capacitor is selected based on output voltage ripple and transient response requirements. As a result of the nature of the hysteretic control loop, a minimum ESR of a few tens of mΩ should be maintained for good operation unless a feed-forward resistor is used. Low ESR bulk tantalum or PosCap capacitors work best in most applications. A 1.0μF ceramic capacitor can be used in parallel with this capacitor to filter higher frequency spikes. The output voltage ripple can be estimated by Equation 12:

$$\Delta V_{PP} = \Delta I \times \left[ESR + \left(\frac{1}{8 \times C_{OUT} \times f}\right)\right] \approx 1.1\Delta I \times ESR \quad (12)$$

To calculate the capacitance needed to achieve a given voltage ripple as a result of a load transient from zero output to full current, use Equation 13:

$$C_{OUT} = \frac{L \times \Delta I_{OUT}{}^2}{\left(V_{IN} - V_{OUT}\right) \times \Delta V} \quad (13)$$

If only ceramic or other very low ESR output capacitor configurations are desired, additional voltage ripple must be passed to the feedback pin. For detailed application information, refer to the *Using Ceramic Output Capacitors with the TPS6420x and TPS75003 Buck Controllers* application report.

8.2.2.6 Output Voltage Ripple Effect on V_{OUT} (Buck Controllers)

Output voltage ripple causes V_{OUT} to be higher or lower than the target value by half of the peak-to-peak voltage ripple. For minimum on-time, the ripple adds to the voltage; for minimum off-time, it subtracts from the voltage.

8.2.2.7 Soft-Start Capacitor Selection (Buck Controllers)

The soft-start for BUCK1 and BUCK2 is not intended to be a precision function. However, the startup time (from a positive transition on Enable to V_{OUT} reaching its final value) has a linear relationship to C_{SS} up to approximately 800pF, which results in a startup time of approximately 4ms. Above this value of C_{SS}, the variation in start-up time increases rapidly. This variation can occur from unit to unit and even between the two BUCK controllers in one device. Therefore, do not depend on the soft-start feature for sequencing multiple supplies if values of C_{SS} greater than 800pF are used.

BUCK1 is discussed in this section; it is identical to BUCK2. Soft-start is implemented on the buck controllers by ramping current limit from 0 to its target value (set by R1) over a user-defined time. This time is set by the external soft-start cap connected to pin SS1. If SS1 is left open, a small on-chip capacitor will provide a current limit ramp time of approximately 250µs. Figure 19 shows the effects of R1 and SS1 on the current limit start-up ramp.

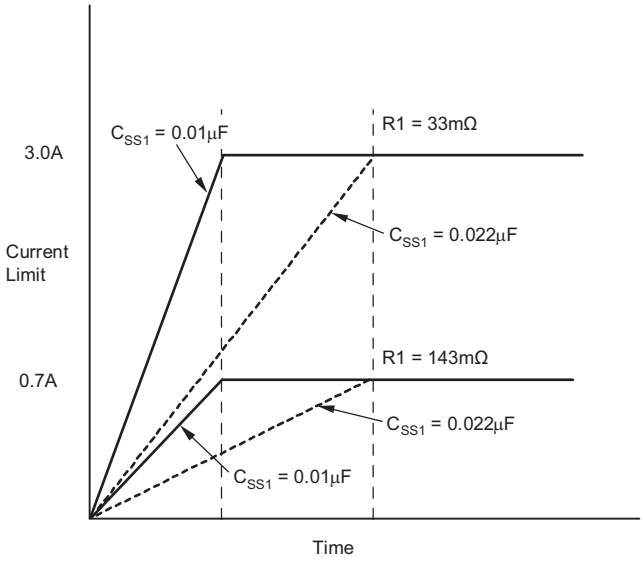


Figure 19. Effects of C_{SS1} and R_1 on Current Ramp Limit

This soft-start current limit ramp can be used to provide inrush current control or output voltage ramp control. While the current limit ramp can be easily understood by looking at Figure 19, the output voltage ramp is a complex function of many variables. The dominant variables in this process are V_{OUT1}, C_{SS1}, I_{OUT1}, and R_1. Less important variables are V_{IN1} and L_1.

The best way to set a target start-up time is through bench measurement under target conditions, adjusting C_{SS1} to get the desired startup profile. To stay above a minimum start-up time, set the nominal start-up time to approximately five times the minimum. To stay below a maximum time, set the nominal start-up time at one-fifth of the maximum. Fastest start-up times occur at maximum V_{IN1}, with minimum V_{OUT1}, L_1, C_{OUT1}, C_{SS1}, and I_{OUT1}. Slowest start-up times occur under opposite conditions.

Refer to Figure 21 to Figure 25 for characterization curves showing how the start-up profile is affected by these critical parameters.

8.2.2.8 Output Voltage Setting Selection (Buck Controllers)

Output voltage is set using two resistors as shown for Buck2 in Figure 18. Output voltage is then calculated using Equation 14:

$$V_{OUT} = V_{FB}\left(\frac{R5}{R6}+1\right) \quad (14)$$

where

- V_{FB} = 1.22V

8.2.2.9 Input Capacitor Selection (LDO)

Although an input capacitor is not required, it is good analog design practice to connect a 0.1μF to 10μF low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, stability, and ripple rejection. A higher value capacitor may be needed if large, fast rise-time load transients are anticipated, or if the device is located far from its power source.

8.2.2.10 Output Capacitor Selection (LDO)

A 2.2μF or greater capacitor is required near the output of the device to ensure stability. The LDO is stable with any capacitor type, including ceramic. If improved transient response or ripple rejection is required, larger and/or lower ESR output capacitors can be used.

8.2.2.11 Soft-Start Capacitor Selection (LDO)

The LDO uses an external soft-start capacitor, C_{SS3}, to provide an RC-ramped reference voltage to the control loop. See the *Functional Block Diagram*. This is a voltage-controlled soft-start, as compared to the current-controlled soft-start used by the buck controllers. The start-up waveform can be approximated by Equation 15:

$$V_{OUT}(t) = V_{OUT,SET}\left(1 - e^{-\frac{t}{RC}}\right) \quad (15)$$

where

- $R = 480 \times 10^3$
- C = capacitance in μF from SS3 to GND

The time taken to reach 90% of final V_{OUT} can be approximated by Equation 16:

$$T_{90\%} = 2.3 \times \left(480 \times 10^3\right) C_{SS3}\ (\mu F) \quad (16)$$

8.2.2.12 Setting Output Voltage (LDO)

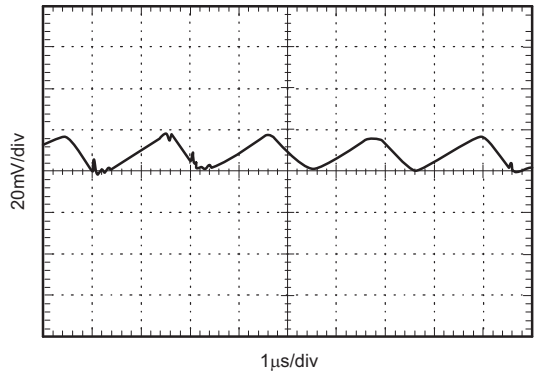
Output voltage is set using two resistors as shown in Figure 18. Output voltage is then calculated using Equation 17:

$$V_{OUT} = V_{FB}\left(\frac{R3}{R4}+1\right) \quad (17)$$

where

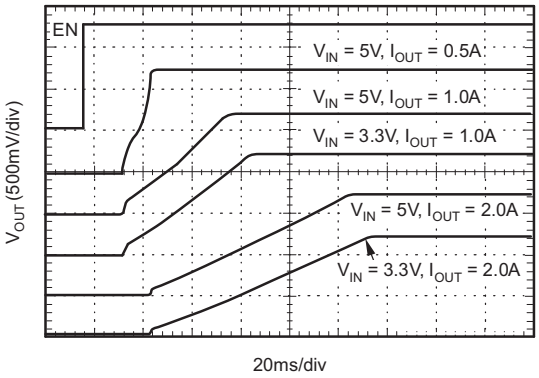
- V_{FB} = 0.507V

8.2.3 Application Curves



V_{IN} = 5 V V_{OUT} = 3.3 V I_{OUT} = 2 A

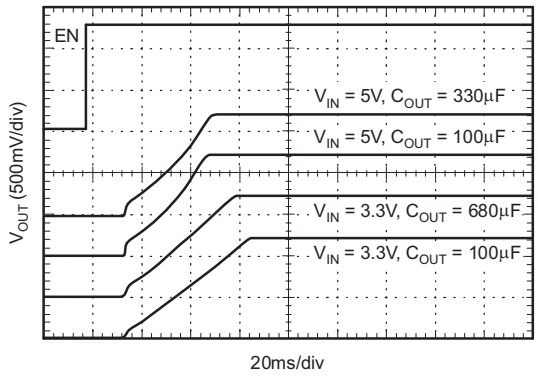
Figure 20. Buck Output Voltage Ripple



See the ***Soft-Start Capacitor Selection (Buck Controllers)*** section.

V_{OUT} = 1.2 V C_{SS} = 0.01 µF

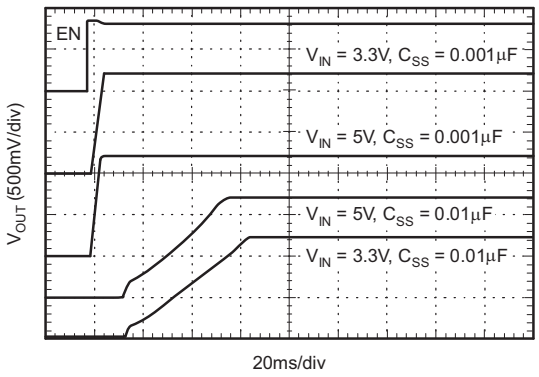
Figure 21. Buck Start-Up vs V_{IN} and I_{OUT}



See the ***Soft-Start Capacitor Selection (Buck Controllers)*** section.

V_{OUT} = 1.2 V C_{SS} = 0.01 µF

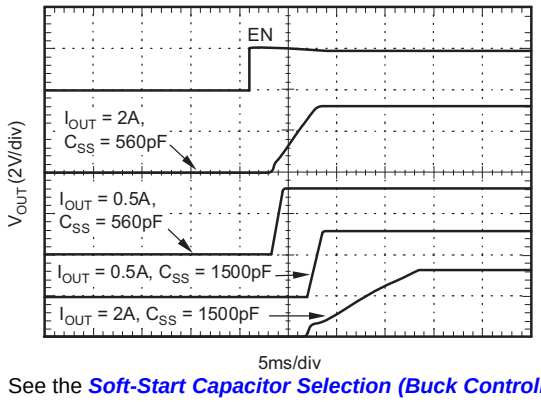
Figure 22. Buck Start-Up vs V_{IN} and C_{OUT}



See the ***Soft-Start Capacitor Selection (Buck Controllers)*** section.

V_{OUT} = 1.2 V I_{OUT} = 1 A

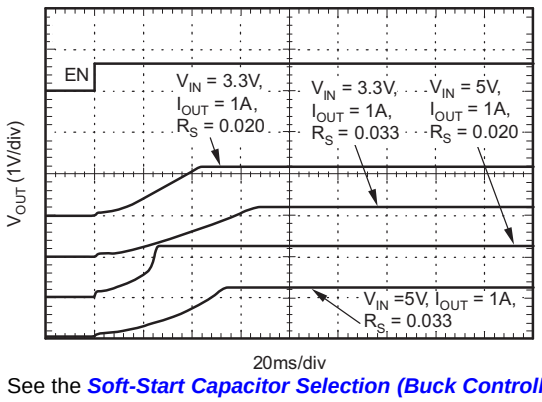
Figure 23. Buck Start-Up vs V_{IN} and C_{SS}



See the ***Soft-Start Capacitor Selection (Buck Controllers)*** section.

V_{IN} = 5 V V_{OUT} = 3.3 V

Figure 24. Buck Start-Up vs I_{OUT} and C_{SS}



See the ***Soft-Start Capacitor Selection (Buck Controllers)*** section.

V_{OUT} = 1.2 V C_{SS} = 0.01 µF

Figure 25. Buck Start-Up vs V_{IN} and R_{SENSE}

9 Power Supply Recommendations

There are three separate blocks internal to the TPS75003 device: two identical buck controllers and one integrated LDO regulator. The input voltage, V_{INX}, to the IN1 and IN2 pins must be within the range specified in the *Electrical Characteristics* and must be greater than the nominal output voltage of BUCK1 or BUCK2, respectively. However, the maximum output voltages, V_{OUT1} and V_{OUT2}, are determined by external component selection and cannot be specified. The input voltage to the LDO regulator, V_{IN3}, must be greater than the drop-out voltage (V_{DO}) added to V_{OUT3} or an absolute value of 2.2 V, whichever is greater. The power supply into the IN1, IN2, and IN3 pins do not need to be equal to each other but all of the design values must adhere to the minimum and maximum specifications of the TPS75003 and external components. Other considerations are based on the relationship of pins used inside the TPS75003 device.

The power supply into IN1 is used as the power supply to drive the gate of the switch connected at SW1. The difference between the voltages at the IN1 pin and IS1 pin is the input to the sensing which controls current limit. The power supply connected at IN1 must be the power supply connected to 33-mΩ sense resistor, and the opposite terminal of the sense resistor must connect directly to IS1 and the source pin(s) of the eternal PMOS FET.

Similarly, the power supply into IN2 is used as the power supply to drive the gate of the switch connected at SW2. The difference between the voltages at the IN2 pin and IS2 pin is the input to the sensing which controls current limit. The power supply connected at IN2 must be the power supply connected to 33-mΩ sense resistor, and the opposite terminal of the sense resistor must connect directly to IS2 and the source pins of the eternal PMOS FET.

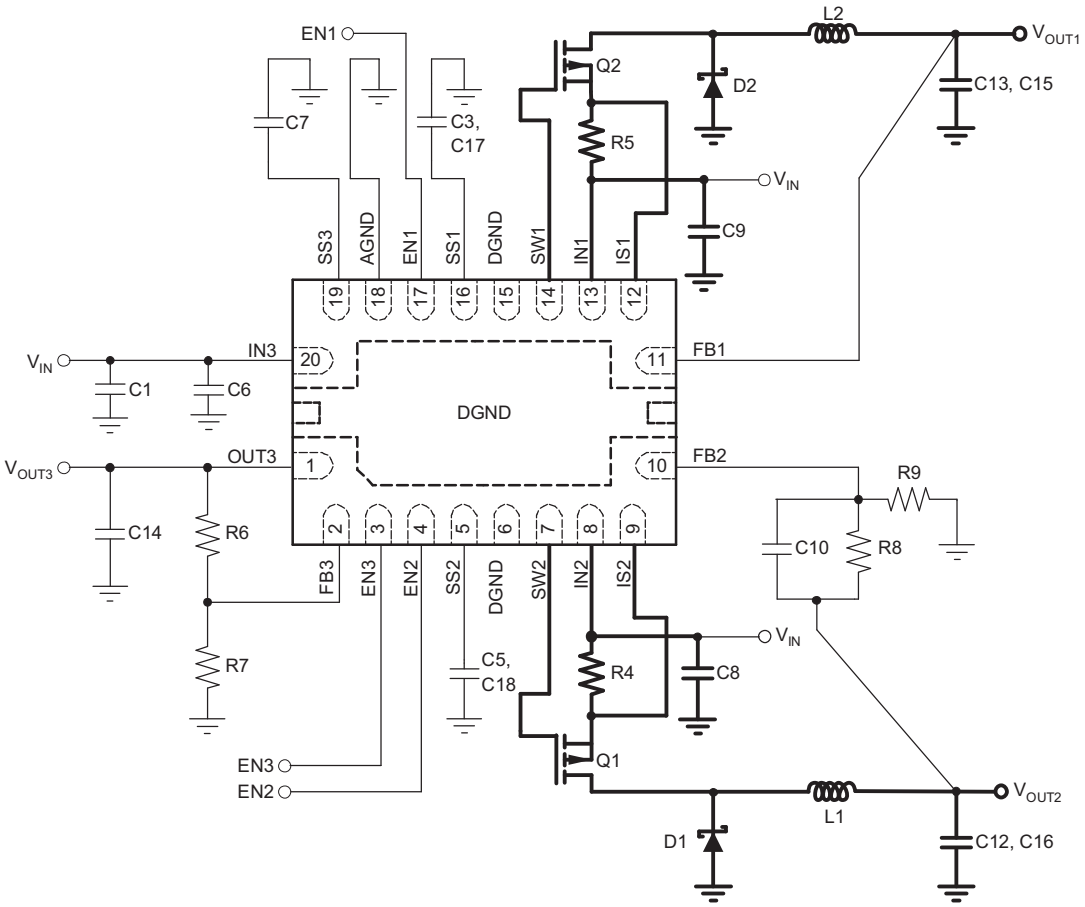
The power supply into IN3 is used as the power supply to the LDO regulator and all internal support circuitry. Unlike the BUCK1 and BUCK2 controllers, the power does not bypass the TPS75003 device. Therefore, the output of the LDO is named OUT3 and up to 300-mA of current will go directly from IN3 to OUT3.

10 Layout

10.1 Layout Guidelines

10.1.1 PCB Layout Considerations

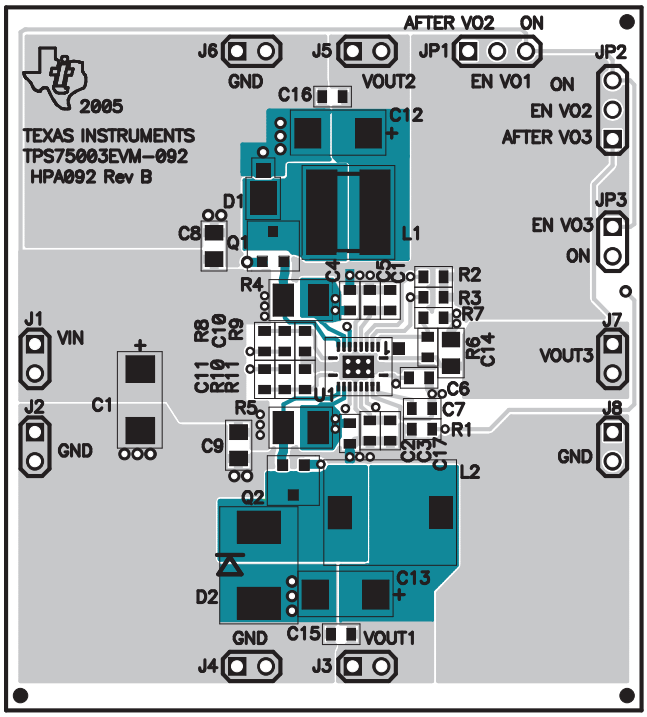
As with any switching regulators, careful attention must be paid to board layout. A typical application circuit and corresponding recommended printed circuit board (PCB) layout with emphasis on the most sensitive areas are shown in Figure 26 through Figure 28.



Note: Most sensitive areas are highlighted by bold lines.

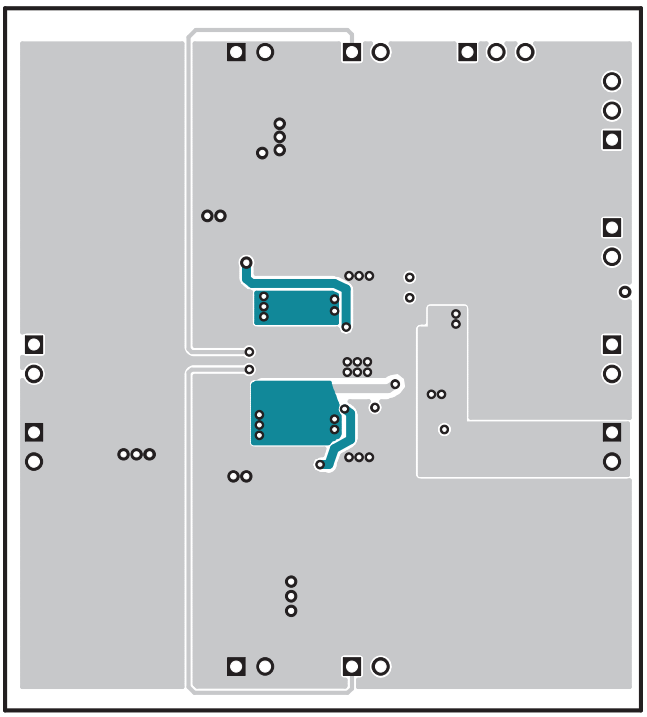
Figure 26. Typical Application Circuit

10.2 Layout Example



Most sensitive areas are highlighted in green.

Figure 27. Recommended PCB Layout, Component Side, Top View



Most sensitive areas are highlighted in green.

Figure 28. Recommended PCB Layout, Bottom Side, Top View

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.1.2 开发支持

有关开发支持，请参阅：

- TPS75003 的设计电子表格
- TPS75003：适用于 TPS75003 的 Gerber 软件

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《TPS75003EVM 用户指南》*
- 德州仪器 (TI)，*《为 Spartan-3 配置和 JTAG 端口使用 3.3V 信号》应用手册*
- 德州仪器 (TI)，*《将陶瓷输出电容器与 TPS6420x 和 TPS75003 降压控制器配合使用》应用手册*

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.5 商标

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Spartan is a trademark of Xilinx, Inc.
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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS75003RHLR	ACTIVE	VQFN	RHL	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	75003	Samples
TPS75003RHLRG4	ACTIVE	VQFN	RHL	20	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	75003	Samples
TPS75003RHLT	ACTIVE	VQFN	RHL	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	75003	Samples
TPS75003RHLTG4	ACTIVE	VQFN	RHL	20	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	75003	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

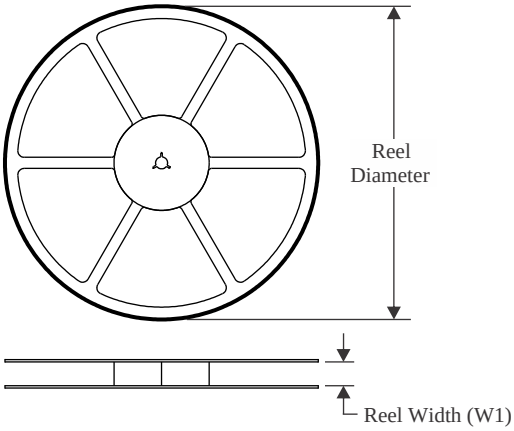
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

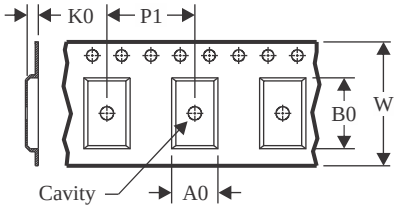
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

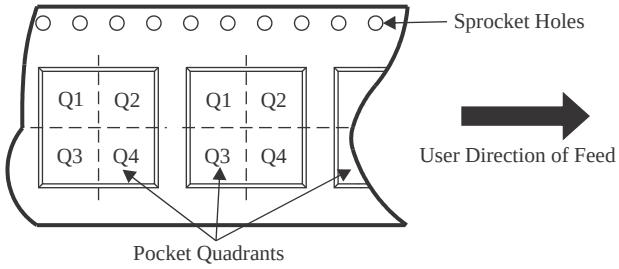


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

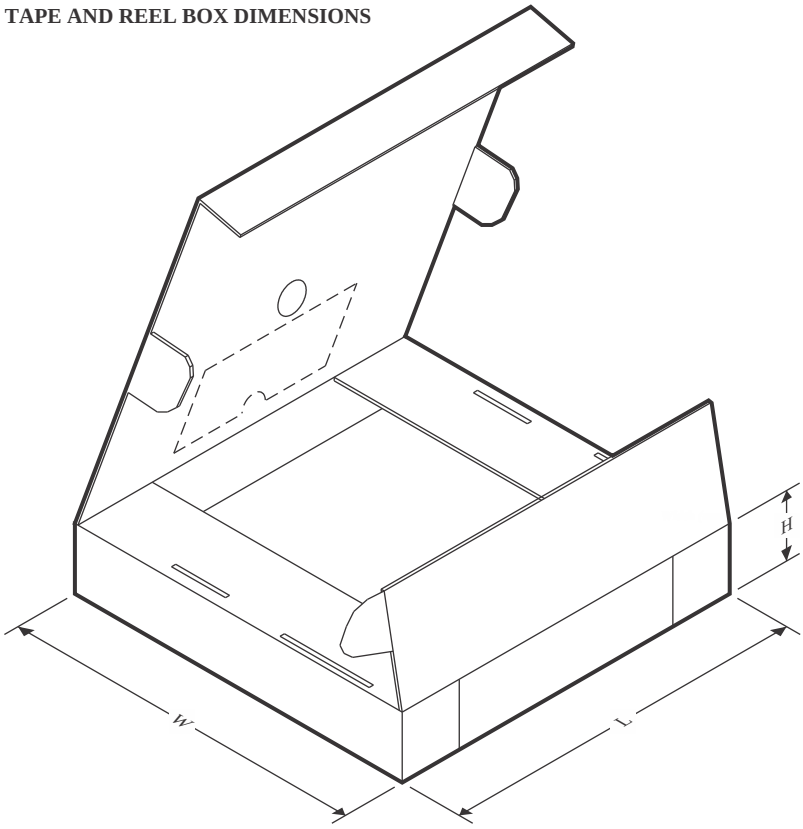
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS75003RHLR	VQFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
TPS75003RHLT	VQFN	RHL	20	250	180.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

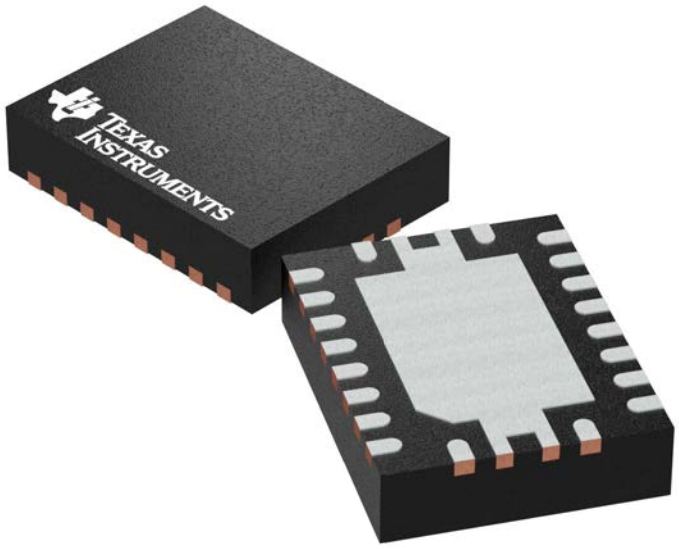
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS75003RHLR	VQFN	RHL	20	3000	356.0	356.0	35.0
TPS75003RHLT	VQFN	RHL	20	250	210.0	185.0	35.0

RHL 20

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

3.5 x 4.5 mm, 0.5 mm pitch



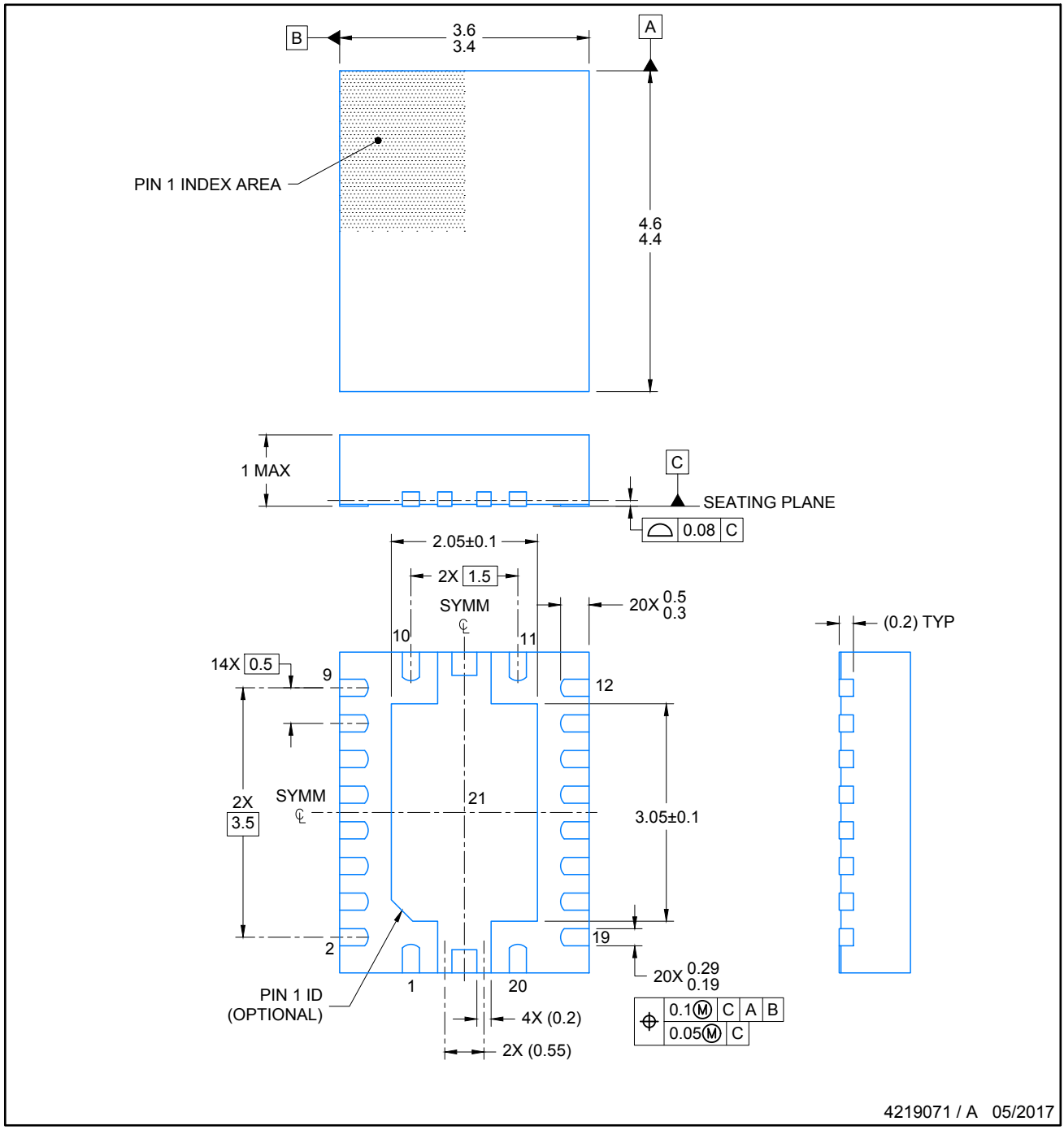
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RHL0020A

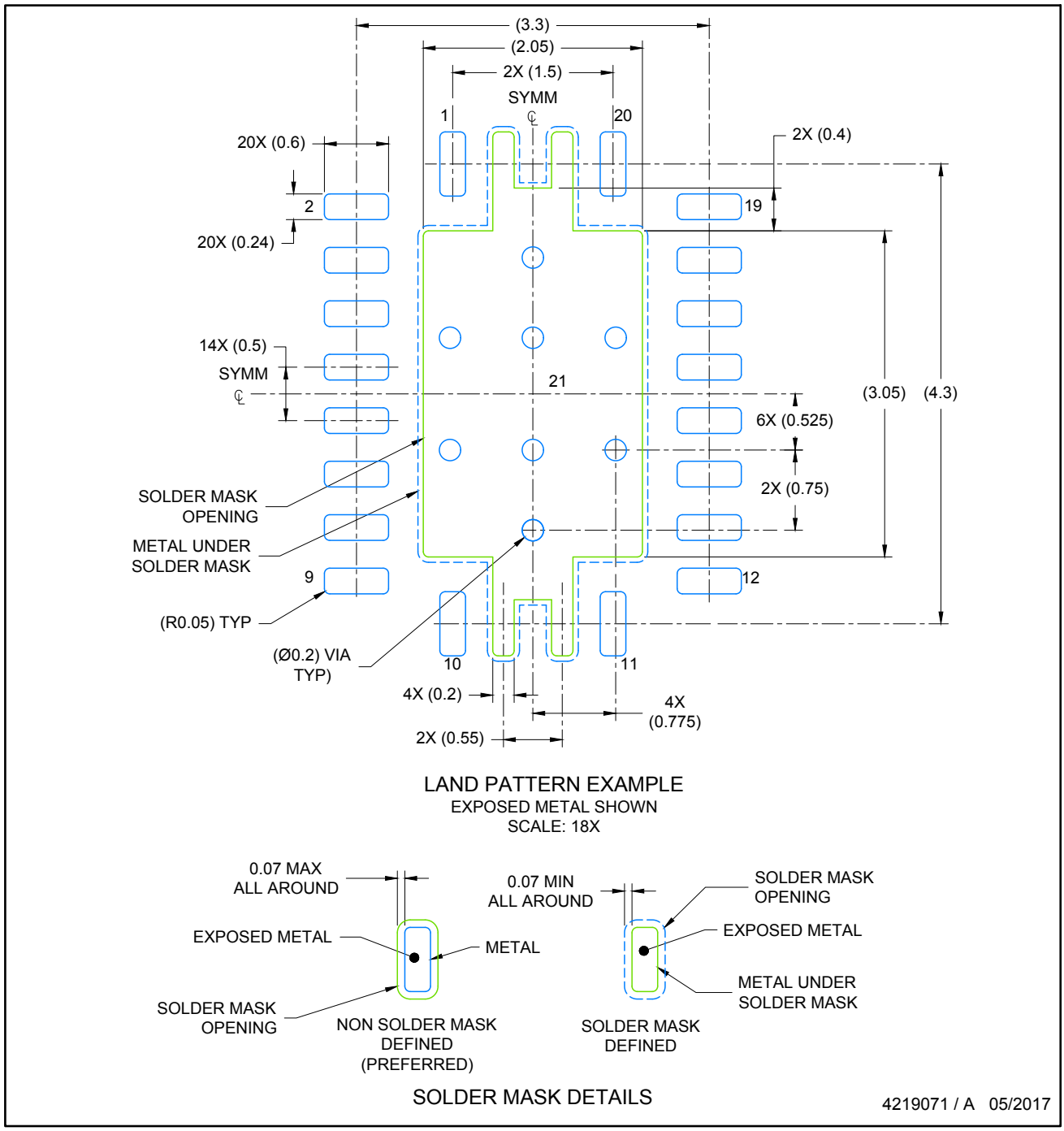
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

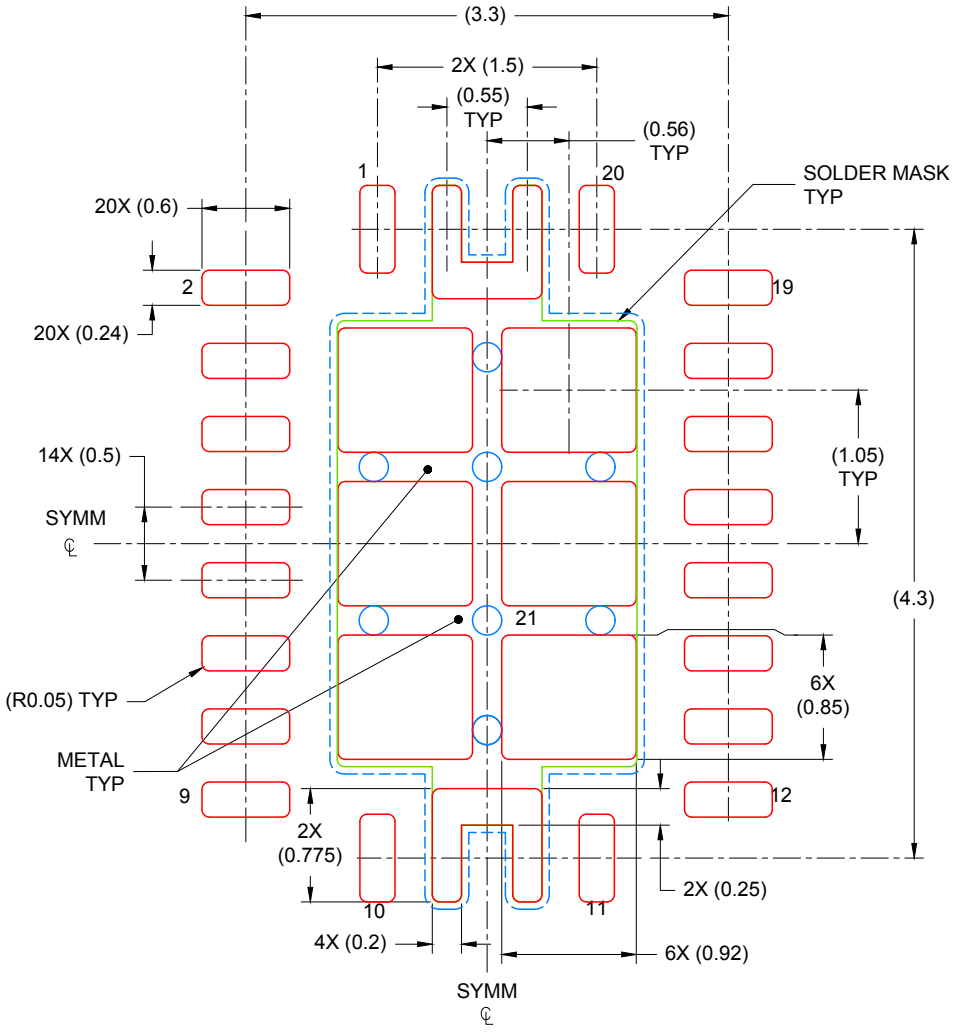


NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to theri locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL

EXPOSED PAD
75% PRINTED COVERAGE BY AREA
SCALE: 20X

4219071 / A 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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