LP3905 Power Management Unit For Low Power Handheld Applications

Check for Samples: LP3905

FEATURES

- **Two Buck Regulators for Powering High Current Processor Functions or Peripheral Devices**
- **Two Linear Regulators for Powering Internal Processor Functions and I/Os**
- **One Enable Pin for Buck1 and Linear Regulators 1 and 2**
- **Separate Enable Pin for Buck2**
- **Thermal and Current Overload Protection**
- **Small 14–Pin WSON Package (4x4mmx0.8mm)**

APPLICATIONS

- **Baseband Processors**
- **Peripheral Processor (Video, Audio)**
- **I/O Power**
- **FPGA Power**

DESCRIPTION

LP3905 is a multi-functional Power Management Unit, optimized for low power handheld applications. This device integrates two 600mA DC-DC buck regulators and two 150mA linear regulators. Fixed and adjustable buck output versions are available. The LP3905 additionally features two enable pins for the device output control and is offered in an WSON package.

KEY SPECIFICATIONS

Buck Regulators

- **Fixed and Adjustable Voltage Options, Range 1.0V to 3.3V(1)**
- **Up to 90% Efficiency**
- **Auto-Switching PFM-PWM Mode and Fixed PWM Mode**
- **2MHz PWM Fixed Switching Frequency (Typ)**
- **600mA Output Current**
- **±4% Output Voltage Accuracy Over Temp**
- **Internal SoftStart**
- **2.2µH Inductor, 10µF Input and Output Caps**

Linear Regulators

- **Output Options in the Range 1.5V to 3.3V(1)**
- **13.5µV_{rms} Output Voltage Noise**
- **PSRR - 70dB @ 1kHz**
- **±3% Output Voltage Accuracy Over Full Line and Load Regulation**
- **0mA to 150mA Output Current**
- **C_{in} = 1.0µF, C_{out} = 0.47µF for 100mA O/P**
- **C_{in} = 1.0µF, C_{out} = 1.0µF for 150mA O/P**
- **80mV Dropout Voltage**

(1) Fixed output voltage devices can be customized to fit system requirements. Please contact Texas Instruments Sales Office.

Typical Application Circuit

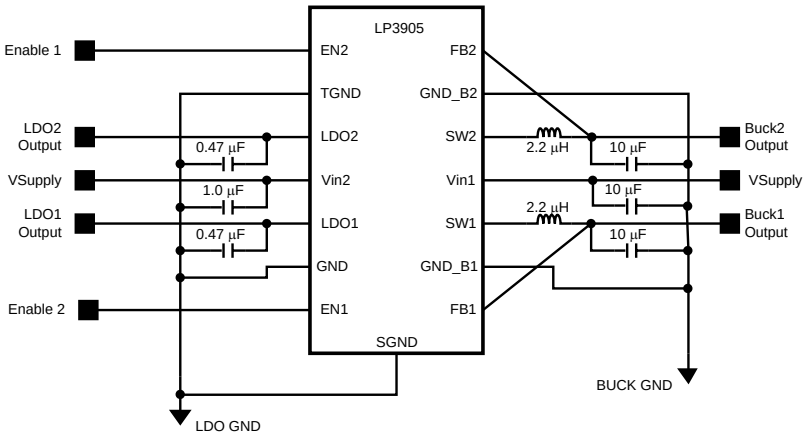

Figure 1. Typical Application Circuit – 14-Pin WSON Package

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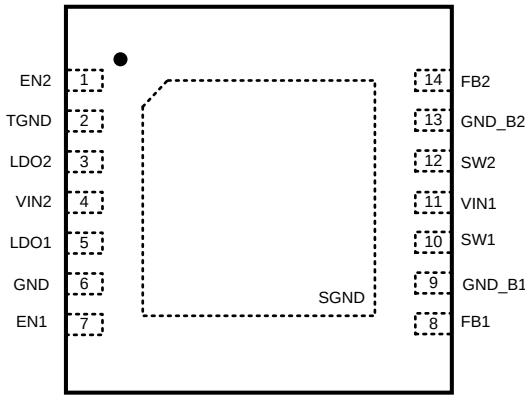


Figure 2. Connection Diagram
14-Pin WSON Package
See Package Number NHL0014B

Block Diagram

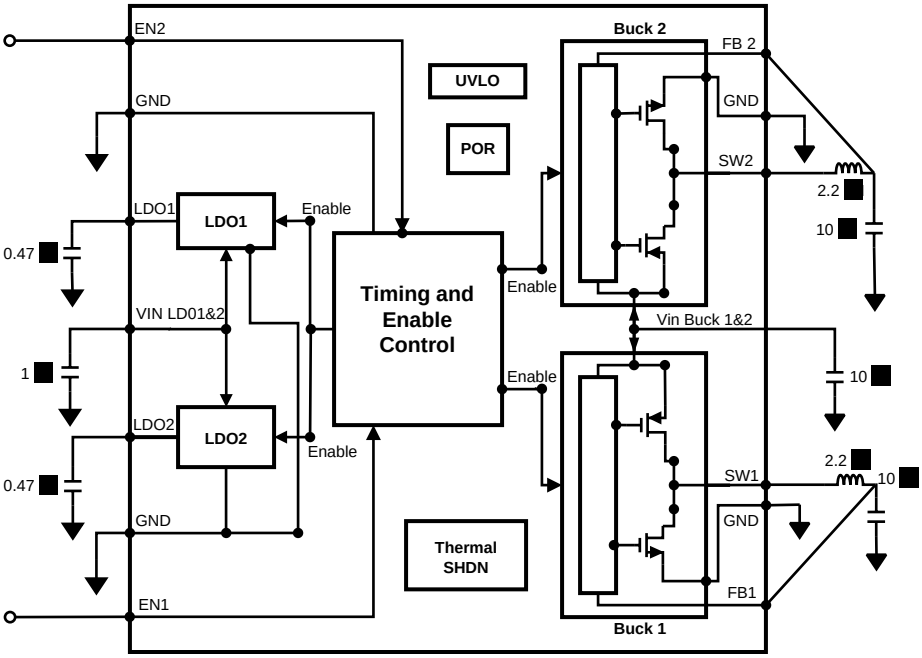


Figure 3. Simplified Functional Diagram

PIN DESCRIPTIONS

Pin No.	Name	Description
1	EN2	Enable Pin for Buck2
2	TGND	Ground Pin
3	LDO2	LDO2 Output Pin
4	VIN2	Input Power Terminal to LDO1 and 2
5	LDO1	LDO1 Output Pin
6	GND	LDO1 and 2 Ground Pin
7	EN1	Enable Pin for Buck1 and LDO1 and 2
8	FB1	Buck1 Feedback Pin
9	GND_B1	Buck1 Ground Pin
10	SW1	Buck1 Switch Pin
11	VIN1	Input Power Terminal to Buck1 and 2
12	SW2	Buck2 Switch Pin
13	GND_B2	Buck2 Ground Pin
14	FB2	Buck2 Feedback Pin
DAP	SGND	Die Attach Pad (DAP)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

$V_{IN}1$,$V_{IN}2$		−0.2V to 6.0V
FB1, FB2, EN1,EN2		(GND−0.2V) to (V_{IN} + 0.2V) to 6.0V (max)
Continuous Power Dissipation(3)		Internally Limited
Junction Temperature (T_{J-MAX})		+150°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec.)		260°C
ESD Rating(4)	Human Body Model	2.5kV

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Internal thermal shutdown circuitry protects the device from permanent damage.
(4) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. MIL-STD-883 3015.7

Operating Ratings(1)(2)

$V_{IN}1$ (Buck1 and 2 Input Voltage),$V_{IN}2$ (LDO1 and 2 Input Voltage)(3)	3V to 5.5V
Recommended Load Current (Buck)	0mA to 600 mA
Recommended Load Current (LDO)	0mA to 100mA with 0.47uF O/P cap 0mA to 150mA with 1.0uF O/P cap
Junction Temperature (T_J) Range	−40°C to +125°C
Ambient Temperature (T_A) Range(4)	−40°C to +85°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is ensured. Operating Ratings do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All voltages are with respect to the potential at the GND pin.
(3) V_{IN1} and V_{IN2} should be tied together at all times for proper Power Up
(4) In Applications where high power dissipation and/or poor package resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (T_{J-MAX}), the maximum power dissipation of the device in the application (P_{D-MAX}) and the junction to ambient thermal resistance of the package (θ_{JA}) in the application, as given by the following equation:$T_{A-MAX}= T_{J-MAX}- (\theta_{JA} x P_{D-MAX})$.

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}) NHL0014B package(1)	37.3ºC/W

(1) Junction to ambient thermal resistance is highly dependent on board layout, PCB material environmental conditions and applications. In applications where high power dissipation exists, special care must be given to thermal dissipation issues in board design. The use of thermal vias under the pad may be required. For more on these topics, please refer to the Application Note: AN-1187: Leadless leadframe Package (LLP) SNOA401.

General Electrical Characteristics(1)(2)(3)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the full junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP3905 Typical Application Circuit (Figure 1)

Parameter		Test Conditions	Min	Typ	Max	Units
Login Input Thresholds						
V_{IN}	Input Voltage Range		3		5.5	V
I_Q	Shutdown Supply Current	All Circuits OFF except for POR and UVLO		6.5	10.0	µA
	No load Supply Current(4)	LDO1 and 2 and Buck1 and 2 on		140	250	
		(PWM only versions) LDO1 and 2 and Buck1 and 2 on		7	10.0	mA
V_{IH}	Logic High Input	V_{IN} = 3.0V to 5.5V	**1.2**			V
V_{IL}	Logic Low Input	V_{IN} = 3.0V to 5.5V			**0.4**	V
I_{EN}	Enable (EN1,2) Input Current(5)	EN1/EN2 = 5.5V and V_{IN}= 5.5V	**2.1**	5	**8.5**	µA
		EN1/EN2 = 0V and V_{IN}= 5.5V		0.001	0.1	µA
V_{UVLO-R}	Battery Under Voltage Lock-Out	V_{IN} Rising		2.7	3.1	V
$T_{SHUTDOWN}$	Thermal Shutdown(4)	Temperature		160		°C
		Hysteresis		20		

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) The parameters in the electrical characteristic table are tested at V_{IN}= 3.8V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) This specification is ensured by design.
(5) There is a 1 MΩ resistor between EN1,EN2 and ground on the device.

Buck Regulator Electrical Characteristics(1)(2)(3)

Buck 1 and 2 have a current rating of I_{max}= 600mA. Unless otherwise specified, limits are set with V_{IN} = $V_{EN1/2}$ = 3.8V, $V_{OUT(Buck1)}$= Vnom1 , $V_{OUT(Buck2)}$= Vnom2 and C_{IN}= C_{OUT}=10µF.
Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the full junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP3905 Typical Application Circuit (Figure 1)(1)(2)(4)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{FB}	Feedback Voltage	See(5)	**-4**		**+4**	%
V_{OUT}	Line Regulation	3.0V ≤ V_{IN} ≤ 5.5V I_O = 1mA		0.045		%/V
	Load Regulation	100 mA ≤ I_O ≤ 600mA		0.002		%/mA
$R_{DSON\ (P)}$	Pin-Pin Resistance for PFET	V_{IN}= V_{GS}= 3.6V		380	500	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for NFET	V_{IN}= V_{GS}= 3.6V(6)		250	400	mΩ
I_{LIM}	Switch Peak Current Limit	Open Loop	**650**	1000	**1220**	mA
F_{OSC}	Internal Oscillator Frequency	PWM Mode		2		MHz
η	Efficiency	IOUT = 5mA, PFM mode(6)	88			%
		IOUT = 300mA, PWM mode(6)	90			

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) The parameters in the electrical characteristic table are tested at V_{IN}= 3.8V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) C_{IN}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(5) For the adjustable version, feedback resistor values should be chosen for the divider network to ensure that at the desired output voltage the feedback pin is at 0.5V. See Buck Converter Applications Information.
(6) This specification is ensured by design.

LDO Regulator Electrical Characteristics[1][2][3]

The linear regulators have a current rating of I_{max}= 150mA with C_{OUT} = 1.0µF. A 100mA rating applies with C_{OUT} = 0.47µF. Unless otherwise specified, limits are set with V_{IN} = 3.8V, $V_{EN1/2}$ = 3.8V, C_{IN} = 1µF, C_{OUT} = 0.47µF, I_{OUT} = 1.0mA. Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the full junction temperature range (−40°C ≤ T_J ≤ +125°C). Unless otherwise noted, specifications apply to the LP3905 Typical Application Circuit (Figure 1)[1][2][4]

Parameter		Test Conditions		Min	Typ	Max	Units
ΔV_{OUT}	Output Voltage Tolerance	Over Full Line and Load Regulation		**−3**		**3**	%
	Line Regulation Error	V_{IN} = 3.8V to 5.5V, I_{OUT} = 1mA			0.05		%/V
	Load Regulation Error	I_{OUT} = 1 mA to 100mA			0.003		%/mA
I_{LOAD}	Load Current	See[5][6]		0			mA
V_{DO}	Dropout Voltage[7]	I_{OUT} = 100mA			80	**150**	mV
I_{SC}	Short Circuit Current Limit	See[8]			300	**500**	mA
I_{OUT}	Maximum Output Current	C_{OUT} = 1.0µF		**150**			mA
PSRR	Power Supply Rejection Ratio[6]	f = 100Hz, I_{OUT} = 100mA			90		dB
		f = 1kHz, I_{OUT} = 100mA			90		
		f = 10kHz, I_{OUT} = 100mA			60		
		f = 50kHz, I_{OUT} = 100mA			35		
		f = 100kHz, I_{OUT} = 100mA			25		
e_n	Output Noise Voltage[6]	BW = 10Hz to 100kHz, V_{IN} = 4.2V Buck1 Turned ON with I_{LOAD}= 0mA, Buck2 Turned OFF	I_{OUT} = 1mA		13.5		μV_{RMS}
			I_{OUT} = 100mA		15.5		
Transient Characteristics[6]							
ΔV_{OUT}	Line Transient[6]	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to ($V_{OUT(NOM)}$ + 1.6V) in 10µs, I_{OUT} = 1 mA		6			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6V) to ($V_{OUT(NOM)}$ + 1.0V) in 10µs, I_{OUT} = 1mA				6	
	Load Transient[6]	I_{OUT} = 1mA to 100mA in 10µs		-70			mV
		I_{OUT} = 100mA to 1mA in 10µs				30	
		I_{OUT} = 1mA to 150mA in 10µs C_{OUT} = 1.0µF		-100			
		I_{OUT} = 150mA to 1mA in 10µs C_{OUT} = 1.0µF				35	
	Overshoot on Startup	See[6]				20	mV

(1) All voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are ensured by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) The parameters in the electrical characteristic table are tested at V_{IN}= 3.8V unless otherwise specified. For performance over the input voltage range refer to datasheet curves.
(4) C_{IN}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(5) The device maintains a stable, regulated output voltage without a load.
(6) This specification is ensured by design.
(7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.
(8) Short Circuit Current is measured with V_{OUT} pulled to 0v and V_{IN} worst case = 5,5V.

Typical Application Circuit

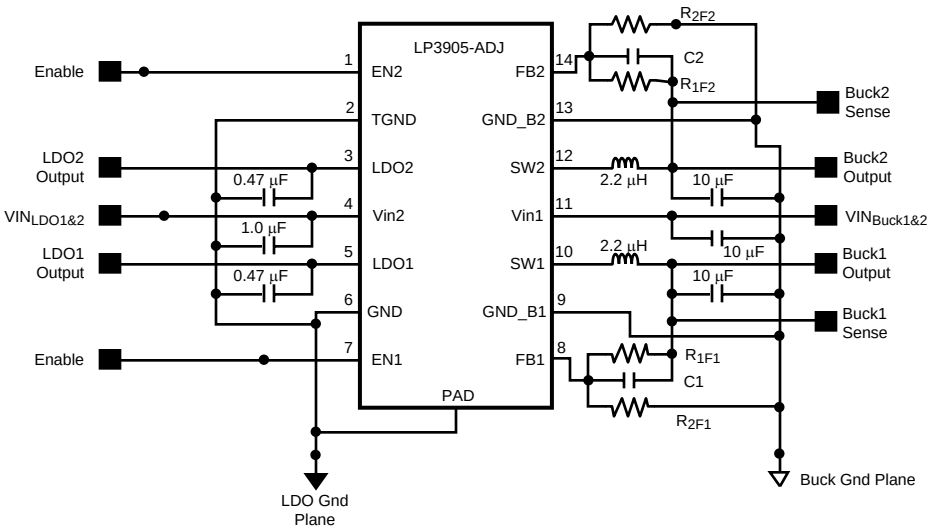


Figure 4. Typical Application Circuit For Adjustable Device

FUNCTIONAL DESCRIPTION

POWER UP/DOWN PROCEDURE

The LP3905 Bucks and LDOs are powered UP/DOWN with 2 control pins, EN1 and EN2. In order for the enable pins to operate, V_{IN1} and V_{IN2} should be set to a voltage level higher than V_{UVLO_R} (specified in electrical characteristic). Once enabled, EN1 will turn on Buck1, LDO1 and LDO2. EN2 can independently be used to enable Buck2. Figure 5 illustrates the power UP/DOWN timing sequence of the LP3905 blocks for $V_{EN} \geq V_{IH\ (min)}$ (enable) and $V_{EN} \leq V_{IL\ (max)}$ (disable).

Both linear regulators have active pulldowns when the outputs are disabled.

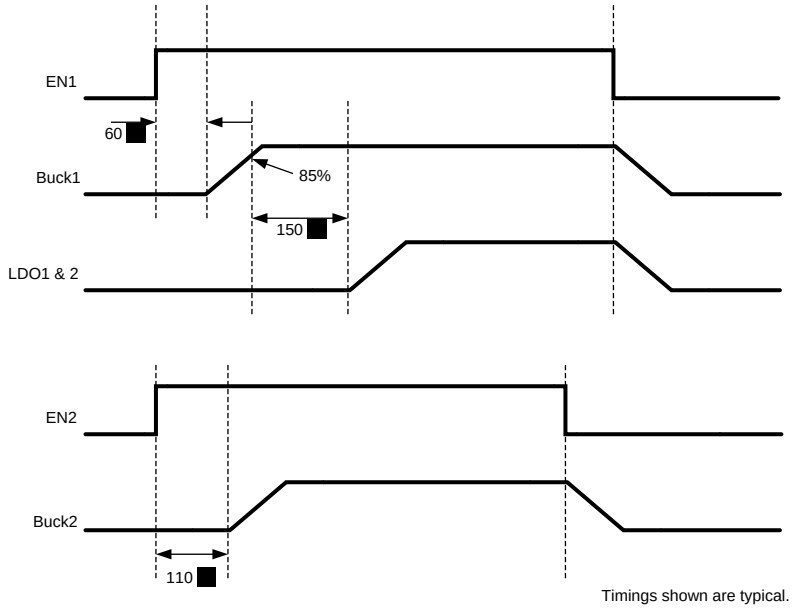


Figure 5. LP3905 Power Up and Power Down Timing Sequence

EN1 and EN2 can be controlled fully independently.

LDOs will be turned on only after Buck1 is powered up. LDOs are powered on simultaneously.

In case EN1 and EN2 are enabled at the same time, power up of Buck2 is delayed by 50µs in order to minimize the inrush current from the battery.

When EN1 and EN2 are disabled, the relevant output voltages are turned off.

DC/DC BUCK REGULATORS

The LP3905 Buck regulators are high efficiency step down DC-DC switching converters used for delivering a constant voltage from either a single Li-Ion or three cell NiMH/NiCd battery to portable devices such as cell phones and PDAs. Using a voltage mode architecture with synchronous rectification, the Buck Regulators have the ability to deliver up to 600 mA depending on the input voltage, output voltage, ambient temperature and the inductor chosen.

There are three modes of operation depending on the current required - PWM, PFM, and shutdown. The standard device operates in PWM mode at load currents of approximately 80 mA or higher, having voltage tolerance of ±4% with 90% efficiency or better. Lighter load currents cause the device to automatically switch into PFM for reduced current consumption and a longer battery life. Shutdown mode turns off the device, offering the lowest current consumption . A fixed mode device is also available which is fixed in PWM mode for both low and high load currents.

An adjustable voltage version is also avalable for which the output voltage can be selected by using two external resistors at each of the two buck outputs.

Additional features include soft-start, under voltage protection, current overload protection, and thermal shutdown protection.

The part uses an internal reference voltage of 0.5V. It is recommended to keep the part in shutdown until the input voltage is 3V or higher.

BUCK CONVERTER BLOCK DIAGRAM

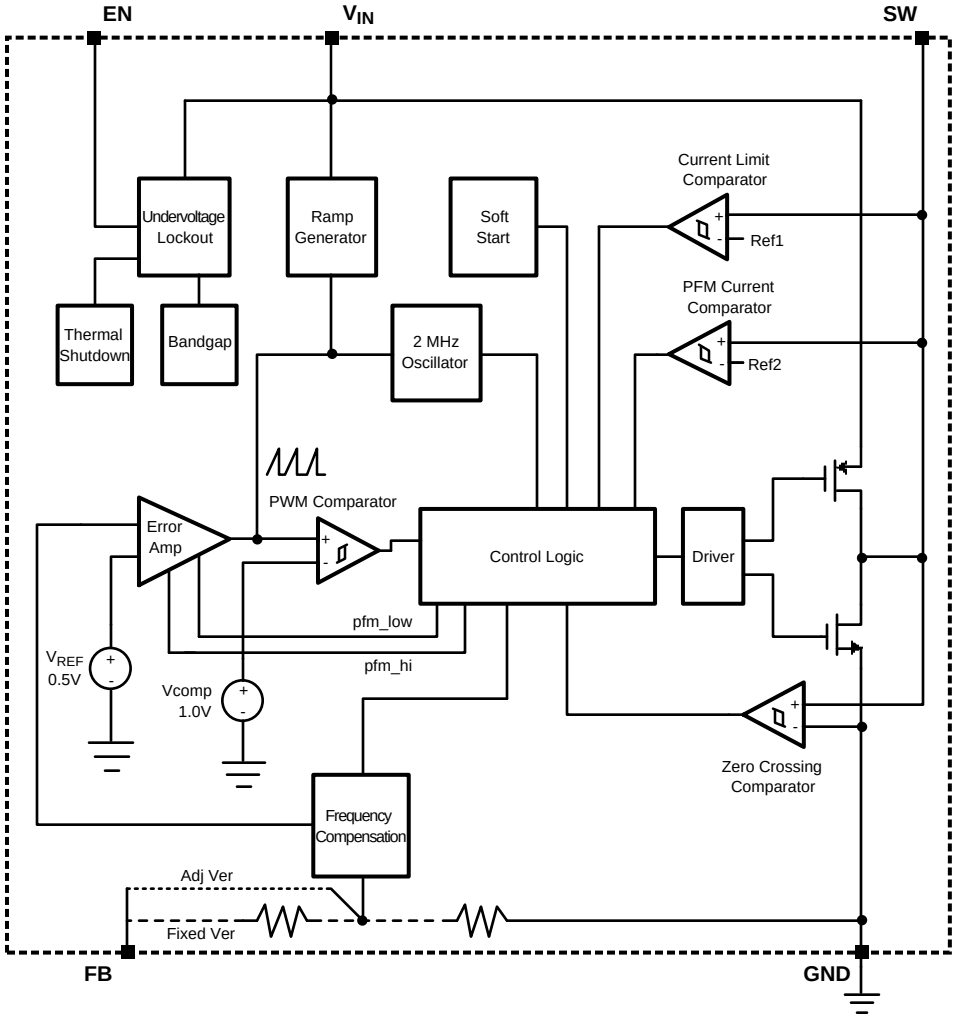


Figure 6. Simplified Functional Diagram

CIRCUIT OPERATION

The LP3905 Buck regulators operate as follows. During the first portion of each switching cycle, the control block in the LP3905 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN}–V_{OUT})/L$, by storing energy in a magnetic field.

During the second portion of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of - V_{OUT}/L.

The output filter stores charge when the inductor current is high, and releases it when inductor current is low, smoothing the voltage across the load.

The output voltage is regulated by modulating the PFET switch on time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier at the SW pin to a low-pass filter formed by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

PWM OPERATION

During PWM operation the converters operate as a voltage-mode controllers with input voltage feed forward. This allows the converters to achieve good load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward inversely proportional to the input voltage is introduced.

While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. At the beginning of each clock cycle the PFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator can also turn off the switch in case the current limit of the PFET is exceeded. Then the NFET switch is turned on and the inductor current ramps down. The next cycle is initiated by the clock turning off the NFET and turning on the PFET.

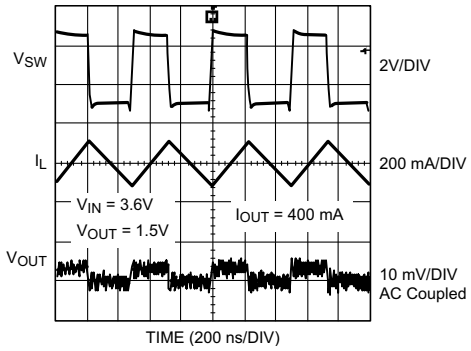


Figure 7. Typical PWM Operation

Internal Synchronous Rectification

While in PWM mode, if enabled, the Bucks use an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Current Limiting

A current limit feature allows the LP3905 Bucks to protect Internal and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 1000 mA (typ). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

PFM OPERATION

At very light loads, the converters enters PFM mode and operate with reduced switching frequency and supply current to maintain high efficiency.

The Bucks will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

A. The inductor current becomes discontinuous.

B. The peak PMOS switch current drops below the I_{MODE} level,

$$\text{Typically} \quad I_{MODE} < 30\ \text{mA} + \frac{V_{IN}}{42\Omega} \tag{1}$$

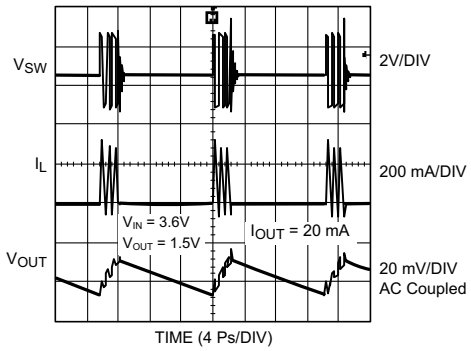


Figure 8. Typical PFM Operation

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between ~0.6% and ~1.7% above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage reaches the 'high' PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is:

$$I_{PFM} = 112\ \text{mA} + \frac{V_{IN}}{27\Omega} \tag{2}$$

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is 16µA (typ), which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the 'low' PFM threshold, the cycle repeats to restore the output voltage (average voltage in pfm mode) to ~1.15% above the nominal PWM output voltage.

If the load current should increase during PFM mode causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode. When V_{IN} =2.8V the part transitions from PWM to PFM mode at ~35mA output current and from PFM to PWM mode at ~85mA , when V_{IN}=3.6V, PWM to PFM transition happens at ~50mA and PFM to PWM transition happens at ~100mA, when V_{IN} =4.5V, PWM to PFM transition happens at ~65mA and PFM to PWM transition happens at ~115mA.

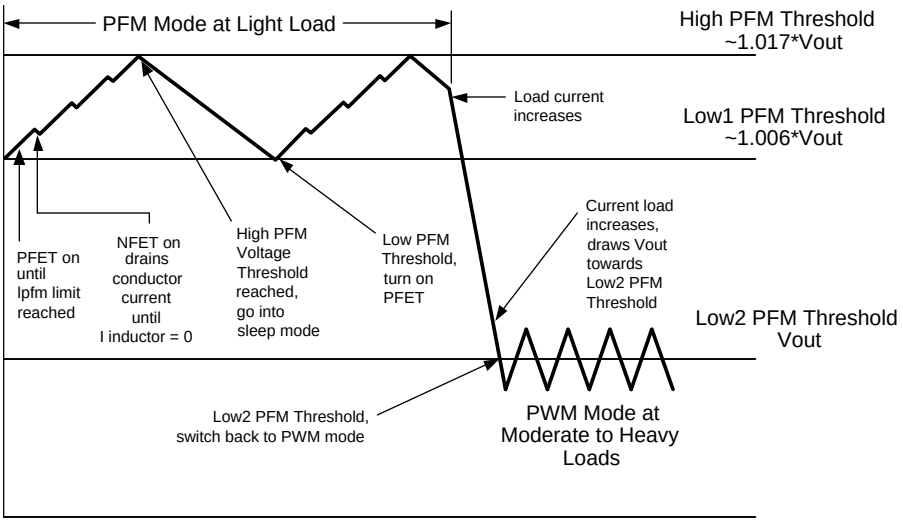


Figure 9. Operation in PFM Mode and Transfer to PWM Mode

SOFT START

The LP3905 Buck Converters have a soft-start circuit that limits in-rush current during start-up. Additionally, in case EN1 and EN2 are enabled at the same time, a typical 500µs delay between Buck1 and Buck2 Power Up prevents any further Inrush current from the battery.

During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after Vin reaches 3V. Soft start is implemented by increasing switch current limit in steps of 70mA, 140mA, 280mA and 1000mA (typ. switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up. Typical start-up times with 22µF output capacitor and 300mA load current is 400µs and with 1mA load current its 275µs.

Application Information

DC - DC CONVERTORS

Adjustable Buck - Output Voltage Selection

The buck converter output voltage of the adjustable version device can be set via the selection of the external feedback resistor network forming the output feedback between the output voltage side of the Inductor and the FB pin and the FB Pin and GND.

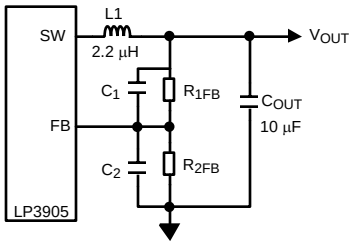


Figure 10. Adjustable Buck Converter Components

V_{OUT} will be adjusted to make the voltage at FB equal to 0.5V. The resistor from FB to ground (R_{FB2}) should be around 200kΩ to keep the current drawn through the resistor network well below the 16µA quiescent current level (PFM mode) but large enough that it is not susceptible to noise. If R2 is 200kΩ and with V_{FB} at 0.5V, the current through the resistor feedback network will be 2.5µA.

The formula for output voltage selection is:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R_{1FB}}{R_{2FB}}\right) \quad (3)$$

V_{OUT} - output voltage (Volts)

V_{FB} - feedback voltage (0.5V)

R_{1FB} - feedback resistor from V_{OUT} to FB

R_{2FB} - feedback resistor from FB to GND

For any out voltage greater than or equal to 1.0V a zero should be added around 45 kHz by the addition of a capacitor C1. The formula for the calculation of C1 is:

$$C_1 = \frac{1}{(2 \times \pi \times R_{1FB} \times 45 \times 10^3)} \quad (4)$$

For recommended component values see Table 1

Table 1. Buck Component Configurations for Various Output Voltage Values

V_{OUT} (V)	RFB1 (kΩ)	RFB2 (kΩ)	C1 (pF)	C2 (pF)	L (µH)	C_{OUT} (µF)
1.0	200	200	18	none	2.2	10
1.2	280	200	12	none	2.2	10
1.4	360	200	10	none	2.2	10
1.5	360	180	10	none	2.2	10
1.6	442	200	8.2	none	2.2	10
1.85	540	200	6.8	none	2.2	10
2.5	402	100	8.2	none	2.2	10
2.8	464	100	8.2	33	2.2	10
3.3	562	100	6.8	33	2.2	10

Buck Inductor Selection

There are two main considerations when choosing an inductor; the inductor should not saturate, and the inductor current ripple is small enough to achieve the desired output voltage ripple. Different saturation current rating specs are followed by different manufacturers so attention must be given to details. Saturation current ratings are typically specified at 25°C so ratings at max ambient temperature of application should be requested from manufacturer.

There are two methods to choose the inductor saturation current rating.

Method 1:

The saturation current is greater than the sum of the maximum load current and the worst case average to peak inductor current. This can be written as:

$$I_{SAT} > I_{OUTMAX} + I_{RIPPLE}$$

$$\text{where } I_{RIPPLE} = \left(\frac{V_{IN} - V_{OUT}}{2 * L}\right) * \left(\frac{V_{OUT}}{V_{IN}}\right) * \left(\frac{1}{f}\right) \quad (5)$$

- I_{RIPPLE}: average to peak inductor current
- I_{OUTMAX}: maximum load current (600mA)
- V_{IN}: maximum input voltage in application
- L : min inductor value including worst case tolerances (30% drop can be considered for method 1)
- f : minimum switching frequency (1.6Mhz)
- V_{OUT}: output voltage

Method 2:

A more conservative and recommended approach is to choose an inductor that has saturation current rating greater than the max current limit of 1220mA.

A 2.2µH inductor with a saturation current rating of at least 1250mA is recommended for most applications.The inductor's resistance should be less than 0.3Ω for good efficiency. For low-cost applications, an unshielded bobbin inductor could be considered. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise shielded inductor, in the event that noise from low-cost bobbin models is unacceptable.

Buck DC/DC Convertor Input Capacitor Selection

A ceramic input capacitor of 10µF, 6.3V is sufficient for most applications. Place the input capacitor as close as possible to the V_{IN} pin of the device. A larger value may be used for improved input voltage filtering. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. The input filter capacitor supplies current to the PFET switch of the LP3905 in the first half of each cycle and reduces voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of the input voltage spikes due to this rapidly changing current. Select a capacitor with sufficient ripple current rating. The input current ripple can be calculated as:

$$I_{RMS} = I_{OUTMAX} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}} + \frac{r^2}{12}\right)}$$

$$r = \frac{(V_{IN} - V_{OUT}) * V_{OUT}}{L * f * I_{OUTMAX} * V_{IN}}$$

The worst case is when $V_{IN} = 2 * V_{OUT}$ (6)

DC/DC CONVERTOR OUTPUT CAPACITOR SELECTION

Use a 10µF, 6.3V ceramic capacitor. Use X7R or X5R types, do not use Y5V. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603. DC bias characteristics vary from manufacturer to manufacturer and dc bias curves should be requested from them as part of the capacitor selection process.

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The output voltage ripple is caused by the charging and discharging of the output capacitor and also due to its R_{ESR} and can be calculated as:

Voltage peak-to-peak ripple due to capacitance can be expressed as follows:

$$V_{PP\text{-}C} = \frac{I_{RIPPLE}}{4*f*C} \tag{7}$$

Voltage peak-to-peak ripple due to ESR can be expressed as follows:

$V_{PP\text{-}ESR} = (2 * I_{RIPPLE}) * R_{ESR}$

Because these two components are out of phase the rms value can be used to get an approximate value of peak-to-peak ripple.

Voltage peak-to-peak ripple, root mean squared can be expressed as follows:

$$V_{PP\text{-}RMS} = \sqrt{V_{PP\text{-}C}^{\,2} + V_{PP\text{-}ESR}^{\,2}} \tag{8}$$

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (R_{ESR}).

The R_{ESR} is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

LINEAR REGULATORS

Capacitor Selection

The LP3955 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer: for capacitance values in the range of 0.47µF to 10µF range, ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1µF ceramic capacitor is in the range of 20mW to 40mW, which easily meets the ESR requirement for stability by the LP3955. For both input and output capacitors careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general. As an example Figure 11 shows a typical graph showing a comparison of capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, as a result of the DC Bias condition the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table (0.7µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

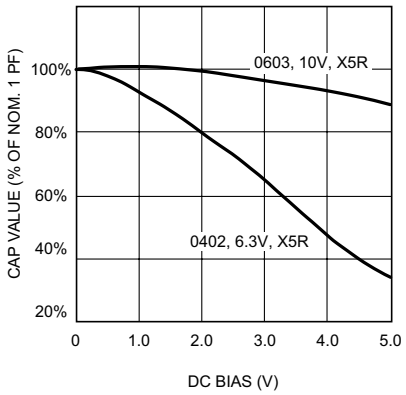


Figure 11. Capacitor Performance (DC Bias)

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to +85°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1µF to 4.7µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

LDO Input Capacitor

An input capacitor is required for stability. The input capacitor should be at least equal to or greater than the output capacitor. It is recommended that a 1µF capacitor be connected between V_{IN2} input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application. There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain 1.0µF ±30% over the entire operating voltage and temperature range.

LDO Output Capacitor

The LP3905 LDOs are designed specifically to work with very small ceramic output capacitors. A ceramic capacitor (dielectric types X5R or X7R) in the 0.47µF to 10µF range, and with ESR between 5mΩ to 500mΩ, is suitable in the application circuit. For this device the output capacitor should be connected between the LDO1 and LDO2 pins and a good ground connection and should be mounted within 1cm of the device.

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5mΩ to 500mΩ for stability.

No-Load Stability

The LP3905 LDOs will remain stable and in regulation with no external load.

Enable Control

A 1MΩ pulldown resistor ties the $EN_{1/2}$ input to ground, this ensures that the device will remain off when the enable pin is left open circuit. To ensure proper operation, the signal source used to drive the $EN_{1/2}$ input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}. EN1 can be used to turn ON Buck1 and LDO1/2. In this case Buck1 will be turned on first. Once Buck1 is powered up, after a typical 150µs delay LDO1/2 will be turned on concurrently.

LP3905 Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability.

Good layout for the LP3905 can be implemented by following a few simple design rules.

1. *Place the Buck inductor and filter capacitors close together and make the traces short.* The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the V_{IN} and GND pin.
2. *Arrange the components so that the switching current loops curl in the same direction.* During the first half of each cycle, current flows from the input filter capacitor through the LP3905 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LP3905 by the inductor to the output filter capacitor and then back through ground forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. *Connect the ground pins of the Bucks and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane (if one is used) with several vias.* This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LP3905 by giving it a low-impedance ground connection.
4. *Use wide traces between the power components and for power connections to the DC-DC converter circuit.* This reduces voltage errors caused by resistive losses across the traces.
5. *Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components.* The voltage feedback trace must remain close to the Buck circuits and should be direct but should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace. A good approach is to route the feedback trace on another layer and to have a ground plane between the top layer and layer on which the feedback trace is routed. In the same manner for the adjustable part it is desired to have the feedback dividers on the bottom layer.
6. *Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry.* Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converters on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	17

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3905SD-A3/NOPB	ACTIVE	WSON	NHL	14	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	3905-A3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

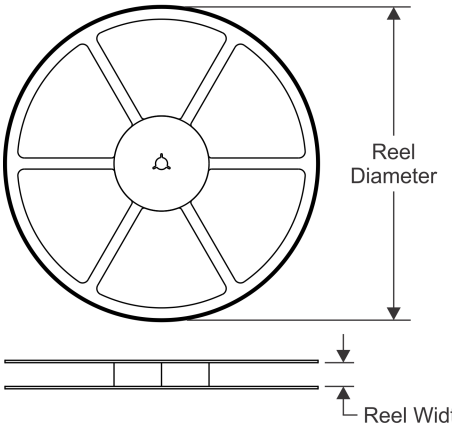
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

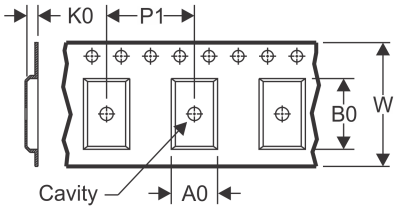
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

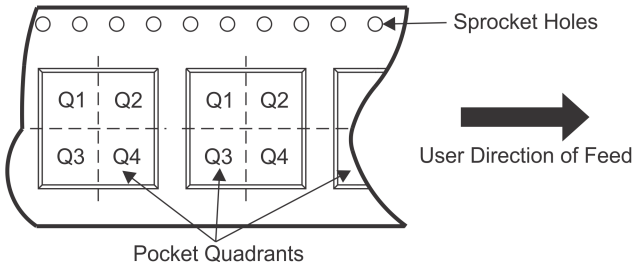


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

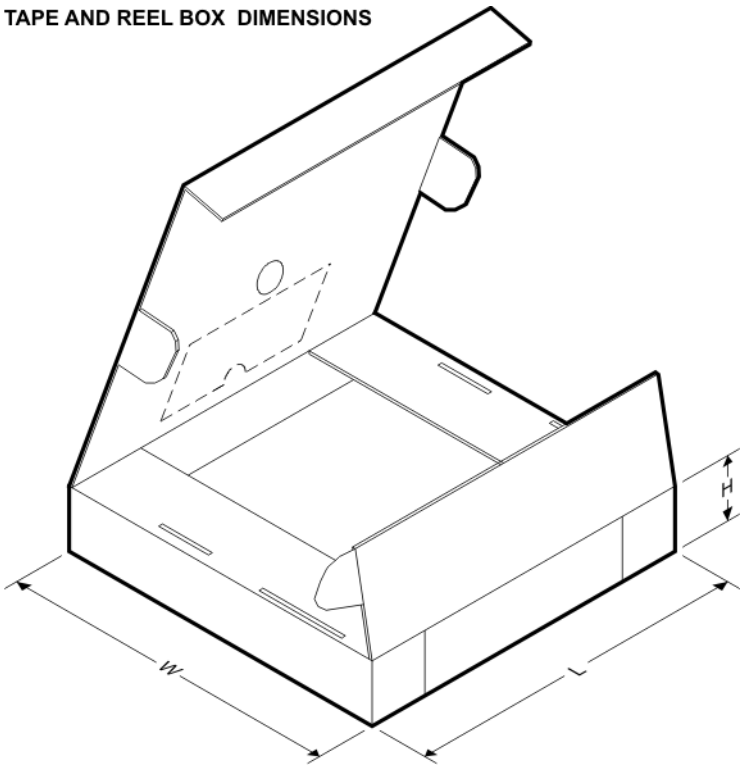
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3905SD-A3/NOPB	WSON	NHL	14	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

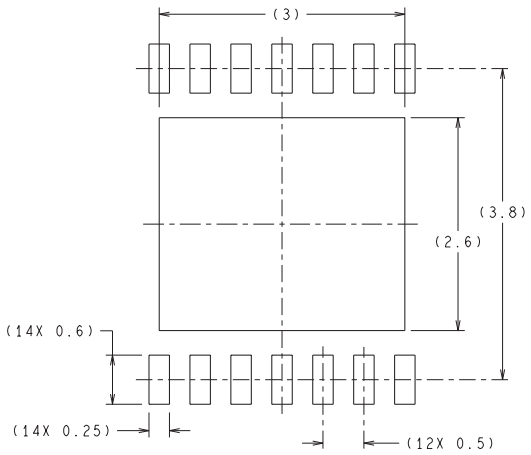
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

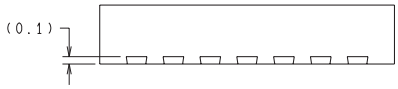
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3905SD-A3/NOPB	WSON	NHL	14	1000	208.0	191.0	35.0

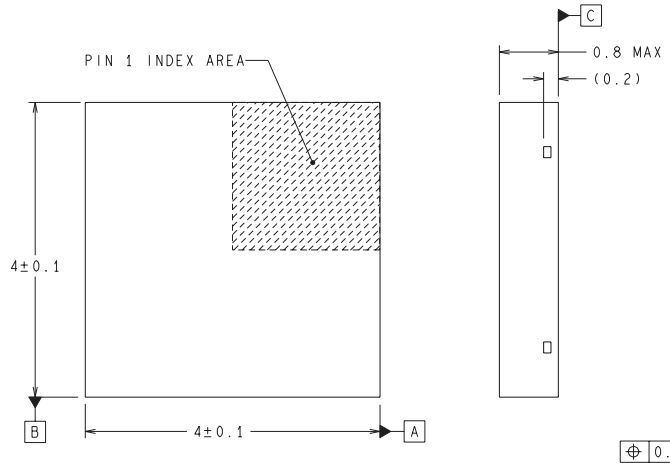
NHL0014B

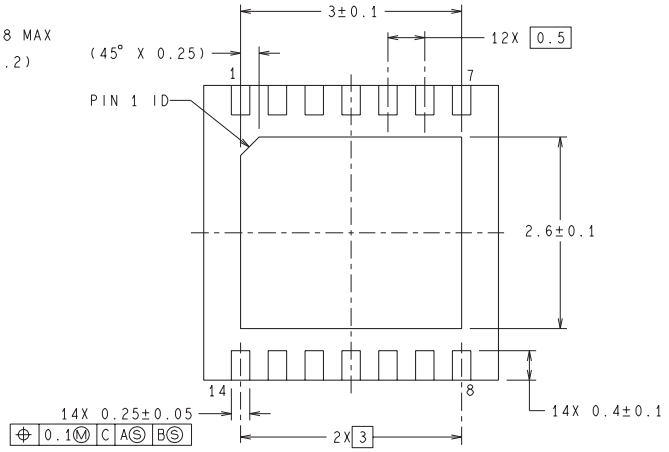


RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY







SDA14B (Rev A)

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