# bq500101 NexFET™功率级

## 1 特性

- 5A 电流时系统效率达 98%
- 最大额定持续电流 10A，峰值 15A
- 高频工作（高达 600kHz）
- 高密度小外形尺寸无引线 (SON) 3.5mm x 4.5mm 封装
- 超低电感封装
- 系统已优化的印刷电路板 (PCB) 封装
- 3.3V 和 5V 脉宽调制 (PWM) 信号兼容
- 输入电压高达 24V
- 集成型自举二极管
- 击穿保护
- 符合 RoHS 绿色环保标准-无铅引脚镀层
- 无卤素
- 包含高效栅极驱动器和场效应管 (FET) 的优化型功率级
- 针对 15W 无线电源发射器设计进行了优化

## 2 应用

- 用于 15W 或 5W 系统的无线电源发射器，符合 WPC (Qi) 1.2 规范
- 专用无线充电器和发射器
- 以无线方式供电的工业和医疗系统
- 更多相关信息，请访问 www.ti.com/wirelesspower

## 3 说明

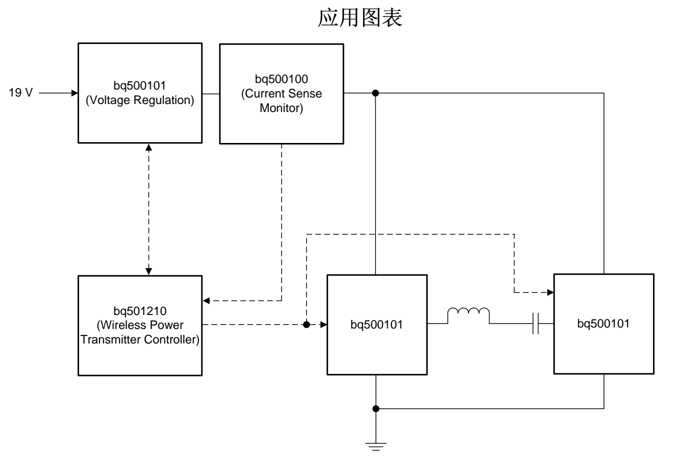
bq500101 NexFET™功率级针对涵盖 WPC v1.2 中等功率规范的无线电源 应用 进行了优化。该器件既可用于固定频率发射器类型中的电源轨电压控制，也可用于固定频率和频率可变两种发射器类型中的线圈驱动器。这个组合在小型 3.5mm x 4.5mm 外形尺寸封装中实现具有高电流、高效率和高速开关功能的器件。此外，印刷电路板 (PCB) 封装已经过优化，可帮助减少设计时间并简化总体系统设计的完成。

器件信息(1)

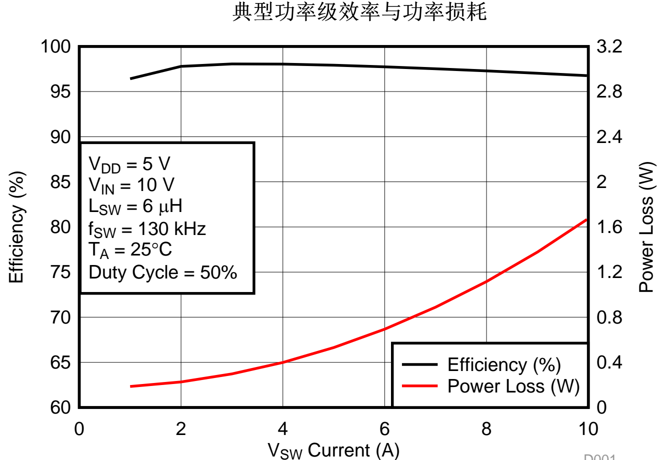
| 订货编号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| bq500101 | DPC (9) | 3.5mm x 4.5mm |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

应用图表




典型功率级效率与功率损耗





An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 修订历史记录

| 日期 | 修订版本 | 注释 |
|---|---|---|
| 2016 年 3 月 | * | 首次发布。 |


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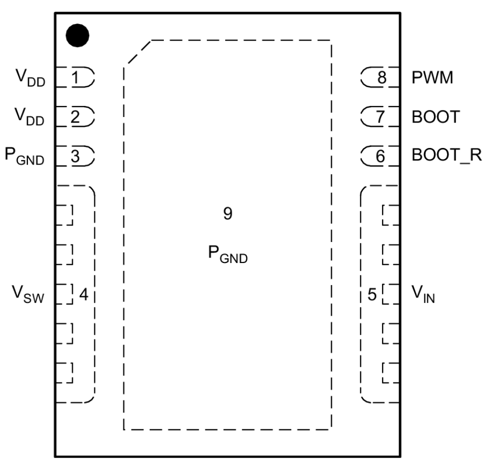
# 5 Pin Configuration and Functions

**SON 3.5 × 4.5 mm (Top View)**




## Pin Functions

| PIN | | DESCRIPTION |
|---|---|---|
| NO. | NAME | |
| 1 | $V_{DD}$ | Supply voltage to gate drivers and internal circuitry. |
| 2 | $V_{DD}$ | Supply voltage to gate drivers and internal circuitry. |
| 3 | $P_{GND}$ | Power ground, needs to be connected to Pin 9 and PCB |
| 4 | $V_{SW}$ | Voltage switching node – pin connection to the inductor. |
| 5 | $V_{IN}$ | Input voltage pin. Connect input capacitors close to this pin. |
| 6 | BOOT_R | Bootstrap capacitor $C_{BOOT}$ connections. Connect a minimum 0.1 µF 16 V X5R, ceramic cap $C_{BOOT}$ from BOOT to BOOT_R pins. The bootstrap capacitor provides the charge to turn on the Control FET. The bootstrap diode is integrated. Boot_R is internally connected to $V_{SW}$. |
| 7 | BOOT | |
| 8 | PWM | Pulse Width modulated tri-state input from external controller. Logic Low sets Control FET gate low and Sync FET gate high. Logic High sets Control FET gate high and Sync FET gate Low. Open or High Z sets both MOSFET gates low if greater than the tri-state shutdown hold-off time ($t_{3HT}$) |
| 9 | $P_{GND}$ | Power ground |

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# 6 Specifications

## 6.1 Absolute Maximum Ratings[1]

$T_A$ = 25°C (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| | $V_{IN}$ to $P_{GND}$ | –0.3 | 30 | V |
| | $V_{SW}$ to $P_{GND}$ , $V_{IN}$ to $V_{SW}$ | –0.3 | 30 | V |
| | $V_{SW}$ to $P_{GND}$, $V_{IN}$ to $V_{SW}$ (<10 ns) | –7 | 33 | V |
| | $V_{DD}$ to $P_{GND}$ | –0.3 | 6 | V |
| | PWM | –0.3 | 6 | V |
| | BOOT to $P_{GND}$ | –0.3 | 35 | V |
| | BOOT to $P_{GND}$ (<10 ns) | –2 | 38 | V |
| | BOOT to BOOT_R | –0.3 | 6 | V |
| | BOOT to BOOT_R (duty cycle <0.2%) | | 8 | V |
| $P_D$ | Power dissipation | | 8 | W |
| $T_J$ | Operating temperature | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | –55 | 150 | °C |

(1) Stresses above those listed in *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to Absolute Maximum rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM)[1] | ±2000 | V |
| | | Charged device model (CDM)[2] | ±500 | |

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

$T_A$ = 25° (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Gate drive voltage | | 4.5 | 5.5 | V |
| $V_{IN}$ | Input supply voltage[1] | | | 24 | V |
| $I_{SW}$ | Continuous $V_{SW}$ current | $V_{IN}$ = 10 V, $V_{DD}$ = 5 V, Duty cycle = 50%, $f_{SW}$ = 130 kHz, $L_{SW}$ = 6 µH[2] | | 10 | A |
| $I_{SW-PK}$ | Peak $V_{SW}$ current[3] | | | 15 | A |
| $f_{SW}$ | Switching frequency | $C_{BOOT}$ = 0.1 µF (min) | | 600 | kHz |
| | On time duty cycle | | | 85% | |
| | Minimum PWM on time | | 40 | | ns |
| | Operating temperature | | –40 | 125 | °C |

(1) Operating at high $V_{IN}$ can create excessive AC voltage overshoots on the switch node ($V_{SW}$) during MOSFET switching transients. For reliable operation, the switch node ($V_{SW}$) to ground voltage must remain at or below the *Absolute Maximum Ratings*.
(2) Measurement made with six 10 µF (TDK C3216X5R1C106KT or equivalent) ceramic capacitors placed across $V_{IN}$ to $P_{GND}$ pins.
(3) System conditions as defined in Note 2. Peak $V_{SW}$ Current is applied for $t_p$ = 10 ms, duty cycle ≤ 1%

## 6.4 Thermal Information

$T_A$ = 25°C (unless otherwise noted)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-case (top of package) thermal resistance[1] | | | 22.8 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance[2] | | | 2.5 | |

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz (0.071 mm thick) Cu pad on a 1.5 inch x 1.5 inch, 0.06 inch (1.52 mm) thick FR4 board.
(2) $R_{\theta JB}$ value based on hottest board temperature within 1mm of the package.


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## 6.5 Electrical Characteristics

$T_A$ = 25°C, $V_{DD}$ = POR to 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **$P_{LOSS}$** | | | | | | |
| Power loss(1) | | $V_{IN}$ = 10 V, $V_{DD}$ = 5 V, $I_{SW}$ = 5 A, $f_{SW}$ = 130 kHz, $L_{SW}$ = 6 µH , $T_J$ = 25°C, Duty Cycle = 50% | | 0.53 | | W |
| Power loss(1) | | $V_{IN}$ = 10 V, $V_{DD}$ = 5 V, $I_{SW}$ = 5 A, $f_{SW}$ = 130 kHz, $L_{SW}$ = 6 µH , $T_J$ = 125°C, Duty Cycle = 50% | | 0.68 | | W |
| **$V_{IN}$** | | | | | | |
| $I_Q$ | $V_{IN}$ quiescent current | PWM = Floating, $V_{DD}$ = 5 V, $V_{IN}$= 24 V | | | 1 | µA |
| **$V_{DD}$** | | | | | | |
| $I_{DD}$ | Standby supply current | PWM = Float | | 130 | | µA |
| $I_{DD}$ | Operating supply current | PWM = 50% Duty cycle, $f_{SW}$ = 130 kHz | | 2 | | mA |
| **POWER-ON RESET AND UNDERVOLTAGE LOCKOUT** | | | | | | |
| $V_{DD}$ Rising | Power-on reset | | | | 4.15 | V |
| $V_{DD}$ Falling | UVLO | | 3.7 | | | V |
| | Hysteresis | | | 0.2 | | V |
| **PWM I/O SPECIFICATIONS** | | | | | | |
| $R_I$ | Input impedance | Pull up to $V_{DD}$ | | 1700 | | kΩ |
| | | Pull down (to GND) | | 800 | | |
| $V_{IH}$ | Logic level high | | 2.65 | | | V |
| $V_{IL}$ | Logic level low | | | | 0.6 | |
| $V_{IH}$ | Hysteresis | | | 0.2 | | |
| $V_{TS}$ | Tri-state voltage | | 1.3 | | 2 | |
| $t_{THOLD(off1)}$ | Tri-state activation time (falling) PWM | | | 60 | | ns |
| $t_{THOLD(off2)}$ | Tri-state activation time (rising) PWM | | | 60 | | |
| $t_{3RD(PWM)}$ | Tri-state exit time PWM (1) | | | | 100 | ns |
| **BOOTSTRAP SWITCH** | | | | | | |
| $V_{FBST}$ | Forward voltage | $I_F$ = 10 mA | | 120 | 240 | mV |
| $I_{RLEAK}$ | Reverse leakage(1) | $V_{BOOT}$ – $V_{DD}$ = 25 V | | | 2 | µA |

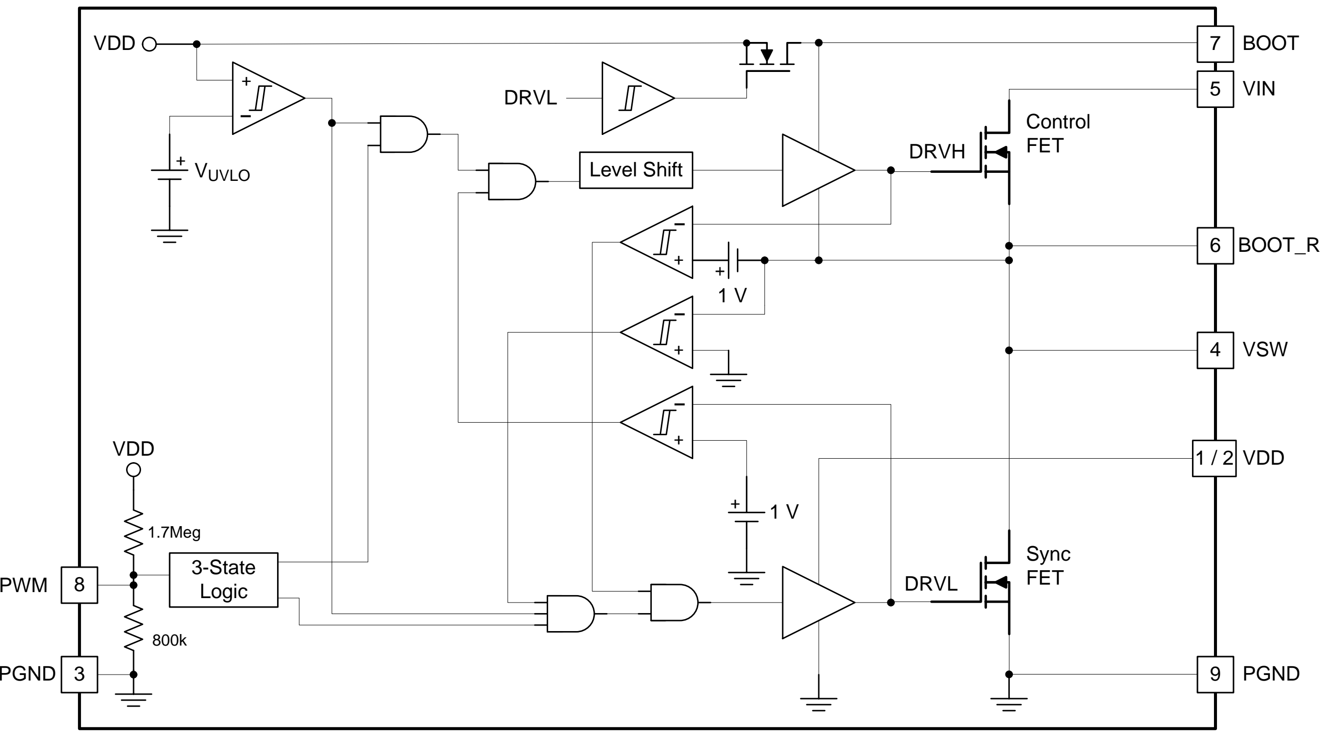
(1) Specified by design

# 7 Detailed Description

## 7.1 Overview

The bq500101 NexFET™ Power Stage is a highly optimized design for use in wireless power transmitter designs. The bq500101 can also be used for synchronous buck applications.

## 7.2 Functional Block Diagram





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## 7.3 Feature Description

### 7.3.1 Powering bq500101 And Gate Drivers

An external $V_{DD}$ voltage is required to supply the integrated gate driver device and provide the necessary gate drive power for the MOSFETS. A 1-µF 10-V X5R or higher ceramic capacitor is recommended to bypass $V_{DD}$ pin to $P_{GND}$. A bootstrap circuit to provide gate drive power for the Control FET is also included. The bootstrap supply to drive the Control FET is generated by connecting a 100-nF 16-V X5R ceramic capacitor $C_{BOOT}$ between BOOT and BOOT_R pins. An optional $R_{BOOT}$ resistor in series with $C_{BOOT}$ can be used to slow down the turn on speed of the Control FET and reduce voltage spikes on the $V_{SW}$ node. A typical 1 Ω to 4.7 Ω value is a compromise between switching loss and $V_{SW}$ spike amplitude.

### 7.3.2 Undervoltage Lockout Protection (UVLO)

The undervoltage lockout (UVLO) comparator evaluates the VDD voltage level. As $V_{VDD}$ rises, both the Control FET and Sync FET gates hold actively low at all times until $V_{VDD}$ reaches the higher UVLO threshold ($V_{UVLO_H}$)., Then the driver becomes operational and responds to PWM command. If VDD falls below the lower UVLO threshold ($V_{UVLO_L}$ = $V_{UVLO_H}$ – Hysteresis), the device disables the driver and drives the outputs of the Control FET and Sync FET gates actively low. Figure 1 shows this function.

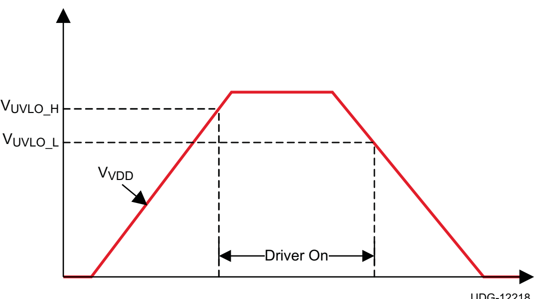


**Figure 1. UVLO Operation**

### 7.3.3 Integrated Boost-Switch

To maintain a BOOT-$V_{SW}$ voltage close to VDD (to get lower conduction losses on the high-side FET), the conventional diode between the VDD pin and the BOOT pin is replaced by a FET which is gated by the DRVL signal.

# 8 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The Power Stage bq500101 is a highly optimized design for wireless power transmitter applications using NexFET devices with a 5-V gate drive. The Control FET and Sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems centric environment. The high-performance gate driver device integrated in the package helps minimize the parasitics and results in extremely fast switching of the power MOSFETs. System level performance curves such as Power Loss, Safe Operating Area and normalized graphs allow engineers to predict the product performance in the actual application.

## 8.2 Typical Application

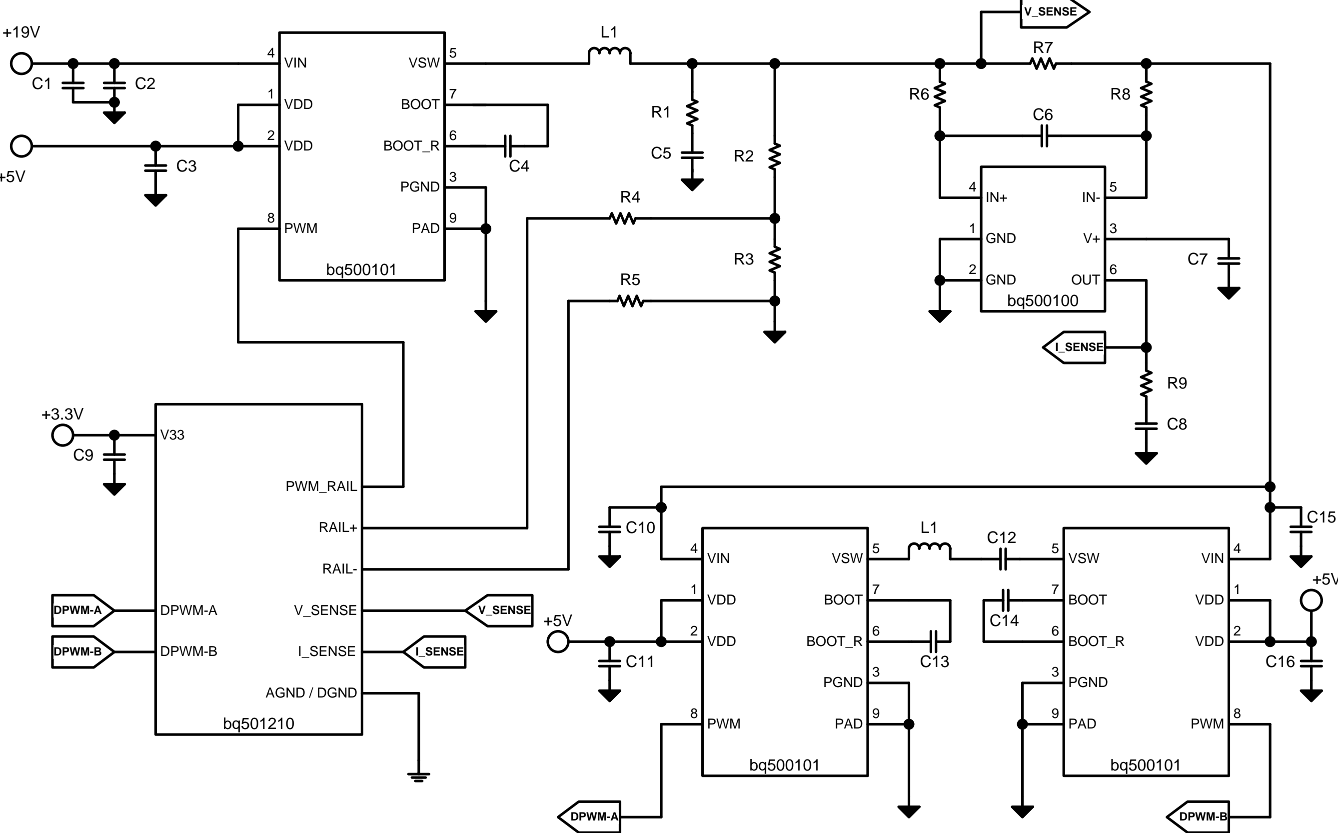


Figure 2. Application Schematic


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## Typical Application (continued)

### 8.2.1 Application Curves

$T_J$ = 125°C, unless stated otherwise

$V_{IN}$ = 10 V $V_{DD}$ = 5 V
$f_{SW}$ = 130 kHz $L_{SW}$ = 6 μH Duty Cycle = 50%

**Figure 3. Power Loss vs Output Current**

$V_{IN}$ = 10 V $V_{DD}$ = 5 V
$f_{SW}$ = 130 kHz $L_{SW}$ = 6 μH Duty Cycle = 50%

**Figure 4. Power Loss vs Temperature**

$V_{IN}$ = 10 V $V_{DD}$ = 5 V
$f_{SW}$ = 130 kHz $L_{SW}$ = 6 μH Duty Cycle = 50%

**Figure 5. Safe Operating Area – PCB Horizontal Mount** (1)

$V_{IN}$ = 10 V $V_{DD}$ = 5 V
$f_{SW}$ = 130 kHz $L_{SW}$ = 6 μH Duty Cycle = 50%

**Figure 6. Typical Safe Operating Area**

$V_{IN}$ = 10 V $V_{DD}$ = 5 V
$I_{SW}$ = 5 A $L_{SW}$ = 6 μH Duty Cycle = 50%

**Figure 7. Normalized Power Loss vs Frequency**

$I_{SW}$ = 5 A $V_{DD}$ = 5 V
$f_{SW}$ = 130 kHz $L_{SW}$ = 6 μH Duty Cycle = 50%

**Figure 8. Normalized Power Loss vs Input Voltage**

(1) LFM: Linear Feet per Minute (Air Flow Velocity)

## Typical Application (continued)

$T_J$ = 125°C, unless stated otherwise

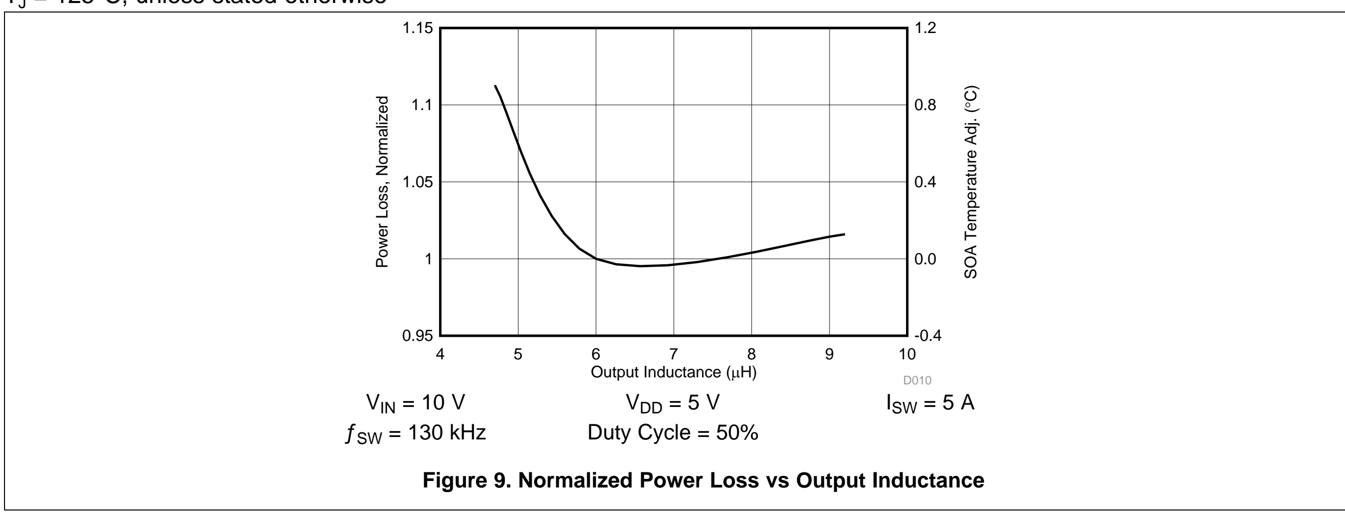


**Figure 9. Normalized Power Loss vs Output Inductance**

1. The Typical bq500101 System Characteristic curves are based on measurements made on a PCB design with dimensions of 4.0 inches (W) × 3.5 inches (L) × 0.062 inch (T) and 6 copper layers of 1-oz. copper thickness. See the *System Example* section for detailed explanation.

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$T_J$ = 125°C, unless stated otherwise

## 8.3 System Example

### 8.3.1 Power Loss Curves

MOSFET centric parameters such as ON-resistance and gate charges are primarily needed by engineers to estimate the loss generated by the devices. In an effort to simplify the design process for engineers, Texas Instruments has provided measured power loss performance curves. Figure 3 plots the power loss of the bq500101 as a function of load current. This curve is measured by configuring and running the bq500101 as the circuit shown in Figure 10. The measured power loss is the bq500101 device power loss which consists of both input conversion loss and gate drive loss. Equation 1 is used to generate the power loss curve.

$$\textbf{Power Loss} = (V_{IN} \times I_{IN}) + (V_{DD} \times I_{DD}) - (V_{SW_AVG} \times I_{OUT}) \quad (1)$$

The power loss curve in Figure 3 is measured at the maximum recommended junction temperature of $T_J$ = 125°C under isothermal test conditions.

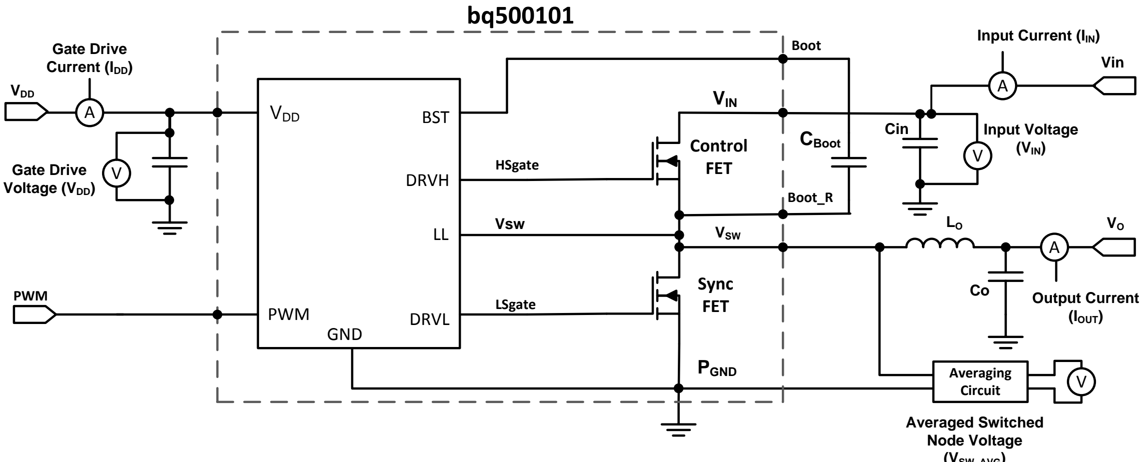


**Figure 10. Power Loss Test Circuit**

### 8.3.2 Safe Operating Area (SOA) Curves

The SOA curves in the bq500101 datasheet give engineers guidance on the temperature boundaries within an operating system by incorporating the thermal resistance and system power loss. Figure 5 and Figure 6 outline the temperature and airflow conditions required for a given load current. The area under the curve dictates the safe operating area. All the curves are based on measurements made on a PCB design with dimensions of 4.0" (W) x 3.5" (L) x 0.062" (T) and 6 copper layers of 1-oz. copper thickness.

### 8.3.3 Normalized Curves

The normalized curves in the bq500101 data sheet give engineers guidance on the Power Loss and SOA adjustments based on their application specific needs. These curves show how the power loss and SOA boundaries will adjust for a given set of systems conditions. The primary Y-axis is the normalized change in power loss and the secondary Y-axis is the change is system temperature required in order to comply with the SOA curve. The change in power loss is a multiplier for the Power Loss curve and the change in temperature is subtracted from the SOA curve.

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## System Example (continued)

### *8.3.3.1 Calculating Power Loss and SOA*

The user can estimate product loss and SOA boundaries by arithmetic means (see the Design Example below). Though the Power Loss and SOA curves in this datasheet are taken for a specific set of test conditions, the following procedure will outline the steps engineers should take to predict product performance for any set of system conditions.

#### 8.3.3.1.1 Design Example

Operating Conditions: Output Current ($I_{SW}$) = 9 A, Input Voltage ($V_{IN}$ ) = 8 V, Switching Frequency ($f_{SW}$) = 300 kHz, Output Inductor ($L_{SW}$) = 5 µH, Duty Cycle = 50%.

#### 8.3.3.1.2 Calculating Power Loss

- Typical Power Loss at 9 A = 1.78 W (Figure 3)
- Normalized Power Loss for switching frequency ≈ 1.03 (Figure 7)
- Normalized Power Loss for input voltage ≈ 0.96 (Figure 8)
- Normalized Power Loss for output inductor ≈ 1.075 (Figure 9)
- **Final calculated Power Loss = 1.78 W × 1.03 × 0.96 × 1.075 ≈ 1.89 W**

#### 8.3.3.1.3 Calculating SOA Adjustments

- SOA adjustment for switching frequency ≈ 0.20°C (Figure 7)
- SOA adjustment for input voltage ≈ –0.30°C (Figure 8)
- SOA adjustment for output inductor ≈ 0.60°C (Figure 9)
- **Final calculated SOA adjustment = 0.2 + (–0.3) + 0.6 ≈ 0.5°C**

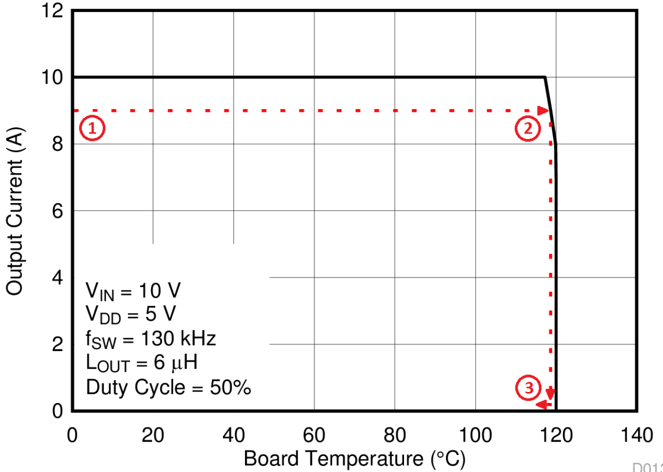


**Figure 11. Power Stage bq500101 SOA, $T_A$ = 25°C**

In the design example above, the estimated power loss of the bq500101 would increase to 1.89 W. In addition, the maximum allowable board and/or ambient temperature would have to decrease by 0.5°C. Figure 11 graphically shows how the SOA curve would be adjusted accordingly.

1. Start by drawing a horizontal line from the application current to the SOA curve.
2. Draw a vertical line from the SOA curve intercept down to the board/ambient temperature.
3. Adjust the SOA board/ambient temperature by subtracting the temperature adjustment value.

In the design example, the SOA temperature adjustment yields a reduction in allowable board/ambient temperature of 0.5°C. In the event the adjustment value is a negative number, subtracting the negative number would yield an increase in allowable board/ambient temperature.


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# 9 Layout

## 9.1 Layout Guidelines

### 9.1.1 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout will yield maximum performance in both areas. Below is a brief description on how to address each parameter.

### 9.1.2 Electrical Performance

The bq500101 has the ability to switch at voltage rates greater than 10 kV/µs. Special care must be then taken with the PCB layout design and placement of the input capacitors, inductor and switch capacitors (SW capacitors).

- The placement of the input capacitors relative to $V_{IN}$ and $P_{GND}$ pins of bq500101 device should have the highest priority during the component placement routine. It is critical to minimize these node lengths. As such, the ceramic input capacitor C1 needs to be placed as close as possible to the $V_{IN}$ and $P_{GND}$ pins (see Figure 12). Notice if there are input capacitors on both sides of the board, an appropriate amount of $V_{IN}$ and GND vias need to be added to interconnect both layers..
- The bootstrap cap $C_{BOOT}$ 0.1-µF 0603 16-V ceramic capacitor C4 in Figure 12 should be closely connected between BOOT and BOOT_R pins.
- The switching node of the inductor should be placed relatively close to the Power Stage bq500101 $V_{SW}$ pins. Minimizing the $V_{SW}$ node length between these two components will reduce the PCB conduction losses and actually reduce the switching noise level. [1]

## 9.2 Layout Example

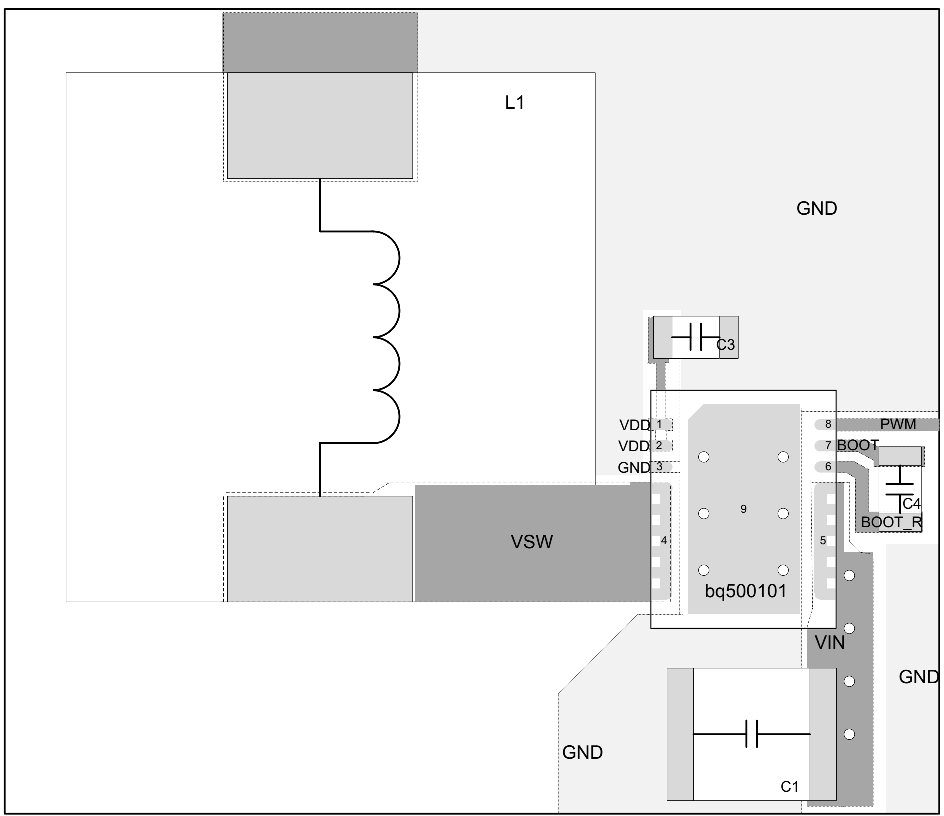


**Figure 12. Recommended PCB Layout (Top Down View)**

(1) Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

## 9.3 Thermal Considerations

The bq500101 has the ability to use the GND planes as the primary thermal path. As such, the use of thermal vias is an effective way to pull away heat from the device and into the system board. Concerns of solder voids and manufacturability problems can be addressed by the use of three basic tactics to minimize the amount of solder attach that will wick down the via barrel:

- Intentionally space out the vias from each other to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed in your design. The example in Figure 12 uses vias with a 10 mil drill hole and a 16 mil capture pad.
- Tent the opposite side of the via with solder-mask.

In the end, the number and drill size of the thermal vias should align with the end user's PCB design rules and manufacturing capabilities.


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# 10 器件和文档支持

## 10.1 商标

NexFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

## 10.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 10.3 Glossary

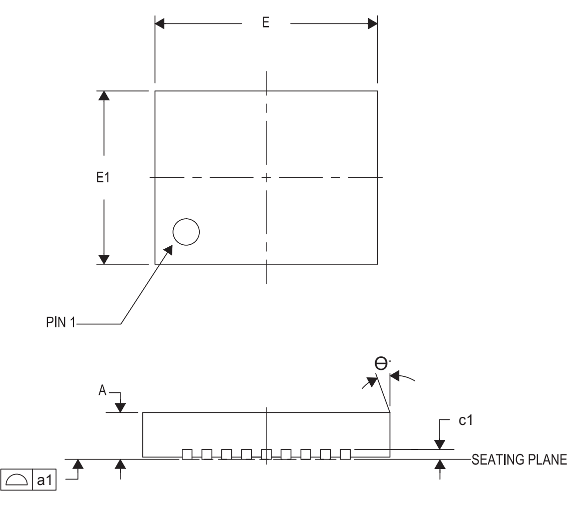
SLYZ022 — *TI Glossary*.

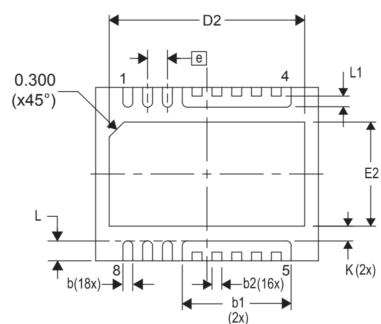
This glossary lists and explains terms, acronyms, and definitions.

## 11 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

### 11.1 机械制图




| DIM | 毫米 | | | 英寸 | | |
|---|---|---|---|---|---|---|
| | 最小值 | 标称值 | 最大值 | 最小值 | 标称值 | 最大值 |
| A | 0.800 | 0.900 | 1.000 | 0.031 | 0.035 | 0.039 |
| a1 | 0.000 | 0.000 | 0.080 | 0.000 | 0.000 | 0.003 |
| b | 0.150 | 0.200 | 0.250 | 0.006 | 0.008 | 0.010 |
| b1 | 2.000 | 2.200 | 2.400 | 0.079 | 0.087 | 0.095 |
| b2 | 0.150 | 0.200 | 0.250 | 0.006 | 0.008 | 0.010 |
| c1 | 0.150 | 0.200 | 0.250 | 0.006 | 0.008 | 0.010 |
| D2 | 3.850 | 3.950 | 4.050 | 0.152 | 0.156 | 0.160 |
| E | 4.400 | 4.500 | 4.600 | 0.173 | 0.177 | 0.181 |
| E1 | 3.400 | 3.500 | 3.600 | 0.134 | 0.138 | 0.142 |
| E2 | 2.000 | 2.100 | 2.200 | 0.079 | 0.083 | 0.087 |
| e | 0.400 典型值 | | | 0.016 典型值 | | |
| K | 0.300 典型值 | | | 0.012 典型值 | | |
| L | 0.300 | 0.400 | 0.500 | 0.012 | 0.016 | 0.020 |
| L1 | 0.180 | 0.230 | 0.280 | 0.007 | 0.009 | 0.011 |
| θ | 0.00 | — | — | 0.00 | — | — |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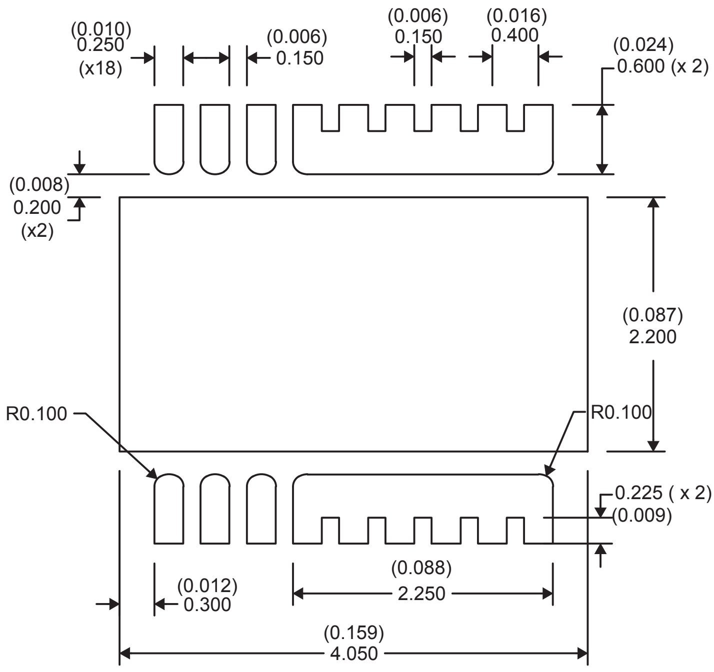
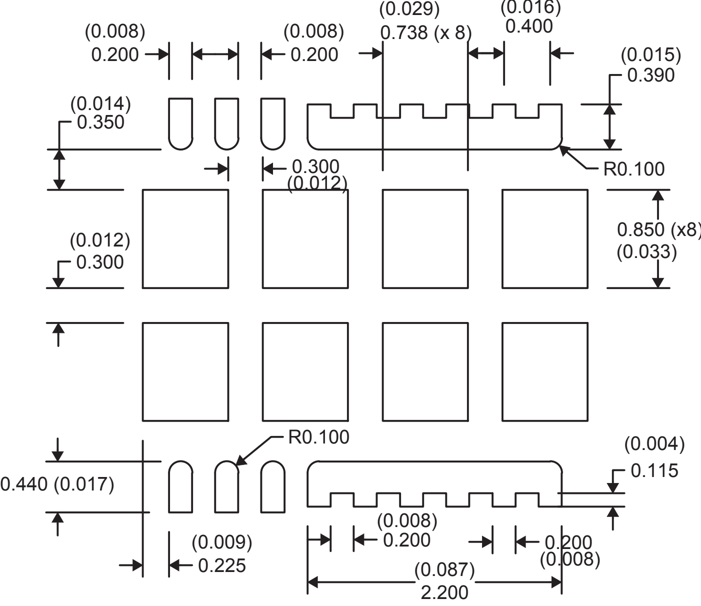
## 11.2 建议印刷电路板 (PCB) 焊盘图案




## 11.3 建议模板开口




NOTE: 尺寸单位为 mm（英寸）。
模板厚度为 100μm。

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| | 产品 | | 应用 |
|---|---|---|---|
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| 数据转换器 | www.ti.com.cn/dataconverters | 消费电子 | www.ti.com/consumer-apps |
| DLP® 产品 | www.dlp.com | 能源 | www.ti.com/energy |
| DSP - 数字信号处理器 | www.ti.com.cn/dsp | 工业应用 | www.ti.com.cn/industrial |
| 时钟和计时器 | www.ti.com.cn/clockandtimers | 医疗电子 | www.ti.com.cn/medical |
| 接口 | www.ti.com.cn/interface | 安防应用 | www.ti.com.cn/security |
| 逻辑 | www.ti.com.cn/logic | 汽车电子 | www.ti.com.cn/automotive |
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| RFID 系统 | www.ti.com.cn/rfidsys | | |
| OMAP应用处理器 | www.ti.com/omap | | |
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邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122
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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ500101DPCR | ACTIVE | VSON-CLIP | DPC | 8 | 2500 | RoHS-Exempt & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 500101 | Samples |
| BQ500101DPCT | ACTIVE | VSON-CLIP | DPC | 8 | 250 | RoHS-Exempt & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 125 | 500101 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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