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**TEXAS INSTRUMENTS**

**TPS650864**

ZHCSG44E – JUNE 2017 – REVISED DECEMBER 2022

# TPS650864 适用于 Xilinx® MPSoC 和 FPGA 的可配置多轨 PMU

## 1 特性

- 5.6V 至 21V 的宽 $V_{IN}$ 范围
- 三个采用 D-CAP2™ 拓扑的可变输出电压同步降压控制器
  - 使用外部 FET 的可扩展输出电流，支持可选电流限制
  - 在 0.41V 至 1.67V 之间以 10mV 为步长或在 1V 至 3.575V 之间以 25mV 为步长的 $I^2C$ DVS 控制
- 三个采用 DCS-Control 拓扑的可变输出电压同步降压转换器
  - 输入电压范围为 3V 至 5.5 V
  - 输出电流高达 3A
  - 在 0.41V 至 1.67V 之间以 10mV 为步长或在 0.425V 至 3.575V 之间以 25mV 为步长的 $I^2C$ DVS 控制
- 三个具有可调节输出电压的 LDO 稳压器
  - LDOA1：$I^2C$ 可选电压的范围为 1.35V 至 3.3V，输出电流可高达 200mA
  - LDOA2 和 LDOA3：$I^2C$ 可选电压的范围为 0.7V 至 1.5V，每个的输出电流可高达 600mA
- 用于 DDR 存储器终端的 VTT LDO
- 三个具有压摆率控制功能的负载开关
  - 输出电流高达 300mA，压降小于标称输入电压的 1.5%
  - 输入电压为 1.8V 时，$R_{DSON}$ < 96m Ω
- 5V 固定输出电压 LDO (LDO5)
  - 用于 SMPS 的栅极驱动器和 LDOA1 的电源
  - 可自动切换至外部 5V 降压以实现更高效率
- 内置可通过工厂 OTP 编程功能实现的灵活性和可配置性
  - 六个 GPI 引脚均可配置为启用（CTL1 至 CTL6）任意所选电压轨或使其进入睡眠模式（CTL3 和 CTL6）
  - 四个 GPO 引脚均可配置为指示任意所选轨道的电源正常
  - 漏极开路中断输出引脚
- $I^2C$ 接口支持标准模式 (100kHz)、快速模式 (400kHz) 和超快速模式 (1MHz)

## 2 应用

- 可编程逻辑控制器
- 机器视觉摄像机
- 视频监控
- 测试和测量
- 嵌入式 PC
- 运动控制
- 便携式超声波设备

## 3 说明

TPS650864 器件系列是一款单芯片电源管理 IC (PMIC)，专为 Xilinx Zynq® 多处理器片上系统 (MPSoC) 和现场可编程门阵列 (FPGA) 系列而设计。TPS650864 器件的输入电压范围为 5.6V 至 21V，支持广泛的应用（请参阅 *器件比较表*）。该器件适用于壁式供电应用或 2、3、4 节串联锂离子电池包（NVDC 或非 NVDC 电源架构）。有关 5V 输入电源的信息，请参阅 *典型应用* 部分。D-CAP2 和 DCS-Control 高频稳压器采用小型无源器件，用于减小解决方案尺寸。D-CAP2 和 DCS-Control 拓扑具有出色的瞬态响应性能，非常适用于具有快速负载开关的处理器内核和系统内存电压轨。$I^2C$ 接口可通过嵌入式控制器 (EC) 或 SoC 进行轻松控制。PMIC 的尺寸为 8mm × 8mm，采用单行 VQFN 封装，所带的散热垫可改善散热功能。

**器件信息**[1]

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TPS650864 [2] | VQFN (64) | 8.00mm x 8.00mm |

(1) 如需更多信息，请参阅 *机械、封装和可订购信息* 部分。
(2) 有关器件选项，请参阅 *器件比较表*。
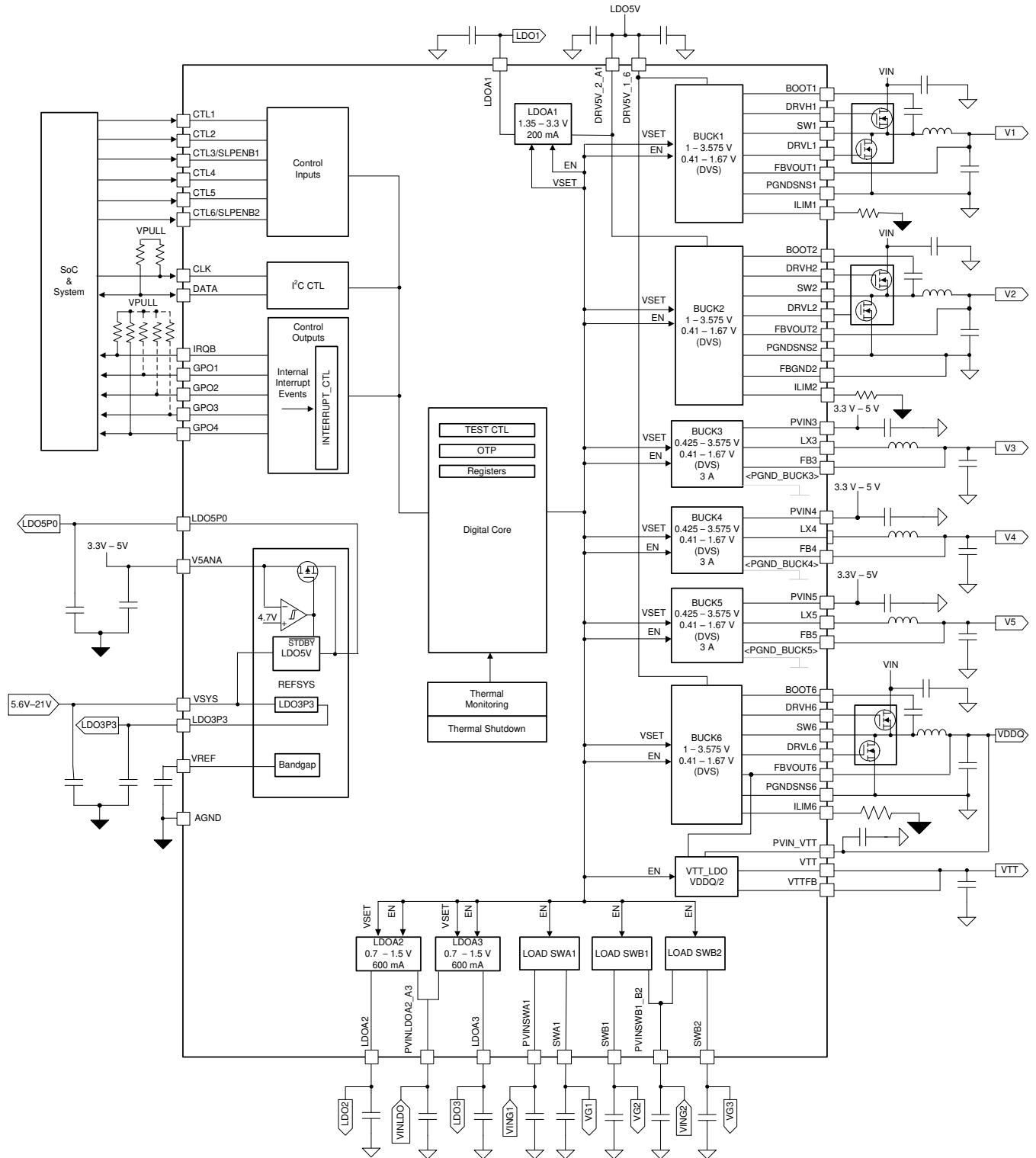
图 3-1. PMIC 功能框图

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# 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

## 5 Device Comparison Table

表 5-1 lists a brief summary of the default values for each part number stored in one-time programmable (OTP) memory. A full summary of each part number can be found in the applications section linked in the *SECTION* column. The step size is indicated by the values in parenthesis. If alternate voltages are available through pin-strapping, they are separated with a comma.

表 5-1. Default Values

| PART NUMBER | APPLICATION | BUCK1 | BUCK2 | BUCK3 | BUCK4 | BUCK5 | BUCK6 | LDOA1 | LDOA2 | LDOA3 | SECTION |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS6508640 | Xilinx Zynq Ultrascale+ ZU7 - ZU15[1] | 3.3 V (25 mV) | 0.85 V, 0.9 V (10 mV) | 1.2 V (25 mV) | 0.9 V (25 mV) | 1.8 V (25 mV) | 1.2 V, 1.35 V (10 mV) | 2.5 V | 1.5 V | 1.2 V | 节 8.3 |
| TPS65086401 | Xilinx Zynq Ultrascale+ ZU2 - ZU5[1] | 1.8 V (25 mV) | 0.85 V (10 mV) | 0.85 V (25 mV) | 3.3 V (25 mV) | 3.3 V (25 mV) | 1.5 V, 1.2 V, 1.1 V (10 mV) | 1.8 V | 1.2 V | 1.2 V | 节 8.4 |
| TPS6508641 | Xilinx Zynq Ultrascale+ ZU2 - ZU5[1] | Ext FB | 0.85 V (10 mV) | 1.1 V, 1.2 V (25 mV) | 3.3 V (25 mV) | 1.2 V (25 mV) | 1.8 V (25 mV) | 1.8 V | 1.2 V | 1.2 V | 节 8.5 |
| TPS65086470 | Xilinx Artix 7[1] | 1 V (10 mV) | 1.8 V (25 mV) | 1.2 V (25 mV) | 2.5 V (25 mV) | 3.3 V (25 mV) | 1.35 V, 1.5 V (25 mV) | 1.8 V | 0.7 V | 0.7 V | 节 8.6 |

(1)    Indicates the original intent of the part number. Parts can be used for alternate applications.

# 6 Pin Configuration and Functions

图 6-1 shows the 64-pin RSK Plastic Quad Flatpack No-Lead package.
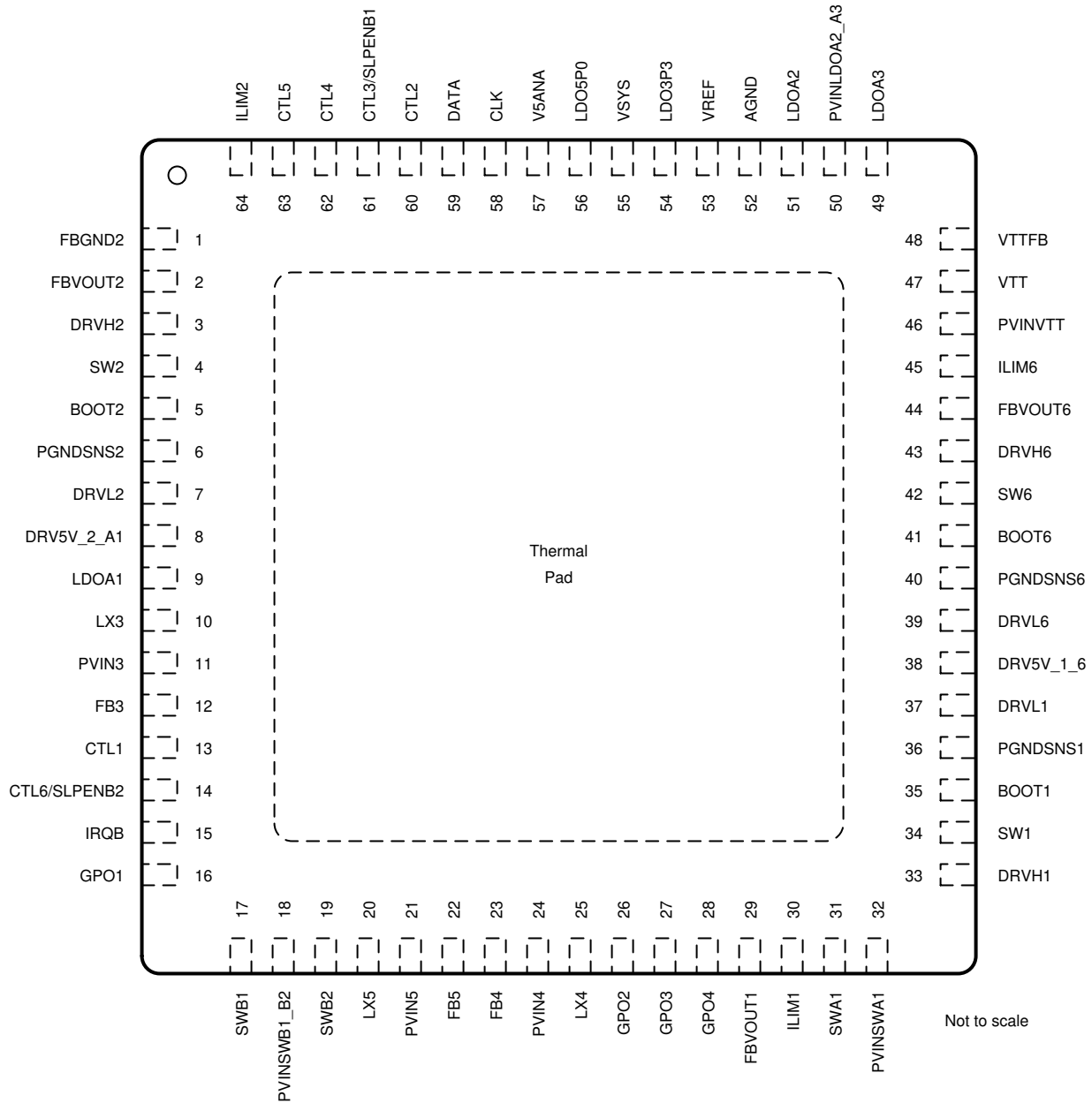


The thermal pad must be connected to the system power ground plane.

图 6-1. 64-Pin RSK VQFN With Exposed Thermal Pad (Top View)

表 6-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| **SMPS REGULATORS** | | | |
| 1 | FBGND2 | I | Remote negative feedback sense for BUCK2 controller. Connect to negative terminal of output capacitor. Connect to ground when not in use. |
| 2 | FBVOUT2 | I | Remote positive feedback sense for BUCK2 controller. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 3 | DRVH2 | O | High-side gate driver output for BUCK2 controller. Leave floating when not in use. |

Product Folder Links: *TPS650864*

表 6-1. Pin Functions (continued)

| PIN NO. | PIN NAME | I/O | DESCRIPTION |
|---|---|---|---|
| 4 | SW2 | I | Switch node connection for BUCK2 controller. Connect to ground when not in use. |
| 5 | BOOT2 | I | Bootstrap pin for BUCK2 controller. Connect a 100-nF ceramic capacitor between this pin and SW2 pin. Leave floating when not in use. |
| 6 | PGNDSNS2 | I | Power GND connection for BUCK2. Connect to ground terminal of external low-side FET. Connect to ground when not in use. |
| 7 | DRVL2 | O | Low-side gate driver output for BUCK2 controller. Leave floating when not in use. |
| 8 | DRV5V_2_A1 | I | 5-V supply to BUCK2 gate driver and LDOA1. Bypass to ground with a 2.2-µF (typical) ceramic capacitor. Shorted on board to LDO5P0 pin typically. Bypass not required if BUCK2 and LDOA1 are not in use. |
| 10 | LX3 | O | Switch node connection for BUCK3 converter. Leave floating when not in use. |
| 11 | PVIN3 | I | Power input to BUCK3 converter. Bypass to ground with a 10-µF (typical) ceramic capacitor. Bypass not required if BUCK3 is not in use. |
| 12 | FB3 | I | Remote feedback sense for BUCK3 converter. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 20 | LX5 | O | Switch node connection for BUCK5 converter. Leave floating when not in use. |
| 21 | PVIN5 | I | Power input to BUCK5 converter. Bypass to ground with a 10-µF (typical) ceramic capacitor. Bypass not required if BUCK5 is not in use. |
| 22 | FB5 | I | Remote feedback sense for BUCK5 converter. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 23 | FB4 | I | Remote feedback sense for BUCK4 converter. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 24 | PVIN4 | I | Power input to BUCK4 converter. Bypass to ground with a 10-µF (typical) ceramic capacitor. Bypass not required if BUCK4 is not in use. |
| 25 | LX4 | O | Switch node connection for BUCK4 converter. Leave floating when not in use. |
| 29 | FBVOUT1 | I | Remote feedback sense for BUCK1 controller. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 30 | ILIM1 | I | Current limit set pin for BUCK1 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET. Connect to ground when BUCK1 not in use. |
| 33 | DRVH1 | O | High-side gate driver output for BUCK1 controller. Leave floating when not in use. |
| 34 | SW1 | I | Switch node connection for BUCK1 controller. Connect to ground when not in use. |
| 35 | BOOT1 | I | Bootstrap pin for BUCK1 controller. Connect a 100-nF ceramic capacitor between this pin and SW1 pin. Leave floating when not in use. |
| 36 | PGNDSNS1 | I | Power GND connection for BUCK1. Connect to ground terminal of external low-side FET. Connect to ground when not in use. |
| 37 | DRVL1 | O | Low-side gate driver output for BUCK1 controller. Leave floating when not in use. |
| 38 | DRV5V_1_6 | I | 5-V supply to BUCK1 and BUCK6 gate drivers. Bypass to ground with a 2.2-µF (typical) ceramic capacitor. Shorted on board to LDO5P0 pin typically. Bypass not required if BUCK1 and BUCK6 are not in use. |
| 39 | DRVL6 | O | Low-side gate driver output for BUCK6 controller. Leave floating when not in use. |
| 40 | PGNDSNS6 | I | Power GND connection for BUCK6. Connect to ground terminal of external low-side FET. Connect to ground when not in use. |
| 41 | BOOT6 | I | Bootstrap pin for BUCK6 controller. Connect a 100-nF ceramic capacitor between this pin and SW6 pin. Leave floating when not in use. |
| 42 | SW6 | I | Switch node connection for BUCK6 controller. Connect to ground when not in use. |
| 43 | DRVH6 | O | High-side gate driver output for BUCK6 controller. Leave floating when not in use. |
| 44 | FBVOUT6 | I | Remote feedback sense for BUCK6 controller and reference voltage for VTT LDO regulation. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 45 | ILIM6 | I | Current limit set pin for BUCK6 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET. Connect to ground when BUCK6 not in use. |
| 64 | ILIM2 | I | Current limit set pin for BUCK2 controller. Fit a resistor from this pin to ground to set current limit of external low-side FET. Connect to ground when BUCK2 not in use. |
| **LDO AND LOAD SWITCHES** | | | |
| 9 | LDOA1 | O | LDOA1 output. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. Leave floating when not in use. |
| 17 | SWB1 | O | Output of load switch B1. Bypass to ground with a 0.1-µF (typical) ceramic capacitor. Leave floating when not in use. |
| 18 | PVINSWB1_B2 | I | Power supply to load switch B1 and B2. Bypass to ground with a 1-µF (typical) ceramic capacitor to improve transient performance. Connect to ground when not in use. |
| 19 | SWB2 | O | Output of load switch B2. Bypass to ground with a 0.1-µF (typical) ceramic capacitor. Leave floating when not in use. |
| 31 | SWA1 | O | Output of load switch A1. Bypass to ground with a 0.1-µF (typical) ceramic capacitor. Leave floating when not in use. |

Product Folder Links: TPS650864

表 6-1. Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 32 | PVINSWA1 | I | Power supply to load switch A1. Bypass to ground with a 1-µF (typical) ceramic capacitor to improve transient performance. Connect to ground when not in use. |
| 46 | PVINVTT | I | Power supply to VTT LDO. Bypass to ground with a 10-µF (minimum) ceramic capacitor. Bypass not required if VTT LDO is not in use. |
| 47 | VTT | O | Output of load VTT LDO. Bypass to ground with 2× 22-µF (minimum) ceramic capacitors. Leave floating when not in use. |
| 48 | VTTFB | I | Remote feedback sense for VTT LDO. Connect to positive terminal of output capacitor. Connect to ground when not in use. |
| 49 | LDOA3 | O | Output of LDOA3. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. Leave floating when not in use. |
| 50 | PVINLDOA2_A3 | I | Power supply to LDOA2 and LDOA3. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. Connect to ground when not in use. |
| 51 | LDOA2 | O | Output of LDOA2. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. Leave floating when not in use. |
| 54 | LDO3P3 | O | Output of 3.3-V internal LDO. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. |
| 56 | LDO5P0 | O | Output of 5-V internal LDO or an internal switch that connects this pin to V5ANA. Bypass to ground with a 4.7-µF (typical) ceramic capacitor. |
| 57 | V5ANA | I | Bias used by converters (BUCK3, BUCK4, and BUCK5) for regulation. Must be same supply as PVINx. Also has an internal load switch that connects this pin to LDO5P0 pin if 5-V is used. Bypass this pin with an optional ceramic capacitor to improve transient performance. |
| **INTERFACE** | | | |
| 13 | CTL1 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. |
| 14 | CTL6/SLPENB2 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. Alternatively, when configured to active-low sleep enable, a group of VRs chosen can be entered into (L) or out of (H) sleep state where their output voltages may be different from those in normal state. |
| 15 | IRQB | O | Open-drain output interrupt pin. Refer to 节 8.13.4, *IRQ: PMIC Interrupt Register*, for definitions. |
| 16 | GPO1 | O | General purpose output that can be configured to either open-drain or push-pull arrangement. Regardless of the configuration, the pin can be programmed either to reflect Power Good status of VRs of any choice or to be controlled by an I$^2$C register bit by the user, which then can be used as an enable signal to an external VR. |
| 26 | GPO2 | O | General purpose output that can be configured to either open-drain or push-pull arrangement. Regardless of the configuration, the pin can be programmed either to reflect Power Good status of VRs of any choice or to be controlled by an I$^2$C register bit by the user, which then can be used as an enable signal to an external VR. |
| 27 | GPO3 | O | General purpose output that can be configured to either open-drain or push-pull arrangement. Regardless of the configuration, the pin can be programmed either to reflect Power Good status of VRs of any choice or to be controlled by an I$^2$C register bit by the user, which then can be used as an enable signal to an external VR. |
| 28 | GPO4 | O | Open-drain output that can be configured to reflect Power Good status of VRs of any choice or to be controlled by an I$^2$C register bit by the user, which then can be used as an enable signal to an external VR. |
| 58 | CLK | I | I$^2$C clock |
| 59 | DATA | I/O | I$^2$C data |
| 60 | CTL2 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. |
| 61 | CTL3/SLPENB1 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. Alternatively, when configured to active-low sleep enable, a group of VRs chosen can be entered into (L) or out of (H) sleep state where their output voltages may be different from those in normal state. |
| 62 | CTL4 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. |
| 63 | CTL5 | I | Active-high VR enable pin. A group of VRs can be assigned to be enabled at assertion or disabled at deassertion of this pin. |
| **REFERENCE** | | | |
| 52 | AGND | — | Analog ground. Do not connect to the thermal pad ground on top layer. Connect to ground of VREF capacitor. |
| 53 | VREF | O | Band-gap reference output. Stabilize it by connecting a 100-nF (typical) ceramic capacitor between this pin and quiet ground. |
| 55 | VSYS | I | System voltage detection and input to internal LDOs (3.3 V and 5 V). Bypass to ground with a 1-µF (typical) ceramic capacitor. |
| **THERMAL PAD** | | | |
| — | Thermal pad (PGND) | — | Connect to PCB ground plane using multiple vias for good thermal and electrical performance. |

Product Folder Links: *TPS650864*

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

|  | MIN | MAX | UNIT |
|---|---|---|---|
| **ANALOG** | | | |
| Input voltage from battery, VSYS | ‒0.3 | 28 | V |
| PVIN3, PVIN4, PVIN5, LDO5P0, DRV5V_1_6, DRV5V_2_A1, DRVL1, DRVL2, DRVL6 | ‒0.3 | 7 | V |
| V5ANA | ‒0.3 | 6 | V |
| PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2 | ‒0.3 | 0.3 | V |
| DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6 | ‒0.3 | 34 | V |
| SW1, SW2, SW6 | ‒5[2] | 28 | V |
| LX3, LX4, LX5 | ‒2[3] | 8 | V |
| Differential voltage, BOOTx to SWx | ‒0.3 | 5.5 | V |
| VREF, LDO3P3, FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5, ILIM1, ILIM2, ILIM6, PVINVTT, VTT, VTTFB, PVINSWA1, SWA1, PVINSWB1_B2, SWB1, SWB2, LDOA1 | ‒0.3 | 3.6 | V |
| PVINLDOA2_A3, LDOA2, LDOA3 | ‒0.3 | 3.3 | V |
| **DIGITAL IO** | | | |
| DATA, CLK, GPO1-GPO3 | ‒0.3 | 3.6 | V |
| CTL1-CTL6, GPO4, IRQB | ‒0.3 | 7 | V |
| Storage temperature, $T_{stg}$ | ‒40 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient for less than 5 ns
(3) Transient for less than 20 ns

## 7.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{ESD}$ | Electrostatic discharge | Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001[1] | ±1000 | V |
| | | Charged Device Model (CDM), per JESD22-C101[2] | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **ANALOG** | | | | | |
| VSYS | | 5.6 | 13 | 21 | V |
| VREF | | −0.3 | | 1.3 | V |
| PVIN3, PVIN4, PVIN5, LDO5P0, V5ANA, DRV5V_1_6, DRV5V_2_A1 | | −0.3 | | 5.5 | V |
| PGNDSNS1, PGNDSNS2, PGNDSNS6, AGND, FBGND2 | | −0.3 | | 0.3 | V |
| DRVH1, DRVH2, DRVH6, BOOT1, BOOT2, BOOT6 | | −0.3 | | 26.5 | v |
| DRVL1, DRVL2, DRVL6 | | −0.3 | | 5.5 | V |
| SW1, SW2, SW6 | | −1 | | 21 | V |
| LX3, LX4, LX5 | | −1 | | 5.5 | V |
| FBVOUT1, FBVOUT2, FBVOUT6, FB3, FB4, FB5 | | −0.3 | | 3.6 | V |
| LDO3P3, ILIM1, ILIM2, ILIM6, LDOA1 | | −0.3 | | 3.3 | V |
| PVINVTT | | −0.3 | BUCK6 | FBVOUT6 | V |
| VTT, VTTFB | | −0.3 | | 0.5 × FBVOUT6 | V |
| PVINSWA1, SWA1, PVINSWB1_B2, SWB1, SWB2 | | −0.3 | | 3.6 | V |
| PVINLDOA2_A3 | | −0.3 | | 1.8 | V |
| LDOA2, LDOA3 | | −0.3 | | 1.5 | V |
| **DIGITAL IO** | | | | | |
| DATA, CLK, CTL1 – CTL6, GPO1 – GPO4, IRQB | | −0.3 | | 3.3 | V |
| **CHIP** | | | | | |
| Operating ambient temperature, $T_A$ | | −40 | 27 | 85 | °C |
| Operating junction temperature, $T_J$ | | −40 | 27 | 125 | °C |

## 7.4 Thermal Information

| | THERMAL METRIC[1] | TPS650864 RSK (VQFN) 64 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 25.8 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 11.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 4.4 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 4.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.7 | °C/W |

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics* application report.

## 7.5 Electrical Characteristics: Total Current Consumption

over recommended free-air temperature range and over recommended input voltage range (typical values are at $T_A$ = 25°C) (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{SD}$ | PMIC shutdown current that includes $I_Q$ for references, LDO5, LDO3P3, and digital core | $V_{SYS}$ = 13 V, all functional output rails are disabled | | 65 | | µA |

Product Folder Links: *TPS650864*

## 7.6 Electrical Characteristics: Reference and Monitoring System

over recommended free-air temperature range and over recommended input voltage range (typical values are at $T_A$ = 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **REFERENCE** | | | | | | |
| $V_{REF}$ | Band-gap reference voltage | | | 1.25 | | V |
| | Accuracy | | −0.5% | | 0.5% | |
| $C_{VREF}$ | Band-gap output capacitor | | 0.047 | 0.1 | 0.22 | μF |
| $V_{SYS\_UVLO\_5V}$ | VSYS UVLO threshold for LDO5 | $V_{SYS}$ falling | 5.24 | 5.4 | 5.56 | V |
| $V_{SYS\_UVLO\_5V\_HYS}$ | VSYS UVLO threshold hysteresis for LDO5 | $V_{SYS}$ rising above $V_{SYS\_UVLO\_5V}$ | | 200 | | mV |
| $V_{SYS\_UVLO\_3V}$ | VSYS UVLO threshold for LDO3P3 | $V_{SYS}$ falling | 3.45 | 3.6 | 3.75 | V |
| $V_{SYS\_UVLO\_3V\_HYS}$ | VSYS UVLO threshold hysteresis for LDO3P3 | $V_{SYS}$ rising above $V_{SYS\_UVLO\_3V}$ | | 150 | | mV |
| $T_{CRIT}$ | Critical threshold of die temperature | $T_J$ rising | 130 | 145 | 160 | °C |
| $T_{CRIT\_HYS}$ | Hysteresis of $T_{CRIT}$ | $T_J$ falling | | 10 | | °C |
| $T_{HOT}$ | Hot threshold of die temperature | $T_J$ rising | 110 | 115 | 120 | °C |
| $T_{HOT\_HYS}$ | Hysteresis of $T_{HOT}$ | $T_J$ falling | | 10 | | °C |
| **LDO5** | | | | | | |
| $V_{IN}$ | Input voltage at $V_{SYS}$ pin | | 5.6 | 13 | 21 | V |
| $V_{OUT}$ | DC output voltage | $I_{OUT}$ = 10 mA | 4.9 | 5 | 5.1 | V |
| $I_{OUT}$ | DC output current | | | 100 | 180 | mA |
| $I_{OCP}$ | Overcurrent protection | Measured with output shorted to ground | 200 | | | mA |
| $V_{TH\_PG}$ | Power Good assertion threshold in percentage of target $V_{OUT}$ | $V_{OUT}$ rising | | 94% | | |
| $V_{TH\_PG\_HYS}$ | Power Good deassertion hysteresis | $V_{OUT}$ rising or falling | | 4% | | |
| $I_Q$ | Quiescent current | $V_{IN}$ = 13 V, $I_{OUT}$ = 0 A | | 20 | | μA |
| $C_{OUT}$ | External output capacitance | | 2.7 | 4.7 | 10 | μF |
| **V5ANA-to-LDO5P0 LOAD SWITCH** | | | | | | |
| $R_{DSON}$ | On resistance | $V_{IN}$ = 5 V, measured from V5ANA pin to LDO5P0 pin at $I_{OUT}$ = 200 mA | | | 1 | Ω |
| $V_{TH\_PG}$ | Power Good threshold for external 5-V supply | $V_{V5ANA}$ rising | | 4.7 | | V |
| $V_{TH\_HYS\_PG}$ | Power Good threshold hysteresis for external 5-V supply | $V_{V5ANA}$ falling | | 100 | | mV |
| $I_{LKG}$ | Leakage current | Switch disabled, $V_{V5ANA}$ = 5 V, $V_{LDO5}$ = 0 V | | | 10 | μA |
| **LDO3P3** | | | | | | |
| $V_{IN}$ | Input voltage at $V_{SYS}$ pin | | 5.6 | 13 | 21 | V |
| $V_{OUT}$ | DC output voltage | $I_{OUT}$ = 10 mA | | 3.3 | | V |
| | Accuracy | $V_{IN}$ = 13 V, $I_{OUT}$ = 10 mA | −3% | | 3% | |
| $I_{OUT}$ | DC output current | | | | 40 | mA |
| $I_{OCP}$ | Overcurrent protection | Measured with output shorted to ground | 70 | | | mA |
| $V_{TH\_PG}$ | Power Good assertion threshold in percentage of target $V_{OUT}$ | $V_{OUT}$ rising | | 92% | | |
| $V_{TH\_PG\_HYS}$ | Power Good deassertion hysteresis | $V_{OUT}$ falling | | 3% | | |

## 7.6 Electrical Characteristics: Reference and Monitoring System (continued)

over recommended free-air temperature range and over recommended input voltage range (typical values are at $T_A$ = 25°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_Q$ | Quiescent current | $V_{IN}$ = 13 V, $I_{OUT}$ = 0 A | | 20 | | µA |
| $C_{OUT}$ | External output capacitance | | 2.2 | 4.7 | 10 | µF |

## 7.7 Electrical Characteristics: Buck Controllers

over recommended input voltage range, $T_A$ = – 40°C to +85°C and $T_A$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BUCK1, BUCK2, BUCK6** | | | | | | |
| $V_{IN}$ | Power input voltage for external HSD FET | | 5.6 | 13 | 21 | V |
| $V_{OUT}$ | DC output voltage VID range and options | VID step size = 10 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111 | 0.41 | See 节 5 | 1.67 | V |
| | | VID step size = 25 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111 | 1[(1)] | See 节 5 | 3.575 | V |
| | DC output voltage accuracy | $V_{OUT}$ = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, $I_{OUT}$ = 100 mA to 7 A | – 2% | | 2% | |
| | Total output voltage accuracy (DC + ripple) in DCM | $I_{OUT}$ = 10 mA, $V_{OUT}$ ⩽ 1 V | – 30 | | 40 | mV |
| $V_{FB\_EXT\_BUCK1}$ | Feedback regulation voltage | Applies only to the Buck1 Controller if programmed for external feedback voltage adjustability | 384 | 400 | 416 | mV |
| $I_{FB\_LKG\_BUCK1}$ | Feedback pin leakage current | Applies only to the Buck1 Controller if programmed for external feedback voltage adjustability | | | 65 | nA |
| $SR(V_{OUT})$ | Output DVS slew rate | VID step size = 10 mV | 2.5 | 3.125 | | mV/µs |
| | | VID step size = 25 mV | 3.125 | 4 | | |
| $I_{LIM\_LSD}$ | Low-side output valley current limit accuracy (programmed by external resistor $R_{LIM}$) | | – 15% | | 15% | |
| $I_{LIMREF}$ | Source current out of ILIM1 pin | T = 25°C | 45 | 50 | 55 | µA |
| $V_{LIM}$ | Voltage at ILIM1 pin | $V_{LIM}$ = $R_{LIM}$ × $I_{LIMREF}$ | 0.2 | | 2.25 | V |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | $V_{OUT}$ = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, $I_{OUT}$ = 7 A | – 0.5% | | 0.5% | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | $V_{IN}$ = 13 V, $V_{OUT}$ = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, $I_{OUT}$ = 0 A to 7 A, referenced to $V_{OUT}$ at $I_{OUT}$ = $I_{OUT\_MAX}$ | 0% | | 1% | |
| $V_{TH\_PG}$ | Power Good deassertion threshold in percentage of target $V_{OUT}$ | $V_{OUT}$ rising | 105.5% | 108% | 110.5% | |
| | | $V_{OUT}$ falling | 89.5% | 92% | 94.5% | |
| $R_{DSON\_DRVH}$ | Driver DRVH resistance | Source, IDRVH = – 50 mA | | 3 | | Ω |
| | | Sink, IDRVH = 50 mA | | 2 | | Ω |
| $R_{DSON\_DRVL}$ | Driver DRVL resistance | Source, IDRVL = – 50 mA | | 3 | | Ω |
| | | Sink, IDRVL = 50 mA | | 0.4 | | Ω |
| $R_{DIS}$ | Output auto-discharge resistance | BUCKx_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | BUCKx_DISCHG[1:0] = 10 | | 200 | | Ω |
| | | BUCKx_DISCHG[1:0] = 11 | | 500 | | Ω |

Product Folder Links: *TPS650864*

## 7.7 Electrical Characteristics: Buck Controllers (continued)

over recommended input voltage range, $T_A$ = – 40°C to +85°C and $T_A$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $C_{BOOT}$ | Bootstrap capacitance | | | 100 | | nF |
| $R_{ON\_BOOT}$ | Bootstrap switch ON resistance | | | | 20 | Ω |

(1)   BUCKx_VID[6:0] = 0000001 – 0011000

## 7.8 Electrical Characteristics: Synchronous Buck Converters

over recommended input voltage range, $T_A$ = – 40°C to +85°C and $T_A$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BUCK3, BUCK4, BUCK5** | | | | | | |
| $V_{IN}$ | Power input voltage | | 3.0 | | 5.5 | V |
| $V_{OUT}$ | DC output voltage VID range and options | VID step size = 10 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111 | 0.41 | See #5 | 1.67 | V |
| | | VID step size = 25 mV, BUCKx_VID[6:0] progresses from 0000001 to 1111111 | 0.425 | See #5 | 3.575 | |
| | DC output voltage accuracy | $V_{IN}$ = 5.0 V, $V_{OUT}$ = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, $I_{OUT}$ = 1.5 A | – 2% | | 2% | |
| | | $V_{IN}$ = 3.3 V, $V_{OUT}$ = 1, 1.2, 1.35, 1.5, 1.8 V, $I_{OUT}$ = 1.5 A | – 2% | | 2% | |
| | | $V_{IN}$ = 5.0 V, $V_{OUT}$ = 1, 1.2, 1.35, 1.5, 1.8 V, 2.5, 3.3 V, $I_{OUT}$ = 100 mA | – 2.5% | | 2.5% | |
| | | $V_{IN}$ = 3.3 V, $V_{OUT}$ = 1, 1.2, 1.35, 1.5, 1.8 V, $I_{OUT}$ = 100 mA | – 2.5% | | 2.5% | |
| $V_{DCM}$ | Total output voltage accuracy (DC + ripple) in DCM | $V_{IN}$ = 5.0 V, $I_{OUT}$ = 10 mA, $V_{OUT}$ ⩽ 1 V | – 30 | | 40 | mV |
| SR($V_{OUT}$) | Output DVS slew rate | VID step size = 10 mV | 2.5 | 3.125 | | mV/µs |
| | | VID step size = 25 mV | 3.125 | 4 | | |
| $I_{OUT}$ | Continuous DC output current | | | | 3 | A |
| $I_{IND\_LIM}$ | HSD FET current limit | | 4.3 | | 7 | A |
| $I_Q$ | Quiescent current | $V_{IN}$ = 5 V, $V_{OUT}$ = 1 V, BUCKx_MODE = 0b | | 35 | | µA |
| Δ $V_{OUT}$/ Δ $V_{IN}$ | Line regulation | $V_{OUT}$ = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, $I_{OUT}$ = 1.5 A | – 0.5% | | 0.5% | |
| Δ $V_{OUT}$/ Δ $I_{OUT}$ | Load regulation | $V_{IN}$ = 5 V, $V_{OUT}$ = 1, 1.2, 1.35, 1.5, 1.8, 2.5, 3.3 V, $I_{OUT}$ = 0 A to 3 A, referenced to $V_{OUT}$ at $I_{OUT}$ = 1.5 A | – 0.2% | | 2% | |
| $V_{TH\_PG}$ | Power Good deassertion threshold in percentage of target $V_{OUT}$ | $V_{OUT}$ rising | | 108% | | |
| | | $V_{OUT}$ falling | | 92% | | |
| $V_{TH\_HYS\_PG}$ | Power Good reassertion hysteresis entering back into $V_{TH\_PG}$ | $V_{OUT}$ rising or falling | | 3% | | |

## 7.8 Electrical Characteristics: Synchronous Buck Converters (continued)

over recommended input voltage range, $T_A$ = – 40°C to +85°C and $T_A$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{DIS}$ | Output auto-discharge resistance | BUCKx_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | BUCKx_DISCHG[1:0] = 10 | | 200 | | |
| | | BUCKx_DISCHG[1:0] = 11 | | 500 | | |

## 7.9 Electrical Characteristics: LDOs

over recommended input voltage range, $T_A$ = – 40°C to +85°C and $T_A$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LDOA1** | | | | | | |
| $V_{IN}$ | Input voltage | | 4.5 | 5 | 5.5 | V |
| $V_{OUT}$ | DC output voltage | Set by LDOA1_VID[3:0] | 1.35 | See 节 5 | 3.3 | V |
| | Accuracy | $I_{OUT}$ = 0 to 200 mA | – 2% | | 2% | V |
| $I_{OUT}$ | DC output current | | | | 200 | mA |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | $I_{OUT}$ = 40 mA | – 0.5% | | 0.5% | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | $I_{OUT}$ = 10 mA to 200 mA | – 2% | | 2% | |
| $I_{OCP}$ | Overcurrent protection | $V_{IN}$ = 5 V, Measured with output shorted to ground | 500 | | | mA |
| $V_{TH\_PG}$ | Power Good deassertion threshold in percentage of target $V_{OUT}$ | $V_{OUT}$ rising | | 108% | | |
| | | $V_{OUT}$ falling | | 92% | | |
| $t_{STARTUP}$ | Start-up time | Measured from EN = H to reach 95% of final value, $C_{OUT}$ = 4.7 µF | | | 500 | µs |
| $I_Q$ | Quiescent current | $I_{OUT}$ = 0 A | | 23 | | µA |
| $C_{OUT}$ | External output capacitance | | 2.7 | 4.7 | 10 | µF |
| | ESR | | | | 100 | mΩ |
| $R_{DIS}$ | Output auto-discharge resistance | LDOA1_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | LDOA1_DISCHG[1:0] = 10 | | 190 | | Ω |
| | | LDOA1_DISCHG[1:0] = 11 | | 450 | | Ω |
| **LDOA2 and LDOA3** | | | | | | |
| $V_{IN}$ | Power input voltage | | $V_{OUT}$ + $V_{DROP}$ [1] | 1.8 | 1.98 | V |
| $V_{OUT}$ | LDOA2 DC output voltage | Set by LDOA2_VID[3:0] | 0.7 | See 节 5 | 1.5 | V |
| | LDOA3 DC output voltage | Set by LDOA3_VID[3:0] | 0.7 | See 节 5 | 1.5 | V |
| | DC output voltage accuracy | $I_{OUT}$ = 0 to 600 mA | – 2% | | 3% | |
| $I_{OUT}$ | DC output current | | | | 600 | mA |
| $V_{DROP}$ | Dropout voltage | $V_{OUT}$ = 0.99 × $V_{OUT\_NOM}$, $I_{OUT}$ = 600 mA | | | 350 | mV |
| $\Delta V_{OUT}/\Delta V_{IN}$ | Line regulation | $I_{OUT}$ = 300 mA | – 0.5% | | 0.5% | |
| $\Delta V_{OUT}/\Delta I_{OUT}$ | Load regulation | $I_{OUT}$ = 10 mA to 600 mA | – 2% | | 2% | |
| $I_{OCP}$ | Overcurrent protection | Measured with output shorted to ground | 0.65 | 1.25 | | A |
| $V_{TH\_PG}$ | Power Good assertion threshold in percentage of target $V_{OUT}$ | $V_{OUT}$ rising | | 108% | | |
| | | $V_{OUT}$ falling | | 92% | | |
| $t_{STARTUP}$ | Start-up time | Measured from EN = H to reach 95% of final value, $C_{OUT}$ = 4.7 µF | | | 500 | µs |

## 7.9 Electrical Characteristics: LDOs (continued)

over recommended input voltage range, $T_A$ = – 40°C to +85°C and $T_A$ = 25°C for typical values (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_Q$ | Quiescent current | $I_{OUT}$ = 0 A | | 20 | | µA |
| PSRR | Power supply rejection ratio | f = 1 kHz, $V_{IN}$ = 1.8 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 300 mA, $C_{OUT}$ = 2.2 µF – 4.7 µF | | 48 | | dB |
| | | f = 10 kHz, $V_{IN}$ = 1.8 V, $V_{OUT}$ = 1.2 V, $I_{OUT}$ = 300 mA, $C_{OUT}$ = 2.2 µF – 4.7 µF | | 30 | | dB |
| $C_{OUT}$ | External output capacitance | | 2.2 | 4.7 | 10 | µF |
| | ESR | | | | 100 | m$\Omega$ |
| $R_{DIS}$ | Output auto-discharge resistance | LDOA[2,3]_DISCHG[1:0] = 01 | | 80 | | $\Omega$ |
| | | LDOA[2,3]_DISCHG[1:0] = 10 | | 180 | | |
| | | LDOA[2,3]_DISCHG[1:0] = 11 | | 475 | | |
| **VTT LDO** | | | | | | |
| $V_{IN}$ | Power input voltage | | | 1.2 | 3.3 | V |
| $V_{OUT}$ | DC output voltage | $V_{IN}$ = 1.2 V, Measured at VTTFB pin | | $V_{IN}$ / 2 | | V |
| | DC output voltage accuracy | Relative to $V_{IN}$ / 2, $I_{OUT} \leqslant$ 10 mA, 1.1 V $\leqslant V_{IN} \leqslant$ 1.35 V | – 10 | | 10 | mV |
| | | Relative to $V_{IN}$ / 2, $I_{OUT} \leqslant$ 500 mA, 1.1 V $\leqslant V_{IN} \leqslant$ 1.35 V | – 25 | | 25 | |
| $I_{OUT}$ | DC Output Current (Rms Value Over Operation) | 1.1 V $\leqslant V_{IN} \leqslant$ 1.5 V | – 500 | 0 | 500 | mA |
| | Pulsed Current (Duty Cycle Limited to Remain Below DC Rms Specification) | source(+) and sink(–): $I_{OCP}$ = 0.95 A, 1.1 V $\leqslant V_{IN} \leqslant$ 1.5 V | – 500 | | 500 | mA |
| | | source(+) and sink(–): $I_{OCP}$ = 1.8 A, 1.1 V $\leqslant V_{IN} \leqslant$ 1.5 V | – 1800 | | 1800 | |
| $\triangle V_{OUT}$/ $\triangle I_{OUT}$ | Load regulation | Relative to $V_{IN}$ / 2, $I_{OUT} \leqslant$ 10 mA, 1.1 V $\leqslant V_{IN} \leqslant$ 1.5 V | – 10 | | 10 | mV |
| | | Relative to $V_{IN}$ / 2, $I_{OUT} \leqslant$ 500 mA, 1.1 V $\leqslant V_{IN} \leqslant$ 1.5 V | – 20 | | 20 | |
| | | Relative to $V_{IN}$ / 2, $I_{OUT} \leqslant$ 1200 mA, 1.1 V $\leqslant V_{IN} \leqslant$ 1.5 V | – 30 | | 30 | |
| | | Relative to $V_{IN}$ / 2, $I_{OUT} \leqslant$ 1800 mA, 1.1 V $\leqslant V_{IN} \leqslant$ 1.5 V | – 40 | | 40 | |
| $\triangle V_{OUT\_TR}$ | Load transient regulation | DC + AC at sense point, 1.1 V $\leqslant V_{IN} \leqslant$ 1.5 V, ($I_{OUT}$ = 0 to 350 mA and 350 mA to 0) AND (0 to – 350 mA and – 350 mA to 0) with 1 µs of rise and fall time $C_{OUT}$ = 40 µF | – 5% | | 5% | |
| $I_{OCP}$ | Overcurrent protection | Measured with output shorted to ground: OTPs with VTT $I_{LIM}$ = 0.95 A | | 0.95 | | A |
| | | Measured with output shorted to ground: OTPs with VTT $I_{LIM}$ = 1.8 A | | 1.8 | | |
| $V_{TH\_PG}$ | Power Good deassertion threshold in percentage of target $V_{OUT}$ | $V_{OUT}$ rising | | 110% | | |
| | | $V_{OUT}$ falling | | 95% | | |
| $V_{TH\_HYS\_PG}$ | Power Good reassertion hysteresis entering back into $V_{TH\_PG}$ | | | 5% | | |
| $I_Q$ | Total ground current | $V_{IN}$ = 1.2 V, $I_{OUT}$ = 0 A | | | 240 | µA |

Product Folder Links: TPS650864

## 7.9 Electrical Characteristics: LDOs (continued)

over recommended input voltage range, $T_A = -40°C$ to $+85°C$ and $T_A = 25°C$ for typical values (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{LKG}$ | OFF leakage current | $V_{IN} = 1.2$ V, disabled | | | 1 | µA |
| $C_{IN}$ | External input capacitance | | | 10 | | µF |
| $C_{OUT}$ | External output capacitance | | | 35 | | µF |
| $R_{DIS}$ | Output auto-discharge resistance | VTT_DISCHG = 0 | | 1000 | | kΩ |
| | | VTT_DISCHG = 1 | 60 | 80 | 100 | Ω |

(1)     The minimum value must be equal to or greater than 1.62 V.

## 7.10 Electrical Characteristics: Load Switches

over operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SWA1** | | | | | | |
| $V_{IN}$ | Input voltage range | | 0.5 | | 3.3 | V |
| $I_{OUT}$ | DC output current | | | | 300 | mA |
| $R_{DSON}$ | ON resistance | $V_{IN} = 1.8$ V, measured from PVINSWA1 pin to SWA1 pin at $I_{OUT} = I_{OUT(MAX)}$ | | 60 | 93 | mΩ |
| | | $V_{IN} = 3.3$ V, measured from PVINSWA1 pin to SWA1 pin at $I_{OUT} = I_{OUT(MAX)}$ | | 100 | 165 | |
| $V_{TH\_PG}$ | Power Good deassertion threshold in percentage of target $V_{OUT}$ | $V_{OUT}$ rising | | 108% | | |
| | | $V_{OUT}$ falling | | 92% | | |
| $V_{TH\_HYS\_PG}$ | Power Good reassertion hysteresis entering back into $V_{TH\_PG}$ | $V_{OUT}$ rising or falling | | 2% | | |
| $I_{INRUSH}$ | Inrush current upon turnon | $V_{IN} = 3.3$ V, $C_{OUT} = 0.1$ µF | | | 10 | mA |
| $I_Q$ | Quiescent current | $V_{IN} = 3.3$ V, $I_{OUT} = 0$ A | | 10.5 | | µA |
| | | $V_{IN} = 1.8$ V, $I_{OUT} = 0$ A | | 9 | | |
| $I_{LKG}$ | Leakage current | Switch disabled, $V_{IN} = 1.8$ V | | 7 | 370 | nA |
| | | Switch disabled, $V_{IN} = 3.3$ V | | 10 | 900 | |
| $C_{OUT}$ | External output capacitance | | | 0.1 | | µF |
| $R_{DIS}$ | Output auto-discharge resistance | SWA1_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | SWA1_DISCHG[1:0] = 10 | | 200 | | |
| | | SWA1_DISCHG[1:0] = 11 | | 500 | | |
| **SWB1, SWB2, SWB1_2** | | | | | | |
| $V_{IN}$ | Input voltage range | | 0.5 | | 3.3 | V |
| $I_{OUT}$ | DC current per output | | | | 400 | mA |
| $R_{DSON}$ | ON resistance per output | $V_{IN} = 1.8$ V, measured from PVINSWB1_B2 pin to SWBx pin at $I_{OUT} = I_{OUT(MAX)}$, per output switch | | 68 | 92 | mΩ |
| | | $V_{IN} = 3.3$ V, measured from PVINSWB1_B2 pin to SWBx pin at $I_{OUT} = I_{OUT(MAX)}$, per output switch | | 75 | 125 | mΩ |
| $V_{TH\_PG}$ | Power Good deassertion threshold in percentage of target $V_{OUT}$ | $V_{OUT}$ rising | | 108% | | |
| | | $V_{OUT}$ falling | | 92% | | |
| $V_{TH\_HYS\_PG}$ | Power Good reassertion hysteresis entering back into $V_{TH\_PG}$ | $V_{OUT}$ rising or falling | | 2% | | |
| $I_{INRUSH}$ | Inrush current upon turning on | $V_{IN} = 3.3$ V, $C_{OUT} = 0.1$ µF | | | 10 | mA |
| $I_Q$ | Quiescent current | $V_{IN} = 3.3$ V, $I_{OUT} = 0$ A | | 10.5 | | µA |
| | | $V_{IN} = 1.8$ V, $I_{OUT} = 0$ A | | 9 | | |

Product Folder Links: *TPS650864*

## 7.10 Electrical Characteristics: Load Switches (continued)

over operating free-air temperature range (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{LKG}$ | Leakage current | Switch disabled, $V_{IN}$ = 1.8 V | | 7 | 460 | nA |
| | | Switch disabled, $V_{IN}$ = 3.3 V | | 10 | 1150 | |
| $C_{OUT}$ | External output capacitance | | | 0.1 | | µF |
| $R_{DIS}$ | Output auto-discharge resistance | SWBx_DISCHG[1:0] = 01 | | 100 | | Ω |
| | | SWBx_DISCHG[1:0] = 10 | | 200 | | |
| | | SWBx_DISCHG[1:0] = 11 | | 500 | | |

## 7.11 Digital Signals: I²C Interface

over recommended free-air temperature range and over recommended input voltage range (typical values are at $T_A$ = 25°C) (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Low-level output voltage | $V_{PULL\_UP}$ = 1.8 V | | | 0.4 | V |
| $V_{IH}$ | High-level input voltage | | 1.2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.4 | V |
| $I_{LKG}$ | Leakage current | $V_{PULL\_UP}$ = 1.8 V | | 0.01 | 0.3 | µA |
| $R_{PULL-UP}$ | Pullup resistance | Standard mode | | | 8.5 | kΩ |
| | | Fast mode | | | 2.5 | |
| | | Fast mode plus | | | 1 | |
| $C_{OUT}$ | Total load capacitance per pin | | | | 50 | pF |

## 7.12 Digital Input Signals (CTLx)

over recommended free-air temperature range and over recommended input voltage range (typical values are at $T_A$ = 25°C) (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 0.85 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.4 | V |

## 7.13 Digital Output Signals (IRQB, GPOx)

Over recommended free-air temperature range and over recommended input voltage range (typical values are at $T_A$ = 25°C) (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ < 2 mA | | | 0.4 | V |
| $I_{LKG}$ | Leakage current | $V_{PULL\_UP}$ = 1.8 V | | | 0.35 | µA |

## 7.14 Timing Requirements

over recommended free-air temperature range and over recommended input voltage range (typical values are at $T_A$ = 25°C) (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **I²C INTERFACE** | | | | | |
| $f_{CLK}$ | Clock frequency (standard mode) | | | 100 | kHz |
| | Clock frequency (fast mode) | | | 400 | kHz |
| | Clock frequency (fast mode plus) | | | 1000 | kHz |
| $t_r$ | Rise time (standard mode) | | | 1000 | ns |
| | Rise time (fast mode) | | | 300 | ns |
| | Rise time (fast mode plus) | | | 120 | ns |

Product Folder Links: *TPS650864*

over recommended free-air temperature range and over recommended input voltage range (typical values are at $T_A = 25°C$) (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_f$ | Rise time (standard mode) | | | 300 | ns |
| | Rise time (fast mode) | | | 300 | ns |
| | Rise time (fast mode plus) | | | 120 | ns |

## 7.15 Switching Characteristics

over operating free-air temperature range and over recommended input voltage range (typical values are at $T_A = 25°C$) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **BUCK CONTROLLERS** | | | | | | |
| $t_{PG}$ | Total turnon time | Measured from enable going high to when output reaches 90% of target value. | | 550 | 850 | µs |
| $T_{ON,MIN}$ | Minimum on-time of DRVH | | | 50 | | ns |
| $T_{DEAD}$ | Driver dead-time | DRVH off to DRVL on | | 15 | | ns |
| | | DRVL off to DRVH on | | 30 | | ns |
| $f_{SW}$ | Switching frequency | Continuous-conduction mode, $V_{IN} = 13$ V, $V_{OUT} \geqslant 1$ V | | 1000 | | kHz |
| **BUCK CONVERTERS** | | | | | | |
| $t_{PG}$ | Total turnon time | Measured from enable going high to when output reaches 90% of target value. | | 250 | 1000 | µs |
| $f_{SW}$ | Switching frequency | Continuous-conduction mode | | See 图 7-10 | | MHz |
| **LDOAx** | | | | | | |
| $t_{STARTUP}$ | Start-up time | Measured from enable going high to when output reaches 95% of final value, $V_{OUT} = 1.2$ V, $C_{OUT} = 4.7$ µF | | 180 | | µs |
| **VTT LDO** | | | | | | |
| $t_{STARTUP}$ | Start-up time | Measured from enable going high to PG assertion, $V_{OUT} = 0.675$ V, $C_{OUT} = 40$ µF | | 22 | | µs |
| **SWA1** | | | | | | |
| $t_{TURN-ON}$ | Turnon time | Measured from enable going high to reach 95% of final value, $V_{IN} = 3.3$ V, $C_{OUT} = 0.1$ µF | | 0.85 | | ms |
| | | Measured from enable going high to reach 95% of final value, $V_{IN} = 1.8$ V, $C_{OUT} = 0.1$ µF | | 0.63 | | ms |
| **SWB1_2** | | | | | | |
| $t_{TURN-ON}$ | Turnon time | Measured from enable going high to reach 95% of final value, $V_{IN} = 3.3$ V, $C_{OUT} = 0.1$ µF | | 1.1 | | ms |
| | | Measured from enable going high to reach 95% of final value, $V_{IN} = 1.8$ V, $C_{OUT} = 0.1$ µF | | 0.82 | | ms |

Product Folder Links: *TPS650864*

## 7.16 Typical Characteristics

Measurements are taken at 25°C.
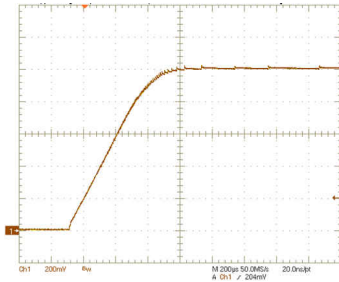


FET = CSD87588N      L = PIMB061H-R22ms
BUCK2_MODE = 0b      $C_{OUT}$ = 2 × 150 µF + 1 × 22 µF

**图 7-1. Example BUCK2 Controller Start-Up**
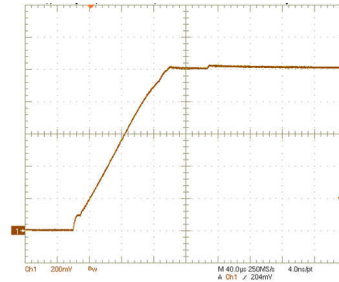


BUCK3_MODE = 0b      L = PIFE32251B-R47ms
     $C_{OUT}$ = 4 × 22 µF

**图 7-2. Example BUCK3 Converter Start-Up**
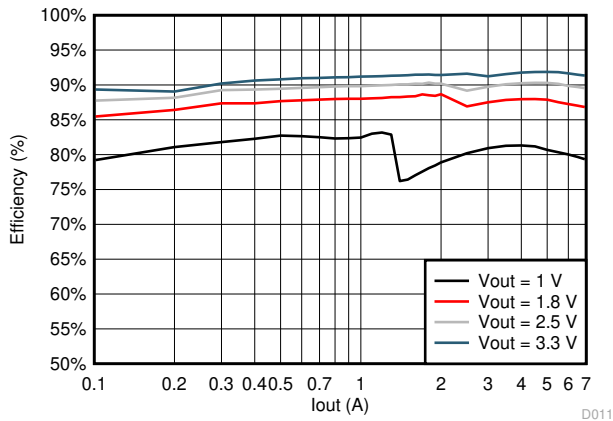


FET = CSD87381P      L = PIMB061H-R47ms
BUCK1_MODE = 0b

**图 7-3. Example BUCK1 Efficiency at $V_{IN}$ = 13 V**
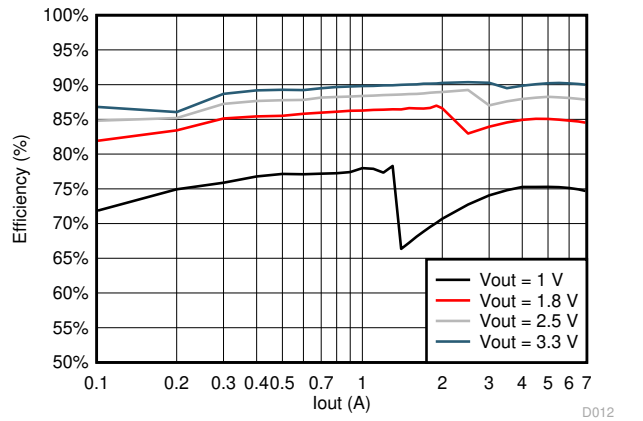


FET = CSD87381P      L = PIMB061H-R47ms
BUCK1_MODE = 0b

**图 7-4. Example BUCK1 Efficiency at $V_{IN}$ = 18 V**
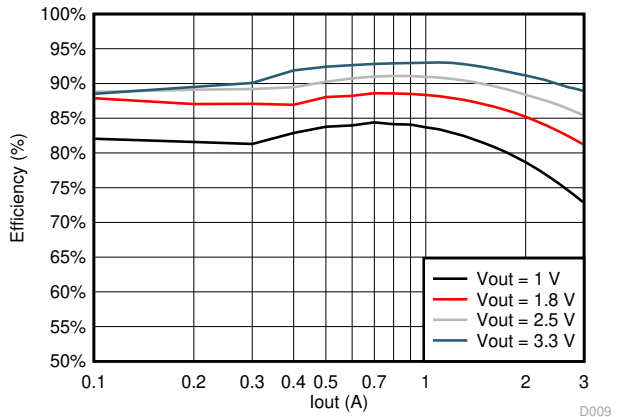


BUCK3_MODE = 0b      L = PIFE32251B-R47ms

**图 7-5. Example BUCK3 Efficiency at $V_{IN}$ = 5 V**
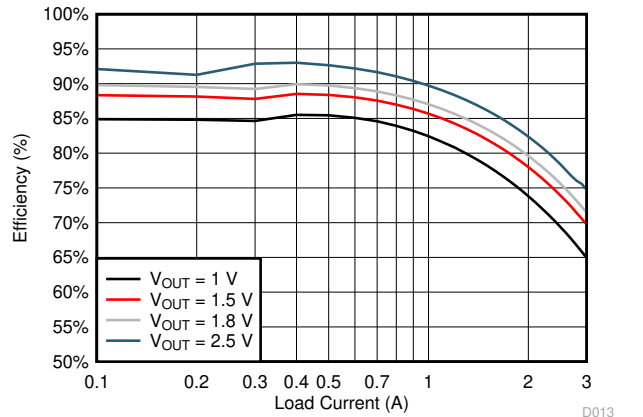


BUCK3_MODE = 0b      L = PIFE32251B-R47ms

**图 7-6. Example BUCK3 Efficiency at $V_{IN}$ = 3.3 V**

## 7.16 Typical Characteristics (continued)

Measurements are taken at 25°C.



L = PIFE32251B-R47ms
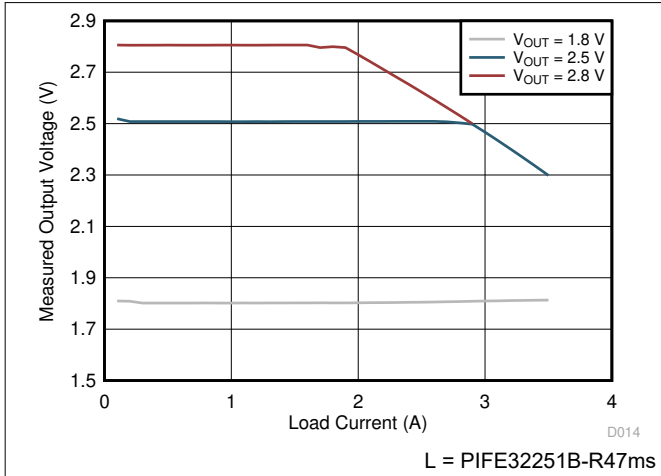
**图 7-7. Converter Load Current Limitations with V_IN = 3.3 V**



FBVOUT6 = PVINVTT = 1.35 V
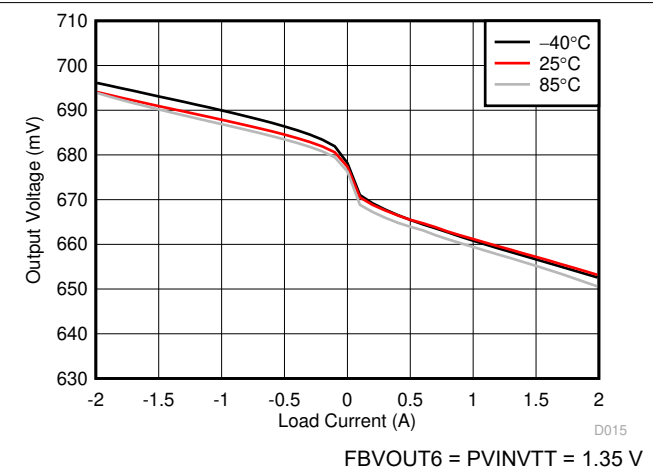
**图 7-8. VTT LDO Regulation**



L = PIFE32251B-R47ms
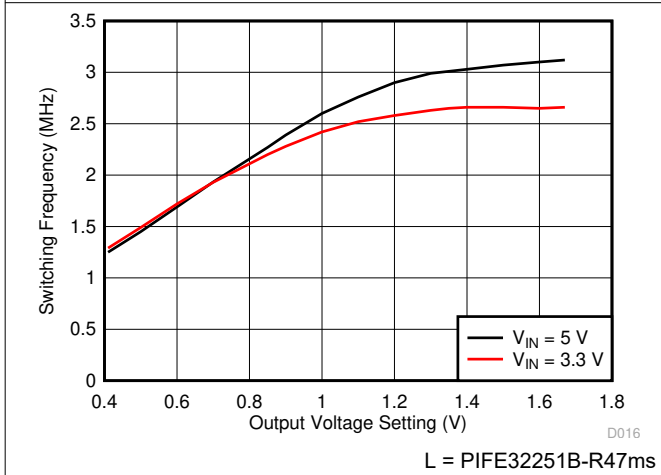
**图 7-9. Converter Switching Frequency (10-mV Step Size)**



L = PIFE32251B-R47ms
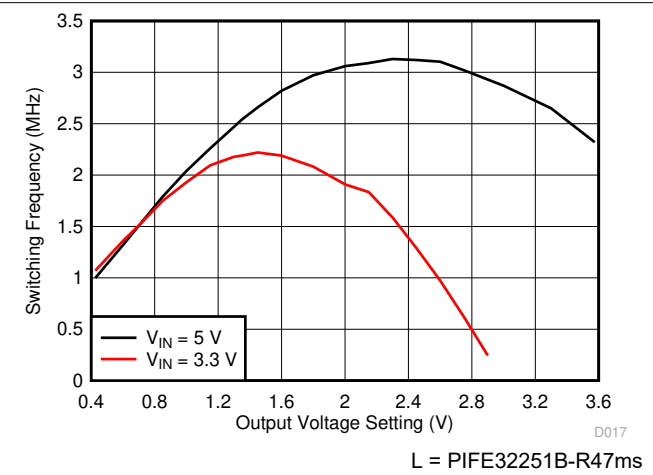
**图 7-10. Converter Switching Frequency (25-mV Step Size)**

Product Folder Links: *TPS650864*

# 8 Detailed Description

## 8.1 Overview

The TPS650864 power-management integrated circuit (PMIC) provides a highly flexible and configurable power solution that can power a wide array of processors along with DDR3/DDR4 memory and other peripherals. Integrated in the PMIC are three step-down controllers (BUCK1, BUCK2, and BUCK6), three step-down converters (BUCK3, BUCK4, and BUCK5), a sink or source LDO (VTT LDO), three low-voltage $V_{IN}$ LDOs (LDOA1 ‒ LDOA3), and three load switches (SWA1, SWB1, and SWB2). With on-chip one-time programmable (OTP) memory, configuration of each rail for default output value, power-up sequence, fault handling, and Power Good mapping into a GPO pin are all conveniently flexible. All VRs have a built-in discharge resistor, and the value can be changed using the DISCHCNT1 ‒ DISCHCNT3 and LDOA1_SWB2_CTRL registers. When enabling a VR, the PMIC automatically disconnects the discharge resistor for that rail without any I2C command. 表 8-1 lists the key characteristics of the voltage rails.

表 8-1. Summary of Voltage Regulators

| RAIL | TYPE | INPUT VOLTAGE (V) | | OUTPUT VOLTAGE RANGE (V) | | | CURRENT (mA) |
|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | TYP | MAX | |
| BUCK1 | Step-down controller | 4.5 | 21 | 0.41 | See 表 5 | 3.575 | scalable |
| BUCK2 | Step-down controller | 4.5 | 21 | 0.41 | See 表 5 | 3.575 | scalable |
| BUCK3 | Step-down converter | 3 | 5.5 | 0.41 | See 表 5 | 3.575 | 3000 |
| BUCK4 | Step-down Converter | 3 | 5.5 | 0.41 | See 表 5 | 3.575 | 3000 |
| BUCK5 | Step-down converter | 3 | 5.5 | 0.41 | See 表 5 | 3.575 | 3000 |
| BUCK6 | Step-down controller | 4.5 | 21 | 0.41 | See 表 5 | 3.575 | scalable |
| LDOA1 | LDO | 4.5 | 5.5 | 1.35 | See 表 5 | 3.3 | 200[1] |
| LDOA2 | LDO | 1.62 | 1.98 | 0.7 | See 表 5 | 1.5 | 600 |
| LDOA3 | LDO | 1.62 | 1.98 | 0.7 | See 表 5 | 1.5 | 600 |
| SWA1 | Load switch | 0.5 | 3.3 | | | | 300 |
| SWB1/SWB2 | Load switch | 0.5 | 3.3 | | | | 400 |
| VTT | Sink and source LDO | 1.1 | 1.8 | | FBVOUT6 / 2 | | See 表 5 |

(1)    When powered from a 5-V supply through the DRV5V_2_A1 pin. Otherwise, max current is limited by max $I_{OUT}$ of LDO5.

## 8.2 Functional Block Diagram
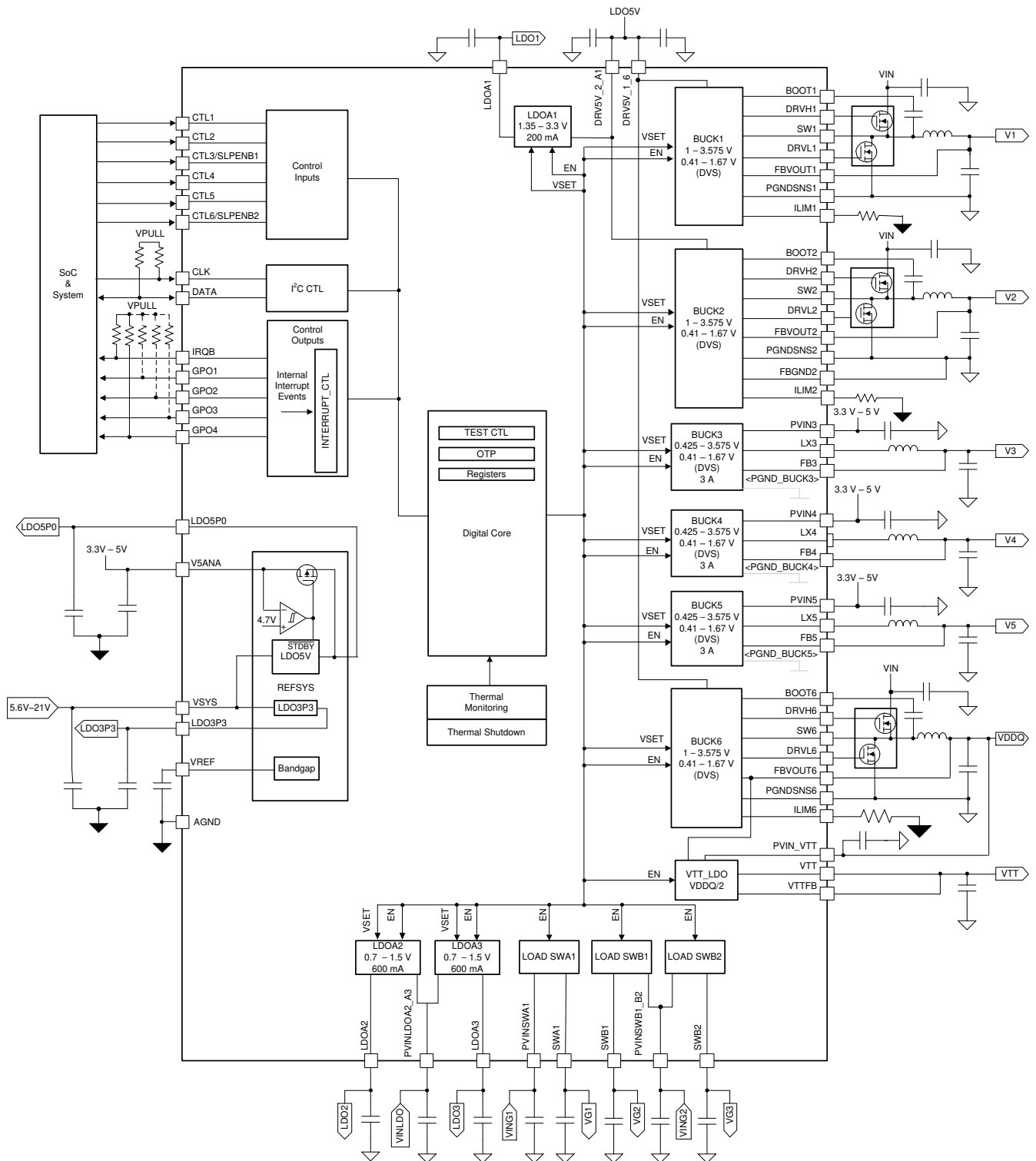


图 8-1. PMIC Functional Block Diagram
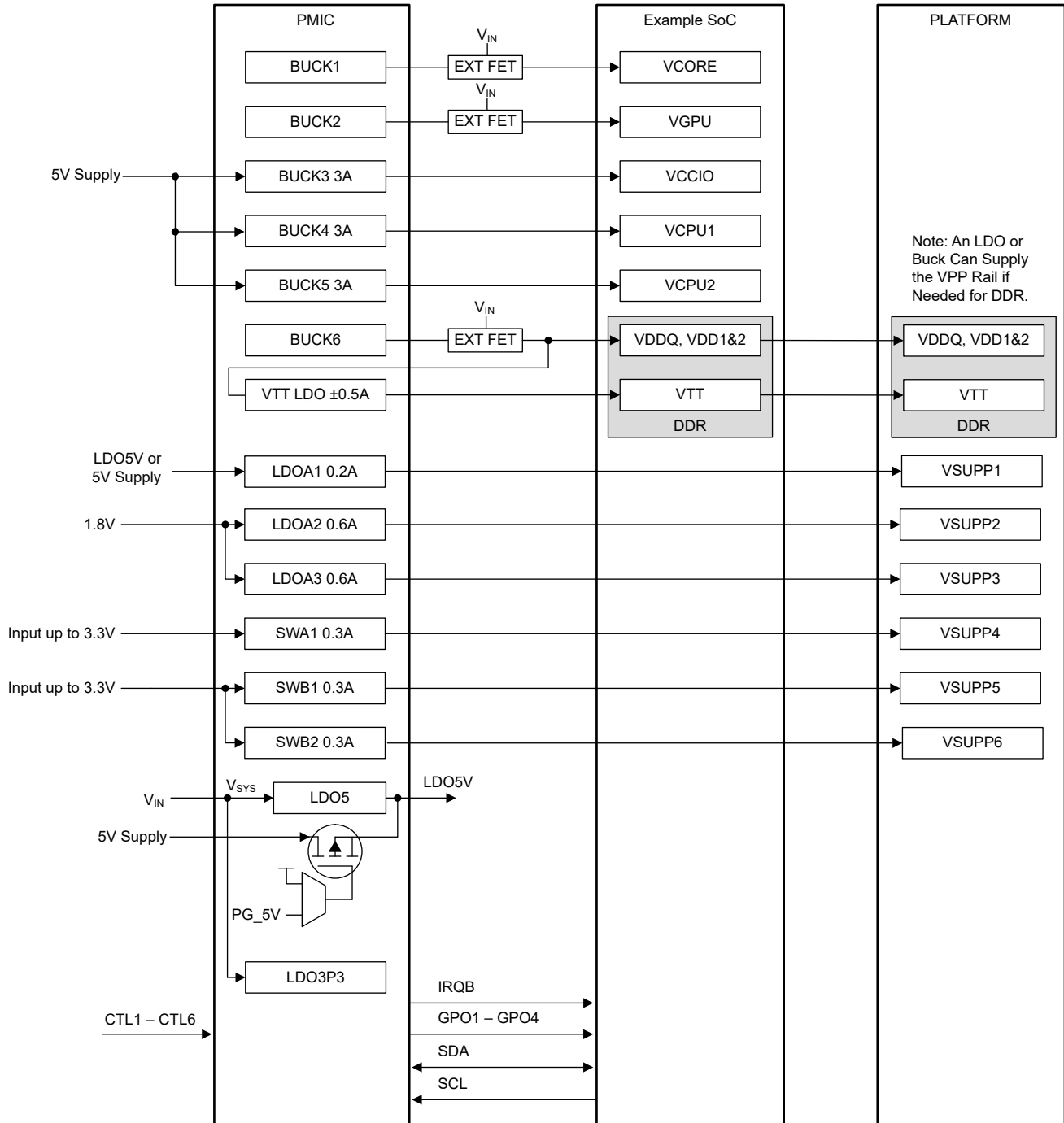
**图 8-2. Power Map Example**

## 8.3 TPS6508640 Design and Settings

The TPS6508640 device is optimized to power the higher range of the Xilinx Zynq Ultrascale+ MPSoC, but is compatible with the lower range as well. See 图 8-3 for an example block diagram. Dashed lines show the option to short VCCINT with VCCBRAM for cases where their voltages are the same and current < 25 A. In this case, the TPS544C25 device is not needed and GPO1 should be shorted to CTL4.
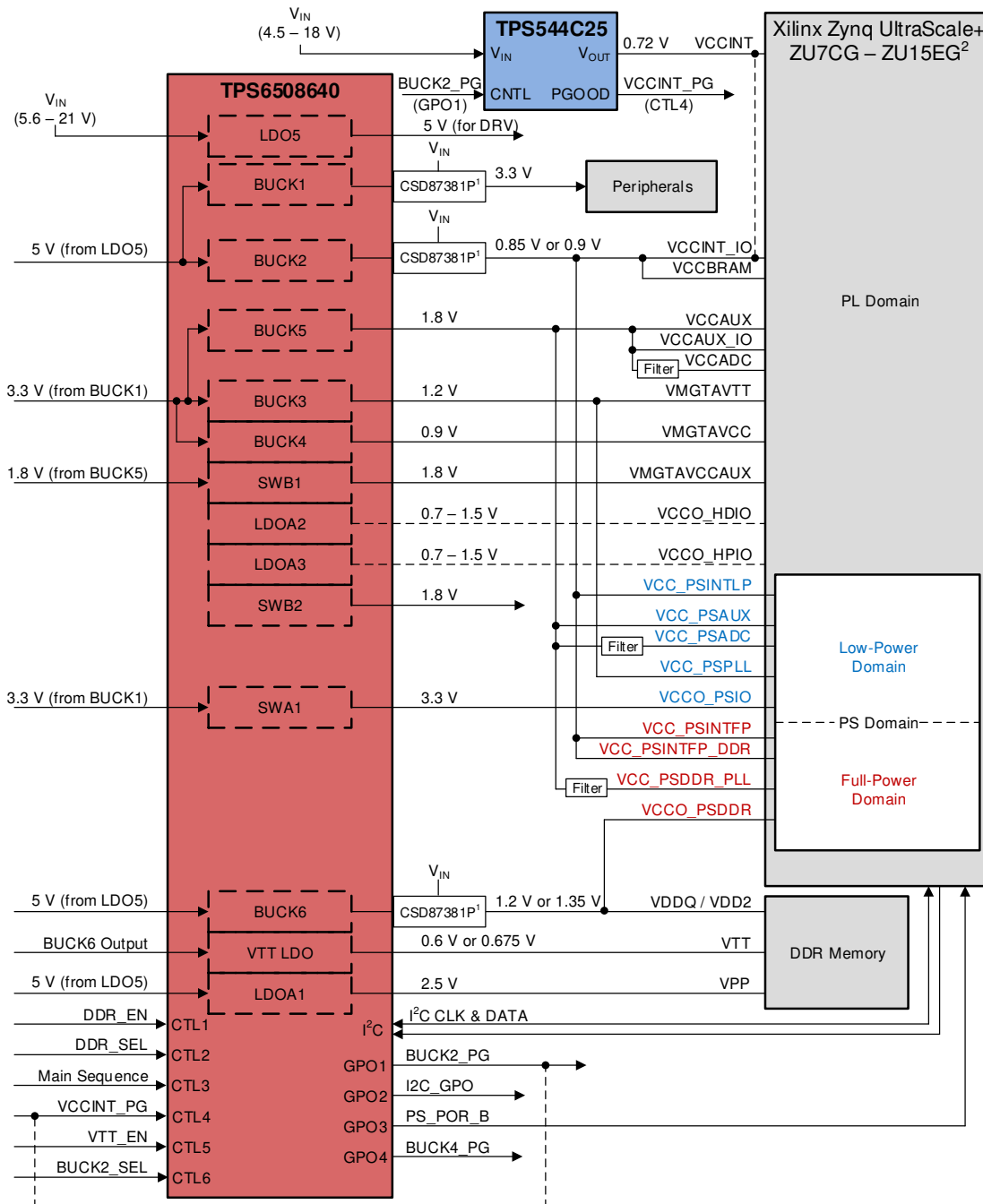


**图 8-3. TPS6508640 Power Map Example**

(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

(2) The TPS6508640 is not limited to the ZU7CG - ZU15EG. It can support other Ultrascale+ devices as long as the use case does not exceed the maximum specifications of the TPS6508640.

Product Folder Links: *TPS650864*

The power up and power down sequences can be seen in 图 8-4 and 图 8-5. Regulators and GPOs are enabled by combination of CTL pins and regulator power good signals.
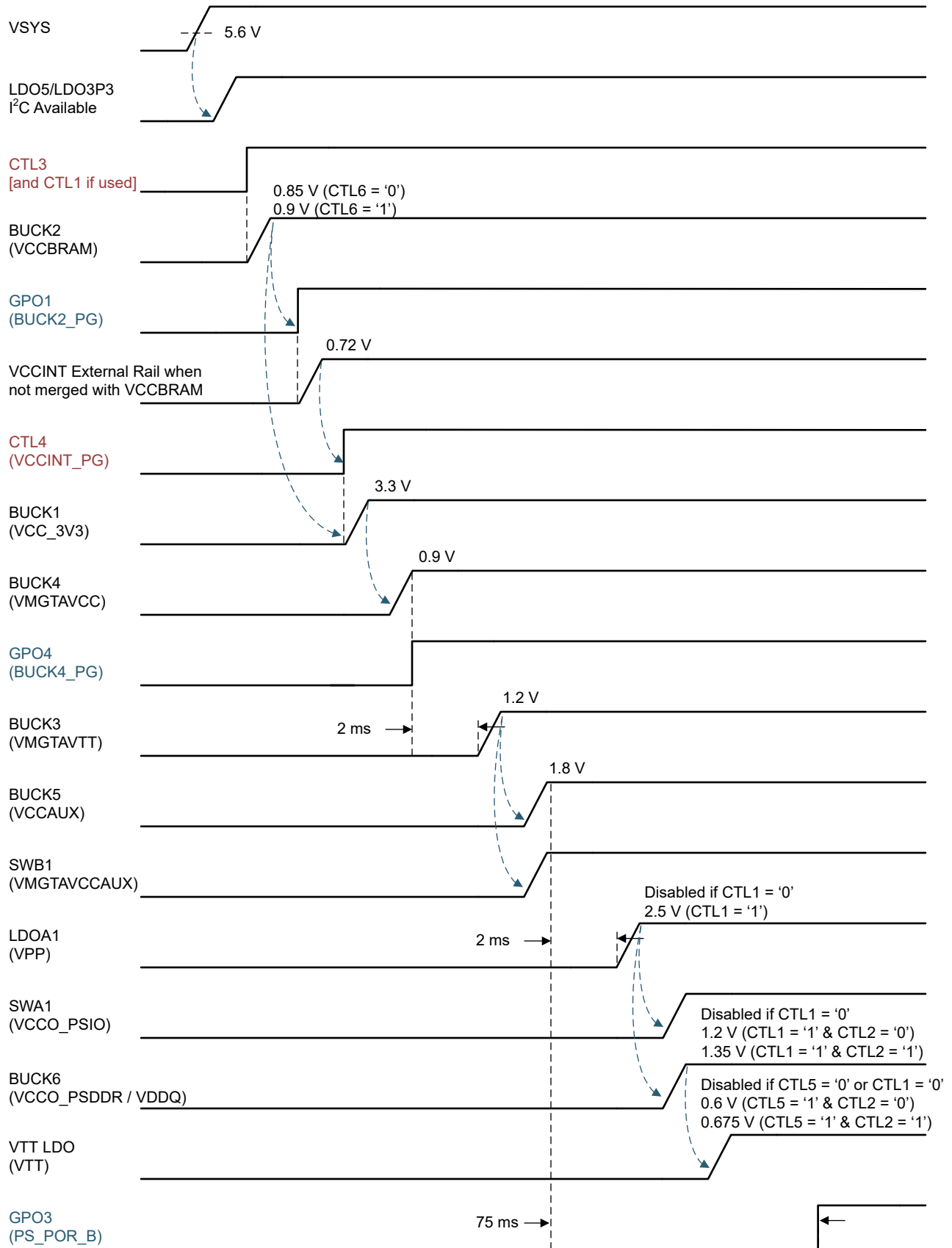
图 8-4. TPS6508640 Power-Up Sequence

Product Folder Links: *TPS650864*
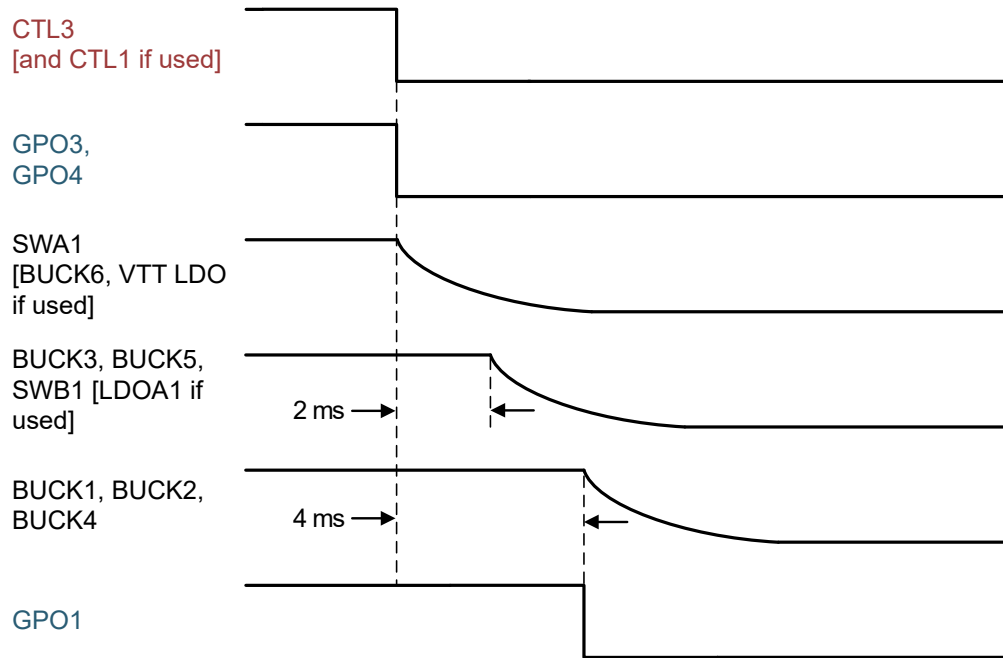
图 8-5. TPS6508640 Power-Down Sequence

TPS6508640 sequence includes an optional slot for an external rail to power VCCINT. When using an external rail, GPO1 should be connected to the enable of the external rail and the power good of the external rail should be connected to CTL4. When merging VCCINT and VCCBRAM, GPO1 can be connected directly to CTL4.

CTL1 and CTL5 are used to enable the portion of the sequencing related to DDR memory. This includes BUCK6, LDOA1, and VTT LDO. Connecting the CTL1 pin to the same input as CTL3 will result in BUCK6 being enabled 2 ms after BUCK5 and LDOA1 being enabled after BUCK6 PG. If CTL5 is connected to the same input as well, VTT LDO will turn on after BUCK6 PG as well.

CTL2 is used to select DDR voltage between 1.2 V (logic level low) and 1.35 V (logic level high).

CTL6 is used to select BUCK2 (VCCBRAM) voltage between 0.85 V (logic level low) and 0.9 V (logic level high). BUCK3 also has SLP_EN = 1b by default, so if using 0.85 V for VCCBRAM (CTL6 logic level low), then to modify BUCK3 VID during operation, BUCK3_SLP_VID register bits should be used.

LDOA2 and LDOA3 are controlled only by I$^2$C.

A summary of the part number specific settings can be seen in 节 8.3.1.

Product Folder Links: *TPS650864*

### 8.3.1 TPS6508640 OTP Summary

The following tables list the TPS6508640 device settings for the buck regulators, general purpose LDOs, VTT LDO, load switches, and GPOs. LDOA1 is used in sequence so all registers with SWB2_LDOA1 will function as LDOA1. Additionally, SWB1 and SWB2 are not merged so all registers with LDOA1_SWB2 will function as SWB2. All values which can be modified by I$^2$C after power on are shown in italics. Additional details (such as GPO power good inputs) can be found in the register map.

表 8-2. TPS6508640 Settings Summary—Buck Regulators

| REGULATOR | DEFAULT VOLTAGE | SLEEP VOLTAGE | STEP SIZE | SLP PIN | SLP_EN | POWER FAULT MASKED | FORCE PWM |
|---|---|---|---|---|---|---|---|
| BUCK1 | *3.3 V* | *3.3 V* | 25 mV | CTL6 | *No* | *No* | *Yes* |
| BUCK2 | *0.9 V* | *0.85 V* | 10 mV | CTL6 | *Yes* | *No* | *Yes* |
| BUCK3 | *1.2 V* | *1.2 V* | 25 mV | CTL6 | *Yes* | *No* | *Yes* |
| BUCK4 | *0.9 V* | *0.9 V* | 25 mV | CTL6 | *No* | *No* | *Yes* |
| BUCK5 | *1.8 V* | *1.8 V* | 25 mV | CTL6 | *No* | *No* | *Yes* |
| BUCK6 | *1.35 V / 1.2 V* | *1.35* | 10 mV | CTL2 & CTL6 | *No* | *No* | *Yes* |

表 8-3. TPS6508640 Settings Summary—General Purpose LDOs

| REGULATOR | DEFAULT VOLTAGE | SLEEP VOLTAGE | ALWAYS ON | SLP PIN | SLP_EN | POWER FAULT MASKED |
|---|---|---|---|---|---|---|
| LDOA1 | *2.5 V* | — | No | — | — | *No* |
| LDOA2 | *1.5 V* | *1.5 V* | No | CTL6 | *No* | *Yes* |
| LDOA3 | *1.2 V* | *1.2 V* | No | CTL6 | *No* | *Yes* |

表 8-4. TPS6508640 Settings Summary—VTT LDO

| REGULATOR | ILIM SETTING | ENABLE PIN | POWER FAULT MASKED |
|---|---|---|---|
| VTT LDO | 1.8 A | CTL3 | *No* |

表 8-5. TPS6508640 Settings Summary—Load Switches

| REGULATOR | POWER GOOD VOLTAGE | SWB1_2 MERGED | POWER FAULT MASKED |
|---|---|---|---|
| SWA1 | 3.3 V | — | *Yes* |
| SWB1 | 1.8 V | No | *Yes* |
| SWB2 | 1.8 V | No | *Yes* |

表 8-6. TPS6508640 Settings Summary—GPOs

| GPO | POWER GOOD (PG) or I$^2$C | STATE | OUTPUT TYPE |
|---|---|---|---|
| GPO1 | PG | — | Push Pull |
| GPO2 | I$^2$C | *Low* | Open Drain |
| GPO3 | PG | — | Open Drain |
| GPO4 | PG | — | Open Drain |

## 8.4 TPS65086401 Design and Settings

The TPS65086401 device is intended to power the lower range of the Xilinx Zynq Ultrascale+ platform. An example block diagram for this system can be seen in 图 8-6.
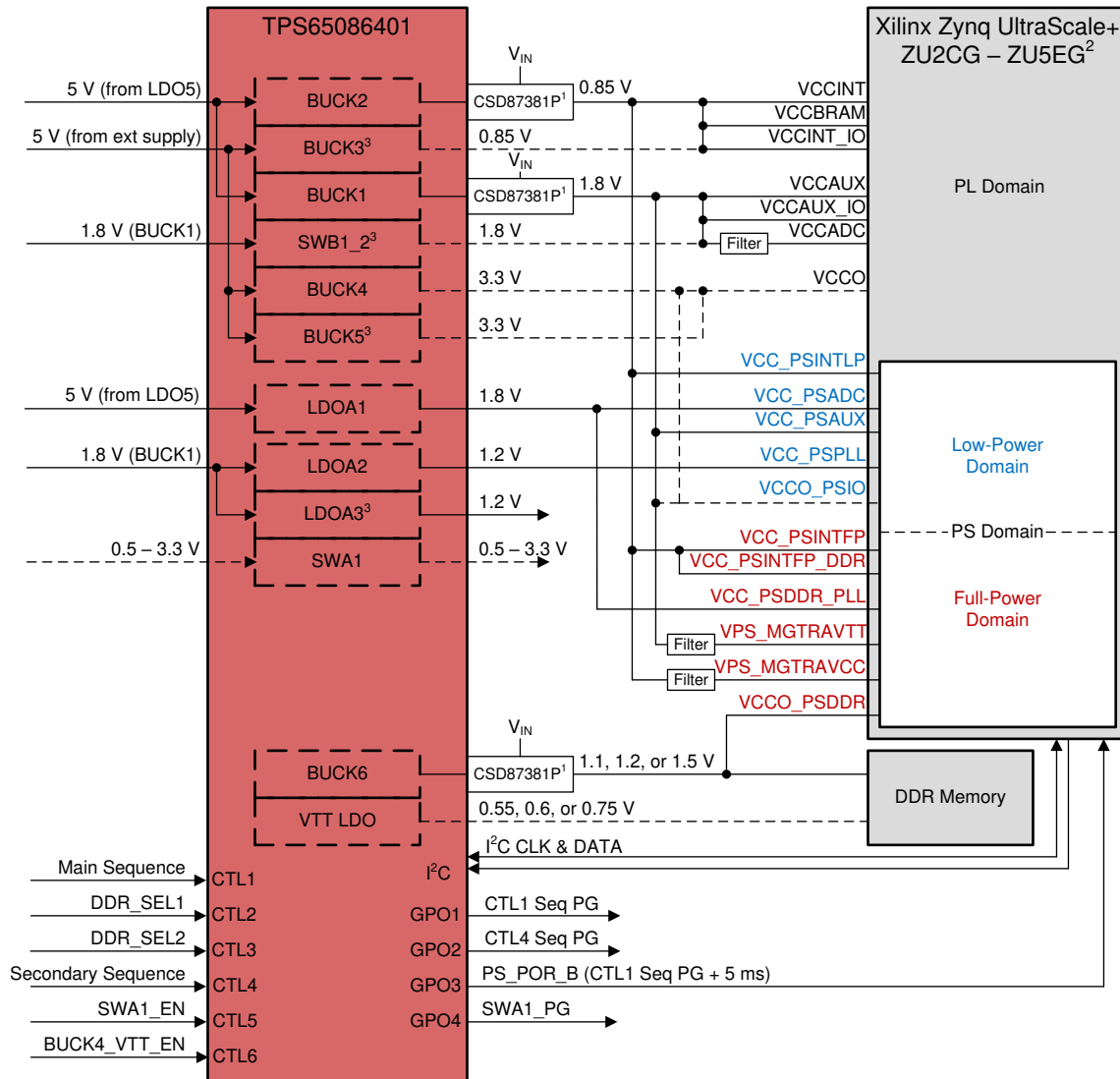


**图 8-6. TPS65086401 Power Map Example**

(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

(2) The TPS65086401 is not limited to the ZU2CG - ZU5EG. It can support other Ultrascale+ devices as long as the use case does not exceed the maximum specifications of the TPS65086401.

(3) PL Domain can be optionally powered by BUCK3, SWB1_2, BUCK5, and LDOA3 to allow it to be enabled and disabled by CTL4. This applies only to use cases where VCCINT current is less than 3 A.

The power up and power down sequences can be seen in 图 8-7 and 图 8-8. Regulators and GPOs are enabled by combination of CTL pins and regulator power good signals.
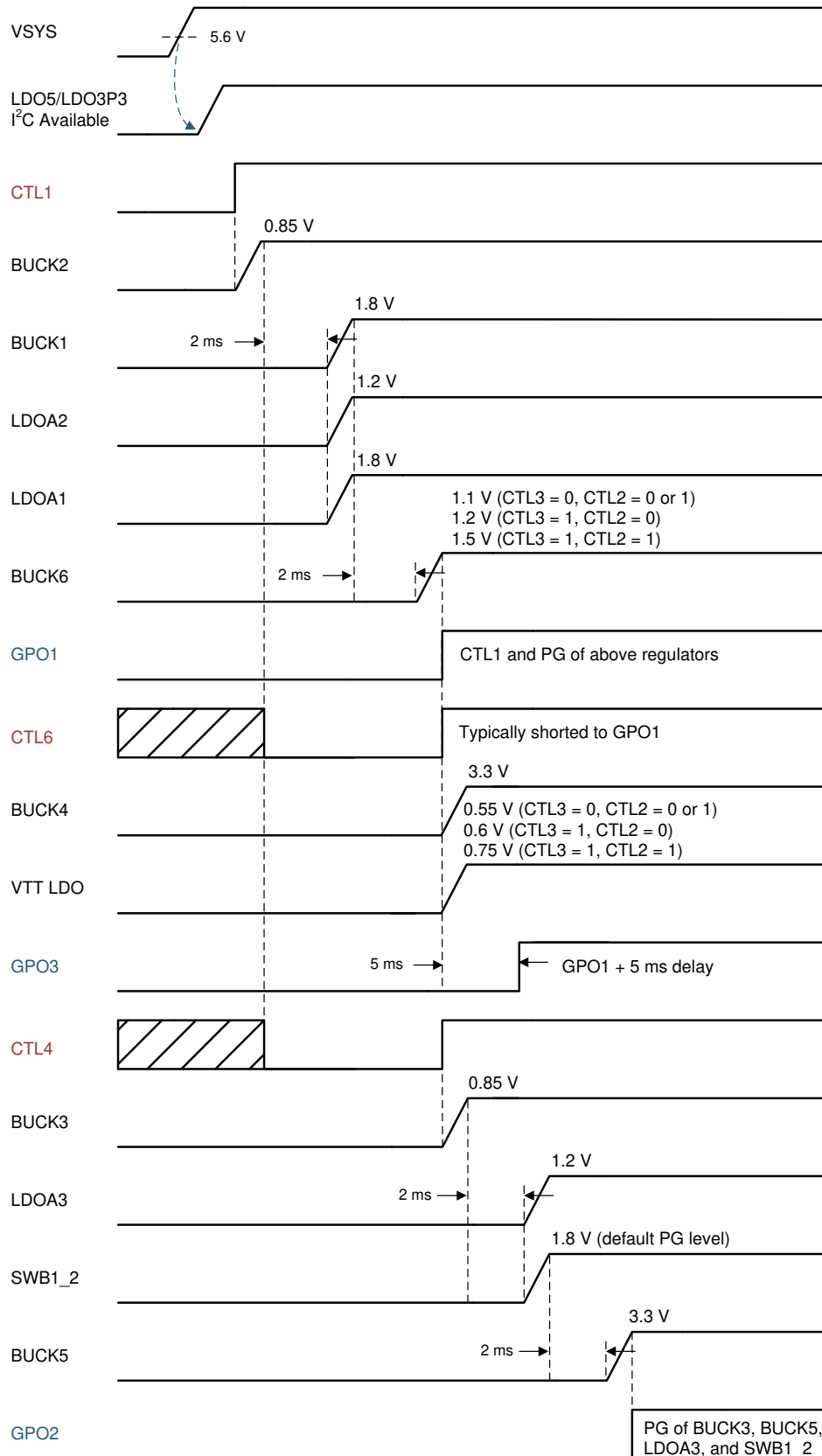
**图 8-7. TPS65086401 Power-Up Sequence**
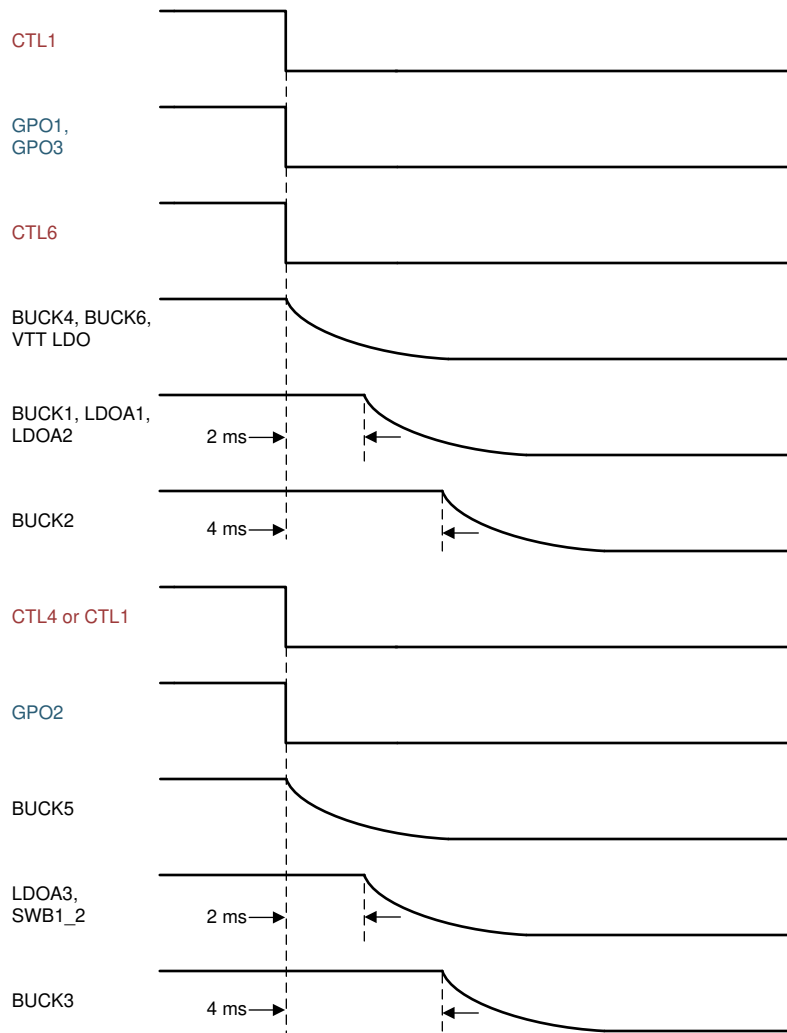
图 8-8. TPS65086401 Power-Down Sequence

CTL1 is used to enable the general system, CTL6 is typically connected to GPO1, and CTL4 can be used or not used depending on the application. CTL5 enables SWA1 independently of the rest of the sequence. CTL2 and CTL3 are used for BUCK6 voltage selection.

A summary of the part number specific settings can be seen in 节 8.4.1.

**8.4.1 TPS65086401 OTP Summary**

The following tables list the TPS65086401 device settings for the buck regulators, general purpose LDOs, VTT LDO, load switches, and GPOs. LDOA1 is used in sequence so all registers with SWB2_LDOA1 will function as LDOA1. Additionally, SWB1 and SWB2 are merged so all registers with LDOA1_SWB2 will be unused. All values which can be modified by I$^2$C after power on are shown in italics. Additional details (such as GPO power good inputs) can be found in the register map.

表 8-7. **TPS65086401 Settings Summary—Buck Regulators**

| REGULATOR | DEFAULT VOLTAGE | SLEEP VOLTAGE | STEP SIZE | SLP PIN | SLP_EN | POWER FAULT MASKED | FORCE PWM |
|---|---|---|---|---|---|---|---|
| BUCK1 | *1.8 V* | *1.8 V* | 25 mV | CTL3 | *No* | *No* | *No* |
| BUCK2 | *0.85 V* | *0.85 V* | 10 mV | CTL3 | *No* | *No* | *No* |
| BUCK3 | *0.85 V* | *0.85 V* | 25 mV | CTL3 | *No* | *No* | *No* |
| BUCK4 | *3.3 V* | *0 V* | 25 mV | CTL6 | *Yes* | *No* | *No* |
| BUCK5 | *3.3 V* | *3.3 V* | 25 mV | CTL3 | *No* | *No* | *No* |
| BUCK6 | *1.5 V / 1.2 V* | *1.1 V* | 10 mV | CTL2 & CTL3 | *Yes* | *No* | *No* |

表 8-8. **TPS65086401 Settings Summary—General Purpose LDOs**

| REGULATOR | DEFAULT VOLTAGE | SLEEP VOLTAGE | ALWAYS ON | SLP PIN | SLP_EN | POWER FAULT MASKED |
|---|---|---|---|---|---|---|
| LDOA1 | *1.8 V* | — | No | — | — | *No* |
| LDOA2 | *1.2 V* | *1.2 V* | — | CTL3 | *No* | *No* |
| LDOA3 | *1.2 V* | *1.2 V* | — | CTL3 | *No* | *No* |

表 8-9. **TPS65086401 Settings Summary—VTT LDO**

| REGULATOR | ILIM SETTING | ENABLE PIN | POWER FAULT MASKED |
|---|---|---|---|
| VTT LDO | 0.95 A | CTL6 | *Yes* |

表 8-10. **TPS65086401 Settings Summary—Load Switches**

| REGULATOR | POWER GOOD VOLTAGE | SWB1_2 MERGED | POWER FAULT MASKED |
|---|---|---|---|
| SWA1 | 3.3 V | — | *No* |
| SWB1 | 1.8 V | Yes | *No* |
| SWB2 | 1.8 V | Yes | *No* |

表 8-11. **TPS65086401 Settings Summary—GPOs**

| GPO | POWER GOOD (PG) or I$^2$C | STATE | OUTPUT TYPE |
|---|---|---|---|
| GPO1 | PG | — | Open Drain |
| GPO2 | PG | — | Open Drain |
| GPO3 | PG | — | Open Drain |
| GPO4 | PG | — | Open Drain |

Product Folder Links: *TPS650864*

## 8.5 TPS6508641 Design and Settings

The TPS6508641 device is intended to power the lower range of the Xilinx Zynq Ultrascale+ platform. It removes the need for an external 5 V regulator when compared with the TPS65086401 device and also supports a wider variety of Zynq Ultrascale+ power states. 图 8-9 shows a simple example block diagram for an always-on system, while 图 8-10 shows a block diagram for full power domain flexibility. See Xilinx's Ultrascale Architecture PCB Design for explanation of the power supply configurations.
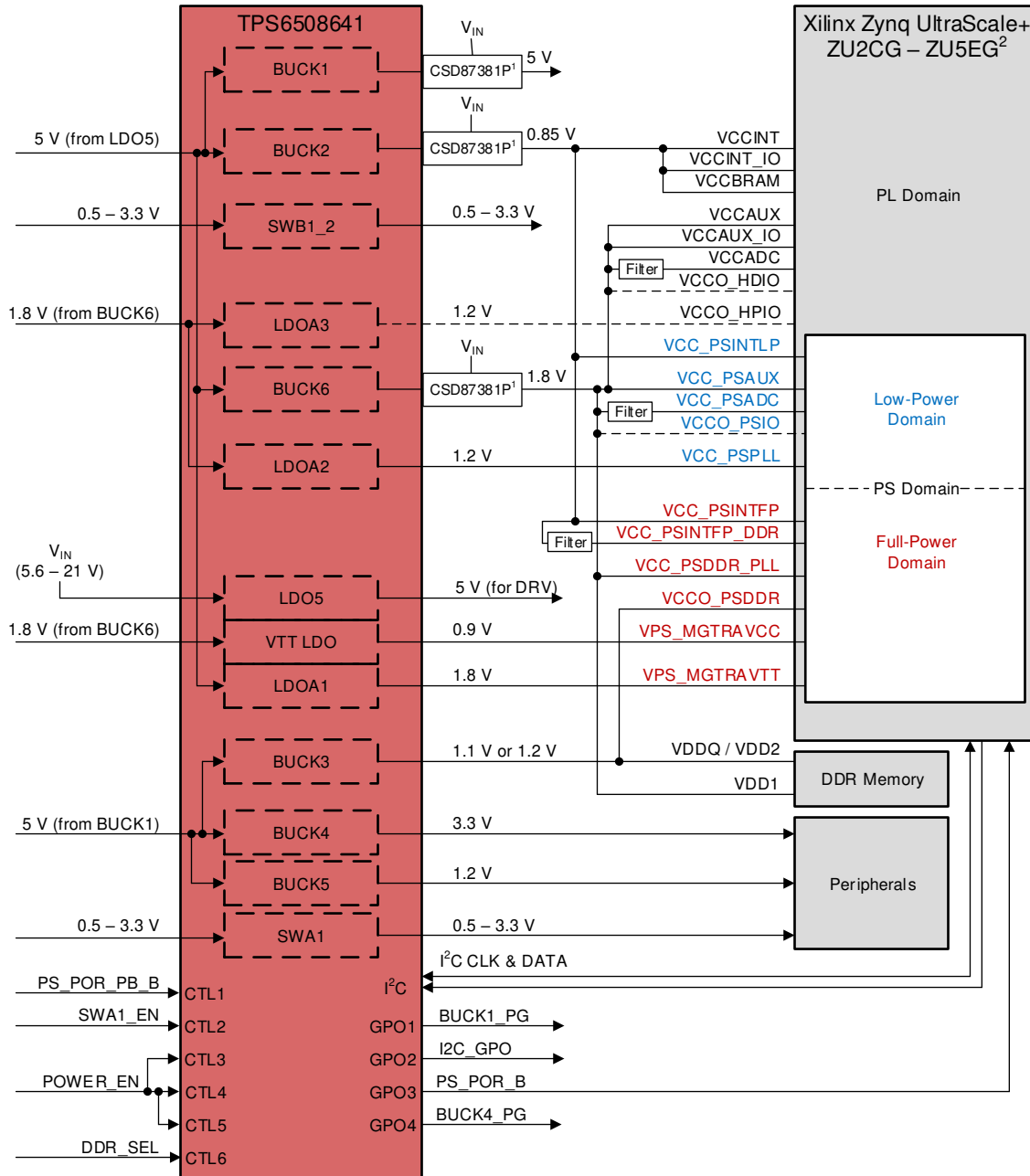


(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.
(2) The TPS6508641 is not limited to the ZU2CG - ZU5EG. It can support other Ultrascale+ devices as long as the use case does not exceed the maximum specifications of the TPS6508641.

**图 8-9. TPS6508641 Always-On Power Map Example**

Product Folder Links: TPS650864

**图 8-10. TPS6508641 Full Power Domain Flexibility Power Map Example**

(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

(2) The TPS6508641 is not limited to the ZU2CG - ZU5EG. It can support other Ultrascale+ devices as long as the use case does not exceed the maximum specifications of the TPS6508641.

The power up and power down sequences can be seen in 图 8-11 and 图 8-12. Regulators and GPOs are enabled by combination of CTL pins and regulator power good signals.

VSYS — 5.6 V

LDO5/LDO3P3
I²C Available

CTL4
(POWER_EN)

BUCK1
(VCC_5V0) — 5 V

CTL3
(PS_FP_PWR_EN_LS)

BUCK2
(VCC_PSINTLP) — 0.85 V

GPO1
(PSINTFP EN)

External Load Switch #1
(VCC_PSINTFP) — 0.85 V

BUCK5
(VCC_1V2) — 1.2 V

BUCK6
(VCC_PSAUX) — 1.8 V

LDOA2
(VCC_PSPLL) — 1.2 V

VTT LDO
(VPS_MGTRAVCC) — 0.9 V

LDOA1
(VPS_MGTRAVTT) — 1.8 V

BUCK3
(VDDQ / VCCO_PSDDR) — 1.1 V (CTL6 = '1') 1.2 V (CTL6 = '0')

BUCK4
(VCC_3V3) — 3.3 V

CTL5
(PL_PWR_EN)

GPO4
(VCCINT_EN)

External Load Switch #2
(VCCINT) — 0.85 V

SWB1_2
(VCCAUX) — 2 ms — 1.8 V

LDOA3
(VCCO_HPIO) — 4 ms — 1.2 V

GPO3
(PS_POR_B) — CTL1 = '1' & 50 ms

**图 8-11. TPS6508641 Power-Up Sequence**

(1) Sequence shown assumes CTL3 is high. If CTL3 is set low before this point, these voltage regulators will already be disabled.

(2) Sequence shown assumes CTL5 is high. If CTL5 is set low before this point, these voltage regulators will already be disabled.

图 8-12. TPS6508641 Power-Down Sequence
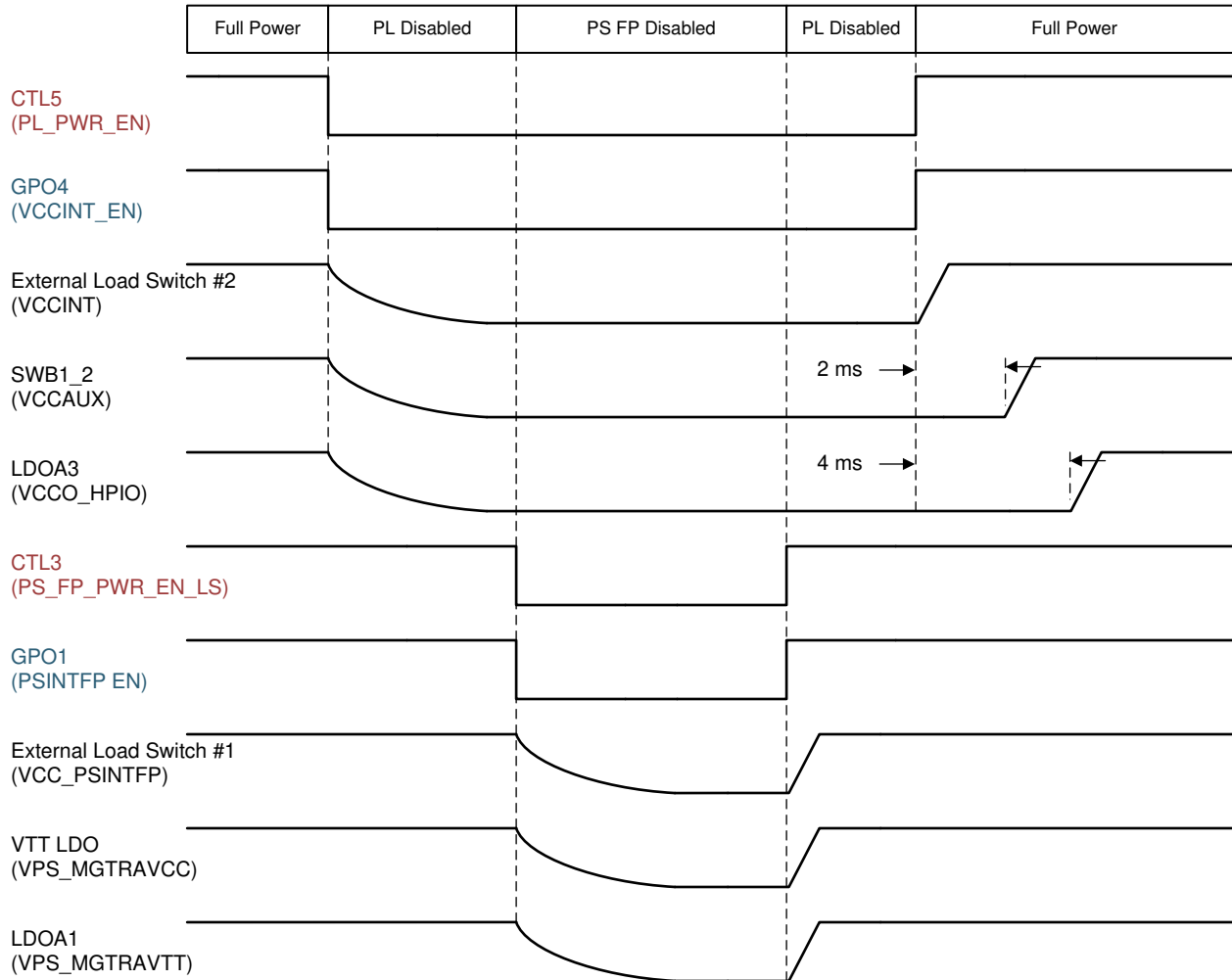
图 8-13. TPS6508641 Low Power States

The TPS6508641 device is designed to be able to support always on and full power domain flexibility power modes. The low power states can be omitted if not required.

CTL4 is used to start the primary power sequence and CTL1, CTL3, and CTL5 should all be high initially to complete the power up sequence. For always-on case, CTL3 and CTL5 can be shorted with CTL4.

CTL6 is used to select BUCK3 voltage between BUCK3_VID and BUCK3_SLP_VID register bits. Logic level low will result in 1.2 V while logic level high will result in 1.1 V.

CTL2 is used to enable and disable SWA1 and is independent of the rest of the sequence.

When CTL1 is set low, GPO3 (PS_POR_B) is set low regardless of the power state and has 50 ms delay before going high after CTL1 goes high. It is used as a reset for the Zynq Ultrascale+ device. It can be pulled up to LDO3P3 (3.3 V) or BUCK6 (1.8 V) as preferred with a 10 kΩ resistor and a pushbutton can short this CTL pin to GND when MPSoC reset is desired.

GPO1 and GPO4 are used to control load switches when utilizing the low power modes. The load switches can be omitted for cases where low power modes are not necessary.

VTT LDO voltage used to power VPS_MGTRAVCC is configured to 0.9 V in order to support all variant speeds, including -3E designs. It is within the absolute voltage range and is not expected to impact performance for non-3E designs based on testing with the Ultra96 board. For more information on VPS_MGTRAVCC voltage, see Xilinx's Ultrascale Architecture PCB Design, *Table 7-2 MPSoC PS Voltage Matrix by Speed/Temperature Grade*.

A summary of the part number specific settings can be seen in 节 8.5.1.

### 8.5.1 TPS6508641 OTP Summary

The following tables list the TPS6508641 device settings for the buck regulators, general purpose LDOs, VTT LDO, load switches, and GPOs. LDOA1 is used in sequence so all registers with SWB2_LDOA1 will function as LDOA1. Additionally, SWB1 and SWB2 are merged so all registers with LDOA1_SWB2 are unused. All values which can be modified by I$^2$C after power on are shown in italics. Additional details (such as GPO power good inputs) can be found in the register map.

表 8-12. TPS6508641 Settings Summary—Buck Regulators

| REGULATOR | DEFAULT VOLTAGE | SLEEP VOLTAGE | STEP SIZE | SLP PIN | SLP_EN | POWER FAULT MASKED | FORCE PWM |
|---|---|---|---|---|---|---|---|
| BUCK1 | Ext FB | Ext FB | — | CTL6 | *No* | *No* | *Yes* |
| BUCK2 | *0.85 V* | *0.85 V* | 10 mV | CTL6 | *No* | *No* | *Yes* |
| BUCK3 | *1.1 V* | *1.2 V* | 25 mV | CTL6 | *Yes* | *No* | *Yes* |
| BUCK4 | *3.3 V* | *3.3 V* | 25 mV | CTL6 | *No* | *No* | *Yes* |
| BUCK5 | *1.2 V* | *1.2 V* | 25 mV | CTL6 | *No* | *No* | *Yes* |
| BUCK6 | *1.8 V* | *1.8 V* | 25 mV | CTL6 | *No* | *No* | *Yes* |

表 8-13. TPS6508641 Settings Summary—General Purpose LDOs

| REGULATOR | DEFAULT VOLTAGE | SLEEP VOLTAGE | ALWAYS ON | SLP PIN | SLP_EN | POWER FAULT MASKED |
|---|---|---|---|---|---|---|
| LDOA1 | *1.8 V* | — | No | — | — | *No* |
| LDOA2 | *1.2 V* | *1.2 V* | No | CTL6 | *Yes* | *No* |
| LDOA3 | *1.2 V* | *1.2 V* | No | CTL6 | *Yes* | *No* |

表 8-14. TPS6508641 Settings Summary—VTT LDO

| REGULATOR | ILIM SETTING | ENABLE PIN | POWER FAULT MASKED |
|---|---|---|---|
| VTT LDO | 1.8 A | CTL3 | *No* |

表 8-15. TPS6508641 Settings Summary—Load Switches

| REGULATOR | POWER GOOD VOLTAGE | SWB1_2 MERGED | POWER FAULT MASKED |
|---|---|---|---|
| SWA1 | 3.3 V | — | *Yes* |
| SWB1 | 1.8 V | Yes | *No* |
| SWB2 | 1.8 V | Yes | *No* |

表 8-16. TPS6508641 Settings Summary—GPOs

| GPO | POWER GOOD (PG) or I$^2$C | STATE | OUTPUT TYPE |
|---|---|---|---|
| GPO1 | PG | — | Open Drain |
| GPO2 | I$^2$C | | Open Drain |
| GPO3 | PG | — | Open Drain |
| GPO4 | PG | — | Open Drain |

## 8.6 TPS65086470 Design and Settings

The TPS65086470 device is originally intended to power a Xilinx Artix 7 platform. 图 8-14 shows an example block diagram for this system.
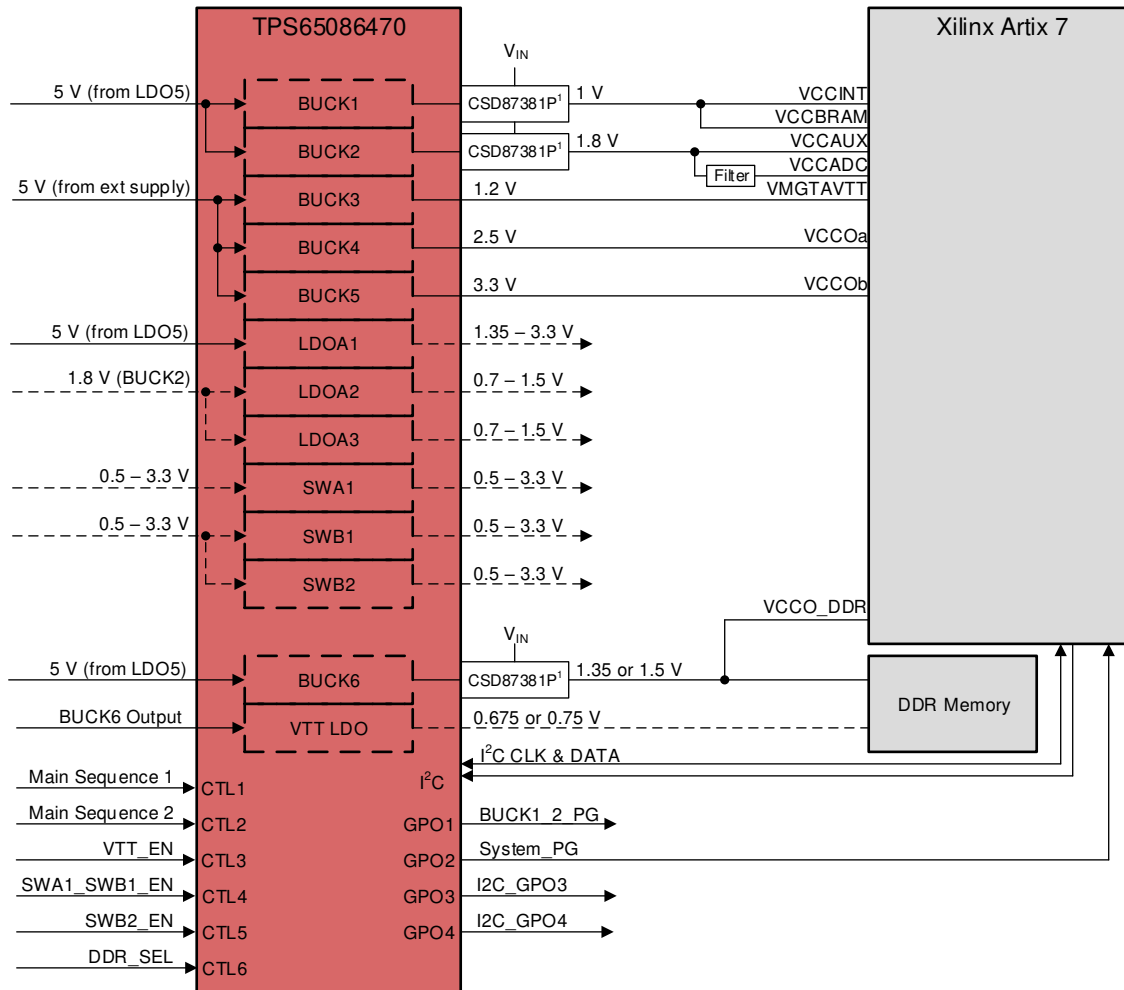


(1) External FETs can be scaled to meet the current requirements of each design; CSD87381P is suitable up to approximately 15 A.

**图 8-14. TPS65086470 Power Map Example**

图 8-15 and 图 8-16 show the power-up and power-down sequences. Regulators and GPOs are enabled by combination of CTL pins and regulator power good signals.
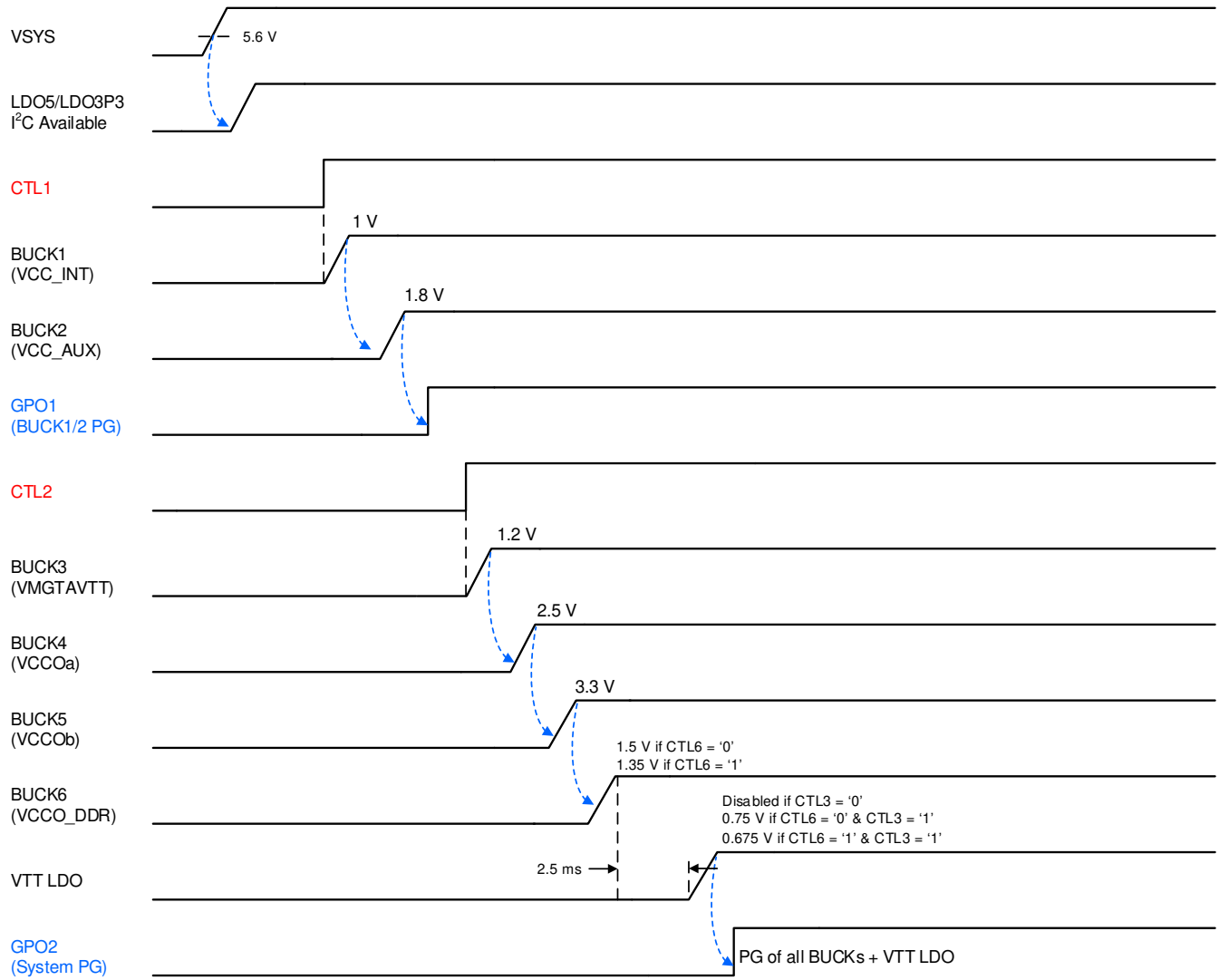
**图 8-15. TPS65086470 Power-Up Sequence**
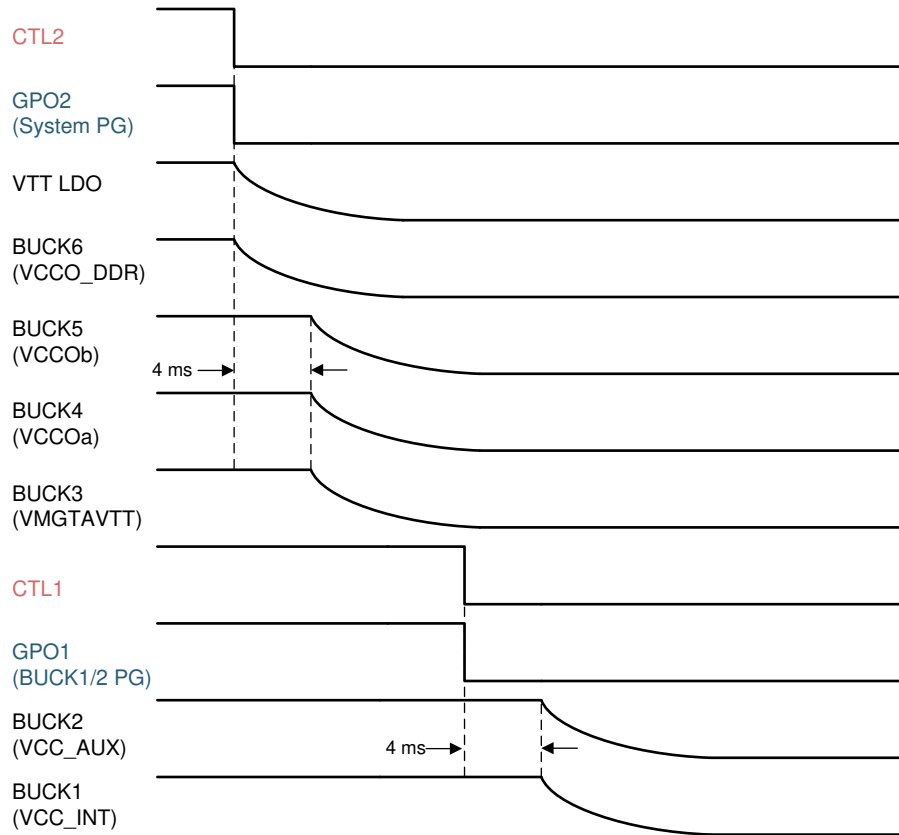
**图 8-16. TPS65086470 Power-Down Sequence**

If CTL1 and CTL2 are set low at the same time, both sequences will occur simultaneously. If CTL1 is set low before CTL2, GPO1 and GPO2 will go low and remaining bucks will be disabled as their PG enable is lost. For example, as BUCK2 is disabled after 4 ms, BUCK3 will start it's 4 ms delay. As such it is recommended to not set CTL1 low before CTL2.

Additionally, CTL4 can be used to enable SWA1 and SWB1. CTL5 can be used to enable SWB2. LDOA2 and LDOA3 are controlled only by I²C.

A summary of the part number specific settings can be seen in 节 8.6.1.

### 8.6.1 TPS65086470 OTP Summary

The following tables list the TPS65086470 device settings for the buck regulators (表 8-17), general purpose LDOs (表 8-18), VTT LDO (表 8-19), load switches (表 8-20), and GPOs (表 8-21). LDOA1 is not used in sequence so all registers with LDOA1_SWB2 will function as LDOA1. Additionally, SWB1 and SWB2 are not merged so all registers with SWB2_LDOA1 will function as SWB2. All values which can be modified by I²C after power on are shown in italics. Additional details (such as GPO power good inputs) can be found in the register map.

#### 表 8-17. TPS65086470 Settings Summary—Buck Regulators

| REGULATOR | DEFAULT VOLTAGE | SLEEP VOLTAGE | STEP SIZE | SLP PIN | SLP_EN | POWER FAULT MASKED | FORCE PWM |
|---|---|---|---|---|---|---|---|
| BUCK1 | *1 V* | *1 V* | 10 mV | CTL6 | *No* | *No* | *No* |
| BUCK2 | *1.8 V* | *1.8 V* | 25 mV | CTL6 | *No* | *No* | *No* |
| BUCK3 | *1.2 V* | *1.2 V* | 25 mV | CTL6 | *No* | *No* | *No* |
| BUCK4 | *2.5 V* | *2.5 V* | 25 mV | CTL6 | *No* | *No* | *No* |
| BUCK5 | *3.3 V* | *3.3 V* | 25 mV | CTL6 | *No* | *No* | *No* |
| BUCK6 | *1.5 V* | *1.35 V* | 25 mV | CTL6 | *Yes* | *No* | *No* |

#### 表 8-18. TPS65086470 Settings Summary—General Purpose LDOs

| REGULATOR | DEFAULT VOLTAGE | SLEEP VOLTAGE | ALWAYS ON | SLP PIN | SLP_EN | POWER FAULT MASKED |
|---|---|---|---|---|---|---|
| LDOA1 | *1.8 V* | — | No | — | — | *Yes* |
| LDOA2 | *0.7 V* | *0.7 V* | — | CTL6 | *No* | *Yes* |
| LDOA3 | *0.7 V* | *0.7 V* | — | CTL6 | *No* | *Yes* |

#### 表 8-19. TPS65086470 Settings Summary—VTT LDO

| REGULATOR | ILIM SETTING | ENABLE PIN | POWER FAULT MASKED |
|---|---|---|---|
| VTT LDO | 0.95 A | CTL3 | *No* |

#### 表 8-20. TPS65086470 Settings Summary—Load Switches

| REGULATOR | POWER GOOD VOLTAGE | SWB1_2 MERGED | POWER FAULT MASKED |
|---|---|---|---|
| SWA1 | 3.3 V | — | *Yes* |
| SWB1 | 1.8 V | No | *Yes* |
| SWB2 | 1.8 V | No | *Yes* |

#### 表 8-21. TPS65086470 Settings Summary—GPOs

| GPO | POWER GOOD (PG) OR I²C | STATE | OUTPUT TYPE |
|---|---|---|---|
| GPO1 | PG | — | Open drain |
| GPO2 | PG | — | Open drain |
| GPO3 | I²C | *Low* | Open drain |
| GPO4 | I²C | *Low* | Open drain |

Product Folder Links: *TPS650864*

## 8.7 SMPS Voltage Regulators

The buck controllers integrate gate drivers for external power stages with programmable current limit (set by an external resistor at ILIMx pin), which allows for optimal selection of external passive components based on the desired system load. The buck converters include integrated power stage and require a minimum number of pins for power input, inductor, and output voltage feedback input. Combined with high-frequency switching, all these features allow use of inductors in small form factor, thus reducing total-system cost and size.

BUCK1 – BUCK6 have selectable auto- and forced-pulse width modulation (PWM) mode through the BUCKx_MODE bit in the BUCKxCTRL register. In default auto mode, the VR automatically switches between PWM and pulsed frequency modulation (PFM) depending on the output load to maximize efficiency.

All controllers and converters can be used with the default $V_{OUT}$ or can have their voltage dynamically changed at any time. This means that the rails can be default programmed for any available $V_{OUT}$ by OTP programming at the factory, so the device starts up with the default voltage, or during operation the rail can be configured by $I^2C$ to another operating $V_{OUT}$ while the rail is enable or disabled. There are two step sizes or ranges available for $V_{OUT}$ selection : 10-mV and 25-mV steps. The step-size range must be selected prior to use and must be programmed in the OTP at the factory. It is not subject to change during operation.

For the 10-mV step-size range $V_{OUT}$ options, see 表 8-22. For the 25-mV step-size range $V_{OUT}$ options, see 表 8-23.

表 8-22. 10-mV Step-Size V$_{OUT}$ Range

| VID BITS | V$_{OUT}$ | VID BITS | V$_{OUT}$ | VID BITS | V$_{OUT}$ |
|---|---|---|---|---|---|
| 0000000 | 0 | 0101011 | 0.83 | 1010110 | 1.26 |
| 0000001 | 0.41 | 0101100 | 0.84 | 1010111 | 1.27 |
| 0000010 | 0.42 | 0101101 | 0.85 | 1011000 | 1.28 |
| 0000011 | 0.43 | 0101110 | 0.86 | 1011001 | 1.29 |
| 0000100 | 0.44 | 0101111 | 0.87 | 1011010 | 1.30 |
| 0000101 | 0.45 | 0110000 | 0.88 | 1011011 | 1.31 |
| 0000110 | 0.46 | 0110001 | 0.89 | 1011100 | 1.32 |
| 0000111 | 0.47 | 0110010 | 0.90 | 1011101 | 1.33 |
| 0001000 | 0.48 | 0110011 | 0.91 | 1011110 | 1.34 |
| 0001001 | 0.49 | 0110100 | 0.92 | 1011111 | 1.35 |
| 0001010 | 0.50 | 0110101 | 0.93 | 1100000 | 1.36 |
| 0001011 | 0.51 | 0110110 | 0.94 | 1100001 | 1.37 |
| 0001100 | 0.52 | 0110111 | 0.95 | 1100010 | 1.38 |
| 0001101 | 0.53 | 0111000 | 0.96 | 1100011 | 1.39 |
| 0001110 | 0.54 | 0111001 | 0.97 | 1100100 | 1.40 |
| 0001111 | 0.55 | 0111010 | 0.98 | 1100101 | 1.41 |
| 0010000 | 0.56 | 0111011 | 0.99 | 1100110 | 1.42 |
| 0010001 | 0.57 | 0111100 | 1.00 | 1100111 | 1.43 |
| 0010010 | 0.58 | 0111101 | 1.01 | 1101000 | 1.44 |
| 0010011 | 0.59 | 0111110 | 1.02 | 1101001 | 1.45 |
| 0010100 | 0.60 | 0111111 | 1.03 | 1101010 | 1.46 |
| 0010101 | 0.61 | 1000000 | 1.04 | 1101011 | 1.47 |
| 0010110 | 0.62 | 1000001 | 1.05 | 1101100 | 1.48 |
| 0010111 | 0.63 | 1000010 | 1.06 | 1101101 | 1.49 |
| 0011000 | 0.64 | 1000011 | 1.07 | 1101110 | 1.50 |
| 0011001 | 0.65 | 1000100 | 1.08 | 1101111 | 1.51 |
| 0011010 | 0.66 | 1000101 | 1.09 | 1110000 | 1.52 |
| 0011011 | 0.67 | 1000110 | 1.10 | 1110001 | 1.53 |
| 0011100 | 0.68 | 1000111 | 1.11 | 1110010 | 1.54 |
| 0011101 | 0.69 | 1001000 | 1.12 | 1110011 | 1.55 |
| 0011110 | 0.70 | 1001001 | 1.13 | 1110100 | 1.56 |
| 0011111 | 0.71 | 1001010 | 1.14 | 1110101 | 1.57 |
| 0100000 | 0.72 | 1001011 | 1.15 | 1110110 | 1.58 |
| 0100001 | 0.73 | 1001100 | 1.16 | 1110111 | 1.59 |
| 0100010 | 0.74 | 1001101 | 1.17 | 1111000 | 1.60 |
| 0100011 | 0.75 | 1001110 | 1.18 | 1111001 | 1.61 |
| 0100100 | 0.76 | 1001111 | 1.19 | 1111010 | 1.62 |
| 0100101 | 0.77 | 1010000 | 1.20 | 1111011 | 1.63 |
| 0100110 | 0.78 | 1010001 | 1.21 | 1111100 | 1.64 |
| 0100111 | 0.79 | 1010010 | 1.22 | 1111101 | 1.65 |
| 0101000 | 0.80 | 1010011 | 1.23 | 1111110 | 1.66 |
| 0101001 | 0.81 | 1010100 | 1.24 | 1111111 | 1.67 |
| 0101010 | 0.82 | 1010101 | 1.25 | | |

Product Folder Links: *TPS650864*

表 8-23. 25-mV Step-Size $V_{OUT}$ Range

| VID BITS | $V_{OUT}$ (Converters) | $V_{OUT}$ (Controllers) | VID BITS | $V_{OUT}$ | VID BITS | $V_{OUT}$ |
|---|---|---|---|---|---|---|
| 0000000 | 0 | 0 | 0101011 | 1.475 | 1010110 | 2.550 |
| 0000001 | 0.425 | 1.000 | 0101100 | 1.500 | 1010111 | 2.575 |
| 0000010 | 0.450 | 1.000 | 0101101 | 1.525 | 1011000 | 2.600 |
| 0000011 | 0.475 | 1.000 | 0101110 | 1.550 | 1011001 | 2.625 |
| 0000100 | 0.500 | 1.000 | 0101111 | 1.575 | 1011010 | 2.650 |
| 0000101 | 0.525 | 1.000 | 0110000 | 1.600 | 1011011 | 2.675 |
| 0000110 | 0.550 | 1.000 | 0110001 | 1.625 | 1011100 | 2.700 |
| 0000111 | 0.575 | 1.000 | 0110010 | 1.650 | 1011101 | 2.725 |
| 0001000 | 0.600 | 1.000 | 0110011 | 1.675 | 1011110 | 2.750 |
| 0001001 | 0.625 | 1.000 | 0110100 | 1.700 | 1011111 | 2.775 |
| 0001010 | 0.650 | 1.000 | 0110101 | 1.725 | 1100000 | 2.800 |
| 0001011 | 0.675 | 1.000 | 0110110 | 1.750 | 1100001 | 2.825 |
| 0001100 | 0.700 | 1.000 | 0110111 | 1.775 | 1100010 | 2.850 |
| 0001101 | 0.725 | 1.000 | 0111000 | 1.800 | 1100011 | 2.875 |
| 0001110 | 0.750 | 1.000 | 0111001 | 1.825 | 1100100 | 2.900 |
| 0001111 | 0.775 | 1.000 | 0111010 | 1.850 | 1100101 | 2.925 |
| 0010000 | 0.800 | 1.000 | 0111011 | 1.875 | 1100110 | 2.950 |
| 0010001 | 0.825 | 1.000 | 0111100 | 1.900 | 1100111 | 2.975 |
| 0010010 | 0.850 | 1.000 | 0111101 | 1.925 | 1101000 | 3.000 |
| 0010011 | 0.875 | 1.000 | 0111110 | 1.950 | 1101001 | 3.025 |
| 0010100 | 0.900 | 1.000 | 0111111 | 1.975 | 1101010 | 3.050 |
| 0010101 | 0.925 | 1.000 | 1000000 | 2.000 | 1101011 | 3.075 |
| 0010110 | 0.950 | 1.000 | 1000001 | 2.025 | 1101100 | 3.100 |
| 0010111 | 0.975 | 1.000 | 1000010 | 2.050 | 1101101 | 3.125 |
| 0011000 | 1.000 | 1.000 | 1000011 | 2.075 | 1101110 | 3.150 |
| 0011001 | 1.025 | 1.025 | 1000100 | 2.100 | 1101111 | 3.175 |
| 0011010 | 1.050 | 1.050 | 1000101 | 2.125 | 1110000 | 3.200 |
| 0011011 | 1.075 | 1.075 | 1000110 | 2.150 | 1110001 | 3.225 |
| 0011100 | 1.100 | 1.100 | 1000111 | 2.175 | 1110010 | 3.250 |
| 0011101 | 1.125 | 1.125 | 1001000 | 2.200 | 1110011 | 3.275 |
| 0011110 | 1.150 | 1.150 | 1001001 | 2.225 | 1110100 | 3.300 |
| 0011111 | 1.175 | 1.175 | 1001010 | 2.250 | 1110101 | 3.325 |
| 0100000 | 1.200 | 1.200 | 1001011 | 2.275 | 1110110 | 3.350 |
| 0100001 | 1.225 | 1.225 | 1001100 | 2.300 | 1110111 | 3.375 |
| 0100010 | 1.250 | 1.250 | 1001101 | 2.325 | 1111000 | 3.400 |
| 0100011 | 1.275 | 1.275 | 1001110 | 2.350 | 1111001 | 3.425 |
| 0100100 | 1.300 | 1.300 | 1001111 | 2.375 | 1111010 | 3.450 |
| 0100101 | 1.325 | 1.325 | 1010000 | 2.400 | 1111011 | 3.475 |
| 0100110 | 1.350 | 1.350 | 1010001 | 2.425 | 1111100 | 3.500 |
| 0100111 | 1.375 | 1.375 | 1010010 | 2.450 | 1111101 | 3.525 |
| 0101000 | 1.400 | 1.400 | 1010011 | 2.475 | 1111110 | 3.550 |
| 0101001 | 1.425 | 1.425 | 1010100 | 2.500 | 1111111 | 3.575 |
| 0101010 | 1.450 | 1.450 | 1010101 | 2.525 | | |

Product Folder Links: TPS650864

### 8.7.1 Controller Overview

The controllers are fast-reacting, high-frequency, scalable output power controllers capable of driving two external N-MOSFETs. They are D-CAP2 controller scheme that optimizes transient responses at high load currents for such applications as CORE and DDR supplies. The output voltage is compared with internal reference voltage after divider resistors. The PWM comparator determines the timing to turn on the high-side MOSFET. The PWM comparator response maintains a very small PWM output ripple voltage. Because the device does not have a dedicated oscillator for control loop on board, switching cycle is controlled by the adaptive on-time circuit. The on-time is controlled to meet the target switching frequency by feed-forwarding the input and output voltage into the on-time one-shot timer.

The D-CAP2 control scheme has an injected ripple from the SW node that is added to the reference voltage to simulate output ripple, which eliminates the need for ESR-induced output ripple from D-CAP™ mode control. Thus, low-ESR output capacitors (such as low-cost ceramic MLCC capacitors) can be used with the controllers.
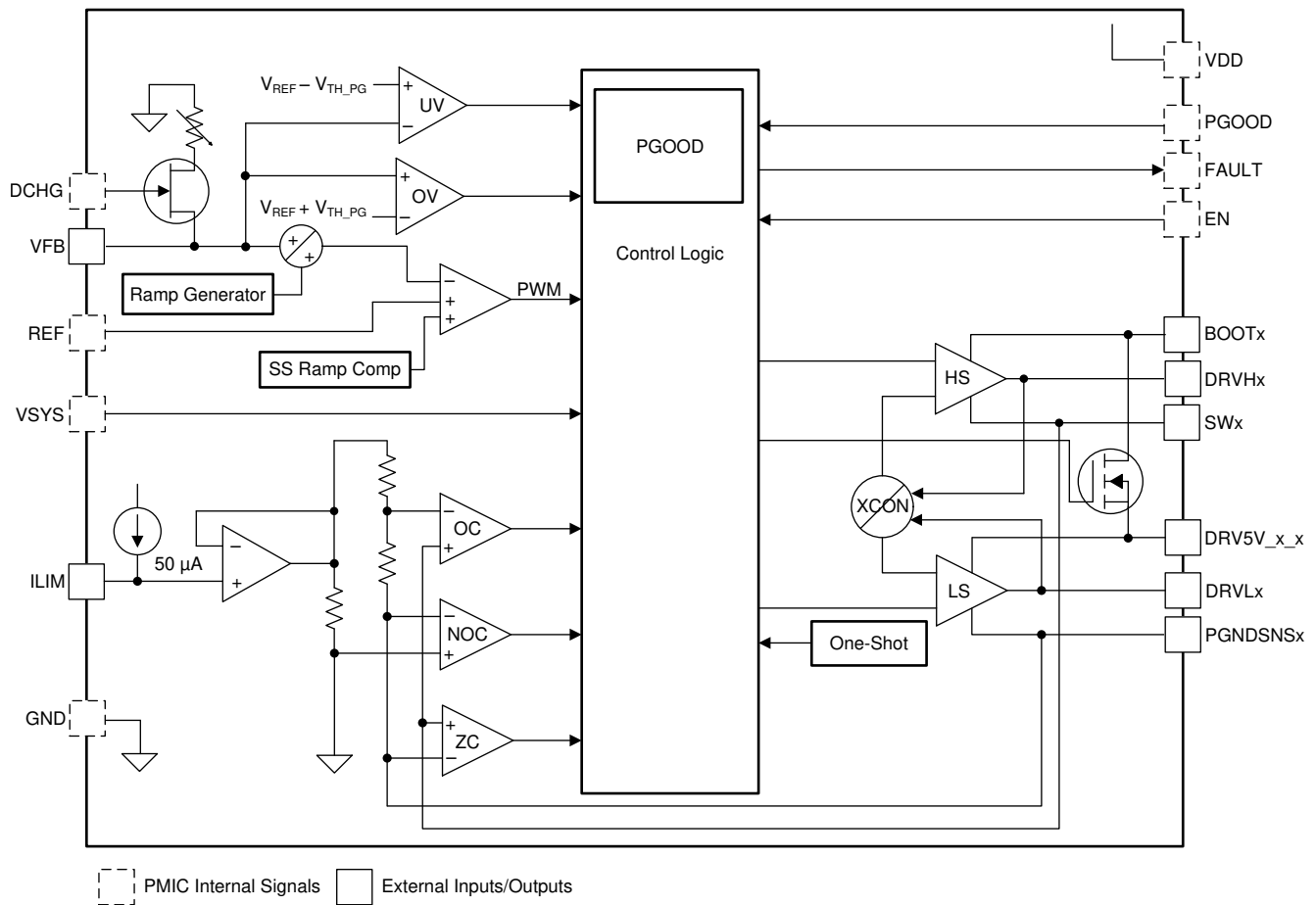


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**图 8-17. Controller Block Diagram**

### 8.7.2 Converter Overview

The PMIC synchronous step-down DCDC converters include a unique hysteretic PWM controller scheme which enables a high switching frequency converter, excellent transient and AC load regulation as well as operation with cost-competitive external components. The converter topology supports forced PWM mode as well as power-save mode operation. Power-save mode operation, or PFM mode, reduces the quiescent current consumption and ensures high conversion efficiency at light loads by skipping switch pulses. In forced PWM mode, the device operates on a quasi-fixed frequency, avoids pulse skipping, and allows filtering of the switch noise by external filter components. The PMIC device offers fixed output voltage options featuring smallest solution size by using only three external components per converter.

A significant advantage of PMIC compared to other hysteretic PWM controller topologies is its excellent AC load transient regulation capability. When the output voltage falls below the threshold of the error comparator, a switch pulse is initiated, and the high-side switch is turned on. The high-side switch remains turned on until a minimum ON-time of $t_{ONmin}$ expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high-side switch current limit. When the high-side switch turns off, the low-side switch rectifier is turned on and the inductor current ramps down until the high-side switch turns on again or the inductor current reaches zero. In forced PWM mode operation, negative inductor current is allowed to enable continuous conduction mode even at no load condition.
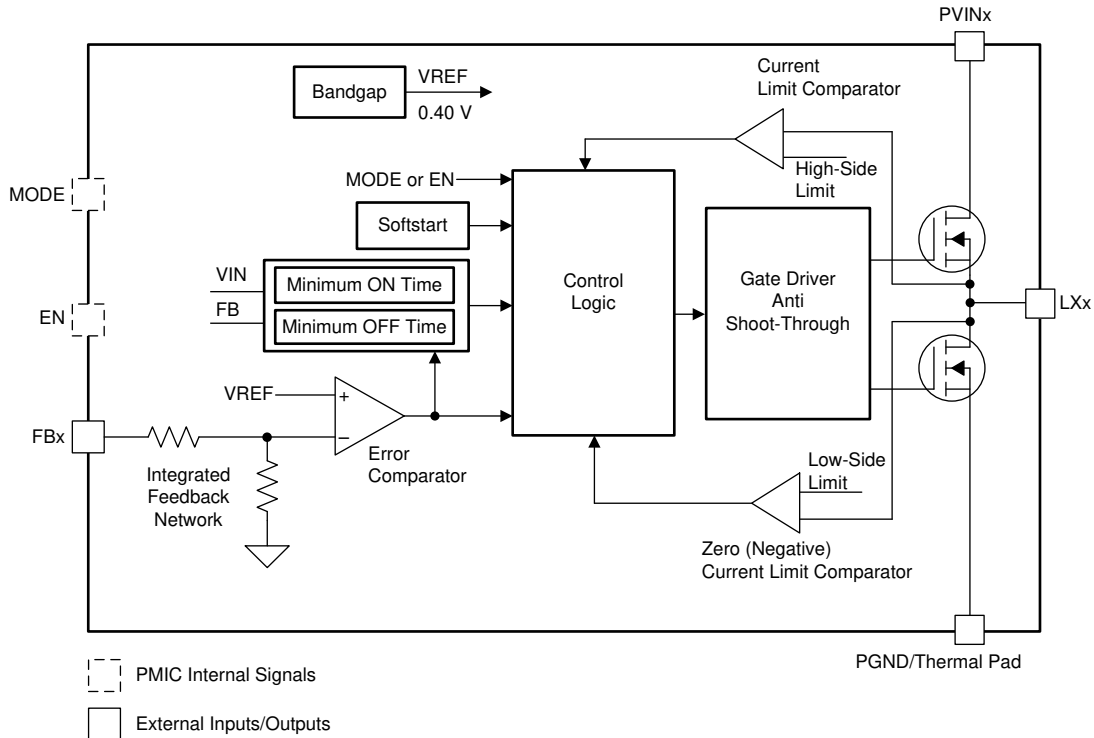


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图 **8-18. Converter Block Diagram**

### 8.7.3 DVS

BUCK1 – BUCK6 support dynamic voltage scaling (DVS) for maximum system efficiency. The VR outputs can slew up and down in 25-mV steps for the converters, and either 10-mV or 25-mV steps for the controllers, using the 7-bit voltage ID (VID) defined in 节 7.7 and 节 7.8. DVS slew rate is minimum 2.5 mV/μs. In order to meet the minimum slew rate, VID progresses to the next code at 3-μs (nom) interval per 10-mV or at 6-μs interval per 25-mV steps. When DVS is active, the VR is forced into PWM mode, unless BUCKx_DECAY = 1, to ensure the output keeps track of VID code with minimal delay. Additionally, PGOOD is masked when DVS is in progress. 图 8-19 shows an example of slew down and up from one VID to another (step size of 10 mV).

Product Folder Links: *TPS650864*
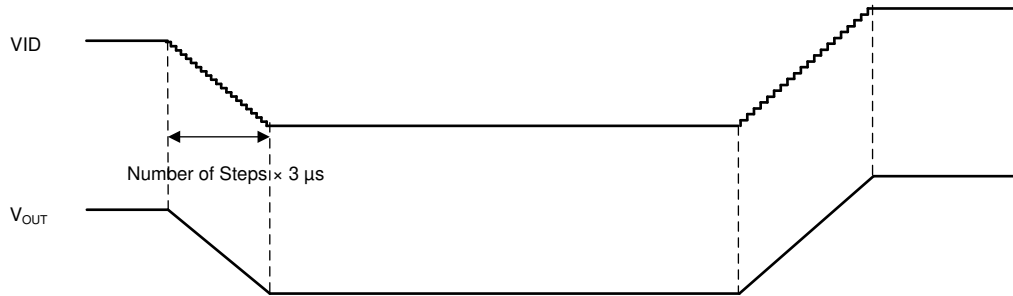
图 **8-19. DVS Timing Diagram I (BUCKx_DECAY = 0)**

As shown in 图 8-20, if a BUCKx_VID[6:0] is set to 7b000 0000, its output voltage will slew down to 0.5 V first, and then will drift down to 0 V as the SMPS stops switching. Subsequently, if a BUCKx_VID[6:0] is set to a value (neither 7b000 0000 nor 7b000 0001) when its output voltage is less than 0.5 V, the VR will ramp up to 0.5 V first with soft-start kicking in, then will slew up to target voltage in the slew rate mentioned previously. It must be noted that a fixed 200 μs of soft-start time is reserved for $V_{OUT}$ to reach 0.5 V. In this case, however, the SMPS is not forced into PWM mode as it otherwise could cause $V_{OUT}$ to droop momentarily if $V_{OUT}$ might have been drifting above 0.5 V for any reason.
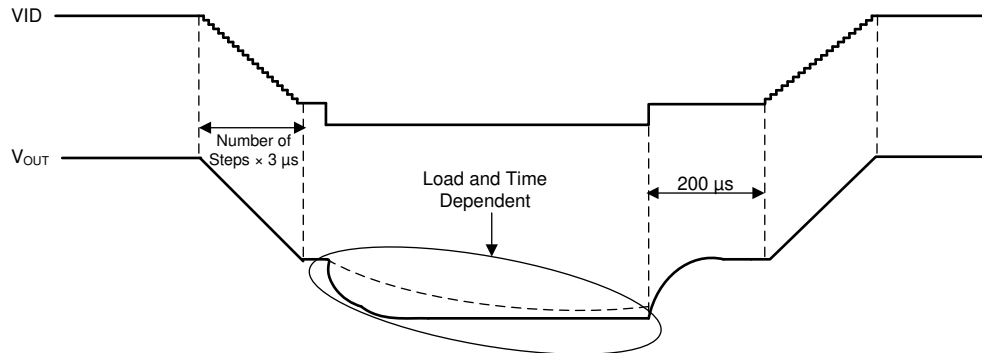
图 **8-20. DVS Timing Diagram II (BUCKx_DECAY = 0)**

### 8.7.4 Decay

In addition to DVS, BUCK1 – BUCK6 can decay down to a lower voltage when BUCKx_DECAY bit in BUCKxCTRL register is set to 1. Decay mode is only used in a downward direction of VID. The VR does not control slew rate. As both high-side and low-side FETs stop switching, the output voltage ramps down naturally, dictated by current drawn from the load and output filtering capacitance. When the VR is in the middle of decay down its PGOOD is masked until $V_{OUT}$ falls below the over-voltage (OV) threshold of the set VID value. 图 8-21 shows two cases that differ from each other as to whether $V_{OUT}$ has reached the target voltage corresponding to a new VID when the VR is commanded to slew back up to a higher voltage. In case that $V_{OUT}$ has not decayed down below VID as denoted case 2, the VR will wait for VID to catch up, and then $V_{OUT}$ will start ramping up to keep up with the VID ramp.
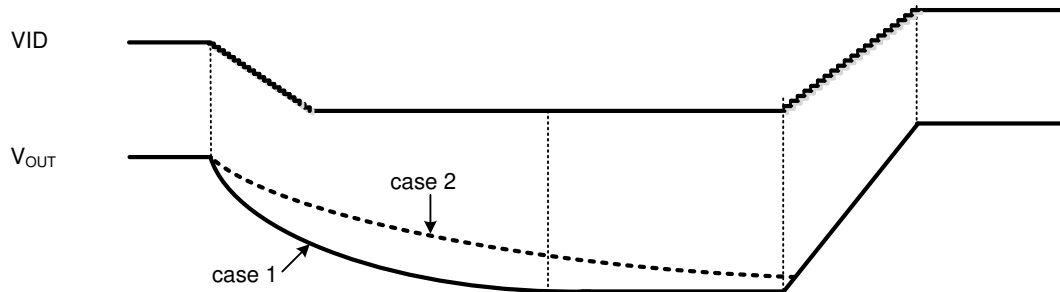


图 8-21. Decay Down to a Lower $V_{OUT}$ and Slew Up
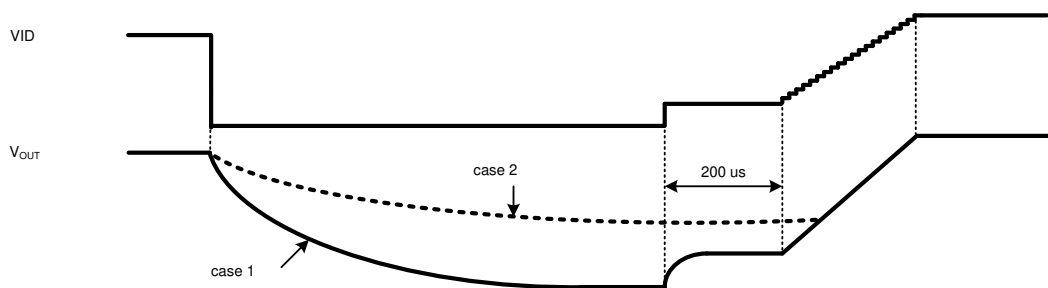


图 8-22. Decay Down to 0 V and Slew Up

Product Folder Links: *TPS650864*

### 8.7.5 Current Limit

The buck controllers (BUCK1, BUCK2, and BUCK6) have inductor-valley current-limit architecture and the current limit is programmable by an external resistor at the ILIMx pin. 方程式 1 shows the calculation for a desired resistor value, depending on specific application conditions. $I_{LIMREF}$ is the current source out of the ILIMx pin that is typically 50 µA, and $R_{DSON}$ is the maximum channel resistance of the low-side FET. The scaling factor is 1.3 to take into account all errors and temperature variations of $R_{DSON}$, $I_{LIMREF}$, and $R_{ILIM}$. Finally, 8 is another scaling factor associated with $I_{LIMREF}$.

$$R_{ILIM} = \frac{R_{DSON} \times 8 \times 1.3 \times \left( I_{LIM} - \dfrac{I_{ripple(min)}}{2} \right)}{I_{LIMREF}}$$

(1)

where

- $I_{LIM}$ is the target current limit. An appropriate margin must be allowed when determining $I_{LIM}$ from maximum output DC load current.
- $I_{ripple(min)}$ is the minimum peak-to-peak inductor ripple current for a given $V_{OUT}$.

$$I_{ripple(min)} = \frac{V_{OUT}(V_{IN(MIN)} - V_{OUT})}{L_{max} \times V_{IN(MIN)} \times f_{sw(max)}}$$

(2)

where

- $L_{max}$ is maximum inductance
- $f_{sw(max)}$ is maximum switching frequency
- $V_{IN(MIN)}$ minimum input voltage to the external power stage

The buck converter limit inductor peak current cycle-by-cycle to $I_{IND\_LIM}$ is specified in 节 7.8.

The current limit circuit also protects against reverse current going back into the low side FET from the load. When operating in Force PWM mode, the inductor current is expected to go negative so it is important to ensure that the $R_{ILIM}$ value is sufficient to account for this. If operating in PFM, this can be neglected. The equation for Force PWM minimum $R_{ILIM}$ value is:

$$R_{ILIM} \geq \frac{R_{DSON} \times 8 \times 1.3 \times \left( \dfrac{I_{ripple(max)}}{2} \right)}{I_{LIMREF}}$$

(3)

where

- $I_{ripple(max)}$ is the maximum peak-to-peak inductor ripple current for a given $V_{OUT}$.

$$I_{ripple(max)} = \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{L_{min} \times V_{IN(MAX)} \times f_{sw(min)}}$$

(4)

where

- $L_{min}$ is minimum inductance
- $f_{sw(min)}$ is minimum switching frequency
- $V_{IN(MAX)}$ maximum input voltage to the external power stage

If $R_{ILIM}$ is too low for the chosen inductor and voltage conditions, then the ripple current at no load will trigger the negative current limit, forcing the low side FET to turn off. This will eventually result in the output voltage increasing above target regulation point due to irregular duty cycle created by current limit being triggered.

Product Folder Links: *TPS650864*

## 8.8 LDOs and Load Switches

### 8.8.1 VTT LDO

Typically powered from the BUCK6 output, the VTT LDO tracks FBVOUT6 and regulates it's output to FBVOUT6 / 2. The LDO current limit is OTP dependent, and it is designed specifically to power DDR memory. The LDO core is a transconductance amplifier with large gain, and it drives a current output stage that either sources or sinks current depending on the deviation of the VTTFB pin voltage from the target regulation voltage.

### 8.8.2 LDOA1 – LDOA3

The TPS650864 device integrates three general purpose LDOs. LDOA1 is powered from a 5-V supply through the DRV5V_2_A1 pin and it can be factory configured to be an Always-On rail (stay on even in case of emergency shutdown) as long as a valid power supply is available at VSYS. See 表 8-24 for LDOA1 output voltage options. LDOA2 and LDOA3 share a power input pin (PVINLDOA2_A3). The output regulation voltages are set by writing to LDOAx_VID[3:0] bits (Reg 0x9A, 0x9B, and 0xAE). See 表 8-25 for LDOA2 and LDOA3 output voltage options. LDOA1 is controlled by the LDOA1_SWB2_CTRL register.

**表 8-24. LDOA1 Output Voltage Options**

| VID BITS | $V_{OUT}$ | VID BITS | $V_{OUT}$ | VID BITS | $V_{OUT}$ | VID BITS | $V_{OUT}$ |
|---|---|---|---|---|---|---|---|
| 0000 | 1.35 | 0100 | 1.8 | 1000 | 2.3 | 1100 | 2.85 |
| 0001 | 1.5 | 0101 | 1.9 | 1001 | 2.4 | 1101 | 3.0 |
| 0010 | 1.6 | 0110 | 2.0 | 1010 | 2.5 | 1110 | 3.3 |
| 0011 | 1.7 | 0111 | 2.1 | 1011 | 2.6 | 1111 | Not Used |

**表 8-25. LDOA2 and LDOA3 Output Voltage Options**

| VID BITS | $V_{OUT}$ | VID BITS | $V_{OUT}$ | VID BITS | $V_{OUT}$ | VID BITS | $V_{OUT}$ |
|---|---|---|---|---|---|---|---|
| 0000 | 0.70 | 0100 | 0.90 | 1000 | 1.10 | 1100 | 1.30 |
| 0001 | 0.75 | 0101 | 0.95 | 1001 | 1.15 | 1101 | 1.35 |
| 0010 | 0.80 | 0110 | 1.00 | 1010 | 1.20 | 1110 | 1.40 |
| 0011 | 0.85 | 0111 | 1.05 | 1011 | 1.25 | 1111 | 1.50 |

### 8.8.3 Load Switches

The PMIC features three general-purpose load switches. SWA1 has its own power input pin (PVINSWA1), while SWB1 and SWB2 share one power input pin (PVINSWB1_B2). All switches have built-in slew rate control during start-up to limit the inrush current.

## 8.9 Power Goods (PGOOD or PG) and GPOs

The device provides information on status of VRs through four GPO pins along with Power Good Status registers defined in 节 8.13.50 and 节 8.13.51. Power Good information of any individual VR and load switch can be assigned to be part of the PGOOD tree as defined from 节 8.13.40 to 节 8.13.47. PGOOD assertion delays are programmable from 0 ms to 15 ms for GPO1, 5 ms to 100 ms for GPO3, and 0 ms to 100 ms for GPO2 and GPO4, respectively, as are defined in 节 8.13.21 and 节 8.13.34.
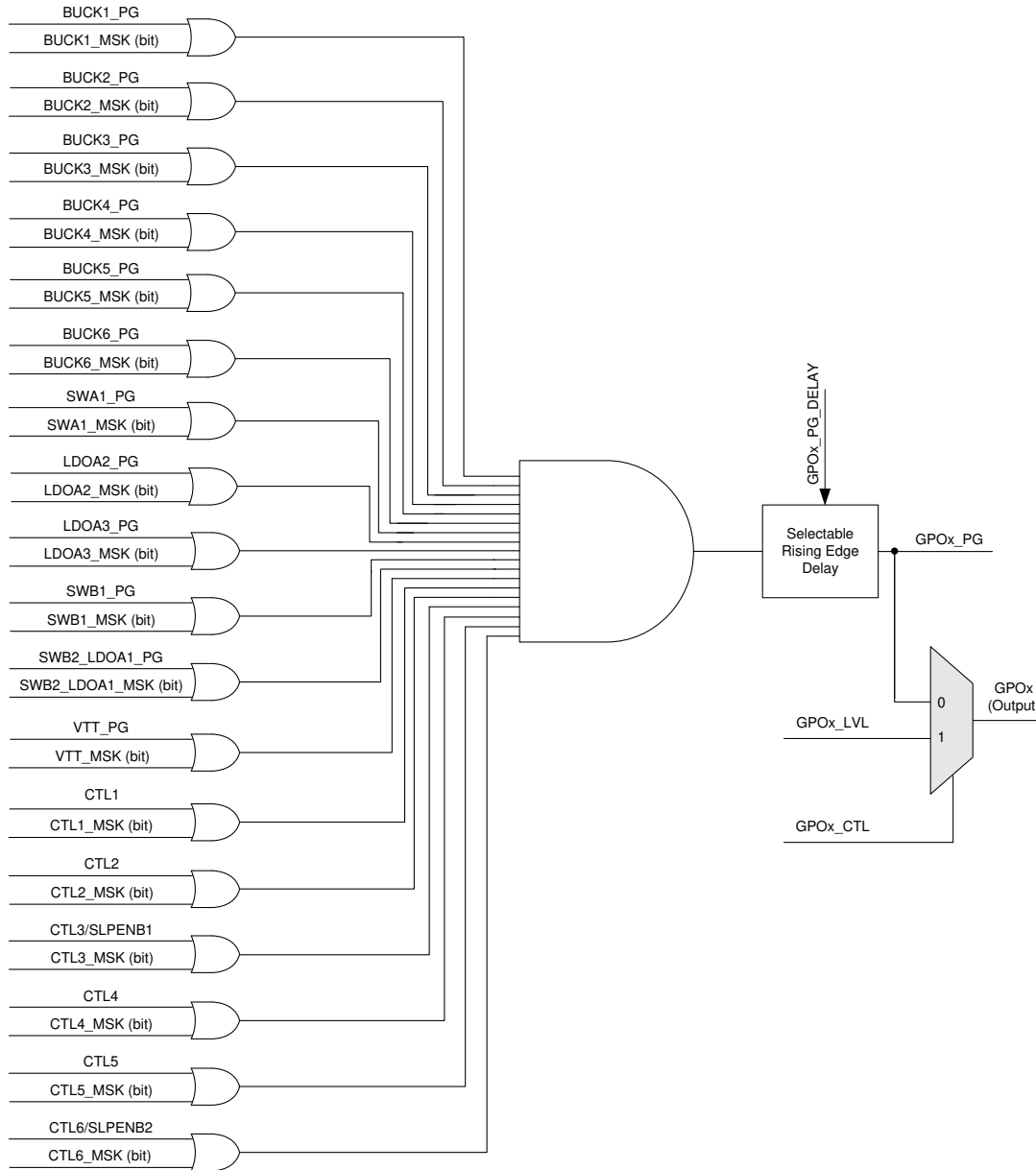
图 8-23. Power Good Tree

Alternatively, the GPOs can be used as general purpose outputs controlled by the user through I$^2$C. Refer to 节 8.13.37 for details on controlling the GPOs in I$^2$C control mode. When configured as push-pull, LDO3P3 is used for logic-level high.

## 8.10 Power Sequencing and VR Control

The device has three different ways of sequencing the rails during power up and power down:

- Rail enabled by CTLx pin
- Rail enabled by Power Good (PG) of previously enabled rail
- Rail enabled by I²C software command

A delay can be added from any CTLx pin or PG to the enable of the subjected enabled rail. This creates a very flexible device capable of many sequence options. If a rail cannot be sequenced automatically, any rail can be enabled or disabled through an I²C command.

### 8.10.1 CTLx Sequencing

The device has six control-input pins (CTL1 – CTL6) to control six SMPS regulators, three LDO regulators, and three load switches. This allows the user to define up to six distinctive groups, to which each VR can be assigned for highly flexible power sequencing. Of the six CTLx pins, CTL3 and CTL6 can be configured alternatively to active-low sleep enable pins. For instance, if a system level SLEEP state is defined such that BUCK1 output regulation voltage is lower than in the normal mode, then BUCK1 SLEEP state can be assigned to CTL3 or CTL6. By being pulled low, either CTL3 or CTL6 can be used to put BUCK1 into SLEEP state, and BUCK1 will regulate its output at a voltage defined by BUCK1_SLP_VID[6:0] in 节 8.13.23. For a demonstration of this feature, 图 8-24 shows how BUCK1 is enabled from the CTL1 pin.

### 8.10.2 PG Sequencing

Any rail can be sequenced by the Power Good of a prior rail. This can be combined with the CTLx method to allow for further sequence control and create more distinctive groups of enables than the six from CTLx. This also allows some of the CTLx pins to be freed up for other purposes such as logic input gates. For a demonstration of this feature, 图 8-24 shows how the BUCK5 is enabled from the BUCK4 PG.
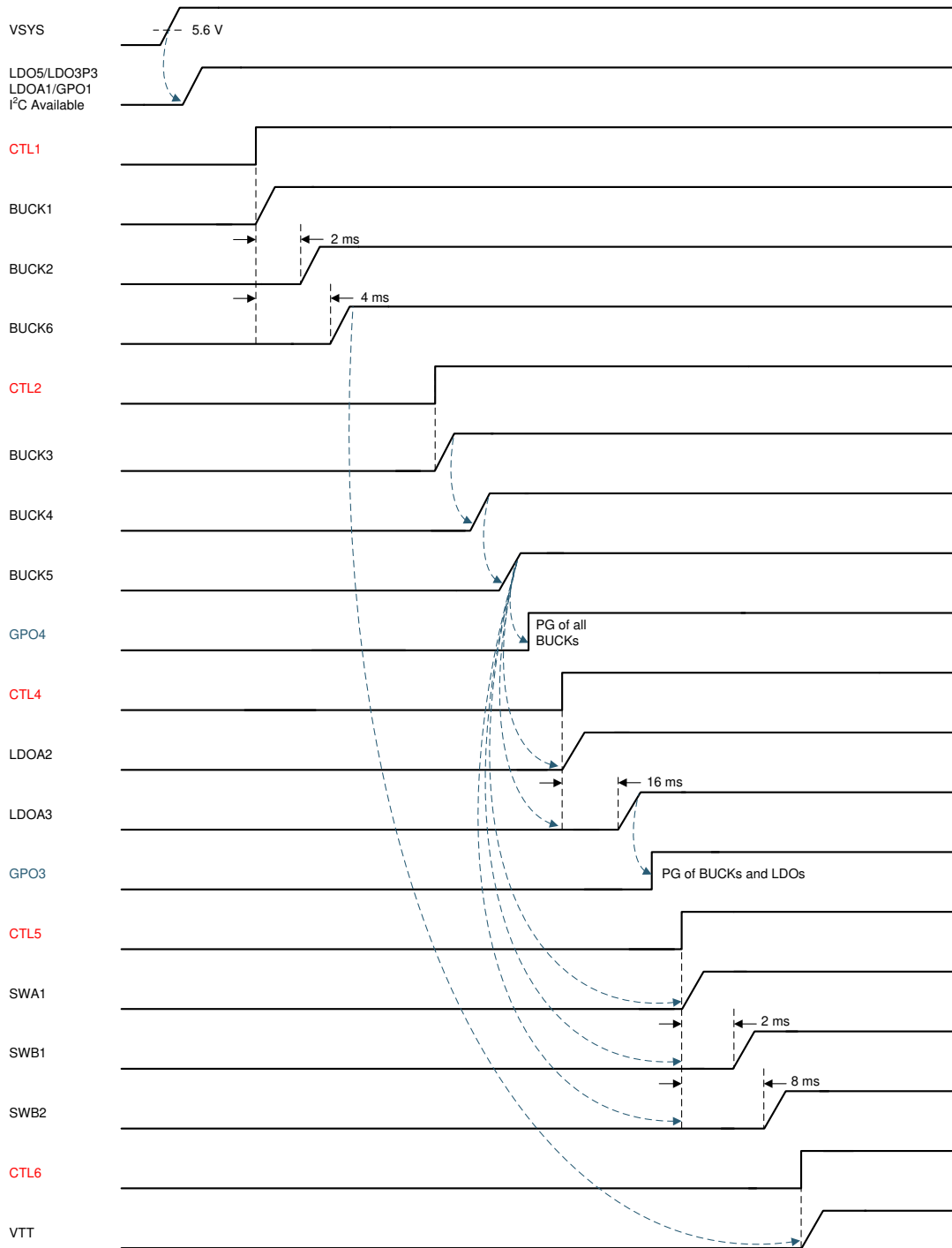
图 8-24. **Generic Power-Up Sequence Example**

Product Folder Links: *TPS650864*

### 8.10.3 Enable Delay

A delay can be added to the enable of any rail after the desired CTLx and PGs are met. This allows for the option to create additional timing groups from either CTLx pins or internal PGs. For a demonstration of this feature, 图 8-24 shows how BUCK2 and BUCK6 are enabled after BUCK1 is enabled from CTL1 pin.

### 8.10.4 Power-Up Sequence

When a valid power supply is detected at the VSYS pin as $V_{SYS}$ crosses above $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO+5V\_HYS}$, the power-up sequence is initiated by driving one of the control input pins high, followed by the rest of pins in order. 图 8-24 is an example where CTL1 – CTL4 are defined to control four groups of VRs, while GPO3 and GPO4 are defined to provide a PGOOD status of two groups. The control input pins do not necessarily have to be pulled up in a staggered manner. For instance, if CTL2 is pulled up from the preceding group of VRs before PGOOD has been asserted at GPO1, the BUCK4 enable will be delayed until the PGOOD is asserted.

For the specific sequencing of a TPS650864 device, see 表 5-1.

### 8.10.5 Power-Down Sequence

The power-down sequence can follow the CTLx pins, or be controlled with the I$^2$C commands. If the internal PGs are used for sequencing or if some rails need to ramp down before others a delay can be added to the deassertion low of the internal enable of the subjected rail. This delay can be independent of the power-up delay option. Thus, power-up and power-down sequences can be different or similar to match the specific application sequences required.

Refer to 图 8-25 for an example of a power-down sequence demonstrating the delay disable of BUCK1 and BUCK2.

For the specific sequencing of a TPS650864 device, see 表 5-1.
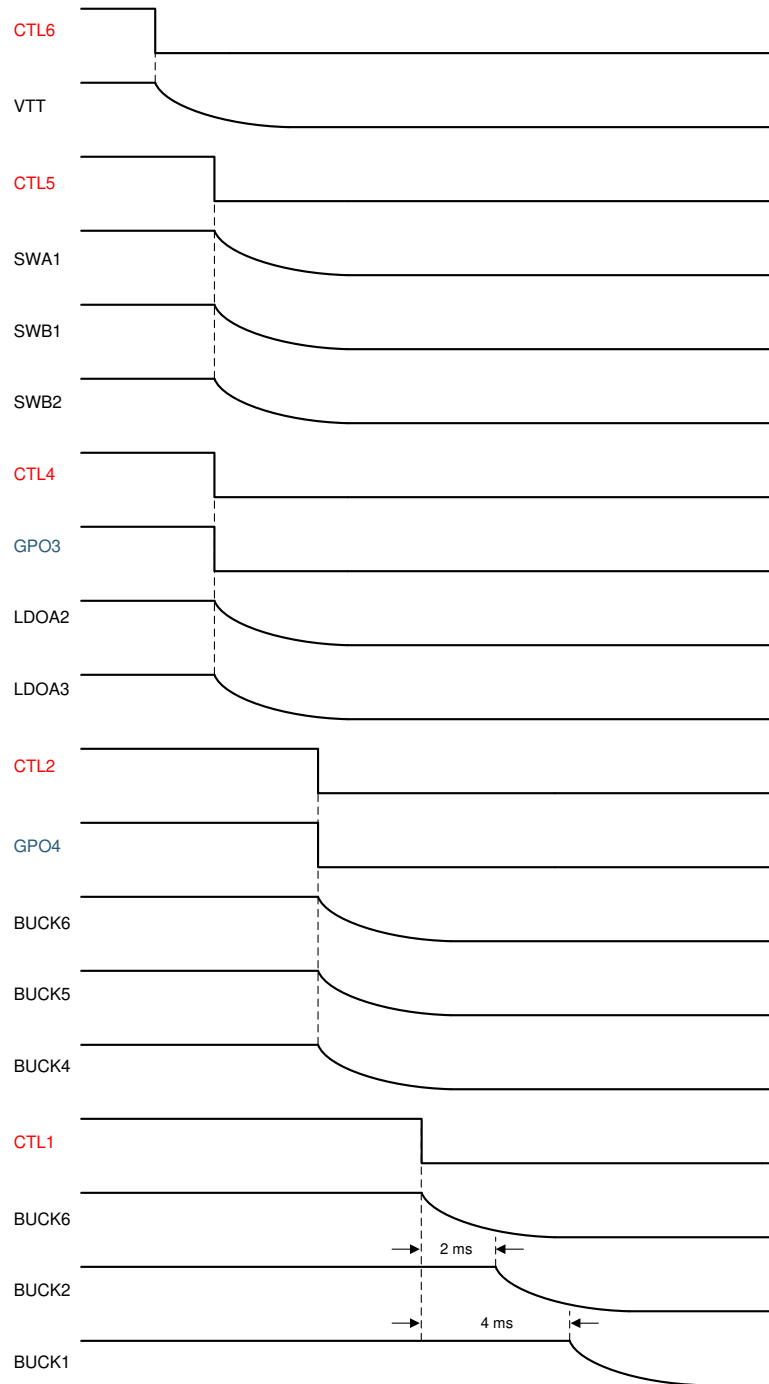
图 **8-25. Generic Power-Down Sequence Example**

Product Folder Links: *TPS650864*

**8.10.6 Sleep State Entry and Exit**
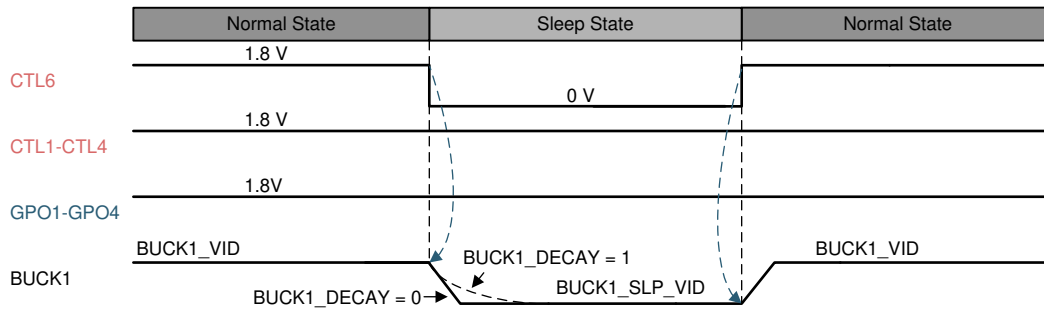


图 **8-26. Sleep State Entry and Exit Sequence Example**

图 8-26 shows an example where BUCK1 is defined to enter Sleep State in response to CTL6 going low.

---

### 备注

All PGOODs from GPO1–GPO4 can stay asserted during the entry and the exit. Depending on status of the BUCK1_DECAY bit defined in the BUCK1CTRL register, BUCK1 output will either decay or slew down to a new voltage defined in BUCK1_SLP_VID[6:0].

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**8.10.7 Emergency Shutdown**
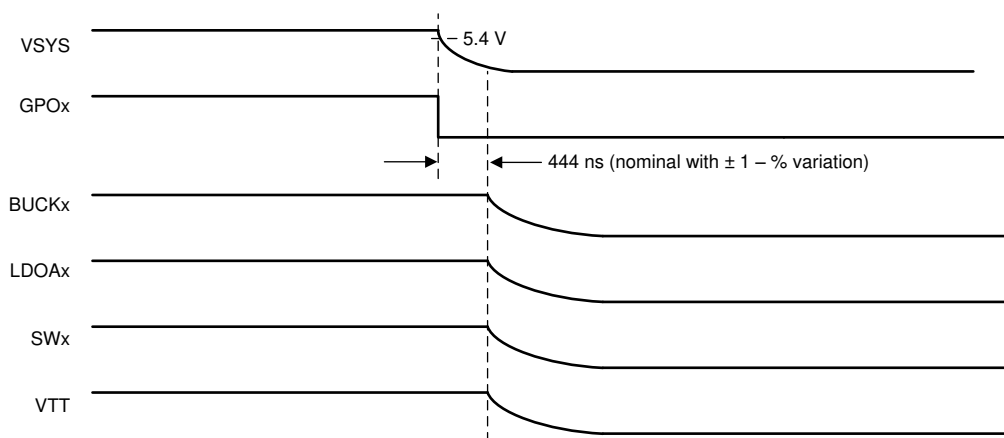


图 **8-27. Emergency Shutdown Sequence**

When $V_{SYS}$ crosses below $V_{SYS\_UVLO\_5V}$, all Power Good pins will be deasserted, and after 444 ns (nominal) of delay all VRs will shut down. Upon shutdown, all internal discharge resistors are set to 100 $\Omega$ to ensure timely decay of all VR outputs. Other conditions that will cause emergency shutdown are the die temperature rising above the critical temperature threshold ($T_{CRIT}$), deassertion of Power Good of any rail (configurable), or failure of any rail to reach power good within 10 ms of being enabled (configurable). If PMIC was shutdown by UVLO, it will wait until VSYS rises above $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$ before reloading the default OTP and checking the state of the CTLx pins. If PMIC was shutdown by temperature, it will wait until temperature drops below $T_{CRIT}$ – $T_{CRIT\_HYS}$ before reloading OTP and checking the state of the CTLx pins. If the PMIC was shutdown by power fault, it will reload OTP after disabling all rails and check the state of the CTLx pins once OTP has finished reloading.

Product Folder Links: TPS650864

## 8.11 Device Functional Modes

### 8.11.1 Off Mode

When power supply at the VSYS pin is less than $V_{SYS\_UVLO\_5V}$ (5.4-V nominal) + $V_{SYS\_UVLO\_5V\_HYS}$ (0.2-V nominal), the device is in off mode, where all output rails are disabled. If the supply voltage is greater than $V_{SYS\_UVLO\_3V}$ (3.6-V nominal) + $V_{SYS\_UVLO\_3V\_HYS}$ (0.15-V nominal) while it is still less than $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$, then the internal band-gap reference (VREF pin) along with LDO3P3 are enabled and regulated at target values.

### 8.11.2 Standby Mode

When power supply at the VSYS pin rises above $V_{SYS\_UVLO\_5V}$ + $V_{SYS\_UVLO\_5V\_HYS}$, the device enters standby mode, where all internal reference and regulators (LDO3P3 and LDO5) are up and running, and I²C interface and CTL pins are ready to respond. All default registers defined in 节 8.13 should have by now been loaded from one-time programmable (OTP) memory. Quiescent current consumption in standby mode is specified in 节 7.5.

### 8.11.3 Active Mode

The device proceeds to active mode when any output rail is enabled either through an input pin as discussed in 节 8.10 or by writing to EN bits through I²C. Output regulation voltage can also be changed by writing to VID bits defined in 节 8.13.

## 8.12 I²C Interface

The I²C interface is a 2-wire serial interface developed by NXP™ (formerly Philips Semiconductor) (see I²C-Bus Specification and user manual, Rev 4, 13 February 2012). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, DATA and CLK. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The PMIC works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when $V_{SYS}$ higher than $V_{SYS\_UVLO\_5V}$ is applied to the PMIC. The I²C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface.

The data transfer protocol for standard and fast modes are exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S-mode, and it is referred to as H/S-mode.

The PMIC device supports 7-bit addressing; however, 10-bit addressing and general call address are not supported. The default device address is 0x5E.

### 8.12.1 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high (see 图 8-28). All I$^2$C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see
图 8-29). All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an acknowledge (see 图 8-30), by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver needs to acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 图 8-28). This releases the bus and stops the communication link with the addressed slave. All I$^2$C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.
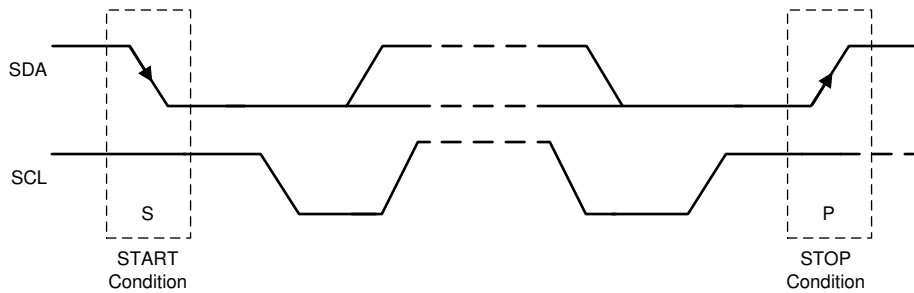


图 8-28. START and STOP Conditions
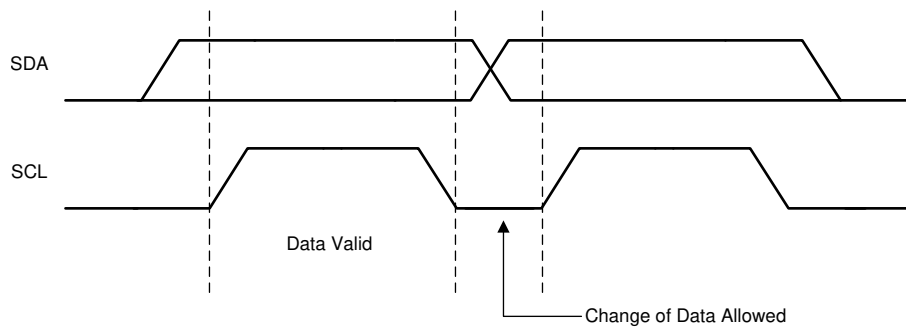


图 8-29. Bit Transfer on the I$^2$C Bus

Product Folder Links: TPS650864
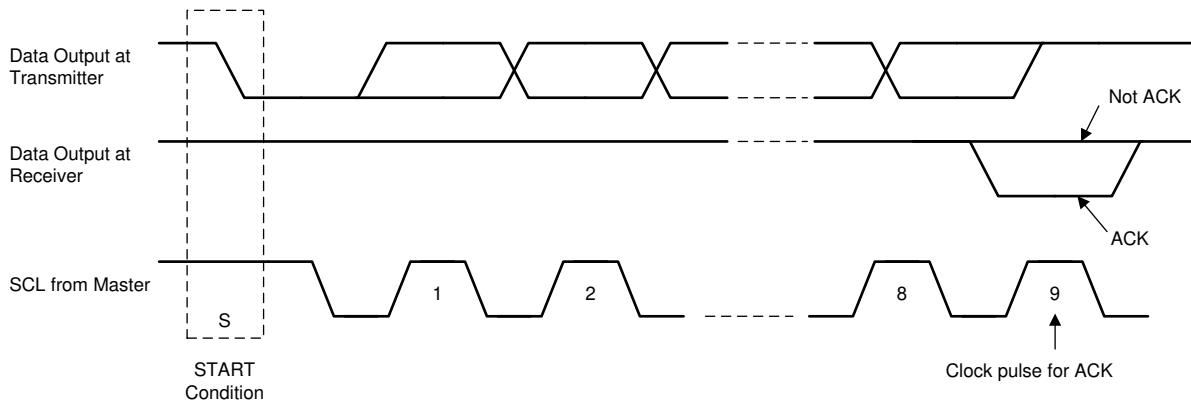
图 8-30. Acknowledge on the I²C Bus
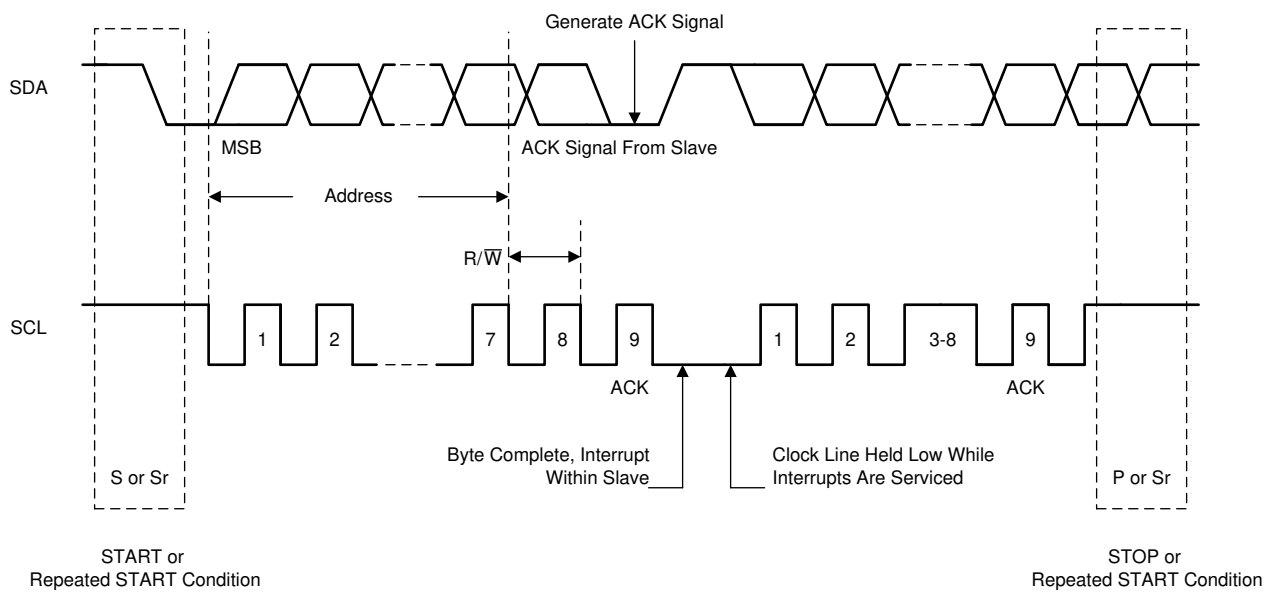


图 8-31. I²C Bus Protocol
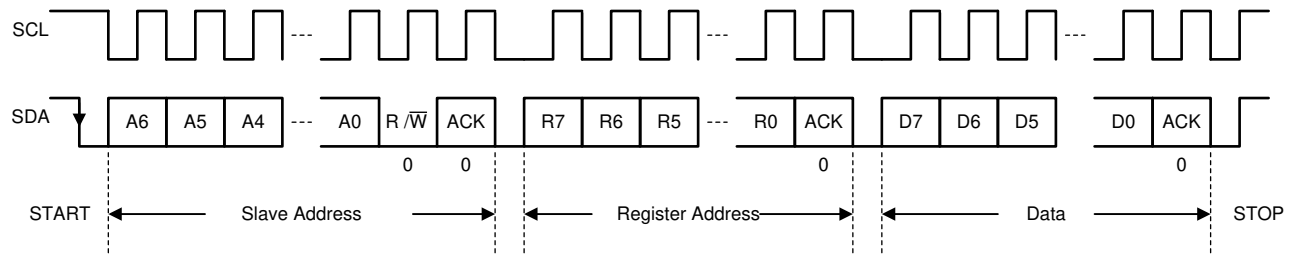
图 **8-32. I²C Interface WRITE to TPS650864 in F/S Mode**
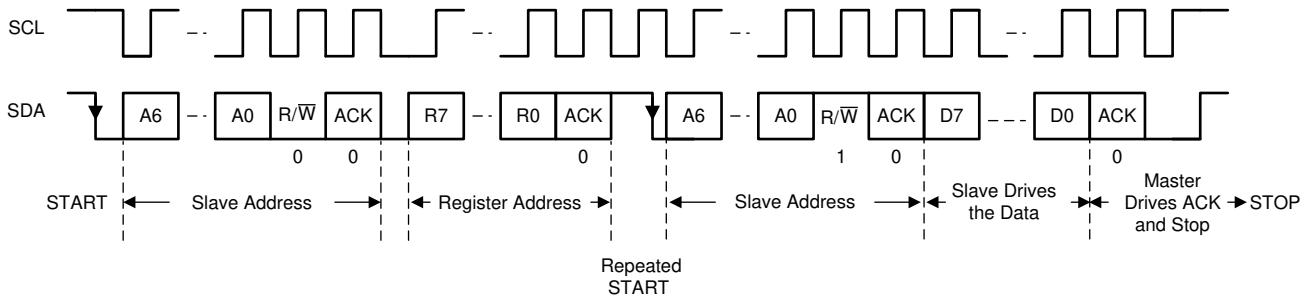


图 **8-33. I²C Interface READ from TPS650864 in F/S Mode (Only Repeated START is Supported)**

## 8.13 Register Maps

### 8.13.1 Register Map Summary

Do not attempt to write a RESERVED R/W bit to the opposite value. When the reset value of a bit register is 0bX, it means the bit value is coming from the OTP memory.

表 **8-26. Register Map Summary**

| Address | Name | Short Description |
|---------|------|-------------------|
| 00h | DEVICEID1 | Device ID code indicating revision |
| 01h | DEVICEID2 | Device ID code indicating revision |
| 02h | IRQ | Interrupt statuses |
| 03h | IRQ_MASK | Interrupt masking |
| 04h | PMIC_STAT | PMIC temperature indicator |
| 05h | SHUTDNSRC | Shutdown root cause indicator bits |
| 20h | BUCK1CTRL | BUCK1 decay control and voltage select |
| 21h | BUCK2CTRL | BUCK2 decay control and voltage select |
| 22h | BUCK3DECAY | BUCK3 decay control |
| 23h | BUCK3VID | BUCK3 voltage select |
| 24h | BUCK3SLPCTRL | BUCK3 voltage select for sleep state |
| 25h | BUCK4CTRL | BUCK4 control |
| 26h | BUCK5CTRL | BUCK5 control |
| 27h | BUCK6CTRL | BUCK6 control |
| 28h | LDOA2CTRL | LDOA2 control |
| 29h | LDOA3CTRL | LDOA3 control |
| 40h | DISCHCTRL1 | Discharge resistors for each rail control |
| 41h | DISCHCTRL2 | Discharge resistors for each rail control |
| 42h | DISCHCTRL3 | Discharge resistors for each rail control |
| 43h | PG_DELAY1 | System Power Good on GPO3 (*if GPO3 is programmed to be system PG*) |
| 91h | FORCESHUTDN | Software force shutdown |
| 92h | BUCK1SLPCTRL | BUCK1 voltage select for sleep state |
| 93h | BUCK2SLPCTRL | BUCK2 voltage select for sleep state |
| 94h | BUCK4VID | BUCK4 voltage select |
| 95h | BUCK4SLPVID | BUCK4 voltage select for sleep state |
| 96h | BUCK5VID | BUCK5 voltage select |
| 97h | BUCK5SLPVID | BUCK5 voltage select for sleep state |
| 98h | BUCK6VID | BUCK6 voltage select |
| 99h | BUCK6SLPVID | BUCK6 voltage select for sleep state |
| 9Ah | LDOA2VID | LDOA2 voltage select |
| 9Bh | LDOA3VID | LDOA3 voltage select |
| 9Ch | BUCK123CTRL | BUCK1, 2, and 3 disable and PFM/PWM mode control |
| 9Dh | PG_DELAY2 | System Power Good on GPO1, 2, and 4 (*if GPOs are programmed to be system PG*) |
| 9Fh | SWVTT_DIS | SWs and VTT I$^2$C disable bits |
| A0h | I2C_RAIL_EN1 | I$^2$C Enable control of individual rails |
| A1h | I2C_RAIL_EN2/GPOCTRL | I$^2$C Enable control of individual rails and I$^2$C controlled GPOs, high or low |
| A2h | PWR_FAULT_MASK1 | Power fault masking for individual rails |
| A3h | PWR_FAULT_MASK2 | Power fault masking for individual rails |
| A4h | GPO1PG_CTRL1 | Power good tree control for GPO1 |
| A5h | GPO1PG_CTRL2 | Power good tree control for GPO1 |

表 8-26. Register Map Summary (continued)

| Address | Name | Short Description |
|---------|------|------------------|
| A6h | GPO4PG_CTRL1 | Power good tree control for GPO4 |
| A7h | GPO4PG_CTRL2 | Power good tree control for GPO4 |
| A8h | GPO2PG_CTRL1 | Power good tree control for GPO2 |
| A9h | GPO2PG_CTRL2 | Power good tree control for GPO2 |
| AAh | GPO3PG_CTRL1 | Power good tree control for GPO3 |
| ABh | GPO3PG_CTRL2 | Power good tree control for GPO3 |
| ACh | MISCSYSPG | Power good tree control with CTL3 and CTL6 for GPO |
| ADh | VTT_DISCH_CTRL | Discharge resistor setting for VTT LDO |
| AEh | LDOA1_SWB2_CTRL | LDOA1 and SWB2 control for discharge, voltage selection, and enable |
| B0h | PG_STATUS1 | Power good statuses for individual rails |
| B1h | PG_STATUS2 | Power good statuses for individual rails |
| B2h | PWR_FAULT_STATUS1 | Power fault statuses for individual rails |
| B3h | PWR_FAULT_STATUS2 | Power fault statuses for individual rails |
| B4h | TEMPCRIT | Critical temperature indicators |
| B5h | TEMPHOT | Hot temperature indicators |

Complex bit access types are encoded to fit into small table cells. 表 8-27 shows the codes that are used for access types in this section.

表 8-27. Access Type Codes

| Access Type | Code | Description |
|-------------|------|-------------|
| Read Type | | |
| R | R | Read |
| Write Type | | |
| W | W | Write |

### 8.13.2 DEVICEID1: 1st PMIC Device and Revision ID Register (offset = 00h) [reset = X]

图 8-34. DEVICEID1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | PART_NUMBER[7] | PART_NUMBER[6] | PART_NUMBER[5] | PART_NUMBER[4] | PART_NUMBER[3] | PART_NUMBER[2] | PART_NUMBER[1] | PART_NUMBER[0] |
| TPS6508640 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086401 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| TPS6508641 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| TPS65086470 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

表 8-28. DEVICEID1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:4 | PART_NUMBER[7:4] | R | X | Device part number ID<br>**0000**: TPS65086x**0**x<br>**0001**: TPS65086x**1**x<br>...<br>**1111**: TPS65086x**F**x |
| 3:0 | PART_NUMBER[3:0] | R | X | Device part number ID<br>**0000**: TPS65086xx**0**<br>**0001**: TPS65086xx**1**<br>...<br>**1111**: TPS65086xx**F** |

### 8.13.3 DEVICEID2: 2nd PMIC Device and Revision ID Register (offset = 01h) [reset = X]

图 8-35. DEVICEID2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | REVID[1] | REVID[0] | OTP_VERSION[1] | OTP_VERSION[0] | PART_NUMBER[11] | PART_NUMBER[10] | PART_NUMBER[9] | PART_NUMBER[8] |
| TPS6508640 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| TPS65086401 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| TPS6508641 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| TPS65086470 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

表 8-29. DEVICEID2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | REVID[1:0] | R | X | Silicon revision ID |
| 5:4 | OTP_VERSION[1:0] | R | X | OTP variation ID<br>**00**: A<br>**01**: B<br>**10**: C<br>**11**: D |
| 3:0 | PART_NUMBER[11:8] | R | X | Device part number ID<br>**0100**: TPS65086**4**xx |

Product Folder Links: *TPS650864*

### 8.13.4 IRQ: PMIC Interrupt Register (offset = 02h) [reset = 0000 0000]

图 8-36. IRQ Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | FAULT | RESERVED | RESERVED | RESERVED | SHUTDN | RESERVED | RESERVED | DIETEMP |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R | R | R | R/W | R | R | R/W |

表 8-30. IRQ Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | FAULT | R/W | 0 | Fault interrupt. Asserted when either condition occurs: power fault of any rail, or die temperature crosses over the critical temperature threshold ($T_{CRIT}$). The user can read **Reg. 0xB2 – 0xB6** to determine what has caused the interrupt.<br>**0**: Not asserted<br>**1**: Asserted. Host to write 1b to clear. |
| 3 | SHUTDN | R/W | 0 | Asserted when PMIC shuts down. To clear indicator, SHUTDNSRC must be cleared first, see 节 8.13.7<br>**0**: Not asserted.<br>**1**: Asserted. Host to write 1b to clear. |
| 0 | DIETEMP | R/W | 0 | Die temp interrupt. Asserted when PMIC die temperature crosses above the hot temperature threshold ($T_{HOT}$).<br>**0**: Not asserted.<br>**1**: Asserted. Host to write 1b to clear. |

### 8.13.5 IRQ_MASK: PMIC Interrupt Mask Register (offset = 03h) [reset = 1111 1111]

图 8-37. IRQ_MASK Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | MFAULT | RESERVED | RESERVED | RESERVED | msHUTDN | RESERVED | RESERVED | MDIETEMP |
| TPS650864 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Access | R/W | R | R | R | R/W | R | R | R/W |

表 8-31. IRQ_MASK Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | MFAULT | R/W | 1 | FAULT interrupt mask.<br>**0**: Not masked.<br>**1**: Masked. |
| 3 | msHUTDN | R/W | 1 | PMIC shutdown event interrupt mask<br>**0**: Not masked.<br>**1**: Masked. |
| 0 | MDIETEMP | R/W | 1 | Die temp interrupt mask.<br>**0**: Not masked.<br>**1**: Masked. |

Product Folder Links: TPS650864

### 8.13.6 PMICSTAT: PMIC Status Register (offset = 04h) [reset = 0000 0000]

图 8-38. PMICSTAT Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | SDIETEMP |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

表 8-32. PMICSTAT Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 0 | SDIETEMP | R | 0 | PMIC die temperature status.<br>**0**: PMIC die temperature is below $T_{HOT}$.<br>**1**: PMIC die temperature is above $T_{HOT}$. |

### 8.13.7 SHUTDNSRC: PMIC Shut-Down Event Register (offset = 05h) [reset = 0000 0000]

图 8-39. SHUTDNSRC Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | COLDOFF | UVLO | PWR_FAULT | CRITTEMP |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R/W | R/W | R/W | R/W |

表 8-33. SHUTDNSRC Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3 | COLDOFF | R/W | 0 | Set by PMIC cleared by host. Host to write 1b to clear.<br>**0**: Cleared<br>**1**: N/A. Not enabled for existing OTPs. |
| 2 | UVLO | R/W | 0 | Set by PMIC cleared by host. Host to write 1b to clear.<br>**0**: Cleared<br>**1**: PMIC was shut down due to a UVLO event ($V_{SYS}$ crosses below 5.4 V). Assertion of this bit sets the SHUTDN bit in 节 8.13.4. |
| 1 | PWR_FAULT | R/W | 0 | Set by PMIC cleared by host. Host to write 1b to clear.<br>**0**: Cleared<br>**1**: PMIC was shut down due to an unmasked power fault event. Assertion of this bit sets the SHUTDN bit in 节 8.13.4. The source of the power fault can be determined from the PWR_FAULT registers (0xB2 and 0xB3). Overcurrent protection will limit $I_{OUT}$ and typically cause a power fault as $V_{OUT}$ droops. |
| 0 | CRITTEMP | R/W | 0 | Set by PMIC cleared by host. Host to write 1b to clear.<br>**0**: Cleared<br>**1**: PMIC was shut down due to the rise of PMIC die temperature above critical temperature threshold ($T_{CRIT}$). Assertion of this bit sets the SHUTDN bit in 节 8.13.4. |

Product Folder Links: TPS650864

### 8.13.8 BUCK1CTRL: BUCK1 Control Register (offset = 20h) [reset = X]

图 8-40. BUCK1CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK1_VID[6] | BUCK1_VID[5] | BUCK1_VID[4] | BUCK1_VID[3] | BUCK1_VID[2] | BUCK1_VID[1] | BUCK1_VID[0] | BUCK1_DECAY |
| TPS6508640 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS65086401 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| TPS6508641 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| TPS65086470 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-34. BUCK1CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK1_VID[6:0] | R/W | X | This field sets the BUCK1 regulator output regulation voltage in normal mode.<br>See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |
| 0 | BUCK1_DECAY | R/W | X | Decay Bit<br>**0**: The output slews down to a lower voltage set by the VID bits.<br>**1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

### 8.13.9 BUCK2CTRL: BUCK2 Control Register (offset = 21h) [reset = X]

图 8-41. BUCK2CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK2_VID[6] | BUCK2_VID[5] | BUCK2_VID[4] | BUCK2_VID[3] | BUCK2_VID[2] | BUCK2_VID[1] | BUCK2_VID[0] | BUCK2_DECAY |
| TPS6508640 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| TPS65086401 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| TPS6508641 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| TPS65086470 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-35. BUCK2CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK2_VID[6:0] | R/W | X | This field sets the BUCK2 regulator output regulation voltage in normal mode.<br>See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |
| 0 | BUCK2_DECAY | R/W | X | Decay Bit<br>**0**: The output slews down to a lower voltage set by the VID bits.<br>**1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

### 8.13.10 BUCK3DECAY: BUCK3 Decay Control Register (offset = 22h) [reset = X]

图 8-42. BUCK3DECAY Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SPARE | SPARE | SPARE | SPARE | SPARE | SPARE | SPARE | BUCK3_DECAY |
| TPS6508640 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086401 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| TPS6508641 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| TPS65086470 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-36. BUCK3DECAY Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | SPARE | R/W | X | Unused. Typically mirror BUCK3_VID by default in OTP. |
| 0 | BUCK3_DECAY | R/W | X | Decay Bit<br>**0**: The output slews down to a lower voltage set by the VID bits.<br>**1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

### 8.13.11 BUCK3VID: BUCK3 VID Register (offset = 23h) [reset = X]

图 8-43. BUCK3VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK3_VID[6] | BUCK3_VID[5] | BUCK3_VID[4] | BUCK3_VID[3] | BUCK3_VID[2] | BUCK3_VID[1] | BUCK3_VID[0] | RESERVED |
| TPS6508640 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086401 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| TPS6508641 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| TPS65086470 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

表 8-37. BUCK3VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK3_VID[6:0] | R/W | X | This field sets the BUCK3 regulator output regulation voltage in normal mode.<br>See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |

Product Folder Links: *TPS650864*

### 8.13.12 BUCK3SLPCTRL: BUCK3 Sleep Control VID Register (offset = 24h) [reset = X]

图 8-44. BUCK3SLPCTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK3_SLP _ VID[6] | BUCK3_SLP _ VID[5] | BUCK3_SLP _ VID[4] | BUCK3_SLP _ VID[3] | BUCK3_SLP _ VID[2] | BUCK3_SLP _ VID[1] | BUCK3_SLP _ VID[0] | BUCK3_SLP _ EN |
| TPS6508640 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086401 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| TPS6508641 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| TPS65086470 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-38. BUCK3SLPCTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK3_SLP_VID[6:0] | R/W | X | This field sets the BUCK3 regulator output regulation voltage in sleep mode if BUCK3_SLP_EN = 1b.<br>See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |
| 0 | BUCK3_SLP_EN | R/W | X | BUCK3 sleep mode enable. BUCK3 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin.<br>**0**: Disable. Uses BUCK3_VID in all cases.<br>**1**: Enabled. Uses BUCK3_SLP_VID when assigned sleep pin is low. |

### 8.13.13 BUCK4CTRL: BUCK4 Control Register (offset = 25h) [reset = X]

图 8-45. BUCK4CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | BUCK4_SLP _ EN[1] | BUCK4_SLP _ EN[0] | RESERVED | RESERVED | BUCK4_ MODE | BUCK4_DIS |
| TPS6508640 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| TPS65086401 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS6508641 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| TPS65086470 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-39. BUCK4CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5:4 | BUCK4_SLP_EN | R/W | X | BUCK4 sleep mode enable. BUCK4 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin.<br>**00**: Disable. Uses BUCK4_VID in all cases.<br>**11**: Enabled. Uses BUCK4_SLP_VID when assigned sleep pin is low.<br>**01,10**: Reserved. Do not write these values. |
| 3:2 | RESERVED | R/W | 11 | Reserved bits. Always write to 11. |
| 1 | BUCK4_MODE | R/W | X | This field sets the BUCK4 regulator operating mode.<br>**0**: Automatic mode<br>**1**: Forced PWM mode |
| 0 | BUCK4_DIS | R/W | X | BUCK4 Disable Bit. Writing 0 to this bit forces BUCK4 to turn off regardless of any control input pin (CTL1 – CTL6) status.<br>**0**: Disable<br>**1**: Enable |

### 8.13.14 BUCK5CTRL: BUCK5 Control Register (offset = 26h) [reset = X]

图 8-46. BUCK5CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | BUCK5_SLP_EN[1] | BUCK5_SLP_EN[0] | RESERVED | RESERVED | BUCK5_MODE | BUCK5_DIS |
| TPS6508640 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| TPS65086401 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| TPS6508641 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| TPS65086470 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-40. BUCK5CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5:4 | BUCK5_SLP_EN | R/W | X | BUCK5 sleep mode enable. BUCK5 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin.<br>**00**: Disable. Uses BUCK5_VID in all cases.<br>**11**: Enabled. Uses BUCK5_SLP_VID when assigned sleep pin is low.<br>**01,10**: Reserved. Do not write these values. |
| 3:2 | RESERVED | R/W | 11 | Reserved bits. Always write to 11. |
| 1 | BUCK5_MODE | R/W | X | This field sets the BUCK5 regulator operating mode.<br>**0**: Automatic mode<br>**1**: Forced PWM mode |
| 0 | BUCK5_DIS | R/W | X | BUCK5 Disable Bit. Writing 0 to this bit forces BUCK5 to turn off regardless of any control input pin (CTL1 – CTL6) status.<br>**0**: Disable.<br>**1**: Enable. |

### 8.13.15 BUCK6CTRL: BUCK6 Control Register (offset = 27h) [reset = X]

图 8-47. BUCK6CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | BUCK6_SLP_EN[1] | BUCK6_SLP_EN[0] | RESERVED | RESERVED | BUCK6_MODE | BUCK6_DIS |
| TPS6508640 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| TPS65086401 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| TPS6508641 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| TPS65086470 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-41. BUCK6CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5:4 | BUCK6_SLP_EN | R/W | X | BUCK6 sleep mode enable. BUCK6 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin.<br>**00**: Disable. Uses BUCK6_VID in all cases.<br>**11**: Enabled. Uses BUCK6_SLP_VID when assigned sleep pin is low.<br>**01,10**: Reserved. Do not write these values. |
| 3:2 | RESERVED | R/W | 11 | Reserved bits. Always write to 11. |
| 1 | BUCK6_MODE | R/W | X | This field sets the BUCK6 regulator operating mode.<br>**0**: Automatic mode<br>**1**: Forced PWM mode |

Product Folder Links: *TPS650864*

表 8-41. BUCK6CTRL Register Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 0 | BUCK6_DIS | R/W | X | BUCK6 Disable Bit. Writing 0 to this bit forces BUCK6 to turn off regardless of any control input pin (CTL1 – CTL6) status.<br>**0**: Disable.<br>**1**: Enable. |

### 8.13.16 LDOA2CTRL: LDOA2 Control Register (offset = 28h) [reset = X]

图 8-48. LDOA2CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | LDOA2_SLP_EN[1] | LDOA2_SLP_EN[0] | RESERVED | RESERVED | RESERVED | LDOA2_DIS |
| TPS6508640 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| TPS65086401 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| TPS6508641 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| TPS65086470 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-42. LDOA2CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5:4 | LDOA2_SLP_EN | R/W | X | LDOA2 sleep mode enable. LDOA2 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin.<br>**00**: Disable. Uses LDOA2_VID in all cases.<br>**11**: Enabled. Uses LDOA2_SLP_VID when assigned sleep pin is low.<br>**01,10**: Reserved. Do not write these values. |
| 3:1 | RESERVED | R/W | 110 | Reserved bits. Always write to '110'. |
| 0 | LDOA2_DIS | R/W | X | LDOA2 Disable Bit. Writing 0 to this bit forces LDOA2 to turn off regardless of any control input pin (CTL1 – CTL6) status.<br>**0**: Disable.<br>**1**: Enable. |

### 8.13.17 LDOA3CTRL: LDOA3 Control Register (offset = 29h) [reset = X]

图 8-49. LDOA3CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | LDOA3_SLP_EN[1] | LDOA3_SLP_EN[0] | RESERVED | RESERVED | RESERVED | LDOA3_DIS |
| TPS6508640 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| TPS65086401 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| TPS6508641 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| TPS65086470 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-43. LDOA3CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5:4 | LDOA3_SLP_EN | R/W | X | LDOA3 sleep mode enable. LDOA3 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin.<br>**00**: Disable. Uses LDOA3_VID in all cases.<br>**11**: Enabled. Uses LDOA3_SLP_VID when assigned sleep pin is low.<br>**01,10**: Reserved. Do not write these values. |
| 3:1 | RESERVED | R/W | 110 | Reserved bits. Always write to '110'. |

表 **8-43. LDOA3CTRL Register Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 0 | LDOA3_DIS | R/W | X | LDOA3 Disable Bit. Writing 0 to this bit forces LDOA3 to turn off regardless of any control input pin (CTL1 – CTL6) status.<br>**0**: Disable<br>**1**: Enable |

Product Folder Links: *TPS650864*

### 8.13.18 DISCHCTRL1: 1st Discharge Control Register (offset = 40h) [reset = X]

All xx_DISCHG[1:0] bits internally set to 00 whenever the corresponding VR is enabled.

图 8-50. DISCHCTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK4_DISCHG[1] | BUCK4_DISCHG[0] | BUCK3_DISCHG[1] | BUCK3_DISCHG[0] | BUCK2_DISCHG[1] | BUCK2_DISCHG[0] | BUCK1_DISCHG[1] | BUCK1_DISCHG[0] |
| TPS6508640 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| TPS65086401 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| TPS6508641 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| TPS65086470 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-44. DISCHCTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | BUCK4_DISCHG[1:0] | R/W | X | BUCK4 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |
| 5:4 | BUCK3_DISCHG[1:0] | R/W | X | BUCK3 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |
| 3:2 | BUCK2_DISCHG[1:0] | R/W | X | BUCK2 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |
| 1:0 | BUCK1_DISCHG[1:0] | R/W | X | BUCK1 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |

### 8.13.19 DISCHCTRL2: 2nd Discharge Control Register (offset = 41h) [reset = X]

All xx_DISCHG[1:0] bits internally set to 00 whenever the corresponding VR is enabled.

#### 图 8-51. DISCHCTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2_DISCHG[1] | LDOA2_DISCHG[0] | SWA1_DISCHG[1] | SWA1_DISCHG[0] | BUCK6_DISCHG[1] | BUCK6_DISCHG[0] | BUCK5_DISCHG[1] | BUCK5_DISCHG[0] |
| TPS6508640 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| TPS65086401 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| TPS6508641 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| TPS65086470 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

#### 表 8-45. DISCHCTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | LDOA2_DISCHG[1:0] | R/W | X | LDOA2 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |
| 5:4 | SWA1_DISCHG[1:0] | R/W | X | SWA1 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |
| 3:2 | BUCK6_DISCHG[1:0] | R/W | X | BUCK6 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |
| 1:0 | BUCK5_DISCHG[1:0] | R/W | X | BUCK5 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |

Product Folder Links: *TPS650864*

### 8.13.20 DISCHCTRL3: 3rd Discharge Control Register (offset = 42h) [reset = X]

All xx_DISCHG[1:0] bits internally set to 00 whenever the corresponding VR is enabled.

图 8-52. DISCHCTRL3 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | SWB2_DISCHG[1] | SWB2_DISCHG[0] | SWB1_DISCHG[1] | SWB1_DISCHG[0] | LDOA3_DISCHG[1] | LDOA3_DISCHG[0] |
| TPS6508640 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| TPS65086401 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| TPS6508641 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| TPS65086470 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-46. DISCHCTRL3 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5:4 | SWB2_DISCHG[1:0] | R/W | X | SWB2 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |
| 3:2 | SWB1_DISCHG[1:0] | R/W | X | SWB1 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |
| 1:0 | LDOA3_DISCHG[1:0] | R/W | X | LDOA3 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |

### 8.13.21 PG_DELAY1: 1st Power Good Delay Register (offset = 43h) [reset = X]

Programmable Power Good delay for GPO3 pin, measured from the moment when all VRs assigned to GPO3 pin reach their regulation range to Power Good assertion. This is an optional register as the PMIC can be programmed for system PG, level shifter or I$^2$C controller GPO.

图 8-53. PG_DELAY1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | GPO3_PG_DELAY[2] | GPO3_PG_DELAY[1] | GPO3_PG_DELAY[0] |
| TPS6508640 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| TPS65086401 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| TPS6508641 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| TPS65086470 | 0 | 0 | 0 | 0 | 0 | — | — | — |
| Access | R | R | R | R | R | R/W | R/W | R/W |

表 8-47. PG_DELAY1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 2:0 | GPO3_PG_DELAY[2:0] | R/W | X | Programmable delay Power Good or level shifter for GPO3 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation.<br>**000**: 2.5 ms<br>**001**: 5.0 ms<br>**010**: 10 ms<br>**011**: 15 ms<br>**100**: 20 ms<br>**101**: 50 ms<br>**110**: 75 ms<br>**111**: 100 ms<br>—: Bits not used. If GPO3 is controlled by I$^2$C rather than PG and is not used internally for VTT LDO enable, these bits have no impact. Default is set to 0b. |

Product Folder Links: *TPS650864*

### 8.13.22 FORCESHUTDN: Force Emergency Shutdown Control Register (offset = 91h) [reset = 0000 0000]

**图 8-54. FORCESHUTDN Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | SDWN |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R/W |

**表 8-48. FORCESHUTDN Register Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 0 | SDWN | R/W | 0 | Forces reset of the PMIC and reset of all registers. The bit is self-clearing. PMIC does not generate I$^2$C ACK for this command because it goes into emergency shutdown. <br> **0**: No action. <br> **1**: PMIC initiates emergency shutdown. |

### 8.13.23 BUCK1SLPCTRL: BUCK1 Sleep Control Register (offset = 92h) [reset = X]

**图 8-55. BUCK1SLPCTRL Register**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK1_ SLP_ VID[6] | BUCK1_ SLP_ VID[5] | BUCK1_ SLP_ VID[4] | BUCK1_ SLP_ VID[3] | BUCK1_ SLP_ VID[2] | BUCK1_ SLP_ VID[1] | BUCK1_ SLP_ VID[0] | BUCK1_ SLP_ EN |
| TPS6508640 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS65086401 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| TPS6508641 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| TPS65086470 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

**表 8-49. BUCK1SLPCTRL Register Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK1_SLP_VID[6:0] | R/W | X | This field sets the BUCK1 regulator output regulation voltage in sleep mode. <br> See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for V$_{OUT}$ options. |
| 0 | BUCK1_SLP_EN | R/W | X | BUCK1 sleep mode enable. BUCK1 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. <br> **0**: Disable. Uses BUCK1_VID in all cases. <br> **1**: Enabled. Uses BUCK1_SLP_VID when assigned sleep pin is low. |

### 8.13.24 BUCK2SLPCTRL: BUCK2 Sleep Control Register (offset = 93h) [reset = X]

图 8-56. BUCK2SLPCTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK2_SLP _ VID[6] | BUCK2_SLP _ VID[5] | BUCK2_SLP _ VID[4] | BUCK2_SLP _ VID[3] | BUCK2_SLP _ VID[2] | BUCK2_SLP _ VID[1] | BUCK2_SLP _ VID[0] | BUCK2_SLP _ EN |
| TPS6508640 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| TPS65086401 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| TPS6508641 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| TPS65086470 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-50. BUCK2SLPCTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK2_SLP_VID[6:0] | R/W | X | This field sets the BUCK2 regulator output regulation voltage in sleep mode. See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |
| 0 | BUCK2_SLP_EN | R/W | X | BUCK2 sleep mode enable. BUCK2 is factory configured to switch to sleep mode voltage either by CTL3/SLPENB1 pin or by CTL6/SLPENB2 pin. **0**: Disable. Uses BUCK2_VID in all cases. **1**: Enabled. Uses BUCK2_SLP_VID when assigned sleep pin is low. |

### 8.13.25 BUCK4VID: BUCK4 VID Register (offset = 94h) [reset = X]

图 8-57. BUCK4VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK4_ VID[6] | BUCK4_ VID[5] | BUCK4_ VID[4] | BUCK4_ VID[3] | BUCK4_ VID[2] | BUCK4_ VID[1] | BUCK4_ VID[0] | BUCK4_ DECAY |
| TPS6508640 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS65086401 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS6508641 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS65086470 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-51. BUCK4VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK4_VID[6:0] | R/W | X | This field sets the BUCK4 regulator output regulation voltage in normal mode. See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |
| 0 | BUCK4_DECAY | R/W | X | Decay Bit **0**: The output slews down to a lower voltage set by the VID bits. **1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

Product Folder Links: *TPS650864*

### 8.13.26 BUCK4SLPVID: BUCK4 Sleep VID Register (offset = 95h) [reset = X]

图 8-58. BUCK4SLPVID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK4_SLP _ VID[6] | BUCK4_SLP _ VID[5] | BUCK4_SLP _ VID[4] | BUCK4_SLP _ VID[3] | BUCK4_SLP _ VID[2] | BUCK4_SLP _ VID[1] | BUCK4_SLP _ VID[0] | RESERVED |
| TPS6508640 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS65086401 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS6508641 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS65086470 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

表 8-52. BUCK4SLPVID Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK4_SLP_VID[6:0] | R/W | X | This field sets the BUCK4 regulator output regulation voltage in sleep mode.<br>See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |

### 8.13.27 BUCK5VID: BUCK5 VID Register (offset = 96h) [reset = X]

图 8-59. BUCK5VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK5_ VID[6] | BUCK5_ VID[5] | BUCK5_ VID[4] | BUCK5_ VID[3] | BUCK5_ VID[2] | BUCK5_ VID[1] | BUCK5_ VID[0] | BUCK5_ DECAY |
| TPS6508640 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| TPS65086401 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS6508641 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086470 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-53. BUCK5VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK5_VID[6:0] | R/W | X | This field sets the BUCK5 regulator output regulation voltage in normal mode.<br>See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |
| 0 | BUCK5_DECAY | R/W | X | Decay Bit<br>**0**: The output slews down to a lower voltage set by the VID bits.<br>**1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

### 8.13.28 BUCK5SLPVID: BUCK5 Sleep VID Register (offset = 97h) [reset = X]

图 8-60. BUCK5SLPVID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK5_SLP _ VID[6] | BUCK5_SLP _ VID[5] | BUCK5_SLP _ VID[4] | BUCK5_SLP _ VID[3] | BUCK5_SLP _ VID[2] | BUCK5_SLP _ VID[1] | BUCK5_SLP _ VID[0] | RESERVED |
| TPS6508640 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| TPS65086401 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS6508641 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086470 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

表 8-54. BUCK5SLPVID Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK5_SLP_VID[6:0] | R/W | X | This field sets the BUCK5 regulator output regulation voltage in sleep mode.<br>See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |

### 8.13.29 BUCK6VID: BUCK6 VID Register (offset = 98h) [reset = X]

图 8-61. BUCK6VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK6_ VID[6] | BUCK6_ VID[5] | BUCK6_ VID[4] | BUCK6_ VID[3] | BUCK6_ VID[2] | BUCK6_ VID[1] | BUCK6_ VID[0] | BUCK6_ DECAY |
| TPS6508640 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| TPS65086401 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| TPS6508641 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| TPS65086470 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-55. BUCK6VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK6_VID[6:0] | R/W | X | This field sets the BUCK6 regulator output regulation voltage in normal mode.<br>See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |
| 0 | BUCK6_DECAY | R/W | X | Decay Bit<br>**0**: The output slews down to a lower voltage set by the VID bits.<br>**1**: The output decays down to a lower voltage set by the VID bits. Decay rate depends on total capacitance and load present at the output. |

### 8.13.30 BUCK6SLPVID: BUCK6 Sleep VID Register (offset = 99h) [reset = X]

图 8-62. BUCK6SLPVID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | BUCK6_SLP _ VID[6] | BUCK6_SLP _ VID[5] | BUCK6_SLP _ VID[4] | BUCK6_SLP _ VID[3] | BUCK6_SLP _ VID[2] | BUCK6_SLP _ VID[1] | BUCK6_SLP _ VID[0] | RESERVED |
| TPS6508640 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| TPS65086401 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| TPS6508641 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| TPS65086470 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R |

表 8-56. BUCK6SLPVID Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:1 | BUCK6_SLP_VID[6:0] | R/W | X | This field sets the BUCK6 regulator output regulation voltage in sleep mode.<br>See 表 8-22 and 表 8-23 for 10-mV and 25-mV step ranges for $V_{OUT}$ options. |

### 8.13.31 LDOA2VID: LDOA2 VID Register (offset = 9Ah) [reset = X]

图 8-63. LDOA2VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2_SLP _VID[3] | LDOA2_SLP _VID[2] | LDOA2_SLP _VID[1] | LDOA2_SLP _VID[0] | LDOA2_ VID[3] | LDOA2_ VID[3] | LDOA2_ VID[1] | LDOA2_ VID[0] |
| TPS6508640 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS65086401 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| TPS6508641 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| TPS65086470 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-57. LDOA2VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:4 | LDOA2_SLP_VID[3:0] | R/W | X | This field sets the LDOA2 regulator output regulation voltage in sleep mode.<br>See 表 8-25 for $V_{out}$ options. |
| 3:0 | LDOA2_VID[3:0] | R/W | X | This field sets the LDOA2 regulator output regulation voltage in normal mode.<br>See 表 8-25 for $V_{out}$ options. |

### 8.13.32 LDOA3VID: LDOA3 VID Register (offset = 9Bh) [reset = X]

图 8-64. LDOA3VID Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA3_SLP _ VID[3] | LDOA3_SLP _ VID[2] | LDOA3_SLP _ VID[1] | LDOA3_SLP _ VID[0] | LDOA3_ VID[3] | LDOA3_ VID[3] | LDOA3_ VID[1] | LDOA3_ VID[0] |
| TPS6508640 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| TPS65086401 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| TPS6508641 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| TPS65086470 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-58. LDOA3VID Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:4 | LDOA3_SLP_VID[3:0] | R/W | X | This field sets the LDOA3 regulator output regulation voltage in sleep mode. See 表 8-25 for $V_{out}$ options. |
| 3:0 | LDOA3_VID[3:0] | R/W | X | This field sets the LDOA3 regulator output regulation voltage in normal mode. See 表 8-25 for $V_{out}$ options. |

### 8.13.33 BUCK123CTRL: BUCK1-3 Control Register (offset = 9Ch) [reset = X]

图 8-65. BUCK123CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | BUCK3 _MODE | BUCK2 _MODE | BUCK1 _MODE | BUCK3 _DIS | BUCK2 _DIS | BUCK1 _DIS |
| TPS6508640 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| TPS65086401 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| TPS6508641 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS65086470 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-59. BUCK123CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5 | BUCK3_MODE | R/W | X | This field sets the BUCK3 regulator operating mode. **0**: Automatic mode **1**: Forced PWM mode |
| 4 | BUCK2_MODE | R/W | X | This field sets the BUCK2 regulator operating mode. **0**: Automatic mode **1**: Forced PWM mode |
| 3 | BUCK1_MODE | R/W | X | This field sets the BUCK1 regulator operating mode. **0**: Automatic mode **1**: Forced PWM mode |
| 2 | BUCK3_DIS | R/W | X | BUCK3 Disable Bit. Writing 0 to this bit forces BUCK3 to turn off regardless of any control input pin (CTL1 – CTL6) status. **0**: Disable **1**: Enable |
| 1 | BUCK2_DIS | R/W | X | BUCK2 Disable Bit. Writing 0 to this bit forces BUCK2 to turn off regardless of any control input pin (CTL1 – CTL6) status. **0**: Disable **1**: Enable |

**表 8-59. BUCK123CTRL Register Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 0 | BUCK1_DIS | R/W | X | BUCK1 Disable Bit. Writing 0 to this bit forces BUCK1 to turn off regardless of any control input pin (CTL1 – CTL6) status.<br>**0**: Disable<br>**1**: Enable |

Product Folder Links: *TPS650864*

### 8.13.34 PG_DELAY2: 2nd Power Good Delay Register (offset = 9Dh) [reset = X]

Programmable Power Good delay for GPO1, GPO2, and GPO4 pins, measured from the moment when all VRs assigned to respective GPO reach their regulation range to Power Good assertion. This is an optional register as the PMIC can be programmed for system PG, level shifter or I²C controller GPO.

图 8-66. PG_DELAY2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | GPO2_PG_DELAY[2] | GPO2_PG_DELAY[1] | GPO2_PG_DELAY[0] | GPO4_PG_DELAY[2] | GPO4_PG_DELAY[1] | GPO4_PG_DELAY[0] | GPO1_PG_DELAY[1] | GPO1_PG_DELAY[0] |
| TPS6508640 | — | — | — | 0 | 0 | 0 | 0 | 0 |
| TPS65086401 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS6508641 | — | — | — | 0 | 0 | 0 | 0 | 0 |
| TPS65086470 | 0 | 0 | 0 | — | — | — | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-60. PG_DELAY2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:5 | GPO2_PG_DELAY[2:0] | R/W | X | Programmable delay Power Good or level shifter for GPO2 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation.<br>**000**: 0 ms<br>**001**: 5.0 ms<br>**010**: 10 ms<br>**011**: 15 ms<br>**100**: 20 ms<br>**101**: 50 ms<br>**110**: 75 ms<br>**111**: 100 ms<br>—: Bits not used. If GPO2 is controlled by I²C rather than PG and is not used internally for VTT LDO enable, these bits have no impact. Default is set to 0b. |
| 4:2 | GPO4_PG_DELAY[2:0] | R/W | X | Programmable delay Power Good or level shifter for GPO4 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation.<br>**000**: 0 ms<br>**001**: 5.0 ms<br>**010**: 10 ms<br>**011**: 15 ms<br>**100**: 20 ms<br>**101**: 50 ms<br>**110**: 75 ms<br>**111**: 100 ms<br>—: Bits not used. If GPO4 is controlled by I²C rather than PG, these bits have no impact. Default is set to 0b. |
| 1:0 | GPO1_PG_DELAY[1:0] | R/W | X | Programmable delay Power Good or level shifter for GPO1 pin. Measured from the moment when all rails grouped to this pin reach their regulation range. All values have ±10% variation.<br>**00**: 0 ms<br>**01**: 5.0 ms<br>**10**: 10 ms<br>**11**: 15 ms<br>—: Bits not used. If GPO1 is controlled by I²C rather than PG, these bits have no impact. Default is set to 0b. |

Product Folder Links: *TPS650864*

### 8.13.35 SWVTT_DIS: SWVTT Disable Register (offset = 9Fh) [reset = X]

图 8-67. SWVTT_DIS Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | SWB2_LDOA1_DIS | SWB1_DIS | SWA1_DIS | VTT_DIS | Reserved | Reserved | Reserved | Reserved |
| TPS6508640 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| TPS65086401 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| TPS6508641 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| TPS65086470 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-61. SWVTT_DIS Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SWB2_LDOA1_DIS | R/W | X | SWB2 or LDOA1 Disable Bit. Writing 0 to this bit forces SWB2 or LDOA1 to turn off regardless of any control input pin (CTL1 – CTL6) status. OTP setting selects either SWB2 or LDOA1. **0**: Disable. **1**: Enable. SWB2 for: TPS65086470 LDOA1 for: TPS6508640, TPS65086401, and TPS6508641 |
| 6 | SWB1_DIS | R/W | X | SWB1 Disable Bit. Writing 0 to this bit forces SWB1 to turn off regardless of any control input pin (CTL1 – CTL6) status. **0**: Disable. **1**: Enable. |
| 5 | SWA1_DIS | R/W | X | SWA1 Disable Bit. Writing 0 to this bit forces SWA1 to turn off regardless of any control input pin (CTL1 – CTL6) status. **0**: Disable. **1**: Enable. |
| 4 | VTT_DIS | R/W | X | VTT Disable Bit. Writing 0 to this bit forces VTT to turn off regardless of any control input pin (CTL1 – CTL6) status. **0**: Disable. **1**: Enable. |
| 3:0 | Reserved | R/W | 0000 | Reserved bits. Always write to 0000. |

Product Folder Links: *TPS650864*

### 8.13.36 I2C_RAIL_EN1: 1st VR Pin Enable Override Register (offset = A0h) [reset = X]

图 8-68. I2C_RAIL_EN1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2_EN | SWA1_EN | BUCK6_EN | BUCK5_EN | BUCK4_EN | BUCK3_EN | BUCK2_EN | BUCK1_EN |
| TPS6508640 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086401 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS6508641 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086470 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-62. I2C_RAIL_EN1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LDOA2_EN | R/W | X | LDOA2 I$^2$C Enable<br>**0**: LDOA2 is enabled or disabled by one of the control input pins or internal PG signal.<br>**1**: LDOA2 is forced on unless LDOA2_DIS = 0b. |
| 6 | SWA1_EN | R/W | X | SWA1 I$^2$C Enable<br>**0**: SWA1 is enabled or disabled by one of the control input pins or internal PG signal.<br>**1**: SWA1 is forced on unless SWA1_DIS = 0b. |
| 5 | BUCK6_EN | R/W | X | BUCK6 I$^2$C Enable<br>**0**: BUCK6 is enabled or disabled by one of the control input pins or internal PG signal.<br>**1**: BUCK6 is forced on unless BUCK6_DIS = 0b. |
| 4 | BUCK5_EN | R/W | X | BUCK5 I$^2$C Enable<br>**0**: BUCK5 is enabled or disabled by one of the control input pins or internal PG signal.<br>**1**: BUCK5 is forced on unless BUCK5_DIS = 0b. |
| 3 | BUCK4_EN | R/W | X | BUCK4 I$^2$C Enable<br>**0**: BUCK4 is enabled or disabled by one of the control input pins or internal PG signal.<br>**1**: BUCK4 is forced on unless BUCK4_DIS = 0b. |
| 2 | BUCK3_EN | R/W | X | BUCK3 I$^2$C Enable<br>**0**: BUCK3 is enabled or disabled by one of the control input pins or internal PG signal.<br>**1**: BUCK3 is forced on unless BUCK3_DIS = 0b. |
| 1 | BUCK2_EN | R/W | X | BUCK2 I$^2$C Enable<br>**0**: BUCK2 is enabled or disabled by one of the control input pins or internal PG signal.<br>**1**: BUCK2 is forced on unless BUCK2_DIS = 0b. |
| 0 | BUCK1_EN | R/W | X | BUCK1 I$^2$C Enable<br>**0**: BUCK1 is enabled or disabled by one of the control input pins or internal PG signal.<br>**1**: BUCK1 is forced on unless BUCK1_DIS = 0b. |

Product Folder Links: *TPS650864*

### 8.13.37 I2C_RAIL_EN2/GPOCTRL: 2nd VR Pin Enable Override and GPO Control Register (offset = A1h) [reset = X]

图 8-69. I2C_RAIL_EN2/GPOCTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | GPO4_LVL | GPO3_LVL | GPO2_LVL | GPO1_LVL | VTT_EN | SWB2_LDOA1_EN | SWB1_EN | LDOA3_EN |
| TPS6508640 | — | — | 0 | — | 0 | 0 | 0 | 1 |
| TPS65086401 | — | — | — | — | 0 | 0 | 0 | 0 |
| TPS6508641 | — | — | 0 | — | 0 | 0 | 0 | 0 |
| TPS65086470 | 0 | 0 | — | — | 0 | 0 | 0 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-63. I2C_RAIL_EN2/GPOCTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | GPO4_LVL | R/W | X | The field is to set GPO4 pin output if the pin is factory-configured as an I$^2$C controlled open-drain general-purpose output. **0**: The pin is driven to logic low. **1**: The pin is driven to logic high. —: Bit not used in this version; GPO4 is controlled by GPO4 PG tree. Default is set to 0b. |
| 6 | GPO3_LVL | R/W | X | The field is to set GPO3 pin output if the pin is factory-configured as either an I$^2$C controlled open-drain or a push-pull general-purpose output. **0**: The pin is driven to logic low. **1**: The pin is driven to logic high. —: Bit not used in this version; GPO3 is controlled by GPO3 PG tree. Default is set to 0b. |
| 5 | GPO2_LVL | R/W | X | The field is to set GPO2 pin output if the pin is factory-configured as either an I$^2$C controlled open-drain or a push-pull general-purpose output. **0**: The pin is driven to logic low. **1**: The pin is driven to logic high. —: Bit not used in this version; GPO2 is controlled by GPO2 PG tree. Default is set to 0b. |
| 4 | GPO1_LVL | R/W | X | The field is to set GPO1 pin output if the pin is factory-configured as either an I$^2$C controlled open-drain or a push-pull general-purpose output. **0**: The pin is driven to logic low. **1**: The pin is driven to logic high. —: Bit not used in this version; GPO1 is controlled by GPO1 PG tree. Default is set to 0b. |
| 3 | VTT_EN | R/W | X | VTT LDO I$^2$C Enable **0**: VTT LDO is enabled or disabled by one of the control input pins or internal PG signals. **1**: VTT LDO is forced on unless VTT_DIS = 0b. |
| 2 | SWB2_LDOA1_EN | R/W | X | SWB2 or LDOA1 I$^2$C Enable. Internal setting selects either SWB2 or LDOA1. **0**: SWB2 or LDOA1 is enabled or disabled by one of the control input pins or internal PG signals. **1**: SWB2 or LDOA1 is forced on unless SWB2_LDOA1_DIS = 0b. SWB2 for: TPS65086470 LDOA1 for: TPS6508640, TPS65086401, and TPS6508641 |
| 1 | SWB1_EN | R/W | X | SWB1 I$^2$C Enable **0**: SWB1 is enabled or disabled by one of the control input pins or internal PG signals. **1**: SWB1 is forced on unless SWB1_DIS = 0b. |

表 8-63. **I2C_RAIL_EN2/GPOCTRL Register Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 0 | LDOA3_EN | R/W | X | LDOA3 I$^2$C Enable<br>**0**: LDOA3 is enabled or disabled by one of the control input pins or internal PG signals.<br>**1**: LDOA3 is forced on unless LDOA3_DIS = 0b. |

### 8.13.38 PWR_FAULT_MASK1: 1st VR Power Fault Mask Register (offset = A2h) [reset = X]

图 8-70. PWR_FAULT_MASK1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2_FLTmsK | SWA1_FLTmsK | BUCK6_FLTmsK | BUCK5_FLTmsK | BUCK4_FLTmsK | BUCK3_FLTmsK | BUCK2_FLTmsK | BUCK1_FLTmsK |
| TPS6508640 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086401 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS6508641 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| TPS65086470 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-64. PWR_FAULT_MASK1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LDOA2_FLTmsK | R/W | X | LDOA2 Power Fault Mask. When masked, power fault from LDOA2 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked |
| 6 | SWA1_FLTmsK | R/W | X | SWA1 Power Fault Mask. When masked, power fault from SWA1 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked |
| 5 | BUCK6_FLTmsK | R/W | X | BUCK6 Power Fault Mask. When masked, power fault from BUCK6 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked |
| 4 | BUCK5_FLTmsK | R/W | X | BUCK5 Power Fault Mask. When masked, power fault from BUCK5 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked |
| 3 | BUCK4_FLTmsK | R/W | X | BUCK4 Power Fault Mask. When masked, power fault from BUCK4 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked |
| 2 | BUCK3_FLTmsK | R/W | X | BUCK3 Power Fault Mask. When masked, power fault from BUCK3 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked |
| 1 | BUCK2_FLTmsK | R/W | X | BUCK2 Power Fault Mask. When masked, power fault from BUCK2 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked |
| 0 | BUCK1_FLTmsK | R/W | X | BUCK1 Power Fault Mask. When masked, power fault from BUCK1 does not cause PMIC to shutdown. **0**: Not Masked **1**: Masked |

### 8.13.39 PWR_FAULT_MASK2: 2nd VR Power Fault Mask Register (offset = A3h) [reset = X]

图 8-71. PWR_FAULT_MASK2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | LDOA1_FLTmsK | VTT_FLTmsK | SWB2_FLTmsK | SWB1_FLTmsK | LDOA3_FLTmsK |
| TPS6508640 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| TPS65086401 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| TPS6508641 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| TPS65086470 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| Access | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-65. PWR_FAULT_MASK2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 6 | RESERVED | R/W | 0 | Reserved bit. Always write to 0b. |
| 5 | RESERVED | R/W | 1 | Reserved bit. Always write to 1b. |
| 4 | LDOA1_FLTmsK | R/W | X | LDOA1 Power Fault Mask. When masked, power fault from LDOA1 does not cause PMIC to shutdown.<br>**0**: Not Masked<br>**1**: Masked |
| 3 | VTT_FLTmsK | R/W | X | VTT LDO Power Fault Mask. When masked, power fault from VTT LDO does not cause PMIC to shutdown.<br>**0**: Not Masked<br>**1**: Masked |
| 2 | SWB2_FLTmsK | R/W | X | SWB2 Power Fault Mask. When masked, power fault from SWB2 does not cause PMIC to shutdown.<br>**0**: Not Masked<br>**1**: Masked |
| 1 | SWB1_FLTmsK | R/W | X | SWB1 Power Fault Mask. When masked, power fault from SWB1 does not cause PMIC to shutdown.<br>**0**: Not Masked<br>**1**: Masked |
| 0 | LDOA3_FLTmsK | R/W | X | LDOA3 Power Fault Mask. When masked, power fault from LDOA3 does not cause PMIC to shutdown.<br>**0**: Not Masked<br>**1**: Masked |

### 8.13.40 GPO1PG_CTRL1: 1st GPO1 PG Control Register (offset = A4h) [reset = X]

图 8-72. GPO1PG_CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2 _msK | SWA1 _msK | BUCK6 _msK | BUCK5 _msK | BUCK4 _msK | BUCK3 _msK | BUCK2 _msK | BUCK1 _msK |
| TPS6508640 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| TPS65086401 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| TPS6508641 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| TPS65086470 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-66. GPO1PG_CTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LDOA2_msK | R/W | X | **0**: LDOA2 PG is part of Power Good tree of GPO1 pin.<br>**1**: LDOA2 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 6 | SWA1_msK | R/W | X | **0**: SWA1 PG is part of Power Good tree of GPO1 pin.<br>**1**: SWA1 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 5 | BUCK6_msK | R/W | X | **0**: BUCK6 PG is part of Power Good tree of GPO1 pin.<br>**1**: BUCK6 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 4 | BUCK5_msK | R/W | X | **0**: BUCK5 PG is part of Power Good tree of GPO1 pin.<br>**1**: BUCK5 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 3 | BUCK4_msK | R/W | X | **0**: BUCK4 PG is part of Power Good tree of GPO1 pin.<br>**1**: BUCK4 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 2 | BUCK3_msK | R/W | X | **0**: BUCK3 PG is part of Power Good tree of GPO1 pin.<br>**1**: BUCK3 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 1 | BUCK2_msK | R/W | X | **0**: BUCK2 PG is part of Power Good tree of GPO1 pin.<br>**1**: BUCK2 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 0 | BUCK1_msK | R/W | X | **0**: BUCK1 PG is part of Power Good tree of GPO1 pin.<br>**1**: BUCK1 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |

### 8.13.41 GPO1PG_CTRL2: 2nd GPO1 PG Control Register (offset = A5h) [reset = X]

图 8-73. GPO1PG_CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CTL5_msK | CTL4_msK | CTL2_msK | CTL1_msK | VTT_msK | SWB2_LDOA1_msK | SWB1_msK | LDOA3_msK |
| TPS6508640 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS65086401 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| TPS6508641 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS65086470 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-67. GPO1PG_CTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CTL5_msK | R/W | X | **0**: CTL5 pin status is part of Power Good tree of GPO1 pin.<br>**1**: CTL5 pin status is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 6 | CTL4_msK | R/W | X | **0**: CTL4 pin status is part of Power Good tree of GPO1 pin.<br>**1**: CTL4 pin status is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 5 | CTL2_msK | R/W | X | **0**: CTL2 pin status is part of Power Good tree of GPO1 pin.<br>**1**: CTL2 pin status is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 4 | CTL1_msK | R/W | X | **0**: CTL1 pin status is part of Power Good tree of GPO1 pin.<br>**1**: CTL1 pin status is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 3 | VTT_msK | R/W | X | **0**: VTT LDO PG is part of Power Good tree of GPO1 pin.<br>**1**: VTT LDO PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 2 | SWB2_LDOA1_msK | R/W | X | **0**: SWB2_LDOA1 PG is part of Power Good tree of GPO1 pin.<br>**1**: SWB2_LDOA1 PG is NOT part of Power Good tree of GPO1 pin and is ignored.<br>SWB2 for: TPS65086470<br>LDOA1 for:TPS6508640, TPS65086401, and TPS6508641 |
| 1 | SWB1_msK | R/W | X | **0**: SWB1 PG is part of Power Good tree of GPO1 pin.<br>**1**: SWB1 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |
| 0 | LDOA3_msK | R/W | X | **0**: LDOA3 PG is part of Power Good tree of GPO1 pin.<br>**1**: LDOA3 PG is NOT part of Power Good tree of GPO1 pin and is ignored. |

Product Folder Links: *TPS650864*

### 8.13.42 GPO4PG_CTRL1: 1st GPO4 PG Control Register (offset = A6h) [reset = X]

图 8-74. GPO4PG_CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2_msK | SWA1_msK | BUCK6_msK | BUCK5_msK | BUCK4_msK | BUCK3_msK | BUCK2_msK | BUCK1_msK |
| TPS6508640 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| TPS65086401 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS6508641 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| TPS65086470 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-68. GPO4PG_CTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LDOA2_msK | R/W | X | **0**: LDOA2 PG is part of Power Good tree of GPO4 pin.<br>**1**: LDOA2 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 6 | SWA1_msK | R/W | X | **0**: SWA1 PG is part of Power Good tree of GPO4 pin.<br>**1**: SWA1 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 5 | BUCK6_msK | R/W | X | **0**: BUCK6 PG is part of Power Good tree of GPO4 pin.<br>**1**: BUCK6 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 4 | BUCK5_msK | R/W | X | **0**: BUCK5 PG is part of Power Good tree of GPO4 pin.<br>**1**: BUCK5 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 3 | BUCK4_msK | R/W | X | **0**: BUCK4 PG is part of Power Good tree of GPO4 pin.<br>**1**: BUCK4 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 2 | BUCK3_msK | R/W | X | **0**: BUCK3 PG is part of Power Good tree of GPO4 pin.<br>**1**: BUCK3 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 1 | BUCK2_msK | R/W | X | **0**: BUCK2 PG is part of Power Good tree of GPO4 pin.<br>**1**: BUCK2 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 0 | BUCK1_msK | R/W | X | **0**: BUCK1 PG is part of Power Good tree of GPO4 pin.<br>**1**: BUCK1 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |

### 8.13.43 GPO4PG_CTRL2: 2nd GPO4 PG Control Register (offset = A7h) [reset = X]

图 8-75. GPO4PG_CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CTL5_msK | CTL4_msK | CTL2_msK | CTL1_msK | VTT_msK | SWB2_LDOA1_msK | SWB1_msK | LDOA3_msK |
| TPS6508640 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS65086401 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS6508641 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS65086470 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-69. GPO4PG_CTRL2 Register Descriptionsr

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CTL5_msK | R/W | X | **0**: CTL5 pin status is part of Power Good tree of GPO4 pin.<br>**1**: CTL5 pin status is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 6 | CTL4_msK | R/W | X | **0**: CTL4 pin status is part of Power Good tree of GPO4 pin.<br>**1**: CTL4 pin status is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 5 | CTL2_msK | R/W | X | **0**: CTL2 pin status is part of Power Good tree of GPO4 pin.<br>**1**: CTL2 pin status is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 4 | CTL1_msK | R/W | X | **0**: CTL1 pin status is part of Power Good tree of GPO4 pin.<br>**1**: CTL1 pin status is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 3 | VTT_msK | R/W | X | **0**: VTT LDO PG is part of Power Good tree of GPO4 pin.<br>**1**: VTT LDO PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 2 | SWB2_LDOA1_msK | R/W | X | **0**: SWB2_LDOA1 PG is part of Power Good tree of GPO4 pin.<br>**1**: SWB2_LDOA1 PG is NOT part of Power Good tree of GPO4 pin and is ignored.<br>SWB2 for: TPS65086470<br>LDOA1 for: TPS6508640, TPS65086401, and TPS6508641 |
| 1 | SWB1_msK | R/W | X | **0**: SWB1 PG is part of Power Good tree of GPO4 pin.<br>**1**: SWB1 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |
| 0 | LDOA3_msK | R/W | X | **0**: LDOA3 PG is part of Power Good tree of GPO4 pin.<br>**1**: LDOA3 PG is NOT part of Power Good tree of GPO4 pin and is ignored. |

Product Folder Links: *TPS650864*

### 8.13.44 GPO2PG_CTRL1: 1st GPO2 PG Control Register (offset = A8h) [reset = X]

#### 图 8-76. GPO2PG_CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2_msK | SWA1_msK | BUCK6_msK | BUCK5_msK | BUCK4_msK | BUCK3_msK | BUCK2_msK | BUCK1_msK |
| TPS6508640 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| TPS65086401 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| TPS6508641 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| TPS65086470 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

#### 表 8-70. GPO2PG_CTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LDOA2_msK | R/W | X | **0**: LDOA2 PG is part of Power Good tree of GPO2 pin.<br>**1**: LDOA2 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 6 | SWA1_msK | R/W | X | **0**: SWA1 PG is part of Power Good tree of GPO2 pin.<br>**1**: SWA1 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 5 | BUCK6_msK | R/W | X | **0**: BUCK6 PG is part of Power Good tree of GPO2 pin.<br>**1**: BUCK6 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 4 | BUCK5_msK | R/W | X | **0**: BUCK5 PG is part of Power Good tree of GPO2 pin.<br>**1**: BUCK5 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 3 | BUCK4_msK | R/W | X | **0**: BUCK4 PG is part of Power Good tree of GPO2 pin.<br>**1**: BUCK4 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 2 | BUCK3_msK | R/W | X | **0**: BUCK3 PG is part of Power Good tree of GPO2 pin.<br>**1**: BUCK3 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 1 | BUCK2_msK | R/W | X | **0**: BUCK2 PG is part of Power Good tree of GPO2 pin.<br>**1**: BUCK2 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 0 | BUCK1_msK | R/W | X | **0**: BUCK1 PG is part of Power Good tree of GPO2 pin.<br>**1**: BUCK1 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |

Product Folder Links: *TPS650864*

### 8.13.45 GPO2PG_CTRL2: 2nd GPO2 PG Control Register (offset = A9h) [reset = X]

图 8-77. GPO2PG_CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CTL5_msK | CTL4_msK | CTL2_msK | CTL1_msK | VTT_msK | SWB2_LDOA1_msK | SWB1_msK | LDOA3_msK |
| TPS6508640 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS65086401 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| TPS6508641 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS65086470 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-71. GPO2PG_CTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CTL5_msK | R/W | X | **0**: CTL5 pin status is part of Power Good tree of GPO2 pin.<br>**1**: CTL5 pin status is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 6 | CTL4_msK | R/W | X | **0**: CTL4 pin status is part of Power Good tree of GPO2 pin.<br>**1**: CTL4 pin status is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 5 | CTL2_msK | R/W | X | **0**: CTL2 pin status is part of Power Good tree of GPO2 pin.<br>**1**: CTL2 pin status is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 4 | CTL1_msK | R/W | X | **0**: CTL1 pin status is part of Power Good tree of GPO2 pin.<br>**1**: CTL1 pin status is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 3 | VTT_msK | R/W | X | **0**: VTT LDO PG is part of Power Good tree of GPO2 pin.<br>**1**: VTT LDO PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 2 | SWB2_LDOA1_msK | R/W | X | **0**: SWB2_LDOA1 PG is part of Power Good tree of GPO2 pin.<br>**1**: SWB2_LDOA1 PG is NOT part of Power Good tree of GPO2 pin and is ignored.<br>SWB2 for: TPS65086470<br>LDOA1 for: TPS6508640, TPS65086401, and TPS6508641 |
| 1 | SWB1_msK | R/W | X | **0**: SWB1 PG is part of Power Good tree of GPO2 pin.<br>**1**: SWB1 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |
| 0 | LDOA3_msK | R/W | X | **0**: LDOA3 PG is part of Power Good tree of GPO2 pin.<br>**1**: LDOA3 PG is NOT part of Power Good tree of GPO2 pin and is ignored. |

### 8.13.46 GPO3PG_CTRL1: 1st GPO3 PG Control Register (offset = AAh) [reset = X]

图 8-78. GPO3PG_CTRL1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2 _msK | SWA1 _msK | BUCK6 _msK | BUCK5 _msK | BUCK4 _msK | BUCK3 _msK | BUCK2 _msK | BUCK1 _msK |
| TPS6508640 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| TPS65086401 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| TPS6508641 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| TPS65086470 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-72. GPO3PG_CTRL1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LDOA2_msK | R/W | X | **0**: LDOA2 PG is part of Power Good tree of GPO3 pin.<br>**1**: LDOA2 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 6 | SWA1_msK | R/W | X | **0**: SWA1 PG is part of Power Good tree of GPO3 pin.<br>**1**: SWA1 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 5 | BUCK6_msK | R/W | X | **0**: BUCK6 PG is part of Power Good tree of GPO3 pin.<br>**1**: BUCK6 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 4 | BUCK5_msK | R/W | X | **0**: BUCK5 PG is part of Power Good tree of GPO3 pin.<br>**1**: BUCK5 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 3 | BUCK4_msK | R/W | X | **0**: BUCK4 PG is part of Power Good tree of GPO3 pin.<br>**1**: BUCK4 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 2 | BUCK3_msK | R/W | X | **0**: BUCK3 PG is part of Power Good tree of GPO3 pin.<br>**1**: BUCK3 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 1 | BUCK2_msK | R/W | X | **0**: BUCK2 PG is part of Power Good tree of GPO3 pin.<br>**1**: BUCK2 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 0 | BUCK1_msK | R/W | X | **0**: BUCK1 PG is part of Power Good tree of GPO3 pin.<br>**1**: BUCK1 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |

Product Folder Links: *TPS650864*

### 8.13.47 GPO3PG_CTRL2: 2nd GPO3 PG Control Register (offset = ABh) [reset = X]

图 8-79. GPO3PG_CTRL2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | CTL5_msK | CTL4_msK | CTL2_msK | CTL1_msK | VTT_msK | SWB2_LDOA1_msK | SWB1_msK | LDOA3_msK |
| TPS6508640 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS65086401 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| TPS6508641 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| TPS65086470 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-73. GPO3PG_CTRL2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CTL5_msK | R/W | X | **0**: CTL5 pin status is part of Power Good tree of GPO3 pin.<br>**1**: CTL5 pin status is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 6 | CTL4_msK | R/W | X | **0**: CTL4 pin status is part of Power Good tree of GPO3 pin.<br>**1**: CTL4 pin status is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 5 | CTL2_msK | R/W | X | **0**: CTL2 pin status is part of Power Good tree of GPO3 pin.<br>**1**: CTL2 pin status is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 4 | CTL1_msK | R/W | X | **0**: CTL1 pin status is part of Power Good tree of GPO3 pin.<br>**1**: CTL1 pin status is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 3 | VTT_msK | R/W | X | **0**: VTT LDO PG is part of Power Good tree of GPO3 pin.<br>**1**: VTT LDO PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 2 | SWB2_LDOA1_msK | R/W | X | **0**: SWB2_LDOA1 PG is part of Power Good tree of GPO3 pin.<br>**1**: SWB2_LDOA1 PG is NOT part of Power Good tree of GPO3 pin and is ignored.<br>SWB2 for: TPS65086470<br>LDOA1 for: TPS6508640, TPS65086401, and TPS6508641 |
| 1 | SWB1_msK | R/W | X | **0**: SWB1 PG is part of Power Good tree of GPO3 pin.<br>**1**: SWB1 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |
| 0 | LDOA3_msK | R/W | X | **0**: LDOA3 PG is part of Power Good tree of GPO3 pin.<br>**1**: LDOA3 PG is NOT part of Power Good tree of GPO3 pin and is ignored. |

Product Folder Links: *TPS650864*

### 8.13.48 MISCSYSPG Register (offset = ACh) [reset = X]

图 8-80. MISCSYSPG Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | GPO1_CTL3_msK | GPO1_CTL6_msK | GPO4_CTL3_msK | GPO4_CTL6_msK | GPO2_CTL3_msK | GPO2_CTL6_msK | GPO3_CTL3_msK | GPO3_CTL6_msK |
| TPS6508640 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| TPS65086401 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| TPS6508641 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| TPS65086470 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-74. MISCSYSPG Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | GPO1_CTL3_msK | R/W | X | **0**: CTL3 pin status is part of Power Good tree of GPO1 pin.<br>**1**: CTL3 pin status is NOT part of Power Good tree of GPO1 pin. |
| 6 | GPO1_CTL6_msK | R/W | X | **0**: CTL6 pin status is part of Power Good tree of GPO1 pin.<br>**1**: CTL6 pin status is NOT part of Power Good tree of GPO1 pin. |
| 5 | GPO4_CTL3_msK | R/W | X | **0**: CTL3 pin status is part of Power Good tree of GPO4 pin.<br>**1**: CTL3 pin status is NOT part of Power Good tree of GPO4 pin. |
| 4 | GPO4_CTL6_msK | R/W | X | **0**: CTL6 pin status is part of Power Good tree of GPO4 pin.<br>**1**: CTL6 pin status is NOT part of Power Good tree of GPO4 pin. |
| 3 | GPO2_CTL3_msK | R/W | X | **0**: CTL3 pin status is part of Power Good tree of GPO2 pin.<br>**1**: CTL3 pin status is NOT part of Power Good tree of GPO2 pin. |
| 2 | GPO2_CTL6_msK | R/W | X | **0**: CTL6 pin status is part of Power Good tree of GPO2 pin.<br>**1**: CTL6 pin status is NOT part of Power Good tree of GPO2 pin. |
| 1 | GPO3_CTL3_msK | R/W | X | **0**: CTL3 pin status is part of Power Good tree of GPO3 pin.<br>**1**: CTL3 pin status is NOT part of Power Good tree of GPO3pin. |
| 0 | GPO3_CTL6_msK | R/W | X | **0**: CTL6 pin status is part of Power Good tree of GPO3 pin.<br>**1**: CTL6 pin status is NOT part of Power Good tree of GPO3 pin. |

Product Folder Links: TPS650864

### 8.13.48.1 VTT_DISCH_CTRL Register (offset = ADh) [reset = X]

图 8-81. VTT_DISCH_CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | VTT_DISCHG | RESERVED | RESERVED | RESERVED | RESERVED |
| TPS6508640 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| TPS65086401 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| TPS6508641 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| TPS65086470 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-75. VTT_DISCH_CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:5 | RESERVED | R/W | X | Reserved bits. Always write to match OTP settings. |
| 4 | VTT_DISCHG | R/W | X | **0**: no discharge<br>**1**: 100 Ω |
| 3:0 | RESERVED | R/W | X | Reserved bits. Always write to match OTP settings. |

### 8.13.49 LDOA1_SWB2_CTRL: LDOA1 and SWB2 Control Register (offset = AEh) [reset = X]

图 8-82. LDOA1_SWB2_CTRL Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA1_DISCHG[1] | LDOA1_DISCHG[0] | LDOA1_SWB2_SDWN_CONFIG | LDOA1_VID[3] | LDOA1_VID[2] | LDOA1_VID[1] | LDOA1_VID[0] | LDOA1_SWB2_EN |
| TPS6508640 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| TPS65086401 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| TPS6508641 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| TPS65086470 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-76. LDOA1_SWB2_CTRL Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:6 | LDOA1_DISCHG[1:0] | R/W | X | LDOA1 discharge resistance<br>**00**: no discharge<br>**01**: 100 Ω<br>**10**: 200 Ω<br>**11**: 500 Ω |
| 5 | LDOA1_SWB2_SDWN_CONFIG | R/W | X | Control for Disabling LDOA1 or SWB2 (OTP dependent) during Emergency Shutdown. When LDOA1 is used in sequence and SWB1 and SWB2 are not merged, this will control SWB2.<br>**0**: LDOA1 or SWB2 will turn off during Emergency Shutdown for factory-programmable duration of 1 ms, 5 ms, 10 ms, or 100 ms.<br>**1**: LDOA1 or SWB2 is controlled by LDOA1_SWB2_EN bit only.<br>LDOA1 for: TPS65086470<br>SWB2 for: TPS6508640<br>Unused for: TPS65086401 and TPS6508641 |
| 4:1 | LDOA1_VID[3:0] | R/W | X | This field sets the LDOA1 regulator output regulation voltage.<br>See 表 8-24 for $V_{OUT}$ options. |
| 0 | LDOA1_SWB2_EN | R/W | X | LDOA1 or SWB2 Enable Bit.<br>**0**: Disable.<br>**1**: Enable.<br>LDOA1 for: TPS65086470<br>SWB2 for: TPS6508640<br>Unused for: TPS65086401 and TPS6508641 |

Product Folder Links: *TPS650864*

### 8.13.50 PG_STATUS1: 1st Power Good Status Register (offset = B0h) [reset = 0000 0000]

#### 图 8-83. PG_STATUS1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2_PGOOD | SWA1_PGOOD | BUCK6_PGOOD | BUCK5_PGOOD | BUCK4_PGOOD | BUCK3_PGOOD | BUCK2_PGOOD | BUCK1_PGOOD |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

#### 表 8-77. PG_STATUS1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LDOA2_PGOOD | R | 0 | LDOA2 Power Good status.<br>**0**: The output is not in target regulation range.<br>**1**: The output is in target regulation range. |
| 6 | SWA1_PGOOD | R | 0 | SWA1 Power Good status.<br>**0**: The output is not in target regulation range.<br>**1**: The output is in target regulation range. |
| 5 | BUCK6_PGOOD | R | 0 | BUCK6 Power Good status.<br>**0**: The output is not in target regulation range.<br>**1**: The output is in target regulation range. |
| 4 | BUCK5_PGOOD | R | 0 | BUCK5 Power Good status.<br>**0**: The output is not in target regulation range.<br>**1**: The output is in target regulation range. |
| 3 | BUCK4_PGOOD | R | 0 | BUCK4 Power Good status.<br>**0**: The output is not in target regulation range.<br>**1**: The output is in target regulation range. |
| 2 | BUCK3_PGOOD | R | 0 | BUCK3 Power Good status.<br>**0**: The output is not in target regulation range.<br>**1**: The output is in target regulation range. |
| 1 | BUCK2_PGOOD | R | 0 | BUCK2 Power Good status.<br>**0**: The output is not in target regulation range.<br>**1**: The output is in target regulation range. |
| 0 | BUCK1_PGOOD | R | 0 | BUCK1 Power Good status.<br>**0**: The output is not in target regulation range.<br>**1**: The output is in target regulation range. |

Product Folder Links: *TPS650864*

### 8.13.51 PG_STATUS2: 2nd Power Good Status Register (offset = B1h) [reset = 0000 0000]

#### 图 8-84. PG_STATUS2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | LDO5 _PGOOD | LDOA1 _PGOOD | VTT _PGOOD | SWB2 _PGOOD | SWB1 _PGOOD | LDOA3 _PGOOD |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

#### 表 8-78. PG_STATUS2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5 | LDO5_PGOOD | R | 0 | LDO5 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range. |
| 4 | LDOA1_PGOOD | R | 0 | LDOA1 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range. |
| 3 | VTT_PGOOD | R | 0 | VTT LDO Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range. |
| 2 | SWB2_PGOOD | R | 0 | SWB2 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range. |
| 1 | SWB1_PGOOD | R | 0 | SWB1 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range. |
| 0 | LDOA3_PGOOD | R | 0 | LDOA3 Power Good status. **0**: The output is not in target regulation range. **1**: The output is in target regulation range. |

### 8.13.52 PWR_FAULT_STATUS1: 1st Power Fault Status Register (offset = B2h) [reset = 0000 0000]

图 8-85. PWR_FAULT_STATUS1 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | LDOA2_PWRFLT | SWA1_PWRFLT | BUCK6_PWRFLT | BUCK5_PWRFLT | BUCK4_PWRFLT | BUCK3_PWRFLT | BUCK2_PWRFLT | BUCK1_PWRFLT |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-79. PWR_FAULT_STATUS1 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LDOA2_PWRFLT | R | 0 | This fields indicates that LDOA2 has lost its regulation.<br>**0**: No Fault.<br>**1**: Power fault has occurred. The host to write 1 to clear. |
| 6 | SWA1_PWRFLT | R | 0 | This fields indicates that SWA1 has lost its regulation.<br>**0**: No Fault.<br>**1**: Power fault has occurred. The host to write 1 to clear. |
| 5 | BUCK6_PWRFLT | R | 0 | This fields indicates that BUCK6 has lost its regulation.<br>**0**: No Fault.<br>**1**: Power fault has occurred. The host to write 1 to clear. |
| 4 | BUCK5_PWRFLT | R | 0 | This fields indicates that BUCK5 has lost its regulation.<br>**0**: No Fault.<br>**1**: Power fault has occurred. The host to write 1 to clear. |
| 3 | BUCK4_PWRFLT | R | 0 | This fields indicates that BUCK4 has lost its regulation.<br>**0**: No Fault.<br>**1**: Power fault has occurred. The host to write 1 to clear. |
| 2 | BUCK3_PWRFLT | R | 0 | This fields indicates that BUCK3 has lost its regulation.<br>**0**: No Fault.<br>**1**: Power fault has occurred. The host to write 1 to clear. |
| 1 | BUCK2_PWRFLT | R | 0 | This fields indicates that BUCK2 has lost its regulation.<br>**0**: No Fault.<br>**1**: Power fault has occurred. The host to write 1 to clear. |
| 0 | BUCK1_PWRFLT | R | 0 | This fields indicates that BUCK1 has lost its regulation.<br>**0**: No Fault.<br>**1**: Power fault has occurred. The host to write 1 to clear. |

### 8.13.53 PWR_FAULT_STATUS2: 2nd Power Fault Status Register (offset = B3h) [reset = 0000 0000]

图 8-86. PWR_FAULT_STATUS2 Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | LDOA1_ PWRFLT | VTT_ PWRFLT | SWB2 _PWRFLT | SWB1_ PWRFLT | LDOA3_ PWRFLT |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

表 8-80. PWR_FAULT_STATUS2 Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4 | LDOA1_PWRFLT | R/W | 0 | This fields indicates that LDOA1 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear. |
| 3 | VTT_PWRFLT | R/W | 0 | This fields indicates that VTT LDO has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear. |
| 2 | SWB2_PWRFLT | R/W | 0 | This fields indicates that SWB2 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear. |
| 1 | SWB1_PWRFLT | R/W | 0 | This fields indicates that SWB1 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear. |
| 0 | LDOA3_PWRFLT | R/W | 0 | This fields indicates that LDOA3 has lost its regulation. **0**: No Fault. **1**: Power fault has occurred. The host to write 1 to clear. |

Product Folder Links: *TPS650864*

### 8.13.54 TEMPCRIT: Temperature Fault Status Register (offset = B4h) [reset = 0000 0000]

Asserted when an internal temperature sensor detects rise of die temperature above the CRITICAL temperature threshold ($T_{CRIT}$). There are 5 temperature sensors across the die.

图 8-87. TEMPCRIT Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | DIE_CRIT | VTT_CRIT | TOP-RIGHT _CRIT | TOP-LEFT _CRIT | BOTTOM-RIGHT _CRIT |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R/W | R/W | R/W | R/W | R/W |

表 8-81. TEMPCRIT Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4 | DIE_CRIT | R/W | 0 | Temperature of rest of die has exceeded $T_{CRIT}$.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 3 | VTT_CRIT | R/W | 0 | Temperature of VTT LDO has exceeded $T_{CRIT}$.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 2 | TOP-RIGHT_CRIT | R/W | 0 | Temperature of die Top-Right has exceeded $T_{CRIT}$. Top-Right corner of die from top view given pin1 is in Top-Left corner.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 1 | TOP-LEFT_CRIT | R/W | 0 | Temperature of die Top-Left has exceeded $T_{CRIT}$.Top-Left corner of die from top view given pin1 is in Top-Left corner.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 0 | BOTTOM-RIGHT_CRIT | R/W | 0 | Temperature of die Bottom-Right has exceeded $T_{CRIT}$. Bottom-Right corner of die from top view given pin1 is in Top-Left corner.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |

Product Folder Links: *TPS650864*

### 8.13.55 TEMPHOT: Temperature Hot Status Register (offset = B5h) [reset = 0000 0000]

Asserted when an internal temperature sensor detects rise of die temperature above the HOT temperature threshold ($T_{HOT}$). There are 5 temperature sensors across the die.

图 8-88. TEMPHOT Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | DIE_HOT | VTT_HOT | TOP-RIGHT_HOT | TOP-LEFT_HOT | BOTTOM-RIGHT_HOT |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R/W | R/W | R/W | R/W | R/W |

表 8-82. TEMPHOT Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4 | DIE_HOT | R/W | 0 | Temperature of rest of die has exceeded $T_{HOT}$.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 3 | VTT_HOT | R/W | 0 | Temperature of VTT LDO has exceeded $T_{HOT}$.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 2 | TOP-RIGHT_HOT | R/W | 0 | Temperature of Top-Right has exceeded $T_{HOT}$. Top-Right corner of die from top view given pin1 is in Top-Left corner.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 1 | TOP-LEFT_HOT | R/W | 0 | Temperature of Top-Left has exceeded THOT. Top-Left corner of die from top view given pin1 is in Top-Left corner.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 0 | BOTTOM-RIGHT_HOT | R/W | 0 | Temperature of Bottom-Right has exceeded $T_{HOT}$. Bottom-Right corner of die from top view given pin1 is in Top-Left corner.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |

Product Folder Links: *TPS650864*

### 8.13.56 OC_STATUS: Overcurrent Fault Status Register (offset = B6h) [reset = 0000 0000]

Asserted when overcurrent condition is detected from a LSD FET.

图 8-89. OC_STATUS Register

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Bit Name | RESERVED | RESERVED | RESERVED | RESERVED | RESERVED | BUCK6_OC | BUCK2_OC | BUCK1_OC |
| TPS650864 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R/W | R/W | R/W |

表 8-83. OC_STATUS Register Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 2 | BUCK6_OC | R/W | 0 | BUCK6 LSD FET overcurrent has been detected.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 1 | BUCK2_OC | R/W | 0 | BUCK2 LSD FET overcurrent has been detected.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |
| 0 | BUCK1_OC | R/W | 0 | BUCK1 LSD FET overcurrent has been detected.<br>**0**: Not asserted.<br>**1**: Asserted. The host to write 1 to clear. |

## 9 Applications, Implementation, and Layout

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The TPS650864 for Xilinx MPSoCs and FPGAs can be used in a variety of ways which is outlined in the following sections. 节 9.2 discusses the design procedure for the general case. Specific OTP information can be found starting with 节 8.6. In general, the PMIC is controlled by the state of the six CTL which can accept up to 3.6 V inputs. How these control pins are set varies based on application. Some examples would be using the PG of external rails, looping GPOs back into CTL pins, connecting a locking push-button, using a push-button circuit, using an embedded controller (such as the msP430G2121), or controlled by the MPSoC itself.

### 9.2 Typical Application

This section describes the general application information and provides a more detailed description on the PMIC that powers a generic multicore-processor application. An example system block diagram for the device powering an SoC and the rest of platform is shown in 图 9-1. The functional block diagram in 图 8-1 outlines the typical external components necessary for proper device functionality.

Product Folder Links: *TPS650864*
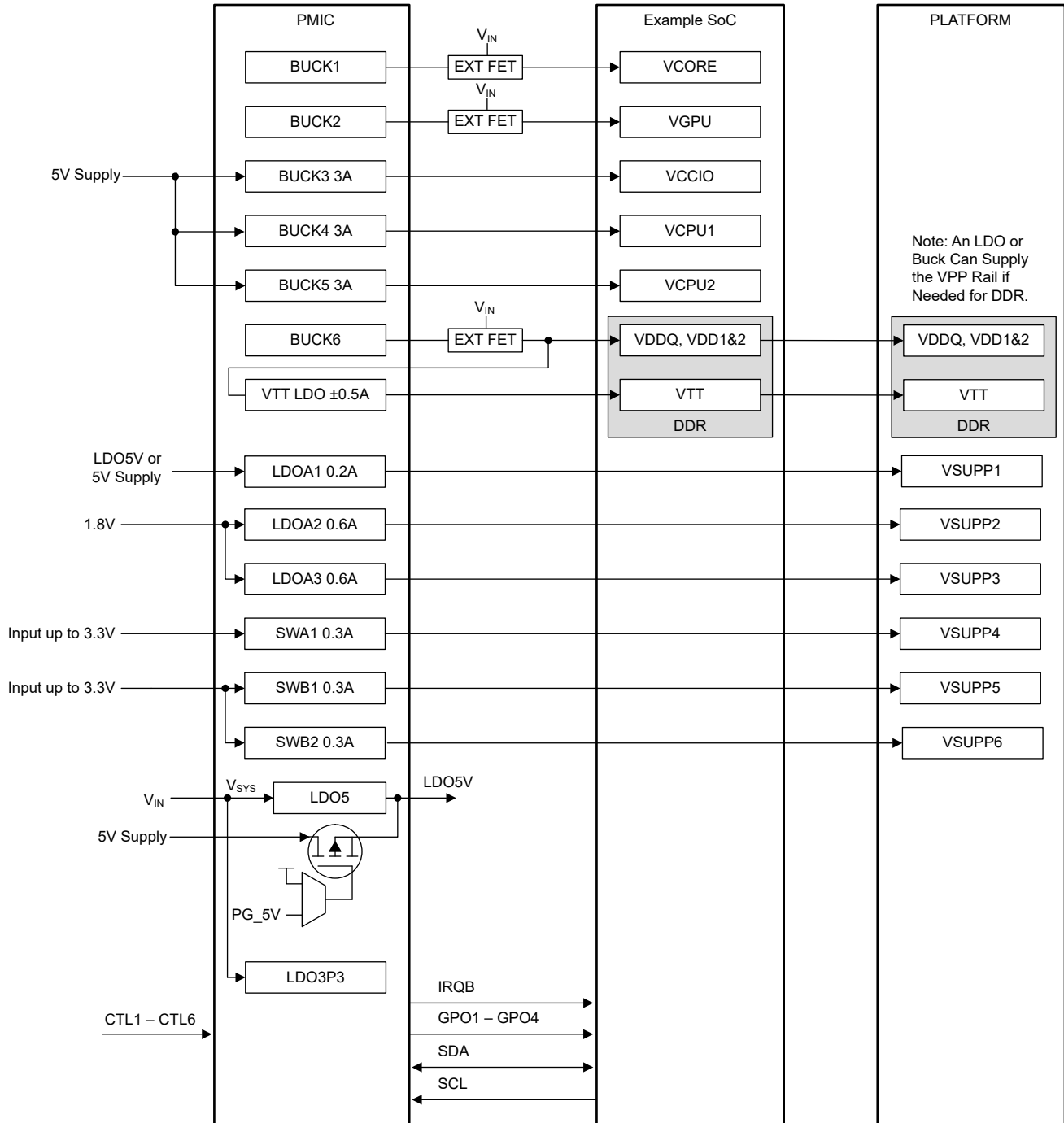
图 9-1. Typical Application Example

Product Folder Links: TPS650864

### 9.2.1 Design Requirements

The PMIC requires decoupling caps on the supply pins. Follow the values for recommended capacitance on these supplies given in 表 7. The controllers, converter, LDOs, and some other features can be adjusted to meet specific application needs. 节 9.2.2 describes how to design and adjust the external components to achieve desired performance.

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Controller Design Procedure

Designing the controller can be broken down into the following steps:

1.  Design the output filter.
2.  Select the FETs.
3.  Select the bootstrap capacitor.
4.  Select the input capacitors.
5.  Set the current limits.

Controllers BUCK1, BUCK2, and BUCK6 require a 5-V supply and capacitors at their corresponding DRV5V_x_x pins. For most applications, the DRV5V_x_x input should come from the LDO5P0 pin to ensure uninterrupted supply voltage; a 2.2-µF, X5R, 20%, 10-V, or similar capacitor must be used for decoupling.
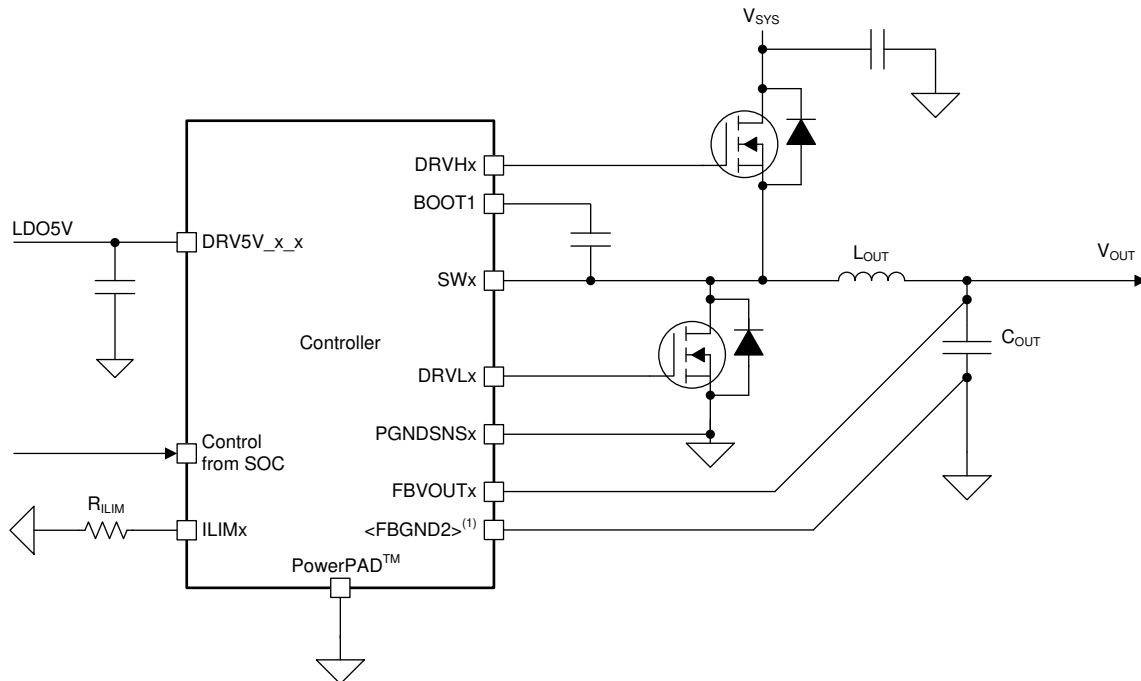
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A.    <FBGND2> is only present for BUCK2.

图 **9-2. Controller Diagram**

#### 9.2.2.1.1 Selecting the Inductor

Placement of an inductor is required between the external FETs and the output capacitors. Together, the inductor and output capacitors make the double-pole that contributes to stability. In addition, the inductor is directly responsible for the output ripple, efficiency, and transient performance. As the inductance used increases, the ripple current decreases, which typically results in an increased efficiency. However, with an increase in inductance used, the transient performance decreases. Finally, the inductor selected must be rated for appropriate saturation current, core losses, and DC resistance (DCR).

Equation 5 shows the calculation for the recommended inductance for the controller.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{sw} \times I_{OUT(MAX)} \times K_{IND}}$$

(5)

where

- $V_{OUT}$ is the typical output voltage
- $V_{IN}$ is the typical input voltage
- $f_{SW}$ is the typical switching frequency when loaded, 1 MHz unless otherwise noted
- $I_{OUT(MAX)}$ is the maximum load current
- $K_{IND}$ is the ratio of $I_{Lripple}$ to the $I_{OUT(MAX)}$. For this application, TI recommends that $K_{IND}$ is set to a value from 0.2 to 0.4. Higher values have improved transient performance, lower values have improved efficiency

With the chosen inductance value, the peak current for the inductor in steady state operation, $I_{L(max)}$, can be calculated using Equation 6. The rated saturation current of the inductor must be higher than the $I_{L(max)}$ current.

$$I_{L(MAX)} = I_{OUT(MAX)} + \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times V_{IN} \times f_{sw} \times L}$$

(6)

#### 9.2.2.1.2 Selecting the Output Capacitors

TI recommends using ceramic capacitors with low ESR values to provide the lowest output voltage ripple. The output capacitor requires an X7R or an X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the controller operates in PFM mode, and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

TI recommends the use of small ceramic capacitors placed between the inductor and load with many vias to the PGND plane for the output capacitors of the BUCK controllers. This solution typically provides the smallest and lowest cost solution available for D-CAP2 controllers.

The selection of the output capacitor is typically driven by the output transient response. Equation 7 and Equation 8 provide a rough estimate of the minimum required capacitance to ensure proper transient response. Because the transient response is significantly affected by the board layout, some experimentation is expected in order to confirm that values derived in this section are applicable to any particular use case. These are not meant to be an absolute requirement, but rather a rough starting point. Alternatively, some known combination values from which to begin are provided in 表 9-1. $V_{UNDER}$ and $V_{OVER}$ values should be greater than or equal to 3% of $V_{OUT}$ setting in order for equations to be meaningful. The equations provide some margin so that actual capacitance requirement may be lower than calculated.

$$C_{OUT} > \frac{I_{TRAN(MAX)}^2 \times L}{(V_{IN} - V_{OUT}) \times V_{UNDER}}$$

(7)

where

- $I_{TRAN(max)}$ is the maximum load current step
- L is the chosen inductance
- $V_{IN}$ is the maximum input voltage
- $V_{OUT}$ is the minimum programmed output voltage
- $V_{UNDER}$ is the maximum allowable undershoot from programmed voltage

$$C_{OUT} > \frac{I_{TRAN(MAX)}^2 \times L}{V_{OUT} \times V_{OVER}}$$

(8)

where

- $V_{OVER}$ is the maximum allowable overshoot from programmed voltage

Another key performance factor can be the ripple voltage while in pulsed frequency modulation mode, also known as discontinuous conduction mode. At light load, the controller will disable the low side FET once it detects a zero-crossing event on the inductor current. It will stay disabled until $V_{OUT}$ crosses below the set VID threshold. This architecture allows significant power savings at light load conditions by minimizing power loss through the low side FET and through switching. The disadvantage is that there is higher voltage ripple since the ripple current is only positive. Additionally, for even higher efficiency, $T_{ON(PFM)}$ for this device is typically 80% longer than $T_{ON(PWM)}$, which can be calculated by dividing the duty cycle by the switching frequency. An estimate for the required capacitance for a given allowable ripple voltage at light load is shown in Equation 9. ESR of the output capacitor is neglected here because ceramic capacitors, which typically have low ESR, are recommended. $V_{OVER}$ should not be set lower than 3% of $V_{OUT}$ value.

$$C_{OUT} > \frac{T_{ON\_EXT}^2 \times V_{OUT} \times (V_{IN} - V_{OUT})}{2 \times V_{IN} \times f_{SW}^2 \times V_{OVER} \times L}$$

(9)

where

- $T_{ON\_EXT}$ is the PFM on time extension constant, 1.8 unless otherwise noted in the part number specific section
- $V_{OUT}$ is the maximum programmed output voltage
- $V_{IN}$ is the maximum input voltage
- $f_{SW}$ is the typical switching frequency when loaded, 1 MHz unless otherwise noted
- $V_{OVER}$ is the maximum allowable overshoot from programmed voltage
- L is the chosen inductance

In cases where the transient current change is very low and ripple voltage allowance is large, the DC stability may become important. DCAP2 is a very stable architecture so this value is likely to be the smallest of those calculated. Equation 10 approximates the amount of capacitance necessary to maintain DC stability. Again, this is provided as a starting point; actual values will vary on a board-to-board case.

$$C_{OUT} > \frac{V_{OUT} \times 50 \ \mu s}{V_{IN} \times f_{SW} \times L}$$

(10)

where

- $V_{OUT}$ is the maximum programmed output voltage
- 50 μs is based on internal ramp setup
- $V_{IN}$ is the minimum input voltage
- $f_{SW}$ is the typical switching frequency
- L is the chosen inductance

Choosing the maximum valuable between Equation 7, Equation 8, Equation 9, and Equation 10 is recommended as a starting point to get the desired performance. All equations are estimates and have not been validated at all

Product Folder Links: *TPS650864*

variable corners. Removing excess capacitance or adding extra capacitance may be necessary during board evaluation. Testing can typically be performed on the evaluation module or on prototype boards.

表 9-1. Known LC Combinations for 1 µs Load Rise and Fall Time

| $I_{TRAN(max)}$ (A) | L (µH) | $V_{OUT}$ (V) | $V_{UNDER}$ (V) | $V_{OVER}$ (V) | $C_{OUT}$(µF) |
|---|---|---|---|---|---|
| 3.5 | 0.47 | 1 | 0.05 | 0.05 | 110 |
| 4 | 0.47 | 1 | 0.05 | 0.05 | 220 |
| 5 | 0.47 | 1.35 | 0.068 | 0.068 | 220 |
| 8 | 0.33 | 1 | 0.05 | 0.06 | 440 |
| 20 | 0.22 | 1 | 0.05 | 0.16 | 550 |

### 9.2.2.1.3 Selecting the FETs

This controller is designed to drive two NMOS FETs. Typically, lower $R_{DSON}$ values are better for improving the overall efficiency of the controller, however higher gate charge thresholds will result in lower efficiency so the two need to be balanced for optimal performance. As the $R_{DSON}$ for the low-side FET decreases, the minimum current limit increases; therefore, ensure selection of the appropriate values for the FETs, inductor, output capacitors, and current limit resistor. TI's CSD85301Q2, CSD87331Q3D, CSD87381P, CSD87588N, and CSD87350Q5D devices are recommended for the controllers, depending on the required maximum current.

### 9.2.2.1.4 Bootstrap Capacitor

To ensure the internal high-side gate drivers are supplied with a stable low-noise supply voltage, a capacitor must be connected between the SWx pins and the respective BOOTx pins. TI recommends placing ceramic capacitors with the value of 0.1 µF for the controllers. During testing, a 0.1-µF, size 0402, 10-V capacitor is used for the controllers.

TI recommends reserving a small resistor in series with the bootstrap capacitor in case the turnon and turnoff of the FETs must be slowed to reduce voltage ringing on the switch node, which is a common practice for controller design.

### 9.2.2.1.5 Setting the Current Limit

The current-limiting resistor value must be chosen based on Equation 1.

### 9.2.2.1.6 Selecting the Input Capacitors

Due to the nature of the switching controller with a pulsating input current, a low ESR input capacitor is required for best input-voltage filtering and also for minimizing the interference with other circuits caused by high input-voltage spikes. For the controller, a typical 2.2-µF capacitor can be used for the DRV5V_x_x pin to handle the transients on the driver. For the FET input, 10 µF of input capacitance (after derating) is recommended for most applications. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. For better input-voltage filtering, the input capacitor can be increased without any limit.

---

备注

Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.

---

TI recommends placing a ceramic capacitor as close as possible to the FET across the respective VSYS and PGND pins of the FETs. The preferred capacitors for the controllers are two Murata GRM21BR61E226ME44: 22-µF, 0805, 25-V, ±20%, or similar capacitors.

### 9.2.2.2 Converter Design Procedure

Designing the converter has only two steps: design the output filter and select the input capacitors.

图 9-3 shows a diagram of the converter.
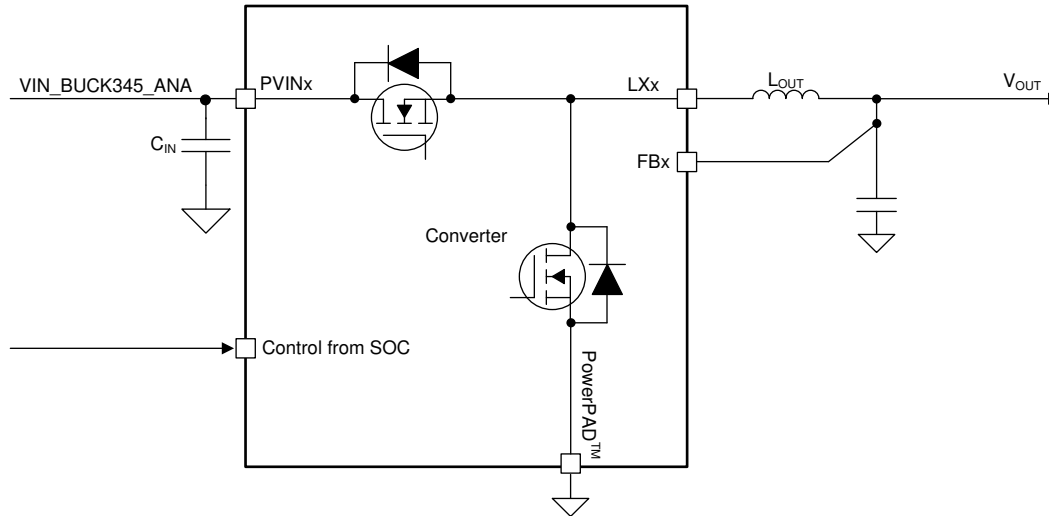
图 **9-3. Converter Diagram**

### 9.2.2.2.1 Selecting the Inductor

Internal parameters for the converters are optimized for either a 0.47 µH or 1 µH inductor, however it is possible to use other inductor values as long as they are chosen carefully and thoroughly tested. The equations from 节 9.2.2.1.1 can be utilized again with the parameters changed to match those of the converters. Switching frequency estimates can be found in 节 7.15.

### 9.2.2.2.2 Selecting the Output Capacitors

Ceramic capacitors with low ESR values are recommended because they provide the lowest output voltage ripple. The output capacitor requires either an X7R or X5R rating. Y5V and Z5U capacitors, aside from the wide variation in capacitance over temperature, become resistive at high frequencies.

At light load currents, the converter operates in PFM mode and the output voltage ripple is dependent on the output-capacitor value and the PFM peak inductor current. Higher output-capacitor values minimize the voltage ripple in PFM mode. To achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC-bias voltage.

For the output capacitors of the BUCK converters, TI recommends placing small ceramic capacitors between the inductor and load with many vias to the PGND plane. This solution typically provides the smallest and lowest-cost solution available.

The minimum output capacitance recommended is 22 µF for stability. Equation 7 and Equation 8 can be used to estimate the required output capacitance for a given load transient. Note that $V_{IN}$ will be different for the converters and that the switching frequency can be estimated using 节 7.15. Equation 9 can be neglected for converters as there is no on time extension and the $V_{IN}$ - $V_{OUT}$ term is typically smaller.

### 9.2.2.2.3 Selecting the Input Capacitors

Due to the nature of the switching converter with a pulsating input current, a low ESR input capacitor is required for best input-voltage filtering and for minimizing the interference with other circuits caused by high input-voltage spikes. For the PVINx pin, 2.5 µF of input capacitance (after derating) is required for most applications. A ceramic capacitor is recommended to achieve the low ESR requirement. However, the voltage rating and DC-bias characteristic of ceramic capacitors must be considered. The input capacitor can be increased without any limit for better input-voltage filtering.

> **备注**
>
> Use the correct value for the ceramic capacitor capacitance after derating to achieve the recommended input capacitance.
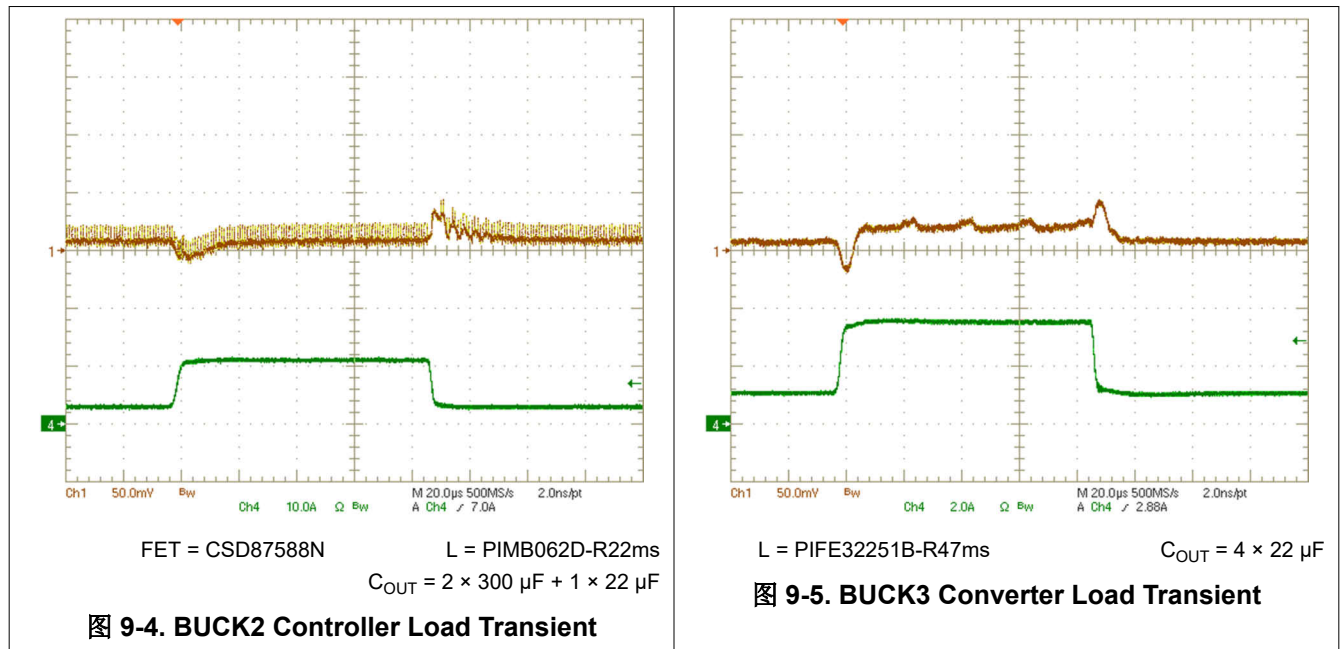
The preferred capacitor for the converters is one Samsung CL05A106MP5NUNC: 10-µF, 0402, 10-V, ±20%, or similar capacitor.

### 9.2.2.3 LDO Design Procedure

The VTT LDO must handle the fast load transients from the DDR memory for termination. Therefore, it is recommended to use ceramic capacitors to maintain a high amount of capacitance with low ESR on the VTT LDO outputs and inputs. The preferred output capacitors for the VTT LDO are the GRM188R60J226MEA0 from Murata (22 µF, 0603, 6.3 V, ±20%, or similar capacitors). The preferred input capacitor for the VTT LDO is the CL05A106MP5NUNC from Samsung (10-µF, 0402, 10-V, ±20%, or similar capacitor).

The remaining LDOs must have input and output capacitors chosen based on the values in 节 7.9.

### 9.2.3 Application Curves



FET = CSD87588N          L = PIMB062D-R22ms

$C_{OUT}$ = 2 × 300 µF + 1 × 22 µF

**图 9-4. BUCK2 Controller Load Transient**



L = PIFE32251B-R47ms          $C_{OUT}$ = 4 × 22 µF

**图 9-5. BUCK3 Converter Load Transient**

### 9.2.4 Layout

#### 9.2.4.1 Layout Guidelines

For a detailed description regarding layout recommendations, refer to the *TPS65086x Design Guide* and to the *TPS65086x Schematic and Layout Checklist*. For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can have stability problems and EMI issues. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitors, output capacitors, and inductors must be placed as close as possible to the device. Use a common-ground node for power ground and use a different, isolated node for control ground to minimize the effects of ground noise. Connect these ground nodes close to the AGND pin by one or two vias. Use of the design guide is highly encouraged in addition to the following list of other basic requirements:

- Do *not* allow the AGND, PGNDSNSx, or FBGND2 to connect to the thermal pad on the top layer.
- To ensure proper sensing based on FET $R_{DSON}$, PGNDSNSx must not connect to PGND until very close to the PGND pin of the FET.
- All inductors, input and output capacitors, and FETs for the converters and controller must be on the same board layer as the IC.
- To achieve the best regulation performance, place feedback connection points near the output capacitors and minimize the control feedback loop as much as possible.
- Bootstrap capacitors must be placed close to the device.
- The internal reference regulators must have their input and output capacitors placed close to the device pins.
- Route DRVHx and SWx as a differential pair. Ensure that there is a PGND path routed in parallel with DRVLx, which provides optimal driver loops.
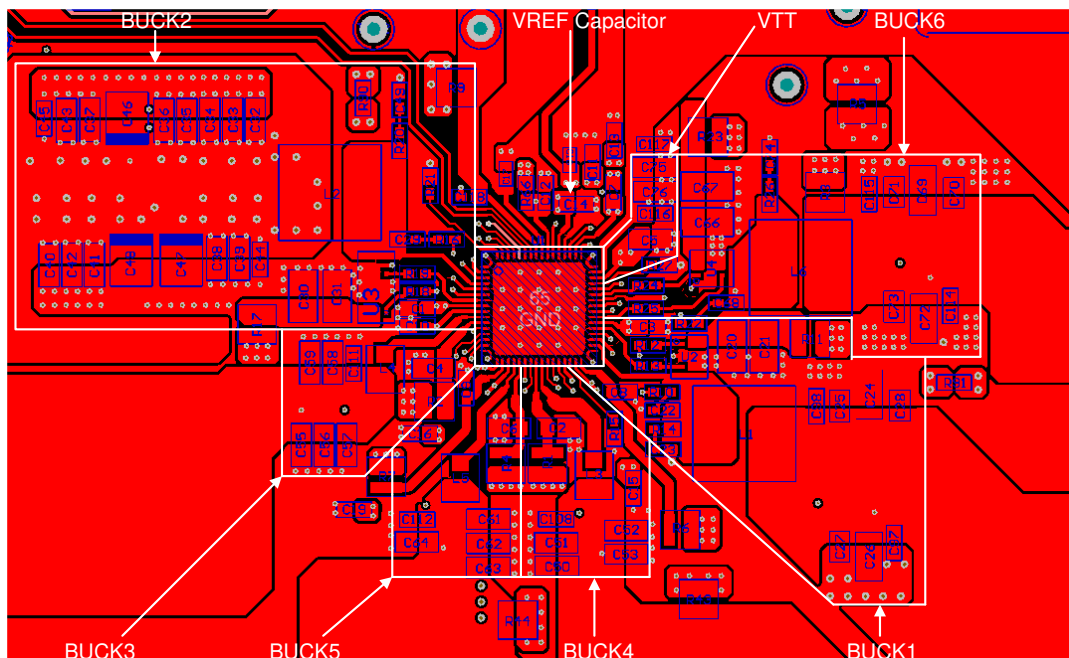
#### 9.2.4.2 Layout Example



**图 9-6. EVM Layout Example With All Components on the Top Layer**

Product Folder Links: *TPS650864*

### 9.2.5 VIN 5-V Application

The PMIC can be operated by a 5-V input voltage to the system because the power path of the controller does not go through the device itself. The concept is simple: supply the controller VINs with the 5-V input, and supply the VSYS with a 5.8-V step-up of the 5 V with a boost or charge pump. The 5.8 V is recommended because the UVLO of the internal LDO5 is at 5.6 V and the device measures the voltage at VSYS and determines the optimum internal compensation and controller settings thus, it is ideal the VSYS be close to the VIN of the controllers.
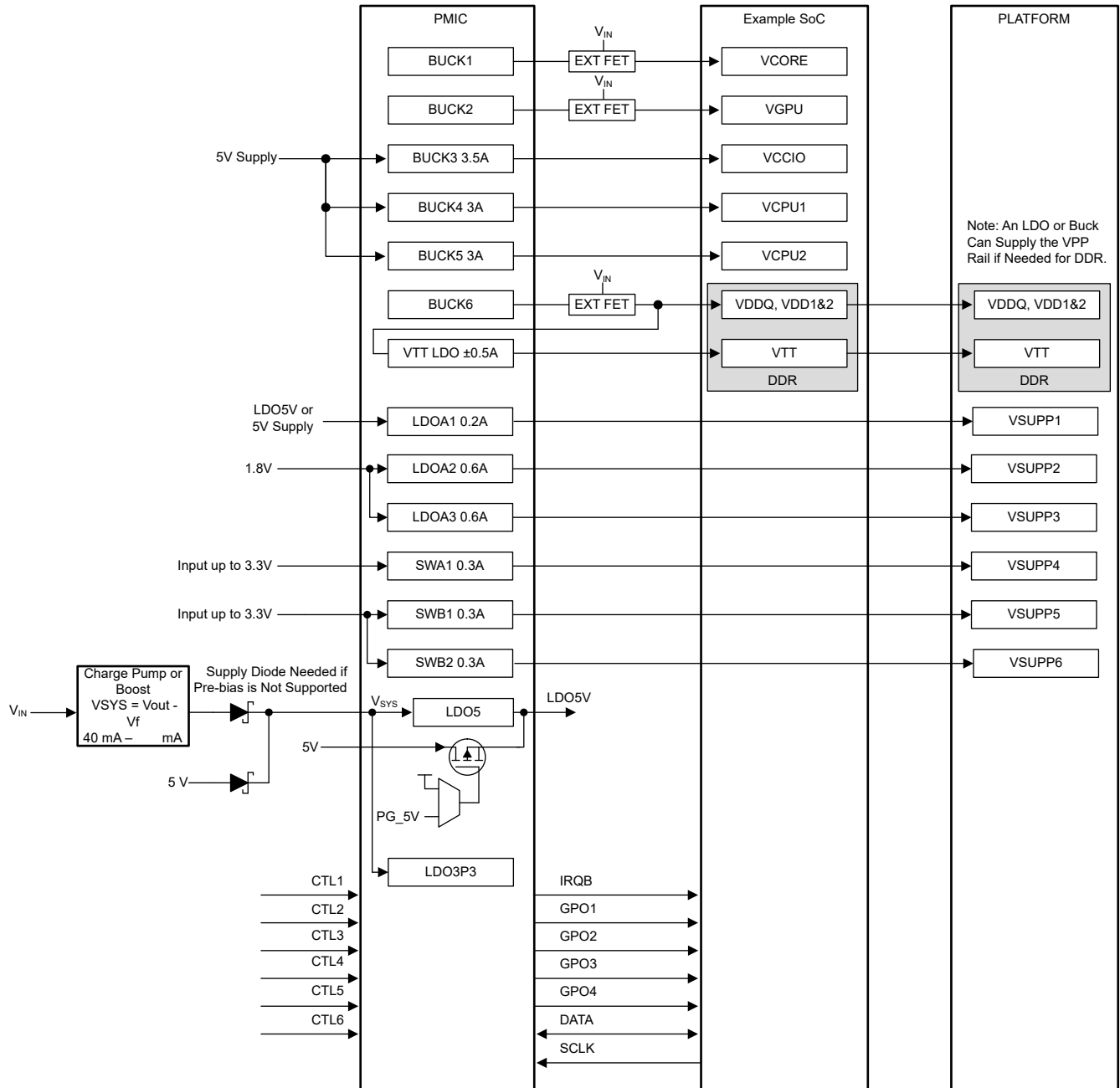


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**图 9-7. VIN 5-V Application**

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### 9.2.5.1 Design Requirements

The PMIC requires a step-up voltage from the 5-V input to 5.8 V for the VSYS supply. TI recommends keeping the VSYS near 5.8 V for optimization of the controllers.

Depending on the application use cases, the supply current to the VSYS can require from 40 mA with the drivers being supplied by the 5-V input to 440 mA with the drivers being supplied by the LDO5 and the LDOA1 being operated at max loading. This means that a charge pump may be used in some applications like the 5-V input but in others, a small boost may be required.

A Schottky diode from the 5-V input to the VSYS is recommended to ensure the VSYS is biased and the internal reference LDOs are on before the step-up regulator is enabled or fully ramped up. If the step-up cannot tolerate pre-bias condition then, 2 diodes may be needed to prevent the initial 5-V supply biasing the output of the step-up.

### 9.2.5.2 Design Procedure

To design a 5-V input application, first provide a step-up voltage from the 5-V input to the VSYS. Design the step-up to output a voltage near 5.8 V. Next, route the 5-V input to the controller and converter VINs. Thus, all power paths (*all high currents*) are routed through the controllers or directly to the converters. None of the high currents are required from the step-up supply. After the input stage is complete, the rest of the system can be designed as normal following the typical application procedure, using 5 V as the input value to the controllers.
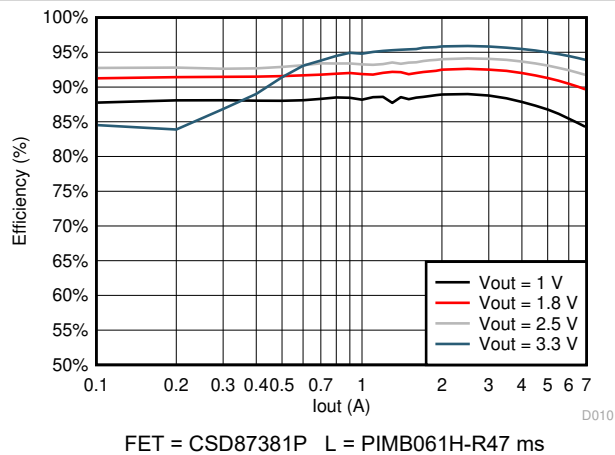
### 9.2.5.3 Application Curves



FET = CSD87381P   L = PIMB061H-R47 ms

**图 9-8. BUCK1 Efficiency at V$_{IN}$ = 5 V**

## 9.3 Power Supply Coupling and Bulk Capacitors

This device is designed to work with several different input voltages. The minimum voltage on the VSYS pin is 5.6 V for the device to start up; however, this is a low power rail. The input to the FETs must be from 4.5 V to 21 V as long as the proper BOM choices are made. Input to the converters should be between 3.3 V and 5 V. For the device to output maximum power, the input power must be sufficient. For the controllers, VIN must be able to supply sufficient input current for the output power of the application. For the converters, PVINx must be able to typically supply 2 A.

A best practice here is to determine power usage by the system and back-calculate the necessary power input based on expected efficiency values.

## 9.4 Do's and Don'ts

- Connect the LDO5V output to the DRV5V_x_x inputs for situations where an external 5-V supply is not initially available or is not available the entire time PMIC is on. If the external 5-V supply is always present, then DRV5V_x_x can be directly connected to remove the V5ANA-to-LDO5P0 load switch $R_{DSON}$.
- Ensure that none of the control pins are potentially floating.
- Include 0-$\Omega$ resistors on the DRVH or BOOT pins of controllers on prototype boards, which allows for slowing the controllers if the system is unable to handle the noise generated by the large switching or if switching voltage is too large due to layout.
- Do **not** connect the V5ANA power input to a different source other than PVINx. A mismatch here causes reference circuits to regulate incorrectly.
- Do **not** supply the V5ANA power input before the VSYS. Reference biasing of the internal FETs may turn on the HS FET passing the input to the output until VSYS is biased.
- Do **not** change the values of the reserved bits when writing I$^2$C. This can have unexpected consequences. Expected values for each OTP are shown in the register map.

Product Folder Links: TPS650864

## 10 Device and Documentation Support

### 10.1 Device Support

#### 10.1.1 第三方产品免责声明

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#### 10.1.2 Development Support

For documentation related to device development see the following:

- Texas Instruments, *TPS65086x Schematic and Layout Checklist*
- Texas Instruments, *TPS65086x Design Guide*

### 10.2 Documentation Support

#### 10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *CSD85301Q2 20 V Dual N-Channel NexFET™ Power MOSFETs* data sheet
- Texas Instruments, *CSD87331Q3D Synchronous Buck NexFET™ Power Block* data sheet
- Texas Instruments, *CSD87588N Synchronous Buck NexFET™ Power Block II* data sheet
- Texas Instruments, *CSD87381P Synchronous Buck NexFET™ Power Block II* data sheet
- Texas Instruments, *CSD87350Q5D Synchronous Buck NexFET™ Power Block* data sheet
- Texas Instruments, *MSP430G2121 Mixed Signal Microcontroller* data sheet
- Texas Instruments, *Power management integrated buck controllers for distant point-of-load applications* white paper
- Texas Instruments, *TPS65086x Evaluation Module* user's guide

### 10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者"按原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 10.5 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
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### 10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.7 术语表

TI 术语表            本术语表列出并解释了术语、首字母缩略词和定义。

Product Folder Links: *TPS650864*

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65086401RSKR | ACTIVE | VQFN | RSK | 64 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T65086401 PG1.0 | Samples |
| TPS65086401RSKT | ACTIVE | VQFN | RSK | 64 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T65086401 PG1.0 | Samples |
| TPS6508640RSKR | ACTIVE | VQFN | RSK | 64 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T6508640 PG1.0 | Samples |
| TPS6508640RSKT | ACTIVE | VQFN | RSK | 64 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T6508640 PG1.0 | Samples |
| TPS6508641RSKR | ACTIVE | VQFN | RSK | 64 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T6508641 PG1.0 | Samples |
| TPS6508641RSKT | ACTIVE | VQFN | RSK | 64 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T6508641 PG1.0 | Samples |
| TPS65086470RSKR | ACTIVE | VQFN | RSK | 64 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T65086470 PG1.0 | Samples |
| TPS65086470RSKT | ACTIVE | VQFN | RSK | 64 | 250 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 85 | T65086470 PG1.0 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**PACKAGE MATERIALS INFORMATION**

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
|----|----|
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS65086401RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086401RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086401RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086401RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS6508640RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS6508640RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS6508640RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS6508640RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS6508641RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS6508641RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS6508641RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS6508641RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086470RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086470RSKR | VQFN | RSK | 64 | 2000 | 330.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086470RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |
| TPS65086470RSKT | VQFN | RSK | 64 | 250 | 180.0 | 16.4 | 8.3 | 8.3 | 1.1 | 12.0 | 16.0 | Q2 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS65086401RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS65086401RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 35.0 |
| TPS65086401RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65086401RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |
| TPS6508640RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 35.0 |
| TPS6508640RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS6508640RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |
| TPS6508640RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |
| TPS6508641RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 35.0 |
| TPS6508641RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS6508641RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |
| TPS6508641RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65086470RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 38.0 |
| TPS65086470RSKR | VQFN | RSK | 64 | 2000 | 367.0 | 367.0 | 35.0 |
| TPS65086470RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |
| TPS65086470RSKT | VQFN | RSK | 64 | 250 | 210.0 | 185.0 | 35.0 |

RSK (S-PVQFN-N64)                    PLASTIC QUAD FLATPACK NO-LEAD

8,15 / 7,85

8,15 / 7,85

64

1

Pin 1 Index Area
Top and Bottom

1,00 / 0,80

0,20 Nominal
Lead Frame

Seating Plane

0,05 / 0,00

⌒ | 0,08 | C

64X 0,55 / 0,45

1        16

64

17

THERMAL PAD

SIZE AND SHAPE SHOWN
ON SEPARATE SHEET

4X | 6,00

49                    32

48        33

0,40

64X 0,25 / 0,15

Bottom View

4207547/C  04/12
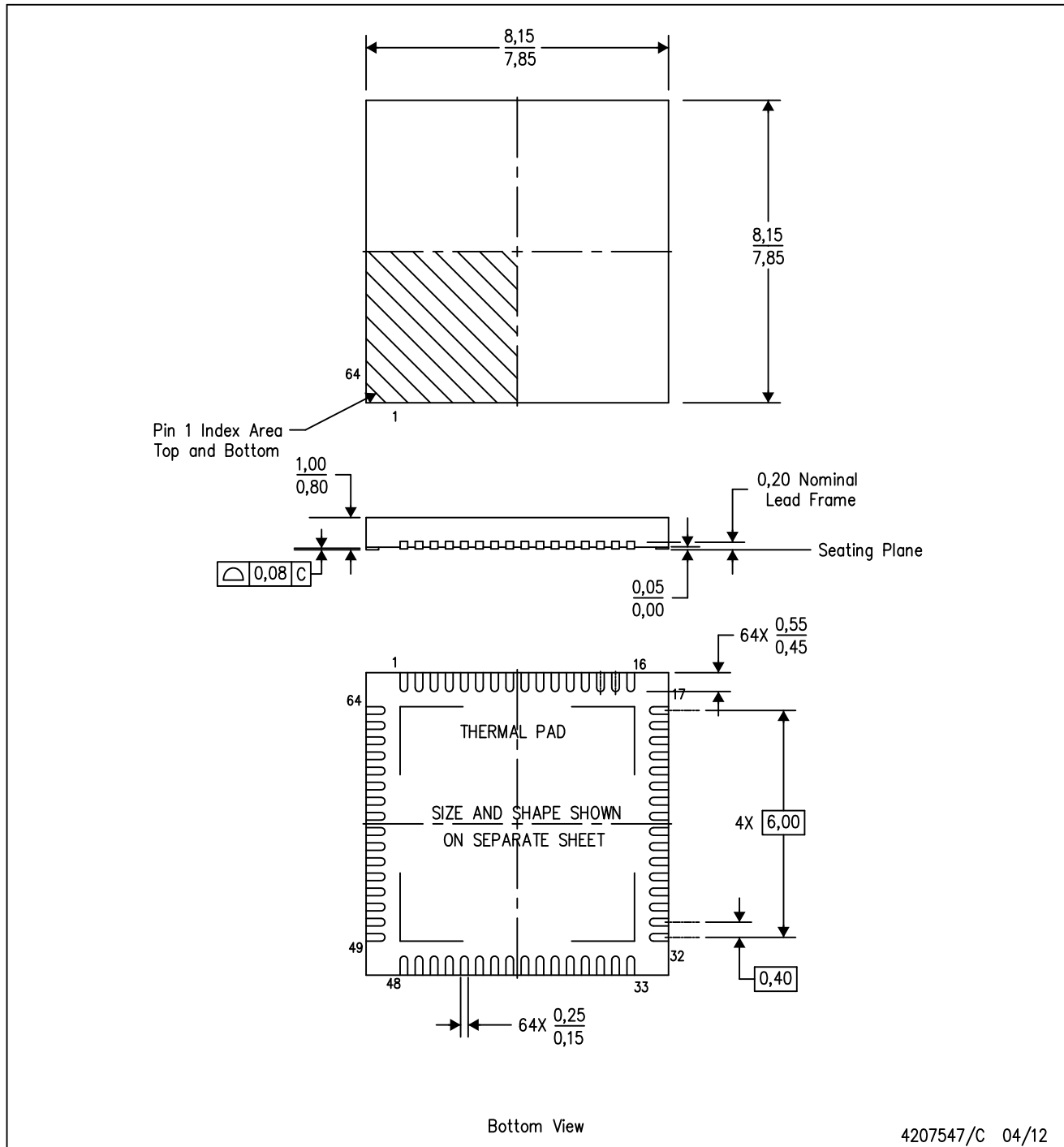
NOTES:    A.  All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5-1994.
          B.  This drawing is subject to change without notice.
          C.  QFN (Quad Flatpack No-Lead) Package configuration.
          D.  The package thermal pad must be soldered to the board for thermal and mechanical performance.
          E.  See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
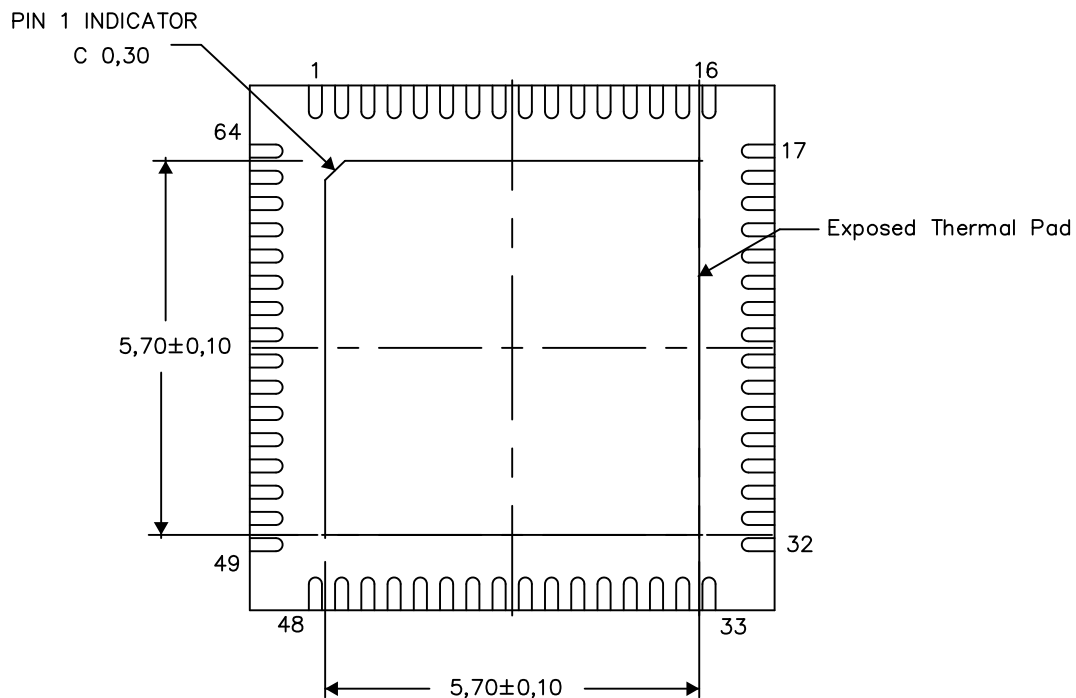
RSK (S−PVQFN−N64)                    PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

PIN 1 INDICATOR
C 0,30

64    1    16    17
5,70±0,10
49    48    32    33
5,70±0,10

Exposed Thermal Pad

Bottom View
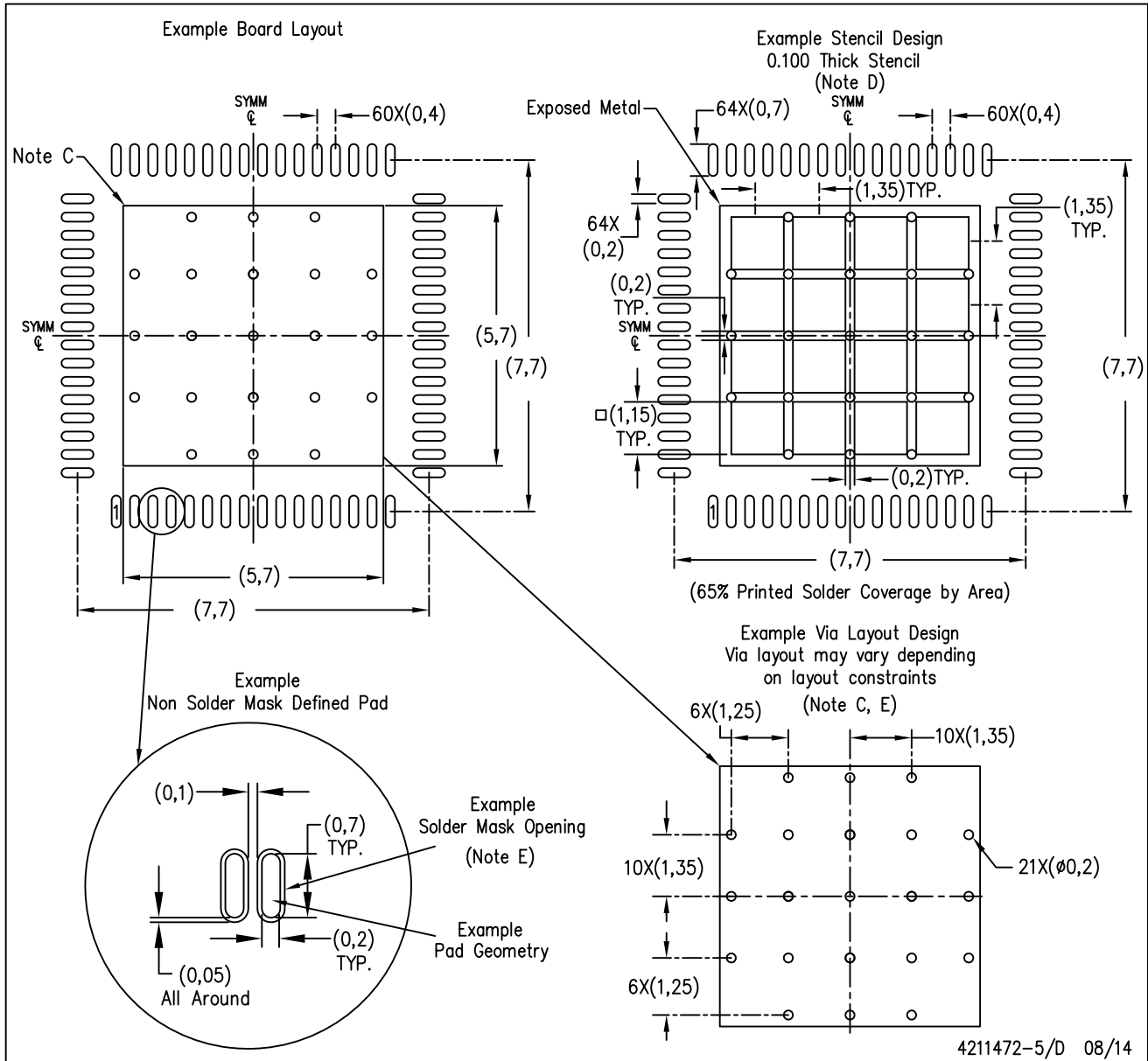
Exposed Thermal Pad Dimensions

4208001−5/H  08/14

NOTE:    A.    All linear dimensions are in millimeters

RSK (S−PVQFN−N64)          PLASTIC QUAD FLATPACK NO−LEAD

Example Board Layout

Note C

SYMM ℄

60X(0,4)

(5,7)

(7,7)

SYMM ℄

(5,7)

(7,7)

Example
Non Solder Mask Defined Pad

(0,1)

(0,7)
TYP.

Example
Solder Mask Opening
(Note E)

(0,2)
TYP.

Example
Pad Geometry

(0,05)
All Around

Example Stencil Design
0.100 Thick Stencil
(Note D)

Exposed Metal

64X(0,7)

SYMM ℄

60X(0,4)

(1,35)TYP.

(1,35)
TYP.

64X
(0,2)

(0,2)
TYP.

SYMM ℄

□(1,15)
TYP.

(0,2)TYP.

(7,7)

(7,7)

(65% Printed Solder Coverage by Area)

Example Via Layout Design
Via layout may vary depending
on layout constraints
(Note C, E)

6X(1,25)

10X(1,35)

10X(1,35)

21X(Ø0,2)

6X(1,25)

4211472−5/D   08/14

NOTES:   A.   All linear dimensions are in millimeters.
B.   This drawing is subject to change without notice.
C.   This package is designed to be soldered to a thermal pad on the board.  Refer to Application Note, Quad Flat−Pack
Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets
for specific thermal information, via requirements, and recommended board layout.  These documents are available at
www.ti.com <http://www.ti.com>.
D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release.  Customers should
contact their board assembly site for stencil design recommendations.  Refer to IPC 7525 for stencil design considerations.
E.   Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting
recommendations for any larger diameter vias placed in the thermal pad.

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