LM3253 High-Current Step-Down Converter for 2G/3G/4G RF Power Amplifiers

Check for Samples: LM3253

FEATURES

- **High-Efficiency PFM and PWM Modes with Internal Synchronous Rectification**
- **Analog Bypass Function with Low Dropout Resistance (45 mΩ typ.)**
- **Dynamically Adjustable Output Voltage, 0.4V to 3.6V (typ.), in PFM and PWM modes**
- **3A Maximum Load Current in PWM Mode**
- **2.7MHz (average) PWM Switching Frequency**
- **Modulated Switching Frequency to Aid Rx Band Compliance**
- **Operates From a Single Li-ion Cell (2.7V to 5.5V)**
- **ACB Reduces Inductor Requirements and Size**
- **Minimum Total Solution Size by Using Small Footprint and Case Size Inductor and Capacitors**
- **16-bump Thin DSBGA Package**
- **Current and Thermal Overload Protection**

APPLICATIONS

- **USB Datacards**
- **Cellular Phones**
- **Hand-Held Radios**
- **RF PC Cards**
- **Battery-Powered RF Devices**

DESCRIPTION

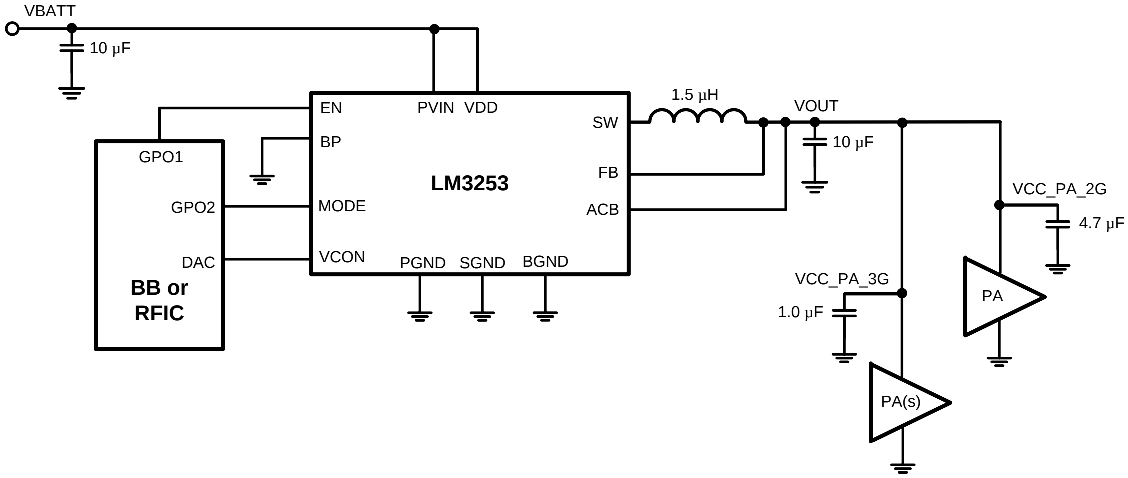
The LM3253 is a DC-DC converter optimized for powering multi-mode 2G/3G/4G RF power amplifiers (PAs) from a single Lithium-Ion cell. The LM3253 steps down an input voltage from 2.7V to 5.5V to a dynamically adjustable output voltage of 0.4V to 3.6V. The output voltage is set through a VCON analog input that adjusts the output voltage to ensure efficient operation at all power levels of the RF PA. The LM3253 is optimized for USB datacard applications.

The LM3253 operates in constant frequency Pulse Width Modulation (PWM) mode producing a small and predictable amount of output voltage ripple. This enables best ECTEL power requirements in GMSK and EDGE spectral compliance, with the minimal amount of filtering and excess headroom. When operating in Pulse Frequency Modulation (PFM) mode, the LM3253 enables the lowest DG09 current consumption and therefore maximizes system efficiency.

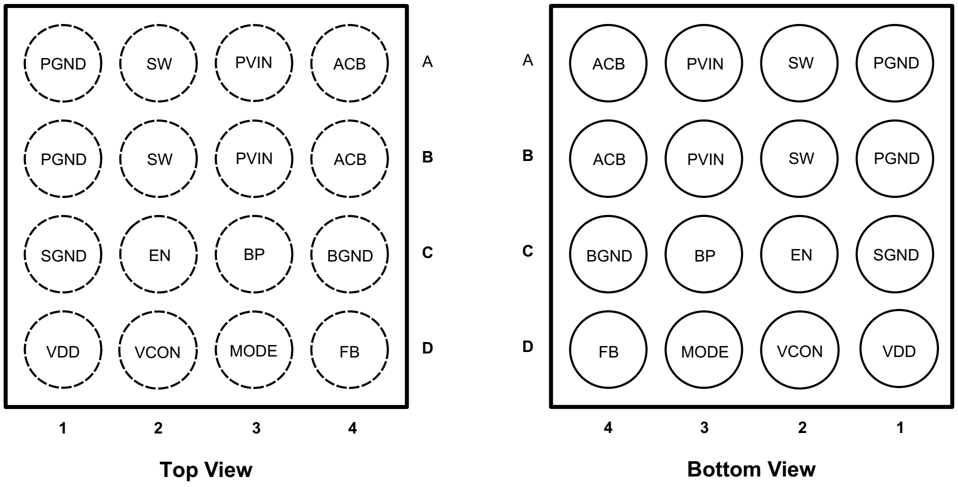
The LM3253 has a unique **A**ctive **C**urrent assist and analog **B**ypass (ACB) feature to minimize inductor size without any loss of output regulation for the entire battery voltage and RF output power range, until dropout. ACB provides a parallel current path, when needed, to limit the maximum inductor current to 1.84A (typ.) while still driving a 3A load. The ACB also enables operation with minimal dropout voltage. The LM3253 is available in a small 2 mm x 2 mm chip-scale 16-bump DSBGA package.

When considering the use of the LM3253 in a system design, contact the Texas Instruments Sales or Field Application engineer for a copy of the "LM3253: DC-DC Converter for 3G/4G RF PAs PCB Layout Considerations."

Typical System Application Diagram



Connection Diagram



Top View

	1	2	3	4
A	PGND	SW	PVIN	ACB
B	PGND	SW	PVIN	ACB
C	SGND	EN	BP	BGND
D	VDD	VCON	MODE	FB

Bottom View

	4	3	2	1
A	ACB	PVIN	SW	PGND
B	ACB	PVIN	SW	PGND
C	BGND	BP	EN	SGND
D	FB	MODE	VCON	VDD

Figure 1. 16-Bump 0.4 mm Pitch Thin DSBGA Package

Pin Descriptions

Pin #	Name	Description
A1	PGND	Power Ground to the internal NFET switch.
B1		
C1	SGND	Signal Analog and Control Ground (Low Current).
D1	VDD	Analog Supply Input.
A2	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier. Connect to an inductor with a saturation current rating that exceeds the $I_{LIM,PFET,Steady\ State}$ Current Limit specification of the LM3253.
B2		
C2	EN	Enable Input. Set this digital input HIGH for normal operation. For shutdown, set low. Pin has an 800 kΩ internal pulldown resistor.
D2	VCON	Voltage Control Analog input. V_{OUT} = 2.5 x VCON.
A3	PVIN	Power Supply Voltage Input to the internal PFET switch and ACB.
B3		
C3	BP	Bypass Mode Input. Set the pin HIGH for forced Bypass mode operation. Set the pin LOW for automatic Analog Bypass Mode (recommended).
D3	MODE	PWM/PFM Mode Selection Input. Setting the pin HIGH allows for PFM or PWM, depending on the load current. Setting the pin LOW forces the part to be in PWM only.
A4	ACB	Analog Current Bypass. Connect to the output at the output filter capacitor.
B4		
C4	BGND	Active Current assist and analog Bypass Ground (High Current).
D4	FB	Feedback Analog Input. Connect to the output at the output filter capacitor.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

VDD, PVIN to SGND		−0.2V to +6.0V
PGND to SGND		−0.2V to +0.2V
EN, FB, VCON, BP, MODE		(SGND −0.2V) to (VDD +0.2V)
SW, ACB		(PGND −0.2V) to (PVIN +0.2V
PVIN to VDD		−0.2V to +0.2V
Continuous Power Dissipation(4)		Internally Limited
Junction Temperature ($T_{J\text{-}MAX}$)		+150°C
Storage Temperature Range		−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 sec)		+260°C
ESD Rating(5)(6)	Human Body Model	2kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to the potential at the GND pins. The LM3253 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin LOW until the input voltage exceeds 2.7V.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 130°C (typ.).

(5) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7) The machine model is a 200 pF capacitor discharged directly into each pin.

(6) Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling procedures can result in damage.

OPERATING RATINGS(1)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0A to 3.0A
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range(2)	−30°C to +90°C

(1) All voltages are with respect to the potential at the GND pins. The LM3253 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin LOW until the input voltage exceeds 2.7V.

(2) In applications where high-power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$. At higher power levels duty cycle usage is assumed to drop (i.e., max power 12.5% usage is assumed) for 2G mode.

THERMAL PROPERTIES

Junction-to-Ambient Thermal	50°C/W
Resistance (θ_{JA}), YFQ Package(1)	

(1) Junction-to-ambient thermal resistance (θ_{JA}) is taken from thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7.

ELECTRICAL CHARACTERISTICS(1)(2)(3)

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_A = T_J \le +90°C$). Unless otherwise noted, all specifications apply to the Typical System Application Diagram with: PVIN = VDD = EN = 3.8V, BP = 0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{FB,\ LOW}$	Feedback voltage at low setting	VCON = 0.16V, MODE = LOW(3)	**0.3500**	0.400	**0.450**	V
$V_{FB,\ HIGH}$	Feedback voltage at high setting	VCON = 1.4V, V_{IN} = 3.9V, MODE = LOW(3)	**3.492**	3.6	**3.708**	V
I_{SHDN}	Shutdown supply current	EN = SW = VCON = 0V(4)		0.02	**4**	µA
I_{q_PFM}	DC bias current into VDD	No switching(5) MODE = HIGH		260	**310**	µA
I_{q_PWM}	DC bias current into VDD	No Switching (5) MODE = LOW		975	**1100**	
$I_{LIM,PFET,\ Transient}$	Positive transient peak current limit	VCON = 0.6V(6)		2.3	**2.5**	A
$I_{LIM,PFET,Steady\ State}$	Positive steady state peak current limit	VCON = 0.6V(6)	**1.78**	1.9	**2.09**	A
$I_{LIM,\ P\_ACB}$	Positive active current assist peak current limit	VCON = 0.6V, VACB = 2.8V(6)	**1.40**	1.70	**2.00**	A
$I_{LIM,\ NFET}$	NFET Switch negative peak current limit	VCON = 1.0V(6)	**−1.69**	−1.50	**−1.31**	A
F_{OSC}	Average internal oscillator frequency	VCON = 1.0V	**2.43**	2.70	**2.97**	MHz
V_{IH}	Logic HIGH input threshold	BP, EN, MODE	**1.2**			V
V_{IL}	Logic LOW input threshold	BP, EN, MODE			**0.5**	
I_{EN}	EN pin pulldown current	EN = 3.6V	**0**	5	**10**	µA
I_{IN}	Pin input current	BP, MODE	**−1**		**1**	
I_{VCON}	VCON pin leakage current	VCON = 1.0V	**−1**		**1**	
Gain	VCON to V_{OUT} Gain	$0.16V \le VCON \le 1.44V$(6)		2.5		V/V

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(1) All voltages are with respect to the potential at the GND pins. The LM3253 is designed for mobile phone applications where turn-on after power-up is controlled by the system controller and where requirements for a small package size overrule increased die size for internal Under Voltage Lock-Out (UVLO) circuitry. Thus, it should be kept in shutdown by holding the EN pin LOW until the input voltage exceeds 2.7V.

(2) Min and Max limits are specified by design, test, or statistical analysis.

(3) The parameters in the electrical characteristics table are tested under open loop conditions at PVIN = VIN = 3.8V. For performance over the input voltage range and closed-loop results, refer to the datasheet curves.

(4) Shutdown current includes leakage current of PFET.

(5) I_q specified here is when the part is not switching. For operating input current at no load, refer to datasheet curves.

(6) Current limit is built-in, fixed, and not adjustable.

SYSTEM CHARACTERISTICS

The following spec table entries are specified by design and verifications providing the component values in the Typical Application Circuit are used (L = 1.5 µH, DCR = 90 mΩ, TOKO DFE252010C (1269AS-H-1R5N), C_{IN} = 10 µF, 6.3V, 0402, Samsung CL05A106MQ5NUN, C_{OUT} = 10 µF + 4.7 µF + 3 x 1.0 µF + 3300 pF: 6.3V, 0402, Samsung CL05A106MQ5NUN, CL05A475MQNRN; 6.3V, 0201 Samsung CL03A105MQ3CSN; 6.3V, 01005 Murata GRM022R60J332K).
These parameters are not verified by production testing. Min and Max values are specified over the ambient temperature range T_A = −30°C to 90°C. Typical values are specified at PVIN = VDD = EN = 3.8V, BP = 0V and T_A = 25°C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{SETUP}	Time for SW pin to become active upon power-up	EN = LOW-to-HIGH	30			µs
t_{ON}	Turn-on time (time for output to reach 90% of final value after EN LOW-to-HIGH transition)	EN = LOW-to-HIGH, V_{IN} = 4.2V, VCON = 1.36V, V_{OUT} = 3.4V, I_{OUT} ≤ 1 mA			50	
$t_{RESPONSE}$	Time for V_{OUT} to rise from 0V to 3V (90% or 2.7V)	V_{IN} = 4.2V R_{LOAD} = 6.8Ω, VCON = 0V to 1.2V			20	µs
	Time for V_{OUT} to fall from 3.6V to 2.6V (10% or 2.7V)	V_{IN} = 4.2V, R_{LOAD} = 6.8Ω, VCON = 1.44V to 1.04V				
	Time for V_{OUT} to rise from 1.8V to 2.8V (90% or 2.7V)	V_{IN} = 4.2V, R_{LOAD} = 1.9Ω, VCON = 0.72V to 1.12V			15	
	Time for V_{OUT} to fall from 2.8V to 1.8V (10% or 1.9V)	V_{IN} = 4.2V, R_{LOAD} = 1.9Ω, VCON = 1.12V to 0.72V				
	Time for V_{OUT} to rise from 0V to 3.4V (90% or 3.1V)	V_{IN} = 4.2V, R_{LOAD} = 1.9Ω, VCON = 0V to 1.4V			20	
	Time for V_{OUT} to fall from 3.4V to 0.4V (10% or 0.7V)	V_{IN} = 4.2V, R_{LOAD} = 1.9Ω, VCON = 1.4V to 0.16V				
t_{Bypass}	Time for V_{OUT} to rise from 0V to PVIN after BP LOW-to-HIGH transition (90%)	VCON = 0V, I_{OUT} ≤ 1mA			20	µs
$t_{Bypass,\ ON}$	Bypass turn-on time. Time for V_{OUT} to rise from 0V to PVIN after EN LOW-to-HIGH transition (90% or 3.24)	EN = V_{IN}= 3.8V, I_{OUT} ≤ 1 mA			50	
R_{tot_drop}	Total dropout resistance in bypass mode	VCON = 1.5V, Max value at V_{IN} = 3.1V, Inductor ESR ≤ 151 mΩ		45	55	mΩ
C_{IN}	Pin input capacitance for BP, EN, MODE	Test frequency = 100 KHz		5		pF
I_{OUT}	Maximum load current in PWM mode	Switcher + ACB	3.0			A
$I_{OUT,\ PU}$	Maximum output transient pullup current limit	Switcher + ACB[1]	3.4			
$I_{OUT,\ PD,\ PWM}$	PWM maximum output transient pulldown current limit				−3.0	
$I_{OUT,\ MAX\text{-}PFM}$	Maximum output load current in PFM mode	V_{IN} = 3.8V, VCON < 1V MODE = HIGH[1]	85			mA
Linearity[2]	Linearity in control range of VCON = 0.16V to 1.44V	V_{IN} = 4.2V[1] Monotonic in nature	−3		+3	%
			−50		+50	mV

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(1) Current limit is built-in, fixed, and not adjustable.
(2) Linearity limits are ±3% or ±50 mV, whichever is larger.

SYSTEM CHARACTERISTICS (continued)

The following spec table entries are specified by design and verifications providing the component values in the Typical Application Circuit are used (L = 1.5 µH, DCR = 90 mΩ, TOKO DFE252010C (1269AS-H-1R5N), C_{IN} = 10 µF, 6.3V, 0402, Samsung CL05A106MQ5NUN, C_{OUT} = 10 µF + 4.7 µF + 3 x 1.0 µF + 3300 pF: 6.3V, 0402, Samsung CL05A106MQ5NUN, CL05A475MQNRN; 6.3V, 0201 Samsung CL03A105MQ3CSN; 6.3V, 01005 Murata GRM022R60J332K).
These parameters are not verified by production testing. Min and Max values are specified over the ambient temperature range T_A = −30°C to 90°C. Typical values are specified at PVIN = VDD = EN = 3.8V, BP = 0V and T_A = 25°C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
η	Efficiency	V_{IN} = 3.8V, V_{OUT} = 1.8V, I_{OUT} = 10 mA MODE = HIGH (PFM)	79	82		%
		V_{IN} = 3.8V, V_{OUT} = 0.5V, I_{OUT} = 5 mA MODE = HIGH (PFM)	58	60		
		V_{IN} = 3.8V, V_{OUT} = 3.5V, I_{OUT} = 1900 mA MODE = LOW (PWM)	89	92		
		V_{IN} = 3.8V, V_{OUT} = 2.5V, I_{OUT} = 250 mA MODE = LOW (PWM)	90	93		
		V_{IN} = 3.8V, V_{OUT} = 1.6V, I_{OUT} = 130 mA MODE = LOW (PWM)	83	86		
		V_{IN} = 3.8V, V_{OUT} = 1V, I_{OUT} = 400 mA MODE = LOW (PWM)	81	84		
V_{RIPPLE}	Ripple voltage at no pulse skipping condition	V_{IN} = 3.4V to 3.6V, V_{OUT} = 0.4V to 3.6V, R_{OUT} = 1.9Ω (3) MODE = LOW		1	3	mVpp
	Ripple voltage at pulse skipping condition	V_{IN} = 5.5V to dropout, V_{OUT} = 3.6V, R_{OUT} = 1.9Ω (3)			8	
	PFM Ripple Voltage	V_{IN} = 3.2V, V_{OUT} < 1.125V, I_{OUT} =10 mA, MODE = HIGH			50	
		V_{IN} = 3.2V, V_{OUT} ≤ 0.5V, I_{OUT} = 5 mA, MODE = LOW			50	
Line_tr	Line transient response	V_{IN} = 3.6V to 4.2V, T_R = T_F = 10 µs, V_{OUT} = 1V, I_{OUT} = 600 mA MODE = LOW		50		mVpk
Load_tr	Load transient response	V_{OUT} = 3.0V, T_R = T_F = 10 µs, I_{OUT} = 0A to 1.2A MODE = LOW		40		mVpk
Max Duty cycle	Maximum duty cycle	MODE = LOW	100			%
PFM_Freq	Minimum PFM Frequency	V_{IN} = 3.2V, V_{OUT} = 1V, I_{OUT} = 10 mA MODE = HIGH	100	160		kHz
		V_{IN} = 3.2V, V_{OUT} = 0.5V, I_{OUT} = 5 mA MODE = HIGH	34	55		

(3) Ripple voltage should be measured at C_{OUT} electrode on a well-designed PC board and using the suggested inductor and capacitors.

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs. Load Current
V_{IN} = 3.8V, I_{OUT} = 10mA to 150mA

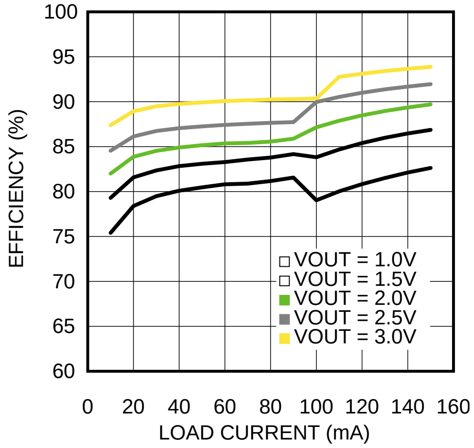

Figure 2.

Efficiency vs. Load Current
V_{IN} = 3.8V, I_{OUT} = 150mA to 750mA

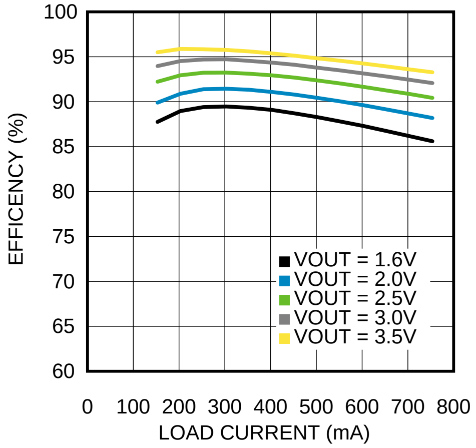

Figure 3.

Efficiency vs. Load Current
V_{IN} = 3.8V, I_{OUT} = 100mA to 1A

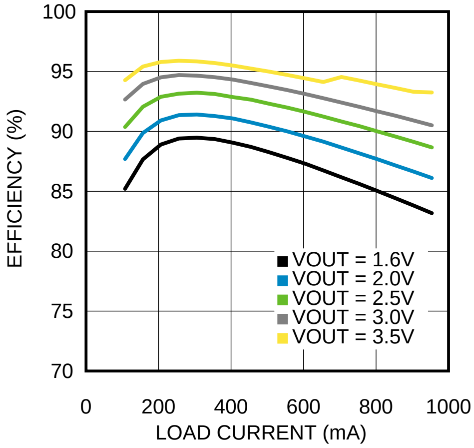

Figure 4.

Efficiency vs. Load Current
V_{IN} = 5V, I_{OUT} = 1A to 2.5A

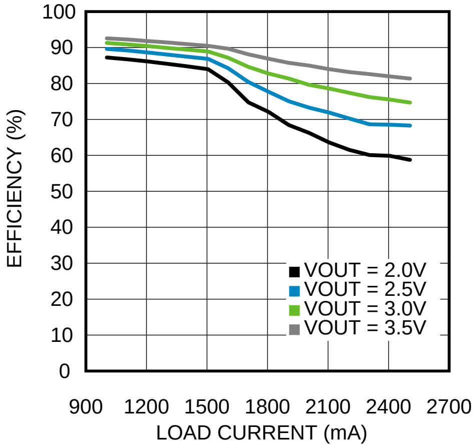

Figure 5.

Output Voltage vs. Supply Voltage
V_{OUT} = 3.4V, V_{IN} = 4.3V down to dropout

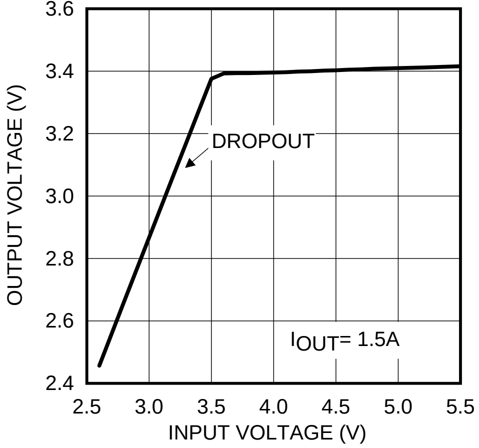

Figure 6.

Output Voltage vs. VCON Voltage
V_{IN} = 4.2V, R_{LOAD} = 6.8Ω, 0.16V < VCON < 1.4V

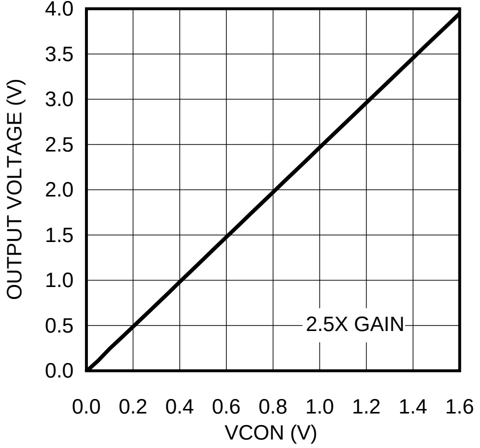

Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Center-Switching Frequency vs. Supply Voltage
V_{OUT} = 2.5V, I_{OUT} = 700mA, V_{IN} = 3.8V

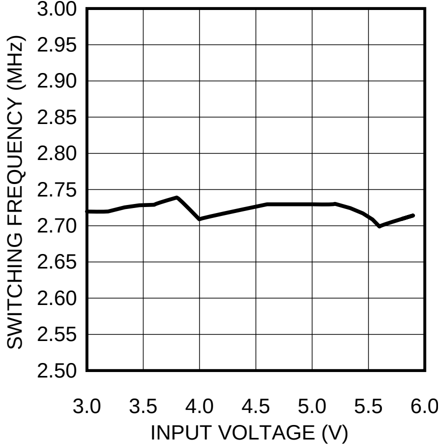

Figure 8.

Quiescent Current (PFM) vs. Supply Voltage
V_{OUT} = 1V, 2.7V < V_{IN}< 5.5V (No Load)

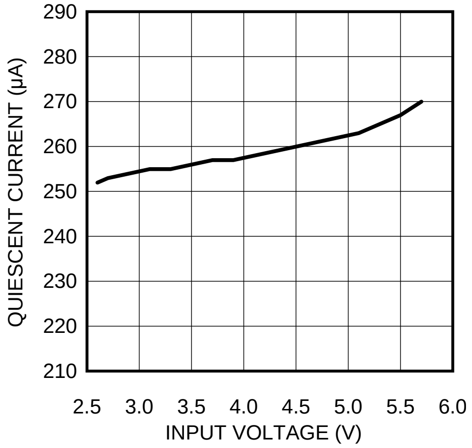

Figure 9.

Quiescent Current (PWM) vs. Supply Voltage
V_{OUT} = 2.5V, 2.7V < V_{IN}< 5.5V (No Load)

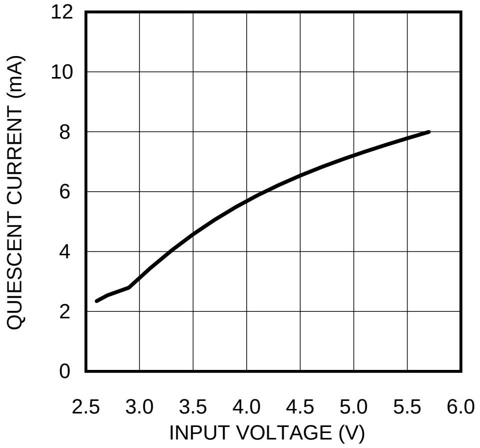

Figure 10.

VCON Transient (3G/4G)
V_{OUT} = 0V to 3V, R_{LOAD} = 6.8Ω, V_{IN} = 3.8V

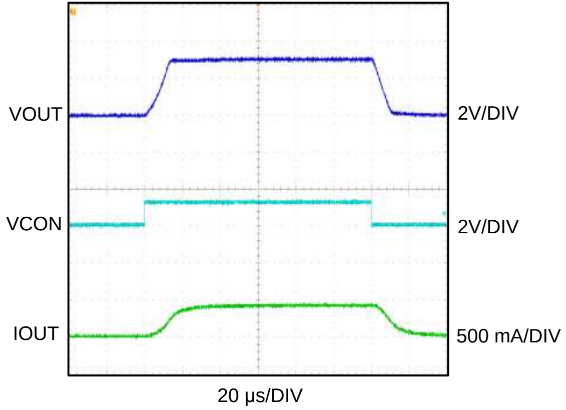

Figure 11.

VCON Transient (2G)
V_{OUT} = 1.4V to 3.4V, R_{LOAD} = 1.9Ω, V_{IN} = 4.2V

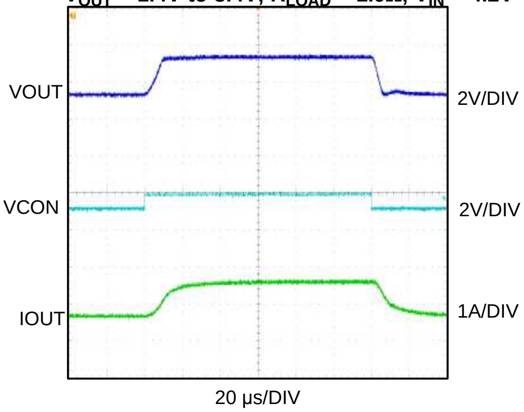

Figure 12.

Load Transient in PFM Mode
V_{OUT} = 1V, I_{OUT} = 0mA to 60mA, V_{IN} = 3.6V

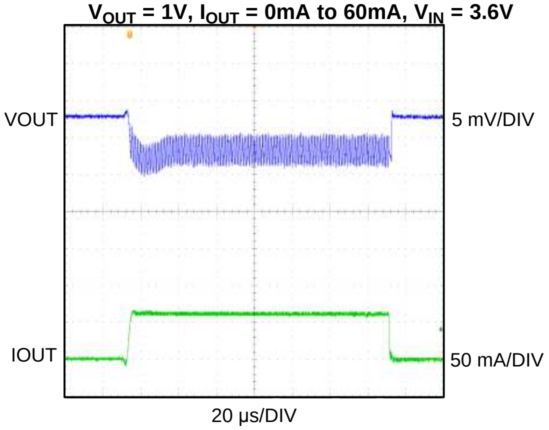

Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Load Transient in PWM Mode
V_{IN} = 3.8V, V_{OUT} = 2.5V, I_{OUT} = 0mA to 300mA

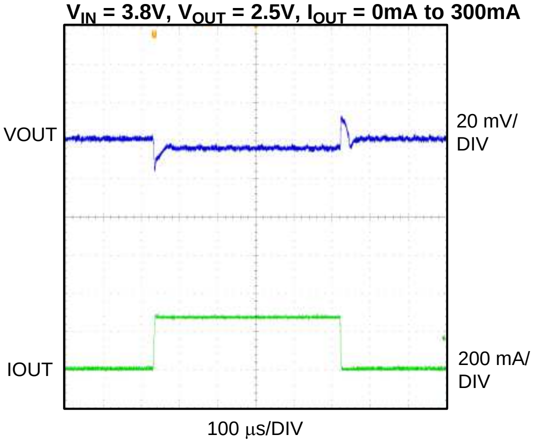

Figure 14.

Load Transient in PWM Mode
V_{IN} = 3.8V, V_{OUT} = 3V, I_{OUT} = 0mA to 700mA

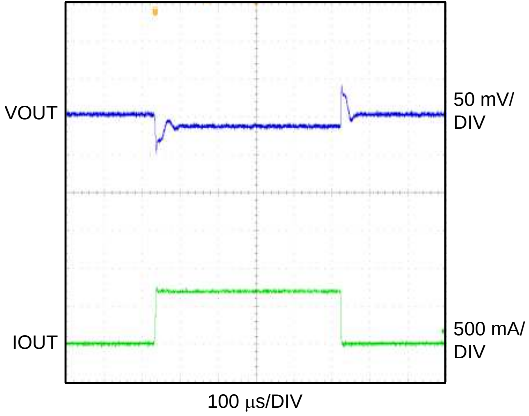

Figure 15.

Load Transient in PWM Mode
V_{IN} = 4.2V, V_{OUT} = 3V, I_{OUT} = 0mA to 1.2A

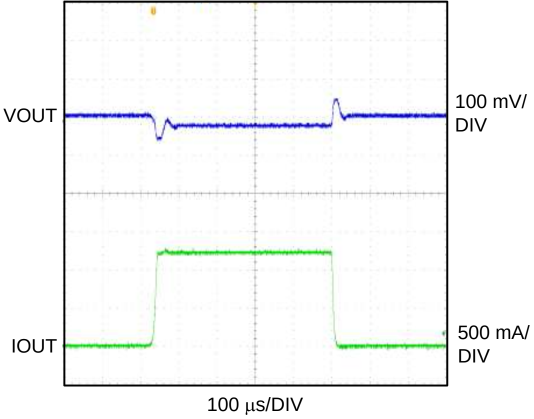

Figure 16.

Line Transient
V_{IN} = 3.6V to 4.2V, V_{OUT} = 2.5V, R_{LOAD} = 6.8Ω

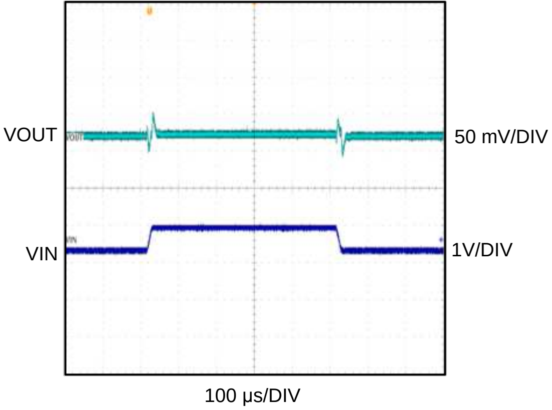

Figure 17.

Line Transient
V_{IN} = 3.6V to 4.2V, V_{OUT} = 1V, R_{LOAD} = 6.8Ω

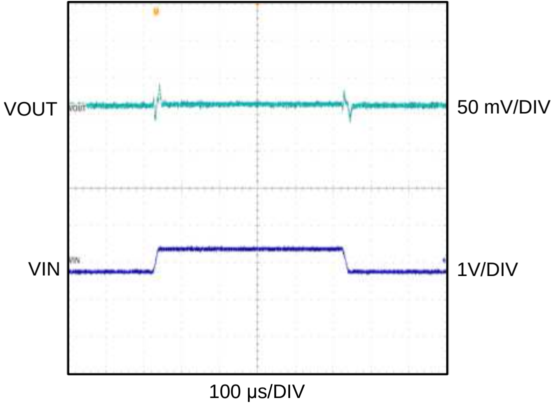

Figure 18.

Startup in PFM Mode
V_{IN} = 3.8V, V_{OUT} = 1V, No Load, EN = LOW to HIGH

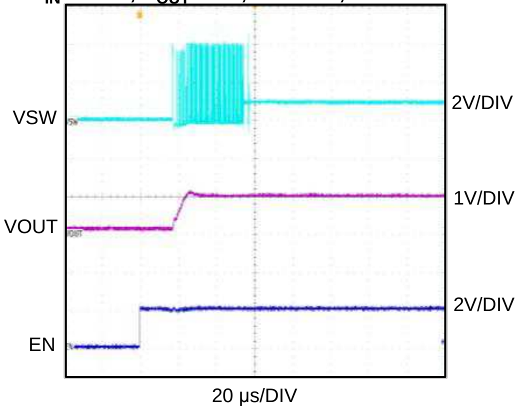

Figure 19.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Startup in PWM Mode
V_{IN} = 4.2V, V_{OUT} = 3.4V, No Load, EN = LOW to HIGH

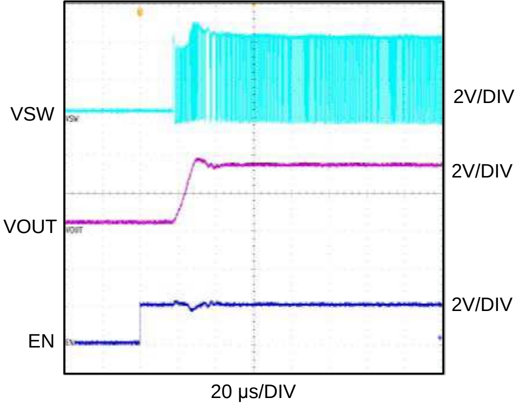

Figure 20.

Timed-Current Limit
V_{IN} = 4.2V, V_{OUT} = 2.5V, R_{LOAD} = 6.8Ω to V_{OUT} Shorted

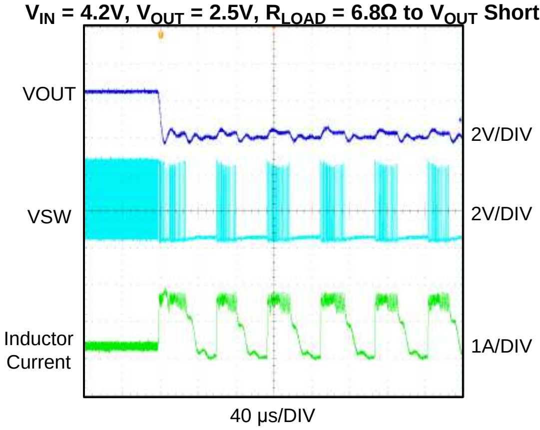

Figure 21.

OPERATION DESCRIPTION

Device Information

The LM3253 is a high-efficiency step-down DC-DC converter optimized to power the RF power amplifier (PA) in cell phones, portable communication devices, or battery-powered RF devices with a single Li-Ion battery. It operates in fixed-frequency PWM mode for 2G transmissions (with MODE = LOW), automatic mode transition between PFM and PWM mode for 3G/4G RF PA operation (with MODE = HIGH), forced bypass mode (with BP = HIGH) or in shutdown mode (with EN = LOW).

The fixed-frequency Pulse Width Modulation (PWM) mode provides high efficiency and very low output voltage ripple. In Pulse Frequency Modulation (PFM) mode, the converter operates with reduced switching frequencies and lower supply current to maintain high efficiencies. The forced bypass mode allows the user to drive the output directly from the input supply through a bypass FET. The shutdown mode turns the LM3253 off and reduces current consumption to 0.02 µA (typ.).

In PWM and PFM modes of operation, the output voltage of the LM3253 can be dynamically programmed from 0.4V to 3.6V (typ.) by adjusting the voltage on VCON. Current overload protection and thermal overload protection are also provided.

The LM3253 was engineered with **A**ctive **C**urrent assist and analog **B**ypass (ACB). This unique feature allows the converter to support maximum load currents of 3A (min.) while keeping a small footprint inductor and meeting all of the transient behaviors required for operation of a multi-mode RF Power Amplifier. The ACB circuit provides an additional current path when the load current exceeds 1.9A (typ.) or as the switcher approaches dropout. Similarly, the ACB circuit allows the converter to respond with faster VCON output voltage transition times by providing extra output current on rising and falling output edges. The ACB circuit also performs the function of analog bypass. Depending upon the input voltage, output voltage and load current, the ACB circuit automatically and seamlessly transitions the converter into analog bypass while maintaining output voltage regulation and low output voltage ripple. Full bypass (100% duty cycle operation) will occur if the total dropout resistance in bypass mode (R_{tot_drop} = 45 mΩ) is insufficient to regulate the output voltage.

The LM3253 16-bump DSBGA package is the best solution for space-constrained applications such as cell phones and other hand-held devices. The high switching frequency, 2.7 MHz (typ.) in PWM mode, reduces the size of input capacitors, output capacitors and of the inductor. Use of a DSBGA package is best suited for opaque case applications and requires special design considerations for implementation. (Refer to DSBGA Package Assembly And Use section below). As the LM3253 does not implement UVLO, the system controller should set EN = LOW and set BP = HIGH during power-up and UVLO conditions. (Refer to Shutdown Mode below).

PWM Operation

When the LM3253 operates in PWM mode, the switching frequency is constant, and the switcher regulates the output voltage by changing the energy-per-cycle to support the load required. During the first portion of each switching cycle, the control block in the LM3253 turns on the internal PFET switch. This allows current to flow from the input through the inductor and to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} – V_{OUT})/L$, by storing energy in its magnetic field.

During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET and to the output filter capacitor and load, which ramps the inductor current down with a slope of $–V_{OUT}/L$. The output filter capacitor stores charge when the inductor current is greater than the load current and releases it when the inductor current is less than the load current, smoothing the voltage across the load.

At the next rising edge of the clock, the cycle repeats. An increase of load pulls the output voltage down, increasing the error signal. As the error signal increases, the peak inductor current becomes higher, thus increasing the average inductor current. The output voltage is therefore regulated by modulating the PFET switch on-time to control the average current sent to the load. The circuit generates a duty-cycle modulated rectangular signal that is averaged using a low pass filter formed by the inductor and output capacitor. The output voltage is equal to the average of the duty-cycle modulated rectangular signal.

PFM Mode

With MODE = HIGH, the LM3253 automatically transitions to from PWM into PFM operation if the average inductor current is less than 75 mA (typ.) and $V_{IN} - V_{OUT} > 0.6V$. The switcher regulates the fixed output voltage by transferring a fixed amount of energy during each cycle and modulating the frequency to control the total power delivered to the output. The converter switches only as needed to support the demand of the load current, therefore maximizing efficiency. If the load current should increase during PFM mode to more than 95 mA (typ.), the part will automatically transition into constant frequency PWM mode. A 20 mA (typ.) hysteresis window exists between PFM and PWM transitions.

After a transient event, the part temporarily operates in 2.7 MHz (typ.) fixed-frequency PWM mode to quickly charge or discharge the output. This is true for start-up conditions or if MODE pin is toggled LOW-to-HIGH. Once the output reaches its target output voltage, and the load is less than 75 mA (typ.), then the part will seamlessly transition into PFM mode (assuming it is not in forced bypass or auto bypass condition).

Active Current Assist and Analog Bypass (ACB)

The 3GPP time mask requirement for 2G requires high current to be sourced by the LM3253. These high currents are required for a small time during transients or under a heavy load. Over-rating the switching inductor for these higher currents would increase the solution size and will not be an optimum solution. So to allow an optimal inductor size for such a load, an alternate current path is provided from the input supply through the ACB pin. Once the switcher current limit $I_{LIM,PFET,SteadyState}$ is reached, the ACB circuit starts providing the additional current required to support the load. The ACB circuit also minimizes the dropout voltage by having the analog bypass FET in parallel with V_{OUT}. The LM3253 can provide up to 3A (min.) of current in bypass mode with a 4A (max.) peak current limit.

Bypass Operation

The Bypass Circuit provides an analog bypass function with very low dropout resistance (R_{tot_drop} = 45 mΩ typ). When BP = LOW the part will be in automatic bypass mode which will automatically determine the amount of bypass needed to maintain voltage regulation. When the input supply voltage to the LM3253 is lowered to a level where the commanded duty cycle is higher than what the converter is capable of providing, the part will go into pulse-skipping mode. The switching frequency will be reduced to maintain a low and well-behaved output voltage ripple. The analog bypass circuit will allow the converter to stay in regulation until full bypass is reached (100% duty cycle operation). The converter comes out of full bypass and back into analog bypass regulation mode with a similar reverse process.

To override the automatic bypass mode, either set VCON > $(V_{IN})/(2.5)$ (but less than V_{IN}) or set BP = HIGH for forced bypass function. Forced bypass function is valid for $2.7V < V_{IN} < 5.5V$.

Shutdown Mode

To shut down the LM3253, pull the EN pin LOW (<0.5V). In shutdown mode, the current consumption is 0.02 µA (typ.) and the PFET switch, NFET synchronous rectifier, reference voltage source, control and bias circuit are turned OFF. To enable the LM3253 pull EN HIGH (>1.2V), and the mode of operation will be dependent on the voltage applied to the MODE pin.

Since the LM3253 does not feature a UVLO (Under Voltage Lock-Out) circuit, the EN pin should be set LOW to turn off the LM3253 during power-up and during UVLO conditions. For cell-phone applications, the system controller determines the power supply sequence; thus, it is up to the system controller to ensure proper sequencing by using all of the available pins and functions properly.

Mode Pin

The MODE pin changes the state of the converter to one of the two allowed modes of operation. Setting the MODE pin HIGH (>1.2V) sets the device for automatic transition between PFM/PWM mode operation. In this mode, the converter operates in PFM mode to maintain the output voltage regulation at very light loads and transitions into PWM mode at loads exceeding 95 mA (typ.). The PWM switching frequency is 2.7 MHz (typ.). Setting the MODE pin LOW (<0.5V) sets the device for PWM mode operation. The switching operation is in PWM mode only, and the switching frequency is also 2.7 MHz (typ.).

Dynamic Adjustment of Output Voltage

The output voltage of the LM3253 can be dynamically adjusted by changing the voltage on the VCON pin. In RF PA applications, peak power is required when the handset is far away from the base station. To maximize the power savings, the LM3253 output should be set just high enough to achieve the desired PA linearity. Hence, during low-power requirements, reduction of supply voltage to the PA can reduce power consumption from the PA, making the operation more efficient and promote longer battery life. Please refer to the Setting the Output Voltage section for further details.

Mode Selection

Table 1 shows the LM3253 parameters for the given modes (PWM or PFM/PWM).

Table 1. Parameters under Different Modes

Parameter/Mode	PWM	PFM/PWM
MODE pin	LOW	HIGH
BP pin	LOW	LOW
Frequency at loads = 75 mA (typ.)	2.7 MHz (typ.)	Variable
Frequency at loads = 95 mA (typ.)	2.7 MHz (typ.)	2.7 MHz (typ.)
V_{OUT}	2.5 x VCON	2.5 x VCON
Max Load Steady State	3 A (min.)	75 mA (min in PFM) or 3.0A (min. in PWM)

Internal Synchronous Rectification

The LM3253 uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop, thus increasing efficiency. The reduced forward voltage drop in the internal NFET synchronous rectifier significantly improves efficiency for low output voltage operation. The NFET is designed to conduct through its intrinsic body diode during the transient intervals, eliminating the need of an external diode.

Current Limit

The LM3253 current limit feature protects the converter during current overload conditions. Both SW and ACB pins have positive and negative current limits. The positive and negative current limits bound the SW and ACB currents in both directions. The SW pin has two positive current limits. The $I_{LIM,PFET,SteadyState}$ current limit triggers the ACB circuit. Once the peak inductor current exceeds $I_{LIM,PFET,SteadyState}$, the ACB circuit starts assisting the switcher and provides just enough current to keep the inductor current from exceeding $I_{LIM,PFET,SteadyState}$ allowing the switcher to operate at maximum efficiency. Transiently a second current limit $I_{LIM,PFET,Transient}$ of 2.3A (typ. or 2.5 max.) limits the maximum peak inductor current possible. The output voltage will fall out of regulation only after both SW and ACB output pin currents reach their respective current limits of $I_{LIM,PFET,Transient}$ and $I_{LIM,P\text{-}ACB}$.

Timed Current Limit

If the load or output short circuit pulls the output voltage to 0.3V or lower, the LM3253 switches to a timed current limit mode. In this mode the internal PFET switch is turned OFF after the current limit comparator trips, for 2~6 µsecs, to force the instantaneous inductor current to ramp down.

Thermal Overload Protection

The LM3253 IC has a thermal overload protection that protects itself from short-term misuse and overload conditions. If the junction temperature exceeds 150°C, the LM3253 shuts down. Normal operation resumes after the temperature drops below 130°C. Prolonged operation in thermal overload condition may damage the device and is therefore not recommended.

APPLICATION INFORMATION

Setting the Output Voltage

DAC Control

An analog voltage to the VCON pin can dynamically program the output voltage from 0.4V (typ.) to 3.6V (typ.) in both PFM and PWM modes of operation, without the need for external resistors. The output voltage is governed by Table 2.

Table 2. Output Voltage Selection

VCON (V)	V_{OUT} (V)
VCON = 0.16V to 1.44V	2.5 x VCON

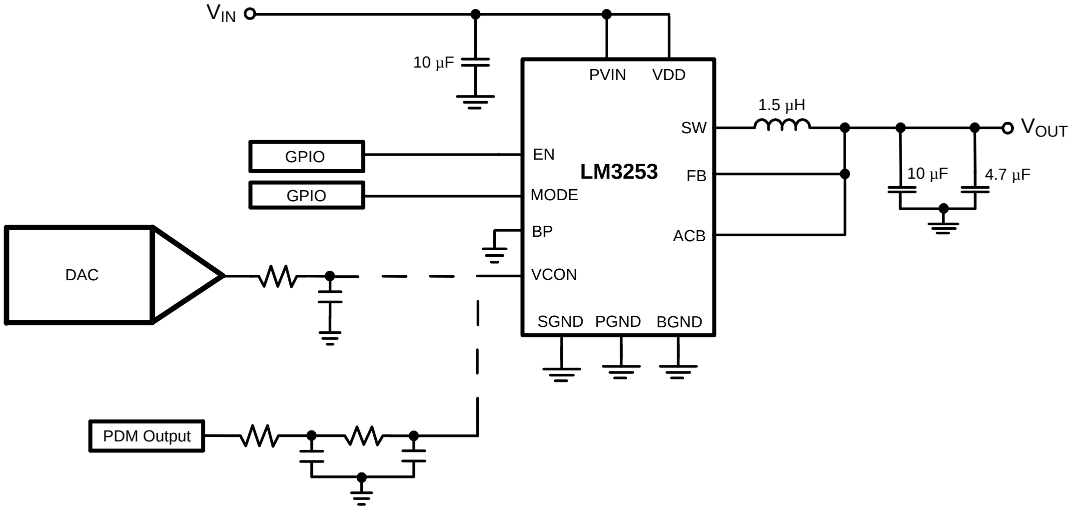

Figure 22. Dynamic Adjustment of Output Voltage with DAC or PDM

PDM-Based VCON Signal

Figure 22 shows the application circuit that enables the LM3253 to dynamically adjust the output voltage using a GPIO pin from the system controller. Figure 23 shows the waveforms when adjusted dynamically. The PDM signal of the GPIO is filtered using a low-pass filter and fed to the VCON pin. As the bitstream of the PDM signal changes, the voltage on the VCON pin changes. Thus, the duty ratio on the GPIO pin can be used to dynamically adjust the output voltage. The double low-pass filter reduces the ripple at VCON to avoid any excessive VCON-induced ripple at the output voltage.

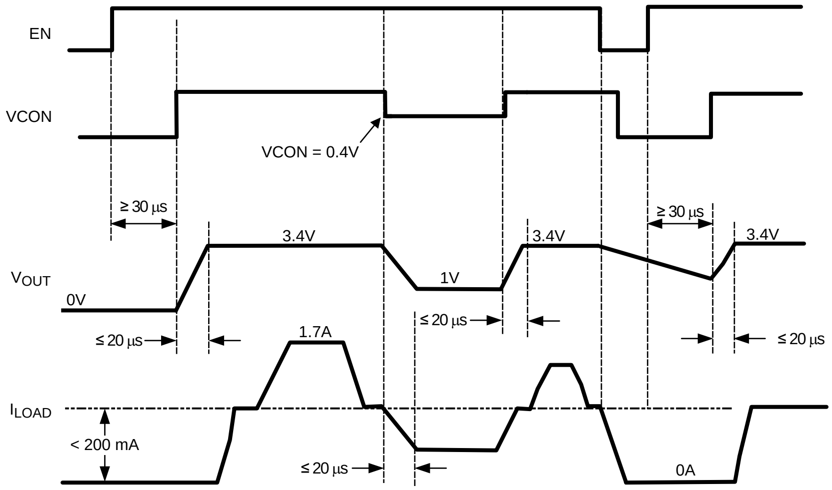

Figure 23. Dynamic Adjustment of Output Voltage with GPIO

VCON Pin

Figure 24 shows the equivalent CRC circuit for the VCON pin. This circuit is internal to the part and should be taken into consideration when driving this pin.

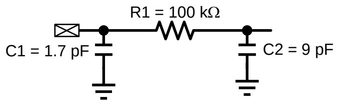

Figure 24. VCON Pin Equivalent CRC Circuit

Inductor Selection

A 1.5 µH inductor is needed for optimum performance and functionality of the LM3253. In the case of 2G transmission current bursts, the effective overall RMS current requirements are reduced. Therefore, please consult with the inductor manufacturers to determine if some of their smaller components will meet your application needs even though the classical inductor specification does not appear to meet the LM3253 RMS current specifications.

The LM3253 automatically manages the inductor peak and RMS (or steady current peak) current through the SW pin. The SW pin has two positive current limits. The first is the 1.90A typical (or 2.09A max.) over-limit current protection. It sets the upper steady-state inductor peak current (as detailed in the Electrical Characteristics Table - $I_{LIM,PFET,SteadyState}$). It is the dominant factor limiting the inductor's I_{SAT} requirement. The second is a over-limit current protection. It limits the maximum peak inductor current during large signal transients (i.e., < 20 µs) to 2.3A typical (or 2.5A maximum). A minimum inductance of 0.3 µH should be maintained at the second current limit.

The ACB circuit automatically adjusts its output current to keep the steady-state inductor current below the steady-state peak current limit. Thus, the inductor RMS current will effectively always be less than the $I_{LIM,PFET,SteadyState}$ during the transmit burst. In addition, as in the case with 2G where the output current comes in bursts, the effective overall RMS current would be much lower.

For good efficiency, the inductor's resistance should be less than 0.2Ω; low DCR inductors (<0.2Ω) are recommended. Table 3 suggests some inductors and suppliers.

Table 3. Suggested Inductors and Their Suppliers

Model	Vendor	Size	I_{SAT} - 30%	DCR
DFE252010C (1269AS-H-1R5N)	TOKO	2.5 mm x 2.0 mm x 1.0 mm	2.7A	90 mΩ
TFM252010A-1R5M	TDK	2.5 mm x 2.0 mm x 1.0 mm	2.9A	80 mΩ
TFM201610-1R5M	TDK	2.0 mm x 1.6 mm x 1.0 mm	2.2A	140 mΩ

Capacitor Selection

The LM3253 is designed to use ceramic capacitors for its input and output filters. Use a 10 µF capacitor for the input and approximately 10 µF actual total output capacitance. Capacitor types such as X5R, X7R are recommended for both filters. These provide an optimal balance between small size, cost, reliability and performance for cell phones and similar applications. Table 4 lists suggested part numbers and suppliers. DC bias characteristics of the capacitors must be considered while selecting the voltage rating and case size of the capacitor. Smaller case sizes for the output capacitor mitigate piezo-electric vibrations of the capacitor when the output voltage is stepped up and down at fast rates. However, they have a bigger percentage drop in value with DC bias. For even smaller total solution size, 0402 case size capacitors are recommended for filtering. Use of multiple 2.2 µF or 1 µF capacitors can also be considered. For RF Power Amplifier applications, split the output capacitor between DC-DC converter and RF Power Amplifiers: 10 µF (C_{OUT1}) + 4.7 µF (C_{OUT2}) + 3 x 1 µF (C_{OUT3}) is recommended. The optimum capacitance split is application dependent, and for stability the actual total capacitance (taking into account effects of capacitor DC bias, temperature de-rating, aging and other capacitor tolerances) should target 10 µF with 2.5V DC bias (measured at 0.5 V_{RMS}). Place all the output capacitors very close to the respective device. A high-frequency capacitor (3300 pF) is highly recommended to be placed next to C_{OUT1}.

Table 4. Suggested Capacitors and Their Suppliers

Capacitance	Model	Size (Wx L) (mm)	Vendor
10 µF	GRM185R60J106M	1.6 x 0.8	Murata
10 µF	CL05A106MQ5NUN	1.0 x 0.5	Samsung
4.7 µF	CL05A475MQ5NRN	1.0 x 0.5	Samsung
1.0 µF	CL03A105MQ3CSN	0.6 x 0.3	Samsung
3300 pF	GRM022R60J332K	0.4 x 0.2	Murata

EN Input Control

Use the system controller to drive the EN HIGH or LOW with a comparator, Schmitt trigger or logic gate. Set EN = HIGH (>1.2V) for normal operation and LOW (<0.5V) for shutdown mode to reduce current consumption to 0.02 µA (typ.) current.

Startup

The waveform Figure 25 in shows the startup condition. First, V_{IN} should take on a value between 2.7V and 5.5V. Next, EN should go HIGH (>1.2V). Finally, VCON should be set to a value that corresponds to the required output voltage (V_{OUT} = VCON x 2.5). V_{OUT} will reach its steady-state value in less than 50 µs. To optimize the startup time and behavior of the output voltage, the LM3253 will always start up in PWM mode (even when MODE = HIGH and output load current ≤ 75mA), then seamlessly transition into PFM mode.

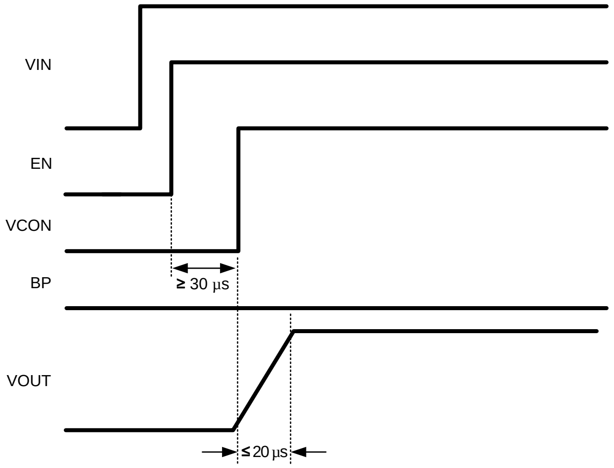

Figure 25. Startup Sequence and Conditions

DSBGA Package Assembly And Use

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Texas Instruments Application Note AN-1112 (SNVA009). Refer to the section *Surface Mount Assembly Considerations.* For best results in assembly, local alignment fiducials on the PC board should be used to facilitate placement of the device.

The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that would otherwise form if the solder-mask and pad overlap, which would hold the device off the surface of the board and interfere with mounting. See Application Note AN-1112 (SNVA009) for specific instructions how to do this.

The 16-bump package used for LM3253 has 265 micron solder balls and requires 0.225 mml pads for mounting the circuit board. The trace to each pad should enter the pad with a 90°entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 5.6 mil wide, for a section approximately 5 mil long, as a thermal relief. Then each trace should neck up or down to its optimal width. An important criterion is symmetry to insure the solder bumps on the LM3253 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A1, A3, B1, and B3 since PGND and PVIN are typically connected to large copper planes, inadequate thermal reliefs can result in inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red-opaque or infrared-opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges that are sensitive to light in the red and infrared range shining on the package's exposed die edges.

Board Layout Considerations

PC board layout is an important part of DC-DC converter design. Please contact TI for detailed PCB layout guidelines. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints between the DSBGA package and the board pads, which can result in erratic or degraded performance. Good layout for the LM3253 can be implemented by following a few simple design rules.

1. Place the LM3253 on pads with a pad size of 0.225 mm and a solder mask opening of 0.325 mm. As a thermal relief, connect to each pad to a trace that has maximally the same width as the solder mask opening and incrementally increase each trace to its optimal width. Each board trace connecting to the solder mask opening should be exactly the same width. This important criterion of symmetry is to insure that the solder bumps on the LM3253 re-flow evenly (see AN-1112: *Surface Mount Assembly Considerations*) (SNVA009).
2. Place the LM3253, inductor and filter capacitors close together and make the trace short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.3 mm of the LM3253.
3. Arrange the components so that the switching current loops curl in the same direction. During the first half of each cycle, current flows from the input filter capacitor through the LM3253 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground through the LM3253 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
4. Connect the ground pins of the LM3253 and filter capacitors together at a single-star connection using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with multiple vias in parallel. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3253 by giving it a low-impedance ground connection.
5. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
6. Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components (such as SW trace to the inductor). The voltage feedback trace must remain close to the LM3253 circuit and should be routed directly from FB to V_{OUT} at the output capacitor and should be routed opposite to noise components. This reduces EMI radiated onto the DC-DC converter’s own voltage feedback trace.
7. Split up output capacitors between LM3253 output and PA(s). Suggestion is to place one-half of output capacitance as close as possible to LM3253 output and the rest as close as possible to PA(s).

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3253TME/NOPB	ACTIVE	DSBGA	YFQ	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S60	Samples
LM3253TMX/NOPB	ACTIVE	DSBGA	YFQ	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-30 to 90	S60	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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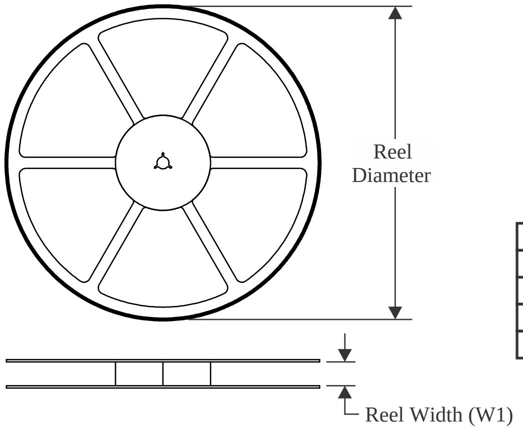
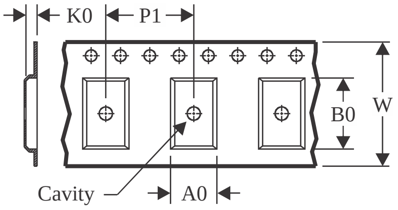
TAPE AND REEL INFORMATION

REEL DIMENSIONS

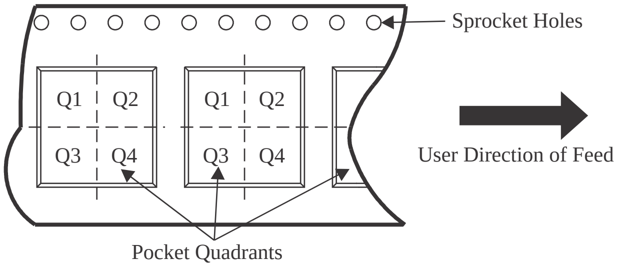


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

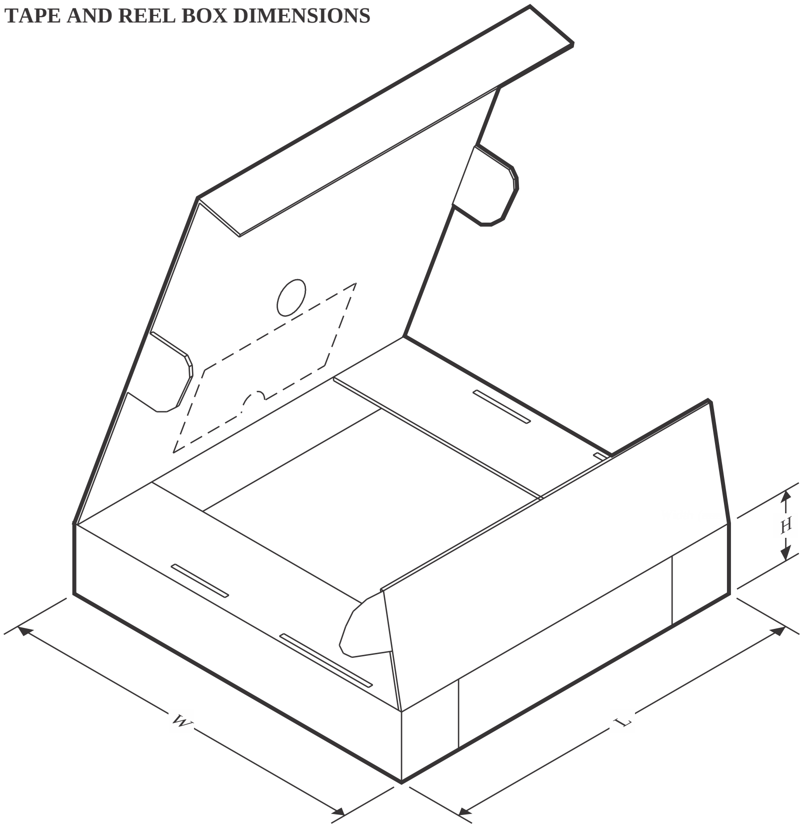
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3253TME/NOPB	DSBGA	YFQ	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM3253TMX/NOPB	DSBGA	YFQ	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

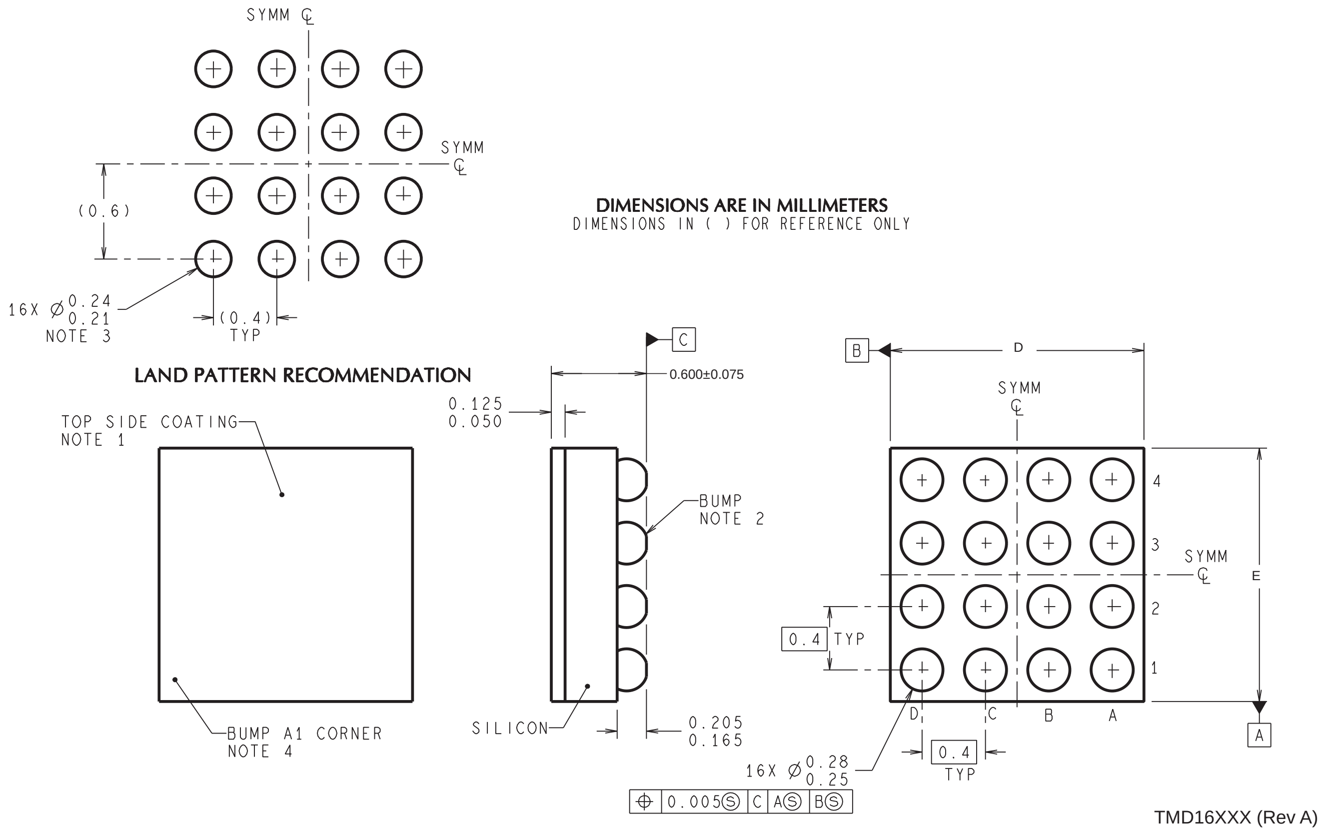
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3253TME/NOPB	DSBGA	YFQ	16	250	208.0	191.0	35.0
LM3253TMX/NOPB	DSBGA	YFQ	16	3000	208.0	191.0	35.0

YFQ0016



D: Max = 2.049 mm, Min =1.989 mm

E: Max = 2.049 mm, Min =1.989 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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