ADS7056超低功耗、超小尺寸 14 位高速 SAR ADC

1 特性

- 2.5MSPS 吞吐量
- 超小尺寸 SAR ADC：
  - 2.25mm^2 尺寸的 X2QFN-8 封装
- 宽工作电压范围：
  - AVDD：2.35V 至 3.6V
  - DVDD：1.65V 至 3.6V（与 AVDD 无关）
  - 温度范围：-40°C 至 +125°C
- 单极输入范围：0V 至 AVDD
- 出色的性能：
  - 14 位 NMC DNL，±2 LSB INL
  - 74.5dB SINAD (2kHz)
  - 73.7dB SINAD (1MHz)
- 超低功耗：
  - 2.5MSPS 下为 3.5mW (3.3V AVDD)
  - 100kSPS 下为 158µW (3.3V AVDD)
- 集成偏移校准
- 与 SPI 兼容的串行接口：60MHz
- 符合 JESD8-7A 标准的数字 I/O

2 应用

- 声纳接收器
- 光线路卡和模块
- 热成像
- 超声波流量计
- 电机控制
- 手持无线电
- 环境传感
- 烟火检测

3 说明

ADS7056 是一款 14 位 2.5MSPS 模数转换器 (ADC)。该器件包含一个基于电容器的逐次逼近型寄存器 (SAR) ADC，该 ADC 支持宽模拟输入电压范围（对于 AVDD 为 0V，对于 AVDD 范围为 2.35V 至 3.6V）。

串行外设接口 (SPI) 兼容串口由 $\overline{CS}$ 和 SCLK 信号控制。输入信号在 $\overline{CS}$ 下降沿进行采样，SCLK 用于转换和串行数据输出。该器件支持宽数字电源范围（1.65V 至 3.6V），可直接连接到各种主机控制器。ADS7056 的标称 DVDD 范围（1.65V 至 1.95V）符合 JESD8-7A 标准。

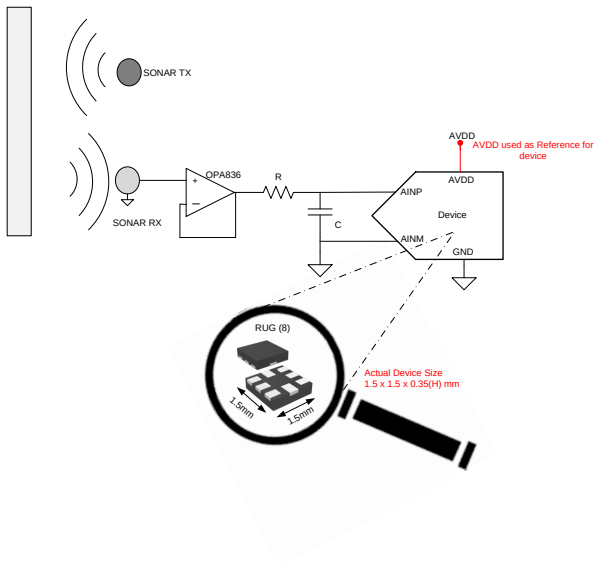
ADS7056 采用 8 引脚微型 X2QFN 封装，可以在扩展的工业温度范围（–40°C 至 +125°C）内正常工作。该器件尺寸微小且功耗极低，非常适合空间受限类电池供电的 应用。

器件信息(1)

部件名称	封装	封装尺寸（标称值）
ADS7056	X2QFN (8)	1.50mm x 1.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用



NOTE: ADS7056 比 0805（2012 公制）SMD 组件小。

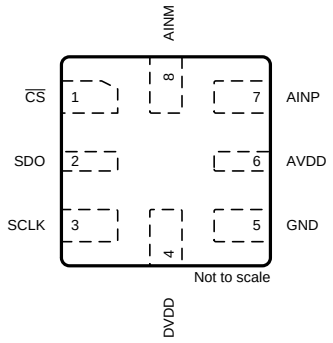
目录

4 修订历史记录

日期	修订版本	注释
2017 年 3 月	*	首次发布。

5 Pin Configuration and Functions

RUG Package
8-Pin X2QFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AINM	8	Analog input	Analog signal input, negative
AINP	7	Analog input	Analog signal input, positive
AVDD	6	Supply	Analog power-supply input, also provides the reference voltage to the ADC
$\overline{CS}$	1	Digital input	Chip-select signal, active low
DVDD	4	Supply	Digital I/O supply voltage
GND	5	Supply	Ground for power supply, all analog and digital signals are referred to this pin
SCLK	3	Digital input	Serial clock
SDO	2	Digital output	Serial data out

6 Specifications

6.1 Absolute Maximum Ratings(1)

	MIN	MAX	UNIT
AVDD to GND	–0.3	3.9	V
DVDD to GND	–0.3	3.9	V
AINP to GND	–0.3	AVDD + 0.3	V
AINM to GND	–0.3	0.3	V
Input current to any pin except supply pins	–10	10	mA
Digital input voltage to GND	–0.3	DVDD + 0.3	V
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage range	2.35	3	3.6	V
DVDD	Digital supply voltage range	1.65	1.8	3.6	V
T_A	Operating free-air temperature	–40	25	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS7056 RUG (X2QFN) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	177.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	76.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at AVDD = 3.3 V, DVDD = 1.65 V to 3.6 V, f_{SAMPLE} = 2.5 MSPS, and V_{AINM} = 0 V (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Full-scale input voltage span(1)			0		AVDD	V
	Absolute input voltage range	AINP to GND		–0.1		AVDD + 0.1	V
		AINM to GND		–0.1		0.1	
C_S	Sampling capacitance				16		pF
SYSTEM PERFORMANCE							
	Resolution				14		Bits
NMC	No missing codes			14			Bits
INL(2)	Integral nonlinearity			–3	±2	3	LSB(3)
DNL	Differential nonlinearity			–0.99	±0.5	1	LSB
E_O (2)	Offset error		After calibration(4)	–6	±2.5	6	LSB
dV_{OS}/dT	Offset error drift with temperature				1.75		ppm/°C
E_G (2)	Gain error			–0.1	±0.01	0.1	%FS
	Gain error drift with temperature				0.5		ppm/°C
SAMPLING DYNAMICS							
t_{CONV}	Conversion time				18 × t_{SCLK}		ns
t_{ACQ}	Acquisition time			95			ns
f_{SAMPLE}	Maximum throughput rate		60-MHz SCLK, AVDD = 2.35 V to 3.6 V			2.5	MHz
	Aperture delay				3		ns
	Aperture jitter, RMS				12		ps

(1) Ideal input span; does not include gain or offset error.
(2) See Figure 32, Figure 33, and Figure 34 for statistical distribution data for INL, offset error, and gain error.
(3) LSB means least significant bit.
(4) See the *OFFCAL State* section for details.

Electrical Characteristics (continued)

at AVDD = 3.3 V, DVDD = 1.65 V to 3.6 V, f_{SAMPLE} = 2.5 MSPS, and V_{AINM} = 0 V (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS						
SNR	Signal-to-noise ratio (5)	AVDD = 3.3 V	72	74.9		dB
		AVDD = 2.5 V		73.7		
THD	Total harmonic distortion (5)(6)	f_{IN} = 2 kHz		–85		dB
		f_{IN} = 250 kHz		–84.8		
		f_{IN} = 1000 kHz		–84.5		
SINAD	Signal-to-noise and distortion (5)	f_{IN} = 2 kHz	71.75	74.5		dB
		f_{IN} = 250 kHz		73.7		
		f_{IN} = 1000 kHz		73.7		
SFDR	Spurious-free dynamic range (5)	f_{IN} = 2 kHz		89.8		dB
		f_{IN} = 250 kHz		88		
		f_{IN} = 1000 kHz		87.5		
$BW_{(fp)}$	Full-power bandwidth	At –3 dB		200		MHz
DIGITAL INPUT/OUTPUT (CMOS Logic Family)						
V_{IH}	High-level input voltage (7)		0.65 DVDD		DVDD + 0.3	V
V_{IL}	Low-level input voltage (7)		–0.3		0.35 DVDD	V
V_{OH}	High-level output voltage (7)	At I_{source} = 500 µA	0.8 DVDD		DVDD	V
		At I_{source} = 2 mA	DVDD – 0.45		DVDD	
V_{OL}	Low-level output voltage (7)	At I_{sink} = 500 µA	0		0.2 DVDD	V
		At I_{sink} = 2 mA	0		0.45	
POWER-SUPPLY REQUIREMENTS						
AVDD	Analog supply voltage		2.35	3	3.6	V
DVDD	Digital I/O supply voltage		1.65	3	3.6	V
I_{AVDD}	Analog supply current	AVDD = 3.3 V, f_{SAMPLE} = 2.5 MSPS		1050	1250	µA
		AVDD = 3.3 V, f_{SAMPLE} = 100 kSPS		48	50	
		AVDD = 3.3 V, f_{SAMPLE} = 10 kSPS		5		
		AVDD = 2.5 V, f_{SAMPLE} = 2.5 MSPS		750		
		Static current with $\overline{CS}$ and SCLK high		0.02		
I_{DVDD}	Digital supply current	DVDD = 1.8 V, CSDO = 20 pF, output code = 2AAAh (8)		630		µA
		DVDD = 1.8 V, static current with $\overline{CS}$ and SCLK high		0.01		

(5) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise noted.
(6) Calculated on the first nine harmonics of the input frequency.
(7) Digital voltage levels comply with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V; see the *Parameter Measurement Information* section for details.
(8) See the *Estimating Digital Power Consumption* section for details.

6.6 Timing Requirements

all specifications are at AVDD = 2.35 V to 3.6 V, DVDD = 1.65 V to 3.6 V, and $C_{LOAD-SDO}$ = 20 pF (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

		MIN	TYP	MAX	UNIT
t_{CLK}	Time period of SCLK	16.66			ns
t_{su_CSCK}	Setup time: $\overline{CS}$ falling edge to SCLK falling edge	7			ns
t_{ht_CKCS}	Hold time: SCLK rising edge to $\overline{CS}$ rising edge	8			ns
t_{ph_CK}	SCLK high time	0.45		0.55	t_{SCLK}
t_{pl_CK}	SCLK low time	0.45		0.55	t_{SCLK}
t_{ph_CS}	$\overline{CS}$ high time	15			ns

6.7 Switching Characteristics

all specifications are at AVDD = 2.35 V to 3.6 V, DVDD = 1.65 V to 3.6 V, and $C_{LOAD-SDO}$ = 20 pF (unless otherwise noted); minimum and maximum values for T_A = –40°C to +125°C; typical values at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CYCLE} (1)	Cycle time		400			ns
t_{CONV}	Conversion time			18 × t_{SCLK}		ns
t_{den_CSDO}	Delay time: $\overline{CS}$ falling edge to data enable				6.5	ns
t_{d_CKDO}	Delay time: SCLK rising edge to (next) data valid on SDO				10	ns
t_{ht_CKDO}	SCLK rising edge to current data invalid		2.5			
t_{dz_CSDO}	Delay time: $\overline{CS}$ rising edge to SDO going to tri-state		5.5			ns

(1) $t_{CYCLE} = 1 / f_{SAMPLE}$.

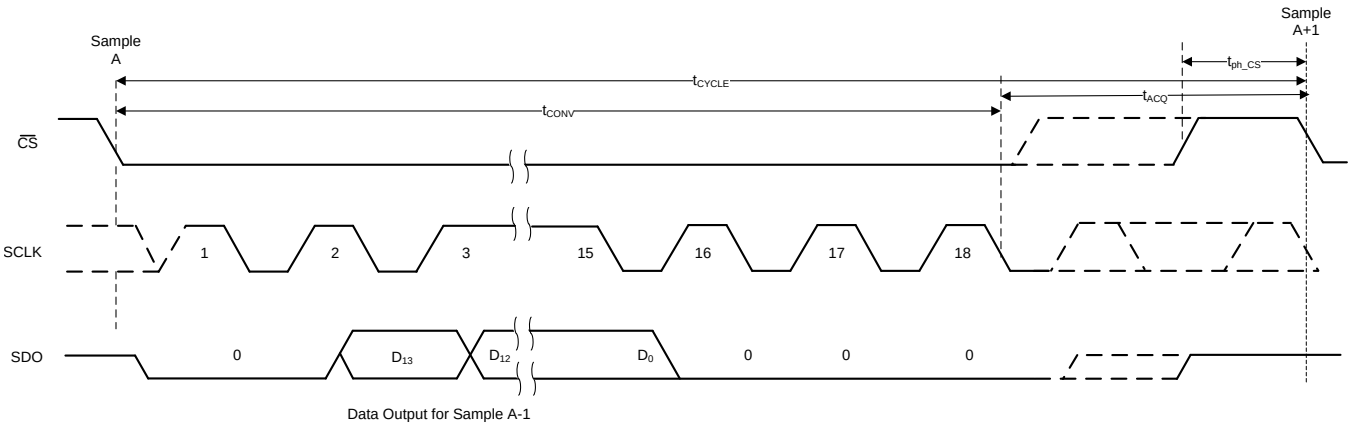


Figure 1. Serial Transfer Frame

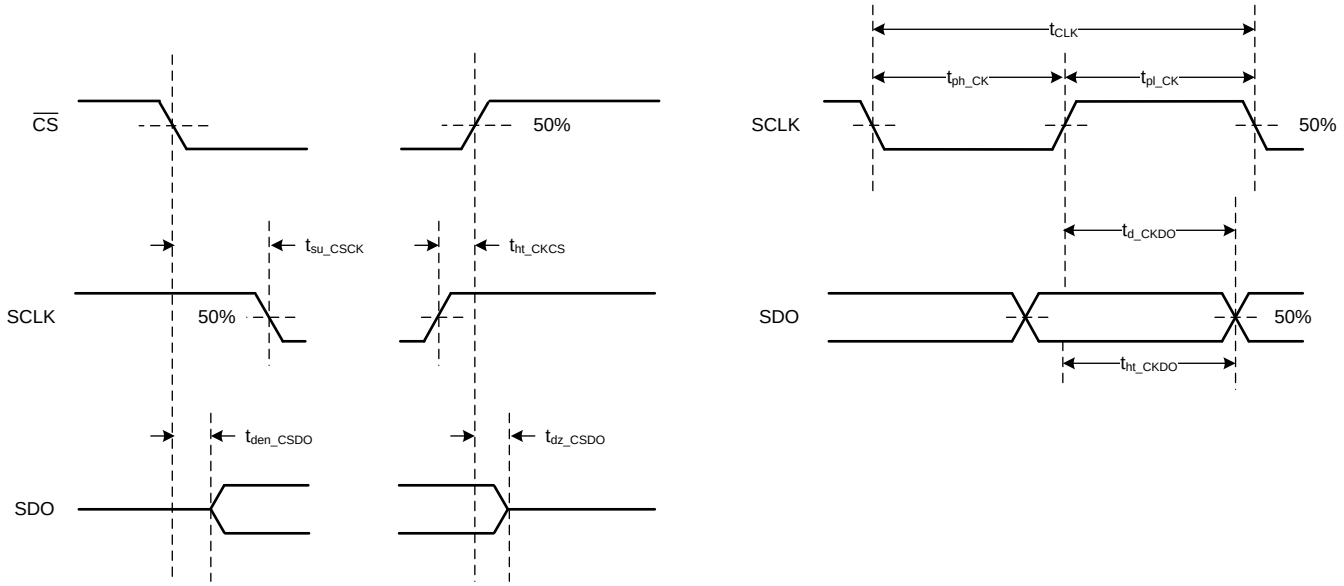
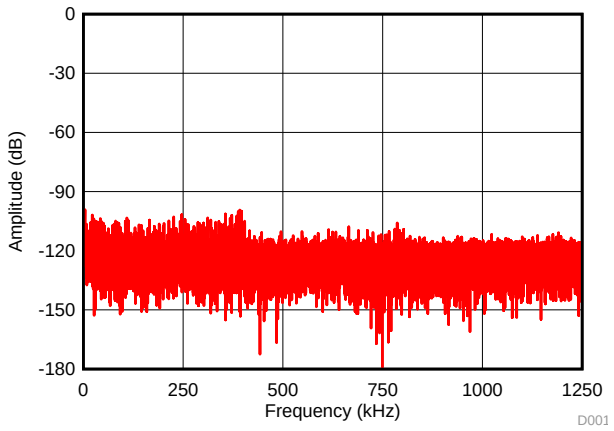


Figure 2. Timing Specifications

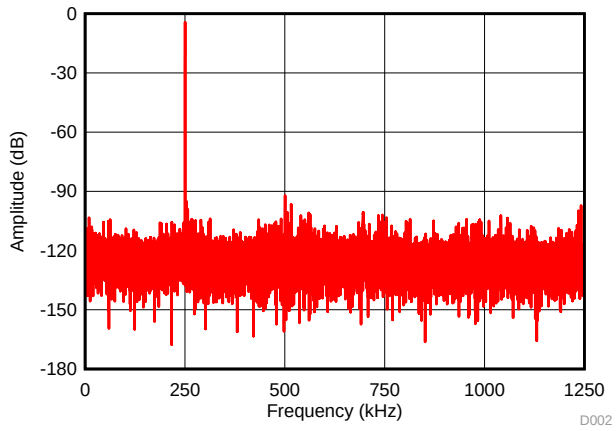
6.8 Typical Characteristics

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{Sample} = 2.5 MSPS (unless otherwise noted)



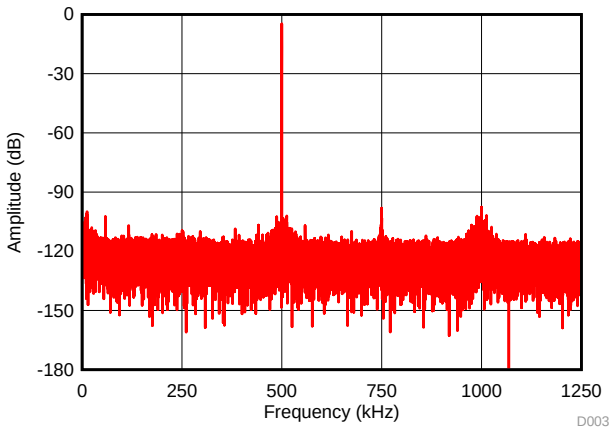
SNR = 75.2 dB, THD = –90.25 dB, ENOB = 12.18 bits

Figure 3. Typical FFT



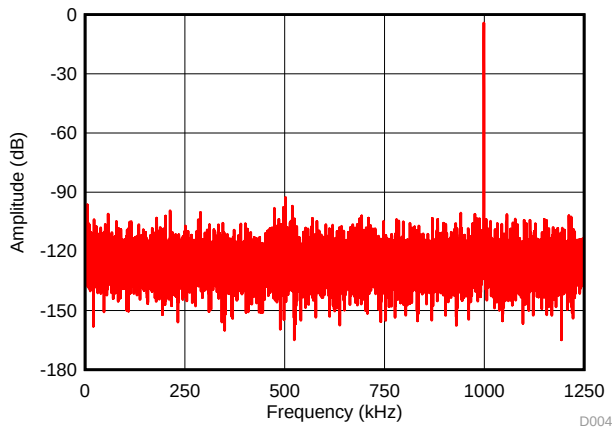
SNR = 74.3 dB, THD = –87.9 dB, f_{IN} = 250 kHz

Figure 4. Typical FFT



SNR = 74.2 dB, THD = –90.25 dB, f_{IN} = 500 kHz

Figure 5. Typical FFT



SNR = 73.9 dB, THD = –87.1 dB, f_{IN} = 1000 kHz

Figure 6. Typical FFT

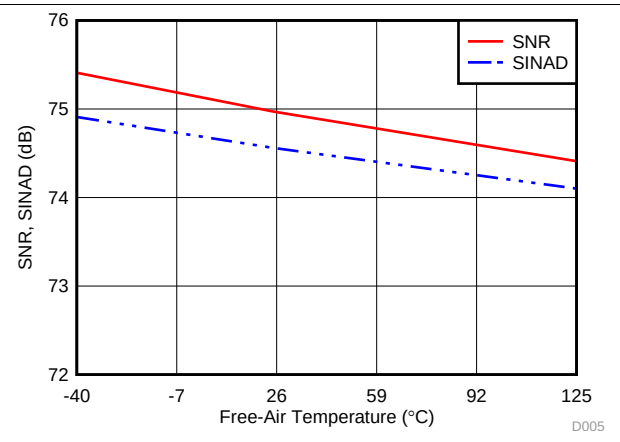


Figure 7. SNR and SINAD vs Temperature

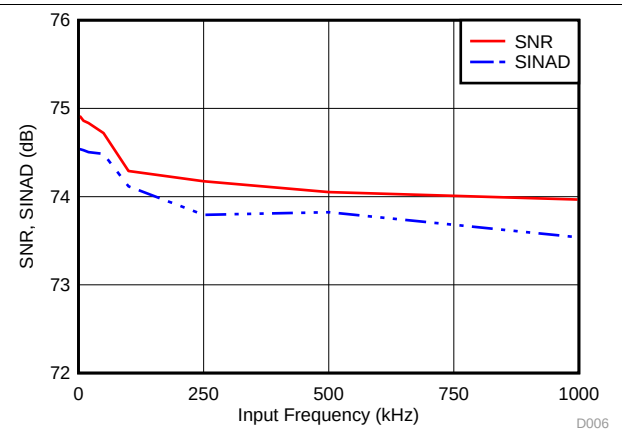


Figure 8. SNR and SINAD vs Input Frequency

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{Sample} = 2.5 MSPS (unless otherwise noted)

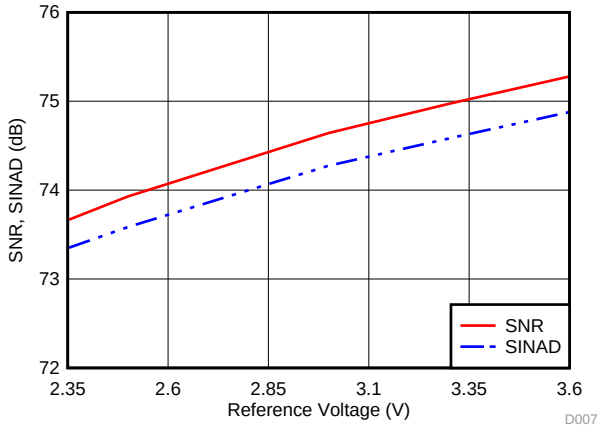


Figure 9. SNR and SINAD vs Reference Voltage (AVDD)

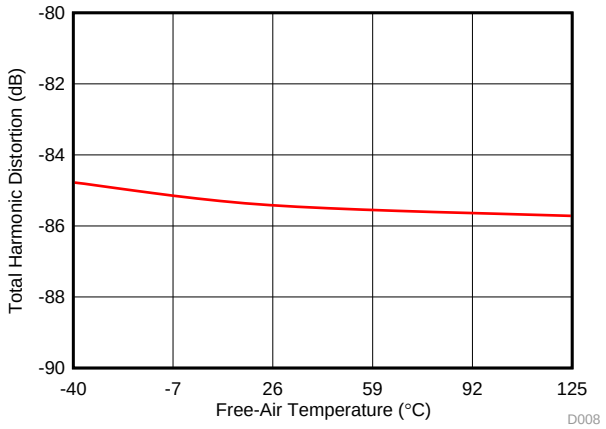


Figure 10. THD vs Temperature

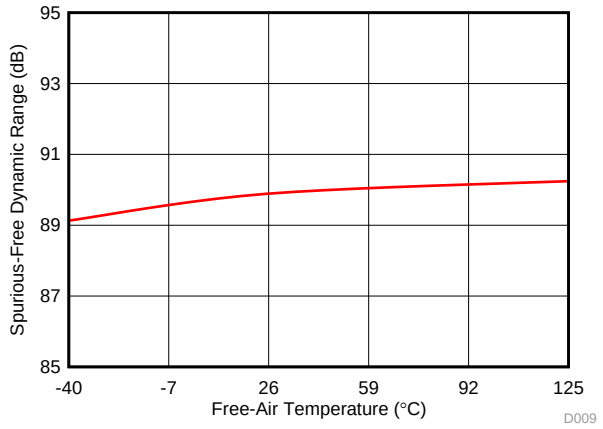


Figure 11. SFDR vs Temperature

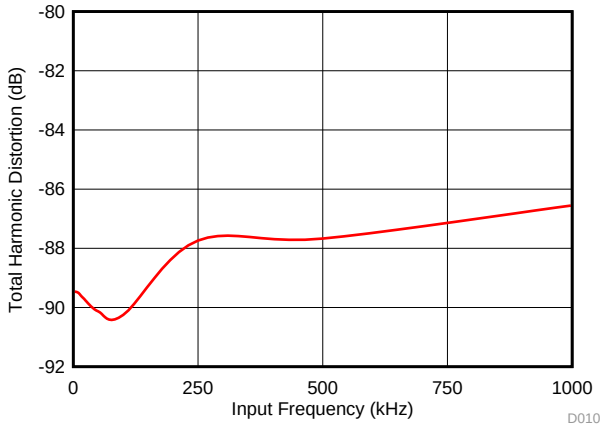


Figure 12. THD vs Input Frequency

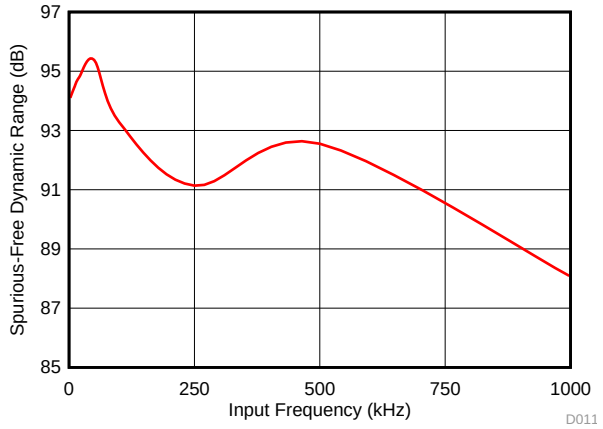


Figure 13. SFDR vs Input Frequency

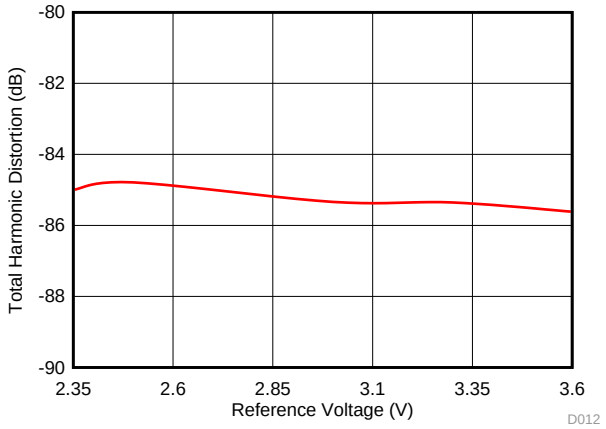


Figure 14. THD vs Reference Voltage (AVDD)

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{Sample} = 2.5 MSPS (unless otherwise noted)

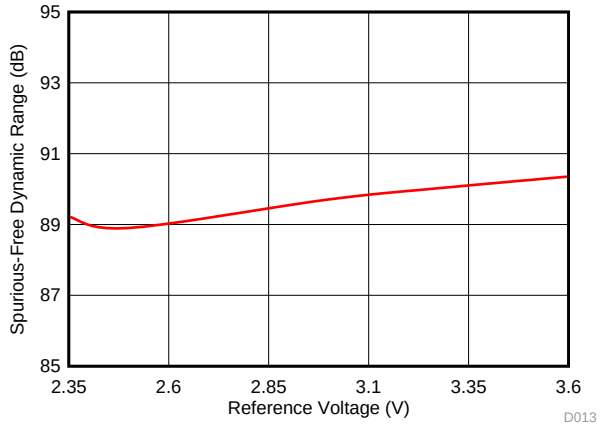
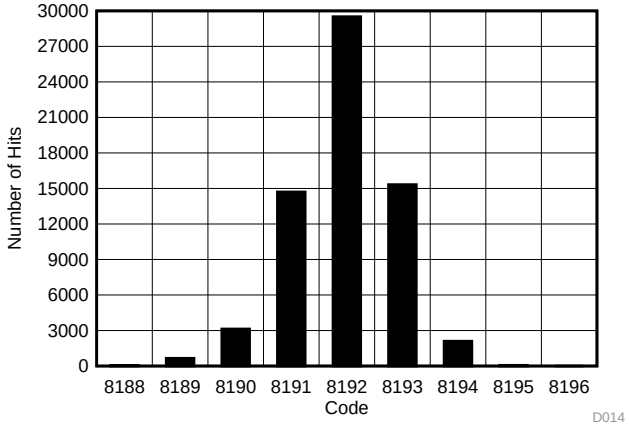


Figure 15. SFDR vs Reference Voltage (AVDD)



Standard deviation of codes = 0.94 LSB, V_{IN} = AVDD / 2

Figure 16. DC Input Histogram

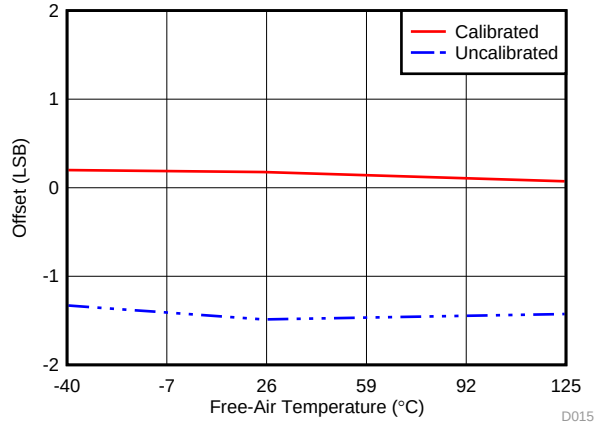


Figure 17. Offset vs Temperature

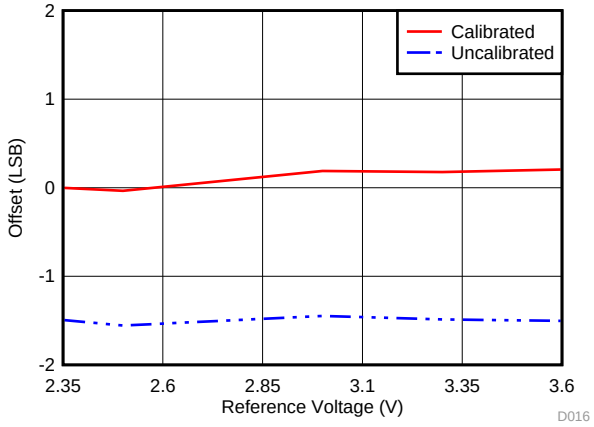


Figure 18. Offset vs Reference Voltage (AVDD)

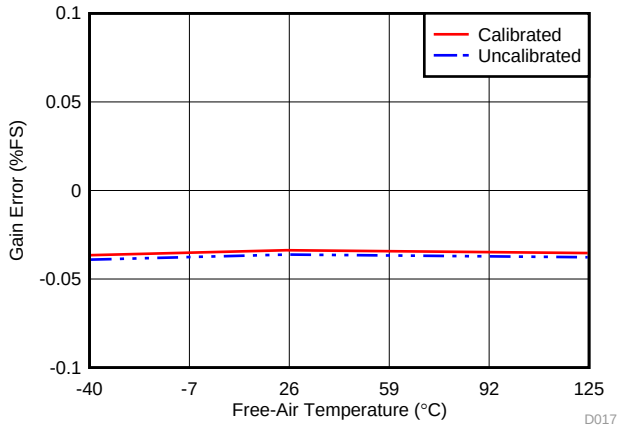


Figure 19. Gain Error vs Temperature

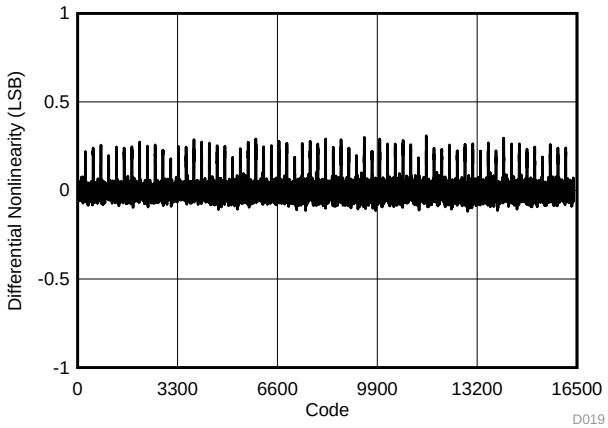


Figure 20. Typical DNL

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{Sample} = 2.5 MSPS (unless otherwise noted)

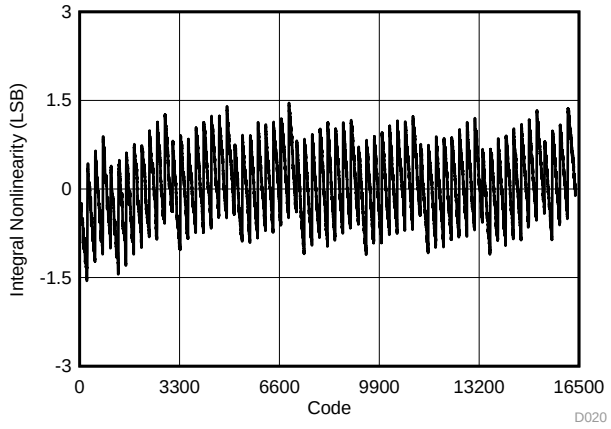


Figure 21. Typical INL

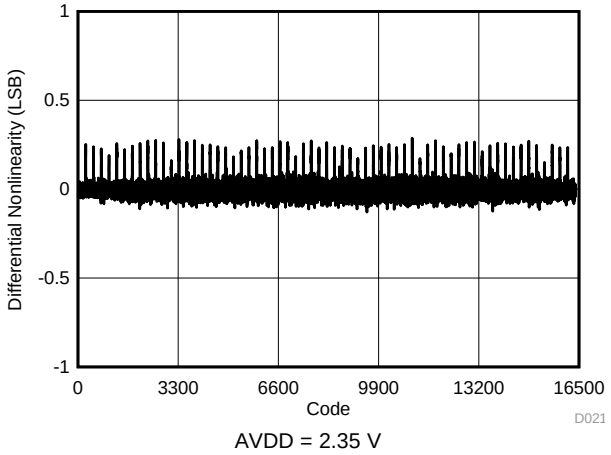


Figure 22. Typical DNL

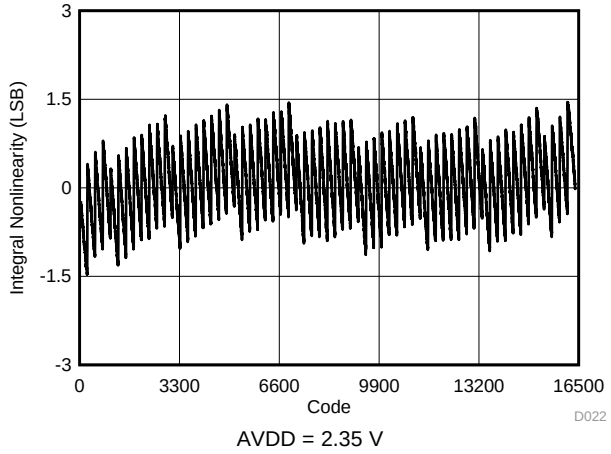


Figure 23. Typical INL

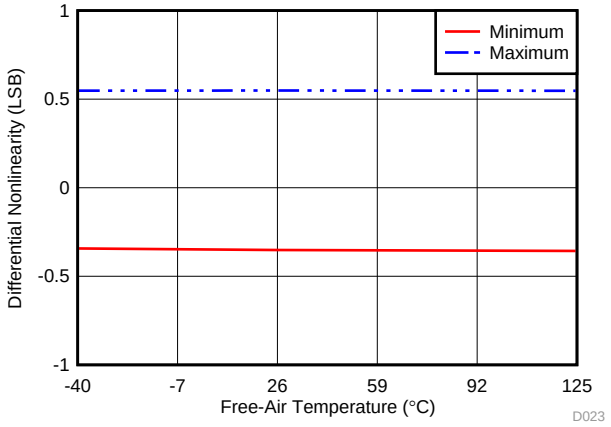


Figure 24. DNL vs Temperature

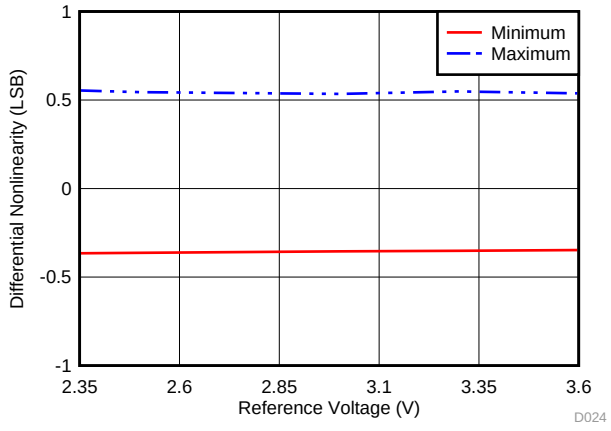


Figure 25. DNL vs Reference Voltage

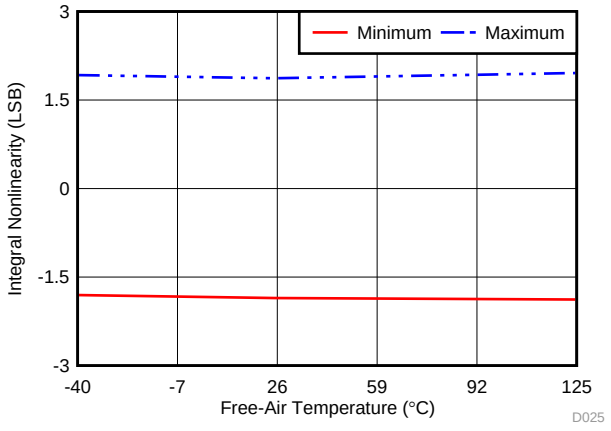


Figure 26. INL vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{Sample} = 2.5 MSPS (unless otherwise noted)

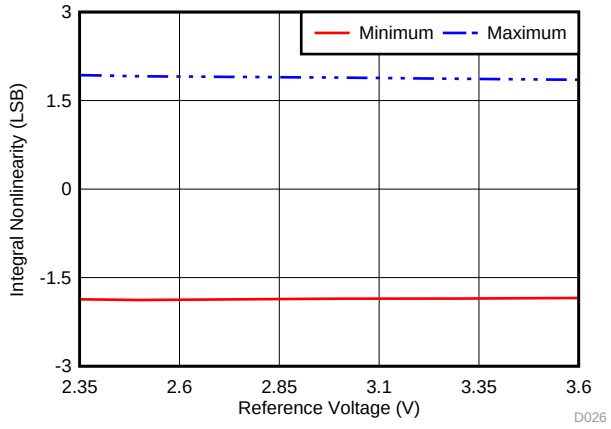


Figure 27. INL vs Reference Voltage

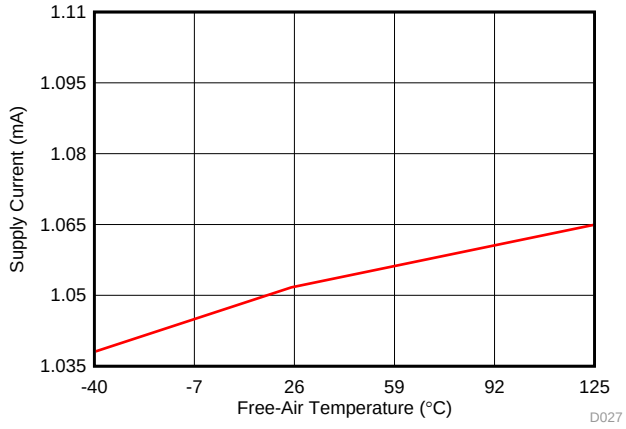


Figure 28. AVDD Current vs Temperature

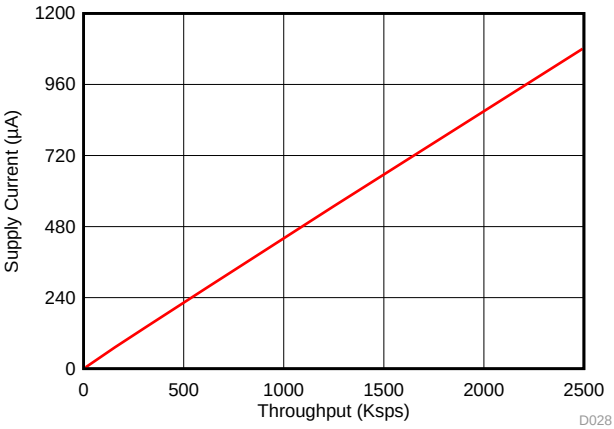


Figure 29. AVDD Current vs Throughput

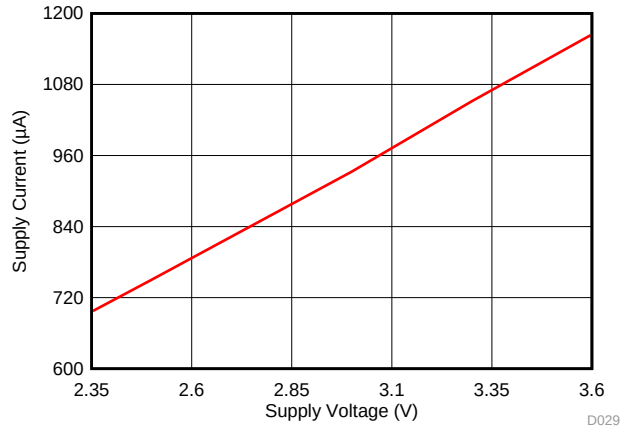


Figure 30. AVDD Current vs AVDD Voltage

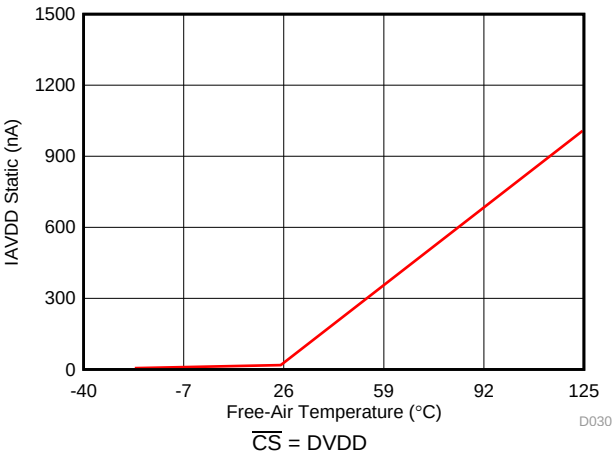


Figure 31. Static AVDD Current vs Temperature

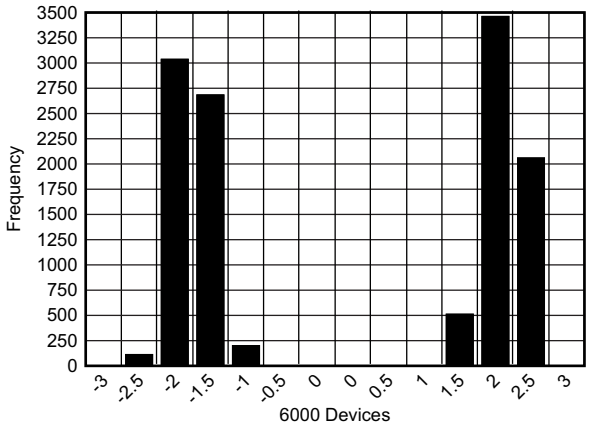


Figure 32. Typical INL Distribution

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 3.3 V, DVDD = 1.8 V, f_{IN} = 2 kHz, and f_{Sample} = 2.5 MSPS (unless otherwise noted)

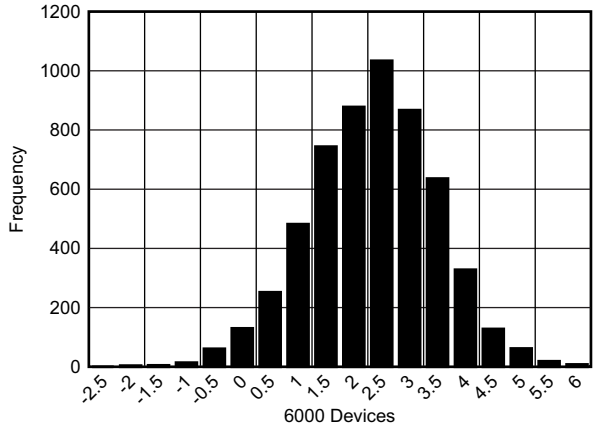


Figure 33. Typical Offset Error Distribution

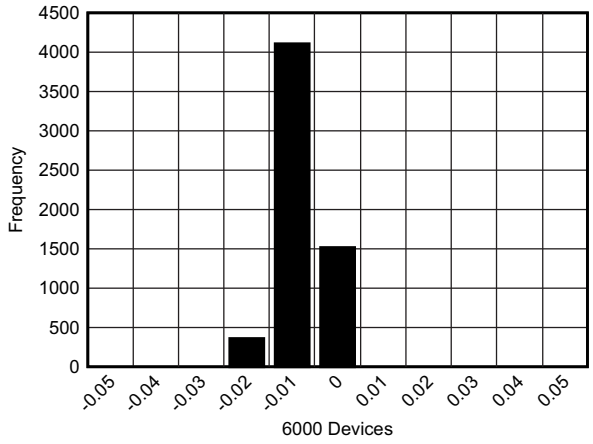


Figure 34. Typical Gain Error Distribution

7 Parameter Measurement Information

7.1 Digital Voltage Levels

The device complies with the JESD8-7A standard for DVDD from 1.65 V to 1.95 V. Figure 35 shows voltage levels for the digital input and output pins.

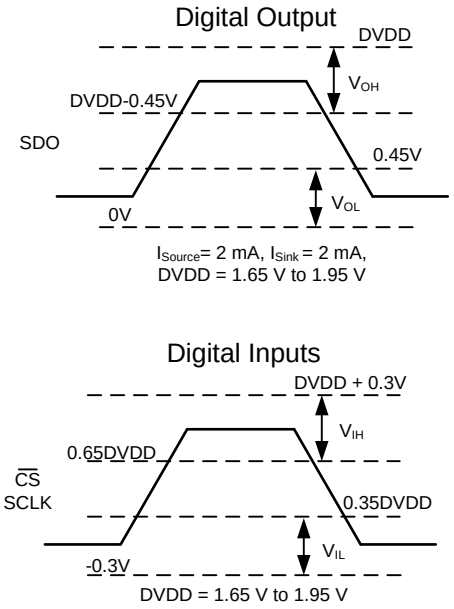


Figure 35. Digital Voltage Levels as per the JESD8-7A Standard

8 Detailed Description

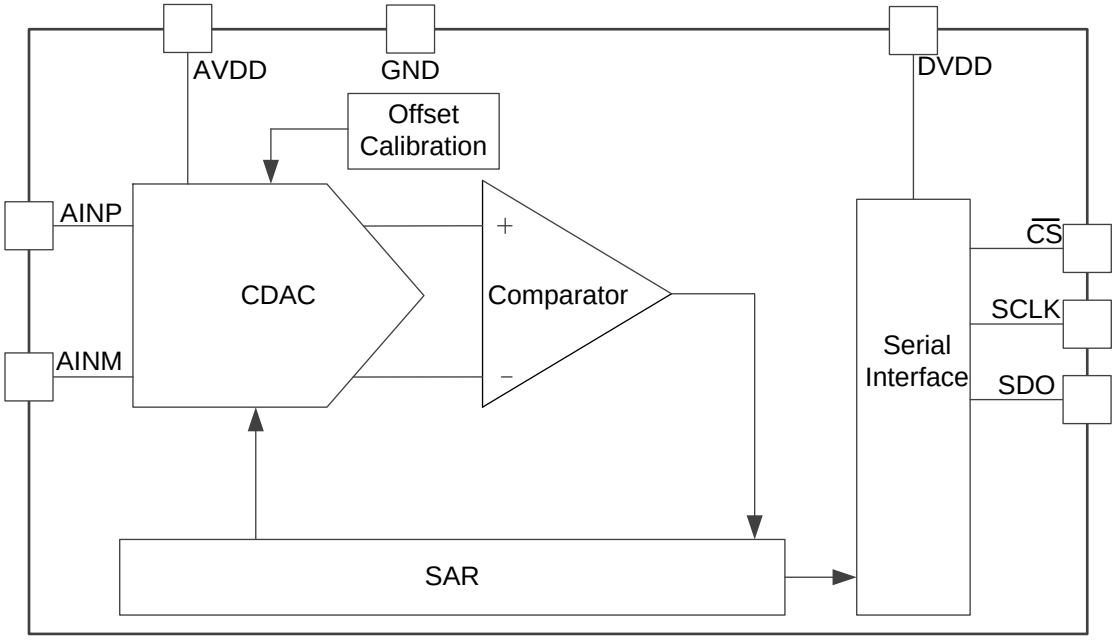
8.1 Overview

The ADS7056 is a 14-bit, 2.5-MSPS, analog-to-digital converter (ADC). The device includes a capacitor-based, successive-approximation register (SAR) ADC that supports a wide analog input voltage range (0 V to AVDD, for AVDD in the range of 2.35 V to 3.6 V). The device uses the AVDD supply voltage as the reference voltage for conversion of analog input to digital output and the AVDD supply voltage also powers the analog blocks of the device. The device has integrated offset calibration feature to calibrate its own offset; see the *OFFCAL State* section for details.

The SPI-compatible serial interface is controlled by the $\overline{CS}$ and SCLK signals. The input signal is sampled with the $\overline{CS}$ falling edge and SCLK is used for conversion and serial data output. The device supports a wide digital supply range (1.65 V to 3.6 V), enabling direct interface to a variety of host controllers. The ADS7056 complies with the JESD8-7A standard for a normal DVDD range (1.65 V to 1.95 V); see the *Digital Voltage Levels* section for details.

The ADS7056 is available in 8-pin, miniature, X2QFN package and is specified over extended industrial temperature range (–40°C to 125°C). Miniature form-factor and extremely low-power consumption make this device suitable for space-constrained, battery-powered applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The device supports a unipolar, single-ended analog input signal. Figure 36 shows a small-signal equivalent circuit of the sample-and-hold circuit. The sampling switch is represented by a resistance (R_{S1} and R_{S2}, typically 50 Ω) in series with an ideal switch (SW_1 and SW_2). The sampling capacitors, C_{S1} and C_{S2}, are typically 16 pF.

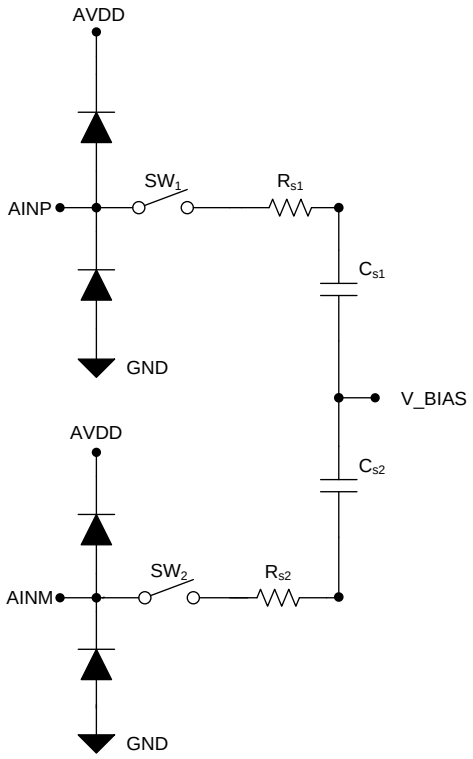


Figure 36. Equivalent Input Circuit for the Sampling Stage

During the acquisition process, both positive and negative inputs are individually sampled on C_{S1} and C_{S2}, respectively. During the conversion process, the device converts for the voltage difference between the two sampled values: $V_{AINP} – V_{AINM}$.

Each analog input pin has electrostatic discharge (ESD) protection diodes to AVDD and GND. Keep the analog inputs within the specified range to avoid turning the diodes on.

The full-scale analog input range (FSR) is 0 V to AVDD and the absolute input range on the AINM and AINP pins is –0.1 V to AVDD + 0.1 V.

Feature Description (continued)

8.3.2 Reference

The device uses the analog supply voltage (AVDD) as the reference voltage for the analog-to-digital conversion. During the conversion process, the internal capacitors are switched to the AVDD pin as per the successive approximation algorithm. As shown in Figure 37, a 3.3-µF (C_{AVDD}), low equivalent series resistance (ESR) ceramic capacitor is recommended to be placed between the AVDD and GND pins. The decoupling capacitor provides the instantaneous charge required by the internal circuit during the conversion process and maintains a stable dc voltage on the AVDD pin.

See the *Power Supply Recommendations* and *Layout Example* sections for component recommendations and layout guidelines.

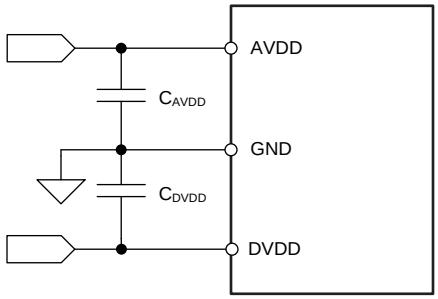


Figure 37. Reference for the Device

Feature Description (continued)

8.3.3 ADC Transfer Function

The device supports a unipolar, single-ended analog input signal. The output is in straight binary format. Figure 38 and Table 1 show the ideal transfer characteristics for the device.

The least significant bit for the device is given by:

$$1\ LSB = V_{REF} / 2^N \quad (1)$$

where:

- V_{REF} = Voltage applied between the AVDD and GND pins and
- N = 14

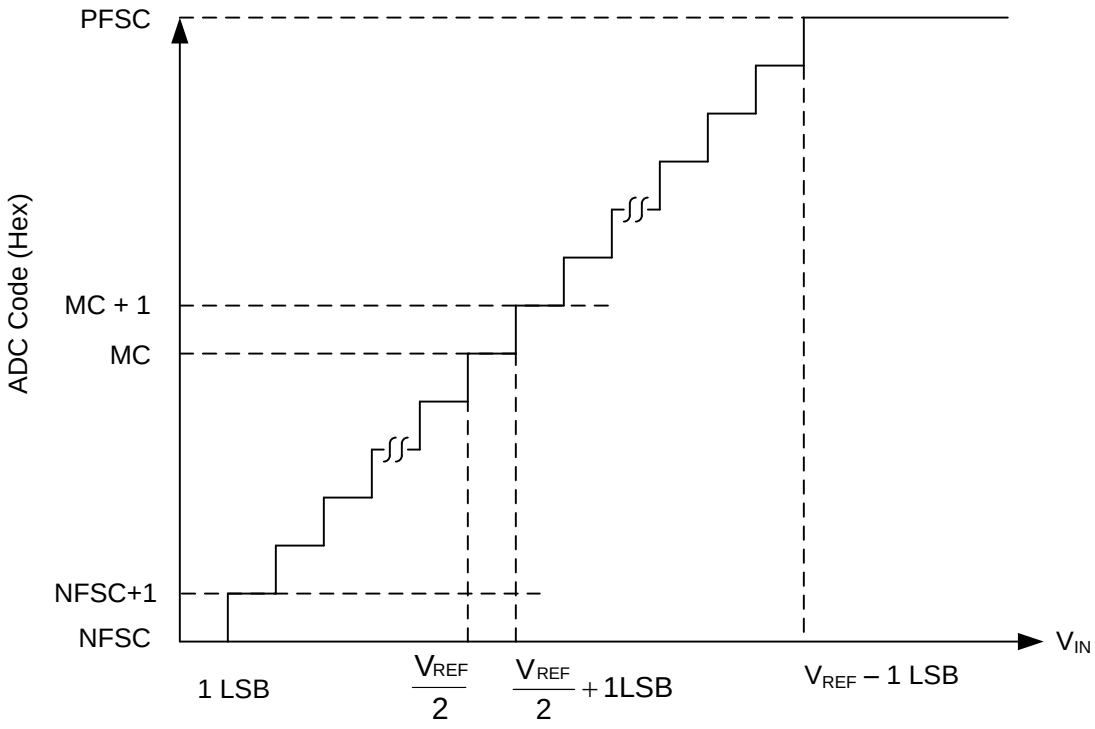


Figure 38. Ideal Transfer Characteristics

Table 1. Transfer Characteristics

INPUT VOLTAGE (AINP – AINM)	CODE	DESCRIPTION	IDEAL OUTPUT CODE (Hex)
≤ 1 LSB	NFSC	Negative full-scale code	0000
1 LSB to 2 LSBs	NFSC + 1	—	0001
V_{REF} / 2 to V_{REF} / 2 + 1 LSB	MC	Mid code	1FFF
V_{REF} / 2 + 1 LSB to V_{REF} / 2 + 2 LSBs	MC + 1	—	2000
≥ V_{REF} – 1 LSB	PFSC	Positive full-scale code	3FFF

8.4 Device Functional Modes

The device supports a simple, SPI-compatible interface to the external host. On power-up, the device is in ACQ state. The $\overline{CS}$ signal defines one conversion and serial data transfer frame. A frame starts with a $\overline{CS}$ falling edge and ends with a $\overline{CS}$ rising edge. The SDO pin is tri-stated when $\overline{CS}$ is high. With $\overline{CS}$ low, the clock provided on the SCLK pin is used for conversion and data transfer and the output data are available on the SDO pin.

As shown in Figure 39, the device supports three functional states: acquisition (ACQ), conversion (CNV), and offset calibration (OFFCAL). The device status depends on the $\overline{CS}$ and SCLK signals provided by the host controller.

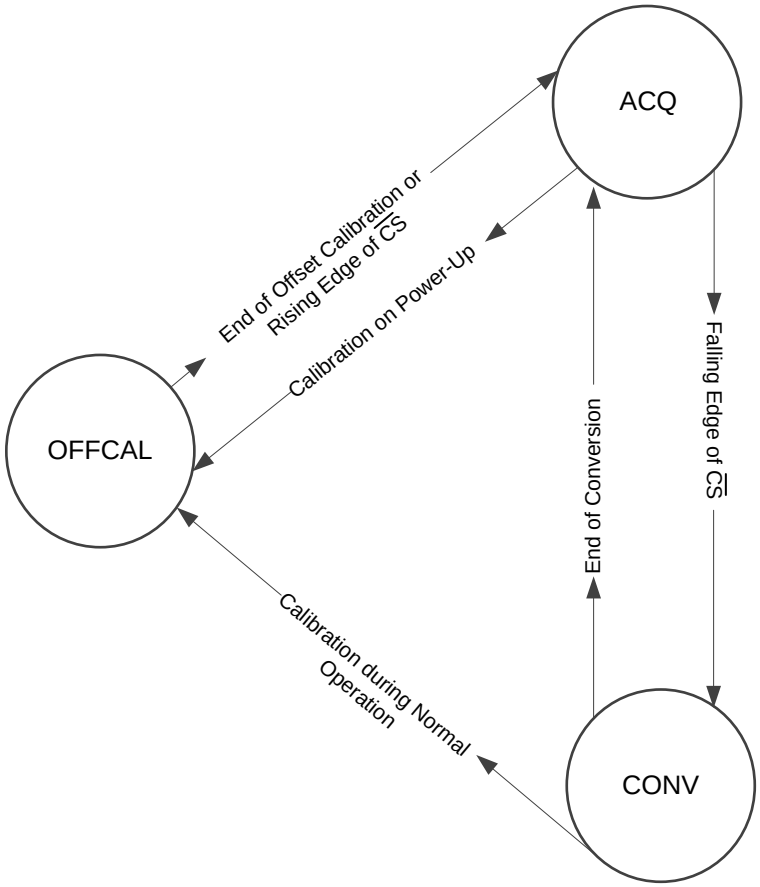


Figure 39. Functional State Diagram

8.4.1 ACQ State

In ACQ state, switches SW_1 and SW_2 connected to the analog input pins close and the device acquires the analog input signal on C_{S1} and C_{S2}. The device enters ACQ state at power-up, at the end of every conversion, and after completing the offset calibration. A $\overline{CS}$ falling edge takes the device from ACQ state to CNV state.

The device consumes extremely low power from the AVDD and DVDD power supplies when in ACQ state.

Device Functional Modes (continued)

8.4.2 CNV State

In the CNV state, the device uses the external clock to convert the sampled analog input signal to an equivalent digital code as per the transfer function illustrated in Figure 38. The conversion process requires a minimum of 18 SCLK falling edges to be provided within the frame. After the end of conversion process, the device automatically moves from CNV state to ACQ state. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided.

Figure 40 shows a detailed timing diagram for the serial interface. In the first serial transfer frame after power-up, the device provides the first data as all zeros. In any frame, the clocks provided on the SCLK pin are also used to transfer the output data for the previous conversion. A leading 0 is output on the SDO pin on the $\overline{CS}$ falling edge. The most significant bit (MSB) of the output data is launched on the SDO pin on the rising edge after the first SCLK falling edge. Subsequent output bits are launched on the subsequent rising edges provided on SCLK. When all 14 output bits are shifted out, the device outputs 0's on the subsequent SCLK rising edges. The device enters ACQ state after 18 clocks and a minimum time of t_{ACQ} must be provided for acquiring the next sample. If the device is provided with less than 18 SCLK falling edges in the present serial transfer frame, the device provides an invalid conversion result in the next serial transfer frame.

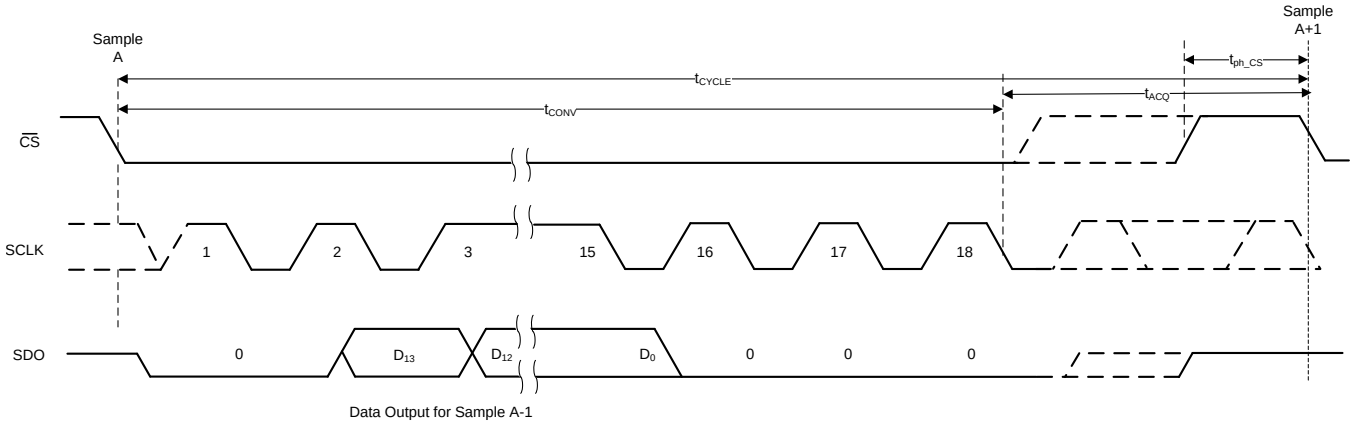


Figure 40. Serial Interface Timing Diagram

8.4.3 OFFCAL State

In OFFCAL state, the device calibrates and corrects for its internal offset errors. In OFFCAL state, the sampling capacitors are disconnected from the analog input pins (AINP and AINM). The offset calibration is effective for all subsequent conversions until the device is powered off. An offset calibration cycle is recommended at power-up and whenever there is a significant change in the operating conditions for the device (such as in the AVDD voltage and operating temperature).

The host controller must provide a serial transfer frame as described in Figure 41 or in Figure 42 to enter OFFCAL state.

Device Functional Modes (continued)

8.4.3.1 Offset Calibration on Power-Up

On power-up, the host must provide 24 SCLKs in the first serial transfer to enter the OFFCAL state. The device provides 0's on SDO during offset calibration. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided. If the host controller enters the OFFCAL state, but pulls the $\overline{CS}$ pin high before providing 24 SCLKs, then the offset calibration process is aborted and the device enters the ACQ state. Figure 41 and Table 2 provide the timing for offset calibration on power-up.

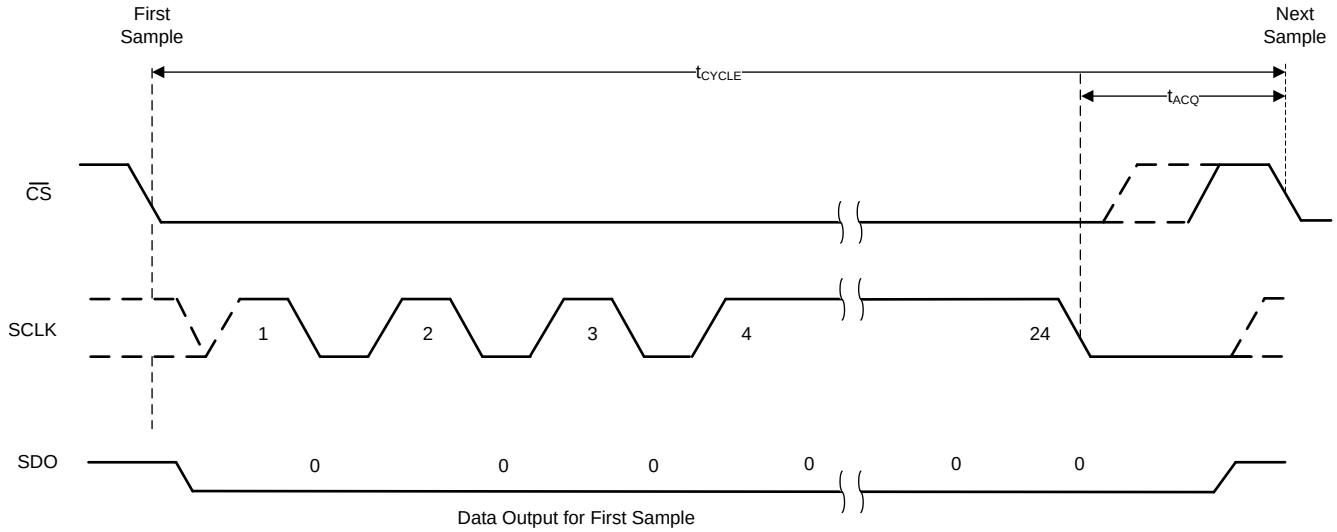


Figure 41. Timing for Offset Calibration on Power-Up

Table 2. Timing Specifications for Offset Calibration on Power-Up(1)

		MIN	TYP	MAX	UNIT
t_{cycle}	Cycle time for offset calibration on power-up	24 × t_{CLK} + t_{ACQ}			ns
t_{ACQ}	Acquisition time	95			ns
f_{SCLK}	Frequency of SCLK			60	MHz

(1) In addition to the timing specifications of Figure 41 and Table 2, the timing specifications described in Figure 2 and the *Timing Requirements* table are also applicable for offset calibration on power-up.

8.4.3.2 Offset Calibration During Normal Operation

During normal operation, the host must provide 64 SCLKs in the serial transfer frame to enter the OFFCAL state. The device provides the conversion result for the previous sample during the first 18 SCLKs and 0's on SDO for the rest of the SCLKs in the serial transfer frame. For acquisition of the next sample, a minimum time of t_{ACQ} must be provided. If the host controller enters the OFFCAL state, but pulls the $\overline{CS}$ high before providing 64 SCLKs, then the offset calibration process is aborted and the device enters ACQ state. Figure 42 and Table 3 provide the timing for offset calibration during normal operation.

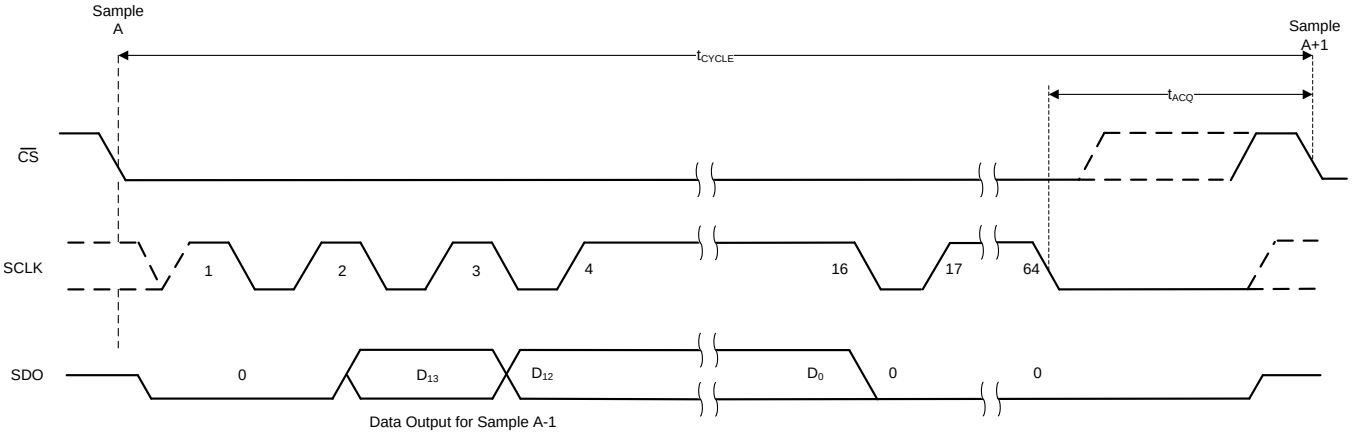


Figure 42. Timing for Offset Calibration During Normal Operation

Table 3. Timing Specifications for Offset Calibration During Normal Operation(1)

		MIN	TYP	MAX	UNIT
t_{cycle}	Cycle time for offset calibration on power-up	64 × t_{CLK} + t_{ACQ}			ns
t_{ACQ}	Acquisition time	95			ns
f_{SCLK}	Frequency of SCLK			60	MHz

(1) In addition to the timing specifications of Figure 42 and Table 3, the timing specifications described in Figure 2 and the *Timing Requirements* table are also applicable for offset calibration during normal operation.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR) analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section details some general principles for designing the input driver circuit, reference driver circuit, and provides typical application circuits designed for the device.

9.2 Typical Applications

9.2.1 Single-Supply Data Acquisition With the ADS7056

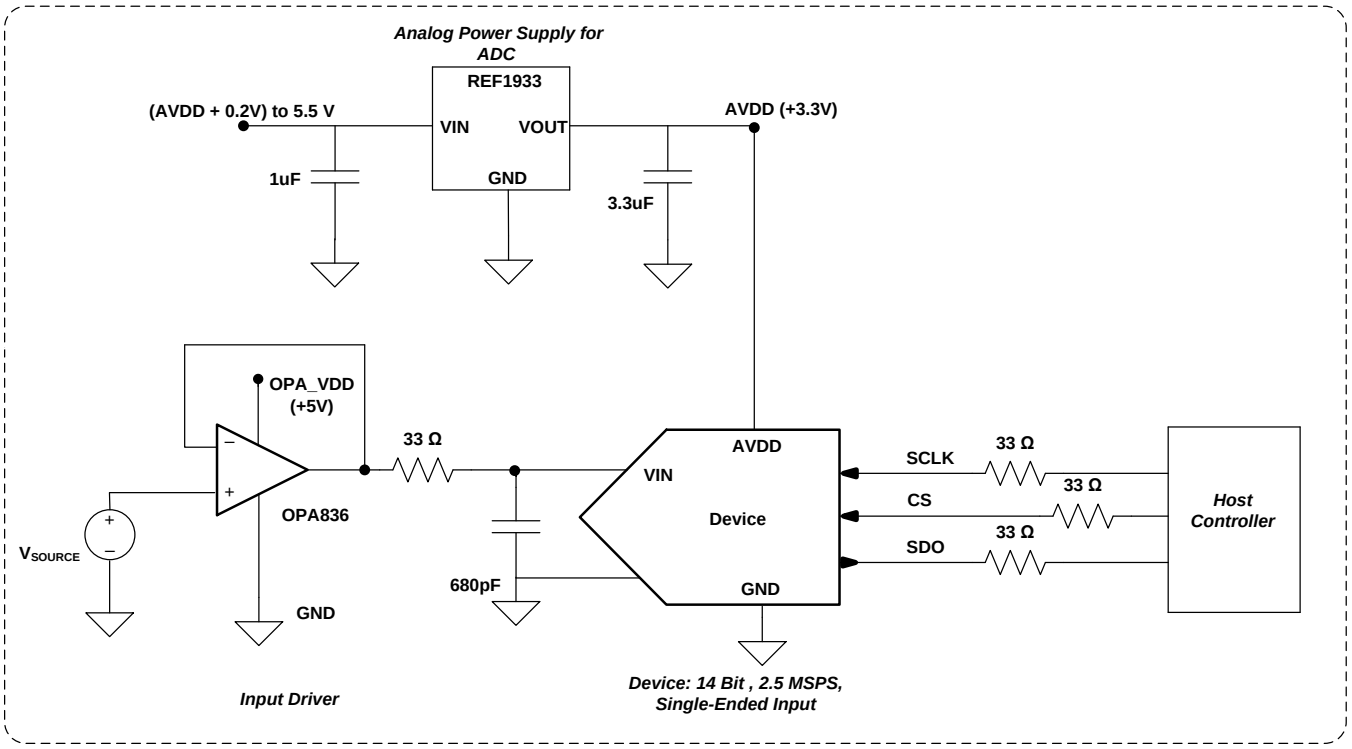


Figure 43. DAQ Circuit: Single-Supply DAQ

9.2.1.1 Design Requirements

The goal of the circuit shown in Figure 43 is to design a single-supply data acquisition (DAQ) circuit based on the ADS7056 with SNR greater than 74 dB and THD less than –85 dB for input frequencies of 2 kHz to 100 kHz at a throughput of 2.5 MSPS for applications such as sonar receivers and ultrasonic flow meters.

9.2.1.2 Detailed Design Procedure

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and charge kickback filter. Careful design of the front-end circuit is critical to meet the linearity and noise performance of a high-precision ADC.

Typical Applications (continued)

9.2.1.2.1 Low Distortion Charge Kickback Filter Design

Figure 44 shows the input circuit of a typical SAR ADC. During the acquisition phase, the SW switch closes and connects the sampling capacitor (C_{SH}) to the input driver circuit. This action introduces a transient on the input pins of the SAR ADC. An ideal amplifier with 0 Ω of output impedance and infinite current drive can settle this transient in zero time. For a real amplifier with non-zero output impedance and finite drive strength, this switched capacitor load can create stability issues.

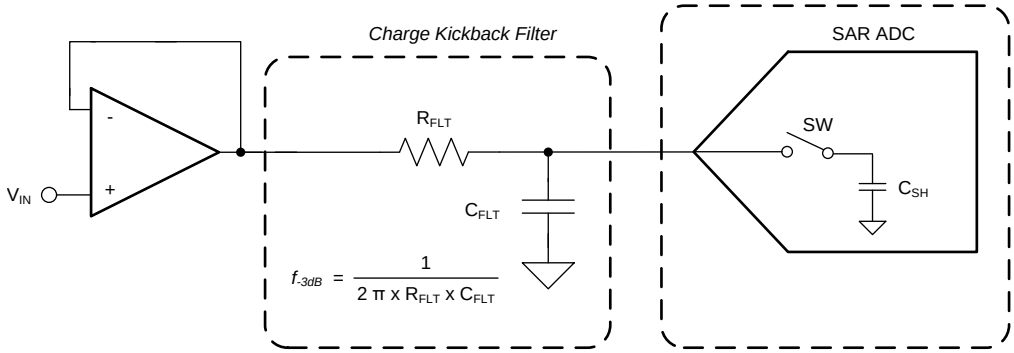


Figure 44. Input Sample-and-Hold Circuit for a Typical SAR ADC

For ac signals, the filter bandwidth must be kept low to band-limit the noise fed into the ADC input, thereby increasing the signal-to-noise ratio (SNR) of the system. Besides filtering the noise from the front-end drive circuitry, the RC filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected across the ADC inputs. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor is at least 20 times the specified value of the ADC sampling capacitance. For this device, the input sampling capacitance is equal to 16 pF. Thus, the value of C_{FLT} is greater than 320 pF. Select a COG- or NPO-type capacitor because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

Driving capacitive loads can degrade the phase margin of the input amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design.

Typical Applications (continued)

9.2.1.2.2 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type as well as the performance goals of the data acquisition system. Some key amplifier specifications to consider when selecting an appropriate amplifier to drive the inputs of the ADC are:

- Small-signal bandwidth: select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the low cutoff frequency RC filter (see the *Low Distortion Charge Kickback Filter Design* section for details.) at the inputs of the ADC. Higher bandwidth also minimizes the harmonic distortion at higher input frequencies. Select the amplifier with the unity-gain bandwidth (UGB) as described in Equation 2 to maintain the overall stability of the input driver circuit.

$$UGB \geq 4 \times \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \quad (2)$$

  where:

  - UGB = unity-gain bandwidth

- Noise: noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. Generally, to ensure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit must be kept below 20% of the input-referred noise of the ADC. As Equation 3 explains, noise from the input driver circuit is band limited by designing a low cutoff frequency RC filter.

$$N_G \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6}\right)^2 + e^2_{n\_RMS} \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{2\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \quad (3)$$

  where:

  - V_{1/f_AMP_PP} is the peak-to-peak flicker noise in µVRMS
  - e_{n_RMS} is the amplifier broadband noise
  - f_{-3dB} is the –3-dB bandwidth of the RC filter and
  - N_G is the noise gain of the front-end circuit, which is equal to 1 in the buffer configuration

- Distortion: both the ADC and the input driver introduce distortion in a data acquisition block. To ensure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10 dB lower than the distortion of the ADC.

For the application circuit of Figure 43, the OPA836 is selected for its high bandwidth (205 MHz), low noise (4.6 nV/√Hz), high output drive capacity (45 mA), and fast settling response (22 ns for 0.1% settling).

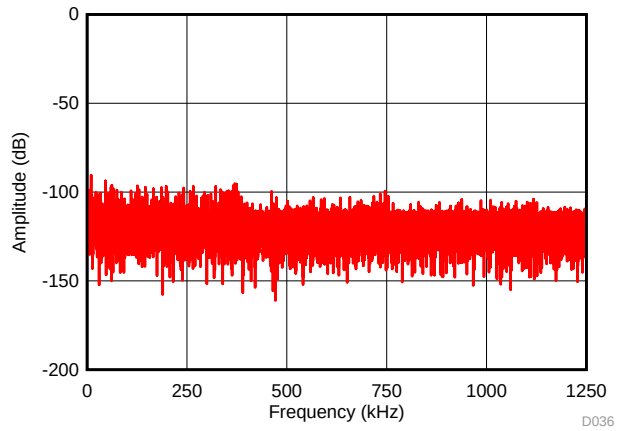
9.2.1.2.3 Reference Circuit

The analog supply voltage of the device is also used as a voltage reference for conversion. Decouple the AVDD pin with a 3.3-µF, low-ESR ceramic capacitor.

Typical Applications (continued)

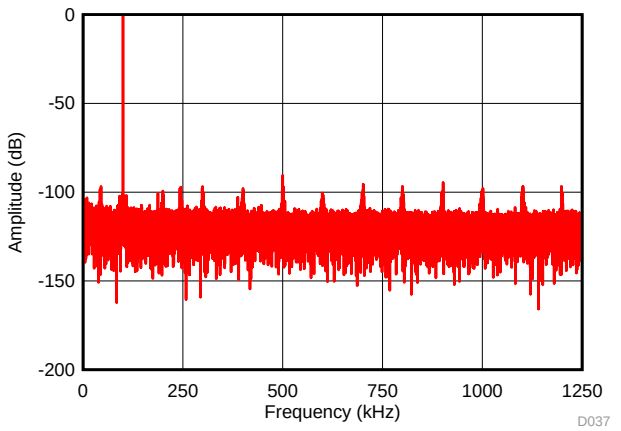
9.2.1.3 Application Curves

Figure 45 and Figure 46 provide the measurement results for the circuit described in Figure 43.



SNR = 75.8 dB, THD = –90.1 dB, SINAD = 75 dB

Figure 45. Test Results for the ADS7056 and OPA836 for a 2-kHz Input



SNR = 75 dB, THD = –88.7 dB, SINAD = 74.3 dB

Figure 46. Test Results for the ADS7056 and OPA836 for a 100-kHz Input

9.2.2 High Bandwidth (1 MHz) Data Acquisition With the ADS7056

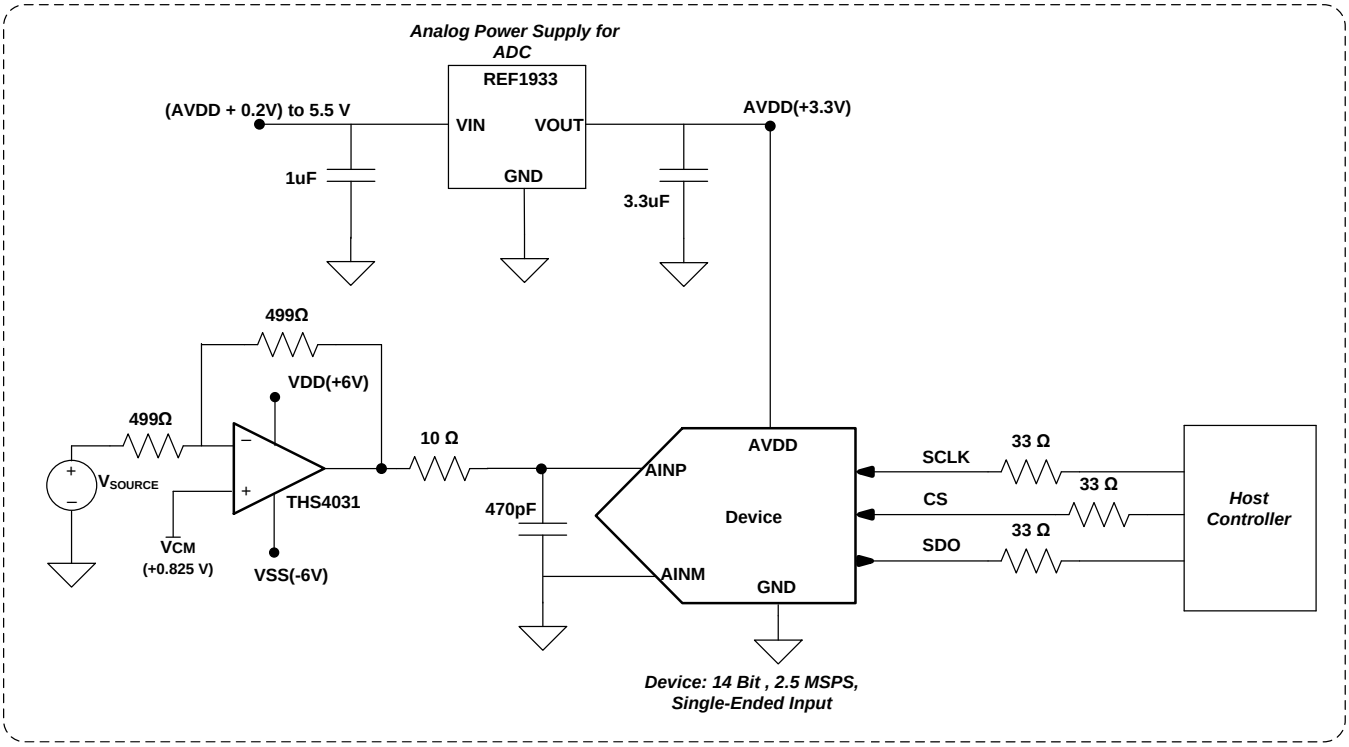


Figure 47. High Bandwidth DAQ Circuit

Typical Applications (continued)

9.2.2.1 Design Requirements

Applications such as ultrasonic flow meters, global positioning systems (GPS), handheld radios, and motor controls need analog-to-digital converters that are interfaced to high-frequency sensors (200 kHz to 1 MHz). The goal of the circuit described in Figure 47 is to design a single-supply digital acquisition (DAQ) circuit based on the ADS7056 with SNR greater than 73 dB and THD less than –85 dB for input frequencies of 200 kHz to 1 MHz at a throughput of 2.5 MSPS.

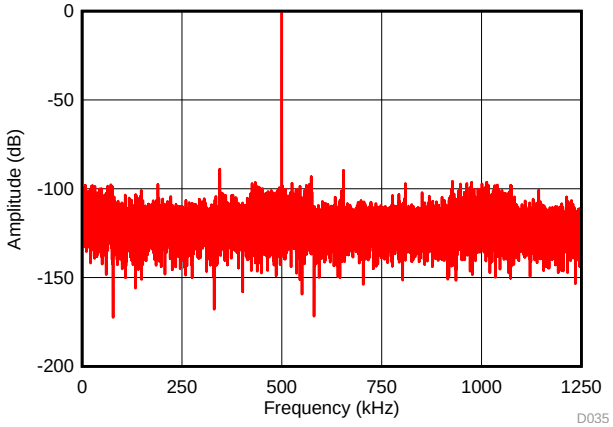
9.2.2.2 Detailed Design Procedure

To achieve a SINAD greater than 73 dB, the operational amplifier must have high bandwidth in order to settle the input signal within the acquisition time of the ADC. The operational amplifier must have low noise to keep the total system noise below 20% of the input-referred noise of the ADC. For the application circuit shown in Figure 47, the THS4031 is selected for its high bandwidth (275 MHz), low total harmonic distortion of –90 dB at 1 MHz, and ultra-low noise of 1.6 nV/√Hz. The THS4031 is powered up from dual power supply (VDD = 6 V and VSS = –6 V).

For chip-select signals, high-frequency system SNR performance is highly dependent on jitter. Thus, selecting a clock source with very low jitter (< 20-ps RMS) is recommended.

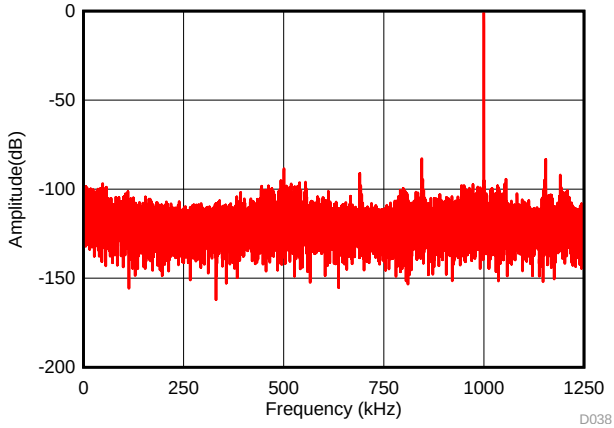
9.2.2.3 Application Curves

Figure 48 shows the FFT plot for the ADS7056 with a 500-kHz input frequency used for the circuit in Figure 47. Figure 49 shows the FFT plot for the ADS7056 with a 1000-kHz input frequency used for the circuit in Figure 47.



SNR = 74.2 dB, THD = –90.4 dB, SINAD = 73.5 dB

Figure 48. Test Results for the ADS7056 and THS4031 for a 500-kHz Input



SNR = 73.5 dB, THD = –87.8 dB, SINAD = 73 dB

Figure 49. Test Results for the ADS7056 and THS4031 for a 1000-kHz Input

Typical Applications (continued)

9.2.3 14-Bit, 10-kSPS DAQ Circuit Optimized for DC Sensor Measurements

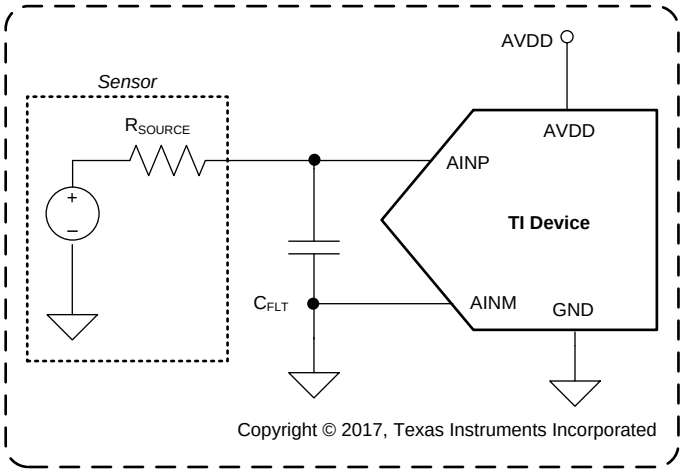


Figure 50. Interfacing the Device Directly With Sensors

In applications such as environmental sensors, gas detectors, and smoke or fire detectors where the input is very slow moving and the sensor can be connected directly to the device operating at a lower throughput rate, a DAQ circuit can be designed without the input driver for the ADC. This type of a use case is of particular interest for applications in which the primary goal is to achieve the absolute lowest power, size, and cost. Typical applications that fall into this category are low-power sensor applications (such as temperature, pressure, humidity, gas, and chemical).

9.2.3.1 Design Requirements

For this design example, use the parameters listed in Table 4 as the input parameters.

Table 4. Design Parameters

DESIGN PARAMETER	GOAL VALUE
Throughput	10 kSPS
SNR at 100 Hz	74 dB
THD at 100 Hz	–85 dB
SINAD at 100 Hz	73 dB
ENOB	12 bits
Power	20 µW

9.2.3.2 Detailed Design Procedure

The ADS7056 can be directly interfaced with sensors at lower throughput without the need of an amplifier buffer. The analog input source drive must be capable of driving the switched capacitor load of a SAR ADC and settling the analog input signal within the acquisition time of the SAR ADC. However, the output impedance of the sensor must be taken into account when interfacing a SAR ADC directly with sensors. Drive the analog input of the SAR ADC with a low impedance source. The input signal requires more acquisition time to settle to the desired accuracy because of the higher output impedance of the sensor. Figure 50 shows the simplified circuit for a sensor as a voltage source with output impedance (R_{source}).

The acquisition time of a SAR ADC (such as the ADS7056) can be increased by reducing throughput in the following ways:

1. Reducing the SCLK frequency to reduce the throughput, or
2. Keeping the SCLK fixed at the highest permissible value (that is, 60 MHz for the device) and increasing the $\overline{CS}$ high time.

Table 5 lists the acquisition time for the above two cases for a throughput of 10 kSPS. Clearly, case 2 provides more acquisition time for the input signal to settle.

Table 5. Acquisition Time with Different SCLK Frequencies

CASE	SCLK	t_{cycle}	CONVERSION TIME (= 18 × t_{SCLK})	ACQUISITION TIME (= t_{cycle} – t_{conv})
1	0.24 MHz	100 µs	75 µs	25 µs
2	60 MHz	100 µs	0.3 µs	99.7 µs

9.2.3.3 Application Curve

When the output impedance of the sensor increases, the time required for the input signal to settle increases and the performance of the SAR ADC starts degrading if the input signal does not settle within the acquisition time of the ADC. The performance of the SAR ADC can be improved by reducing the throughput to provide enough time for the input signal to settle. Figure 51 provides the results for ENOB achieved from the ADS7056 for case 2 at different throughputs with different input impedances at the device input.

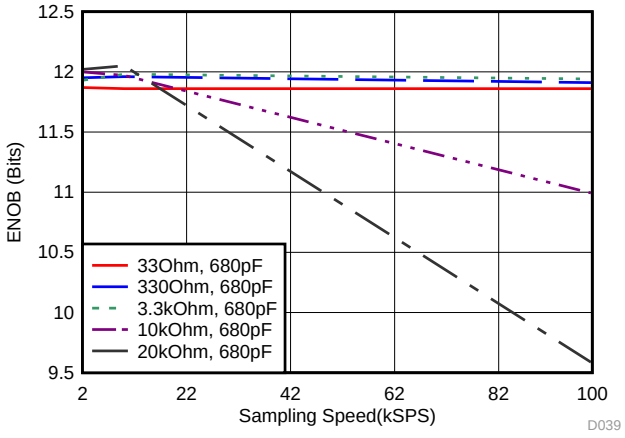


Figure 51. Effective Number of Bits (ENOB) Achieved From the ADS7056 at Different Throughputs

Table 6 shows the results and performance summary for this 14-bit, 10-kSPS DAQ circuit application.

Table 6. Results and Performance Summary for a 14-Bit, 10-kSPS DAQ Circuit for DC Sensor Measurements

DESIGN PARAMETER	GOAL VALUE	ACHIEVED RESULT
Throughput	10 kSPS	10 kSPS
SNR at 100 Hz	74 dB	75 dB
THD at 100 Hz	–85 dB	–89 dB
SINAD at 100 Hz	73 dB	74.3 dB
ENOB	12	12.05
Power	20 µW	17 µW

10 Power Supply Recommendations

10.1 AVDD and DVDD Supply Recommendations

The device has two separate power supplies: AVDD and DVDD. AVDD powers the analog blocks and is also used as the reference voltage for the analog-to-digital conversion. Always set the AVDD supply to be greater than or equal to the maximum input signal to avoid saturation of codes. Decouple the AVDD pin to the GND pin with a 3.3-µF ceramic decoupling capacitor.

DVDD is used for the interface circuits. Decouple the DVDD pin to the GND pin with a 1-µF ceramic decoupling capacitor. Figure 52 shows the decoupling recommendations.

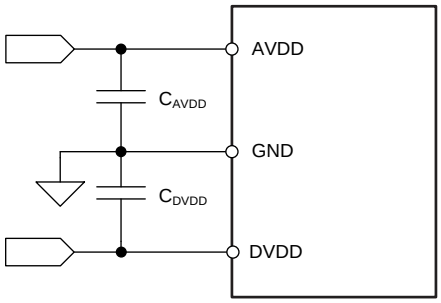


Figure 52. Power-Supply Decoupling

10.2 Optimizing Power Consumed by the Device

- Keep the analog supply voltage (AVDD) in the specified operating range and equal to the maximum analog input voltage.
- Keep the digital supply voltage (DVDD) in the specified operating range and at the lowest value supported by the host controller.
- Reduce the load capacitance on the SDO output.
- Run the device at the optimum throughput. Power consumption reduces proportionally with the throughput.

10.2.1 Estimating Digital Power Consumption

The current consumption from the DVDD supply depends on the DVDD voltage, the load capacitance on the SDO pin ($C_{LOAD\text{-}SDO}$), and the output code, and can be calculated as:

$$I_{DVDD} = C_{LOAD\text{-}SDO} \times V \times f \quad (4)$$

where:

- $C_{LOAD\text{-}SDO}$ = Load capacitance on the SDO pin
- V = DVDD supply voltage
- f = frequency of transitions on the SDO output

The number of transitions on the SDO output depends on the output code, and thus changes with the analog input. The maximum value of f occurs when data output on the SDO change on every SCLK (that is, for output codes of 2AAAh or 1555h). With an output code of 2AAAh, f = 17.5 MHz and when $C_{LOAD\text{-}SDO}$ = 20 pF and DVDD = 1.8 V, I_{DVDD}= 630 µA.

11 Layout

11.1 Layout Guidelines

Figure 53 shows a board layout example for the device. The key considerations for layout are:

- Use a solid ground plane underneath the device and partition the PCB into analog and digital sections
- Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources.
- The power sources to the device must be clean and well-bypassed. Use C_{AVDD} decoupling capacitors in close proximity to the analog (AVDD) power supply pin.
- Use a C_{DVDD} decoupling capacitor close to the digital (DVDD) power-supply pin.
- Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors.
- Connect the ground pin to the ground plane using a short, low-impedance path.
- Place the charge kickback filter components close to the device.

Among ceramic surface-mount capacitors, COG (NPO) ceramic capacitors are recommended because these components provide the most stable electrical properties over voltage, frequency, and temperature changes.

11.2 Layout Example

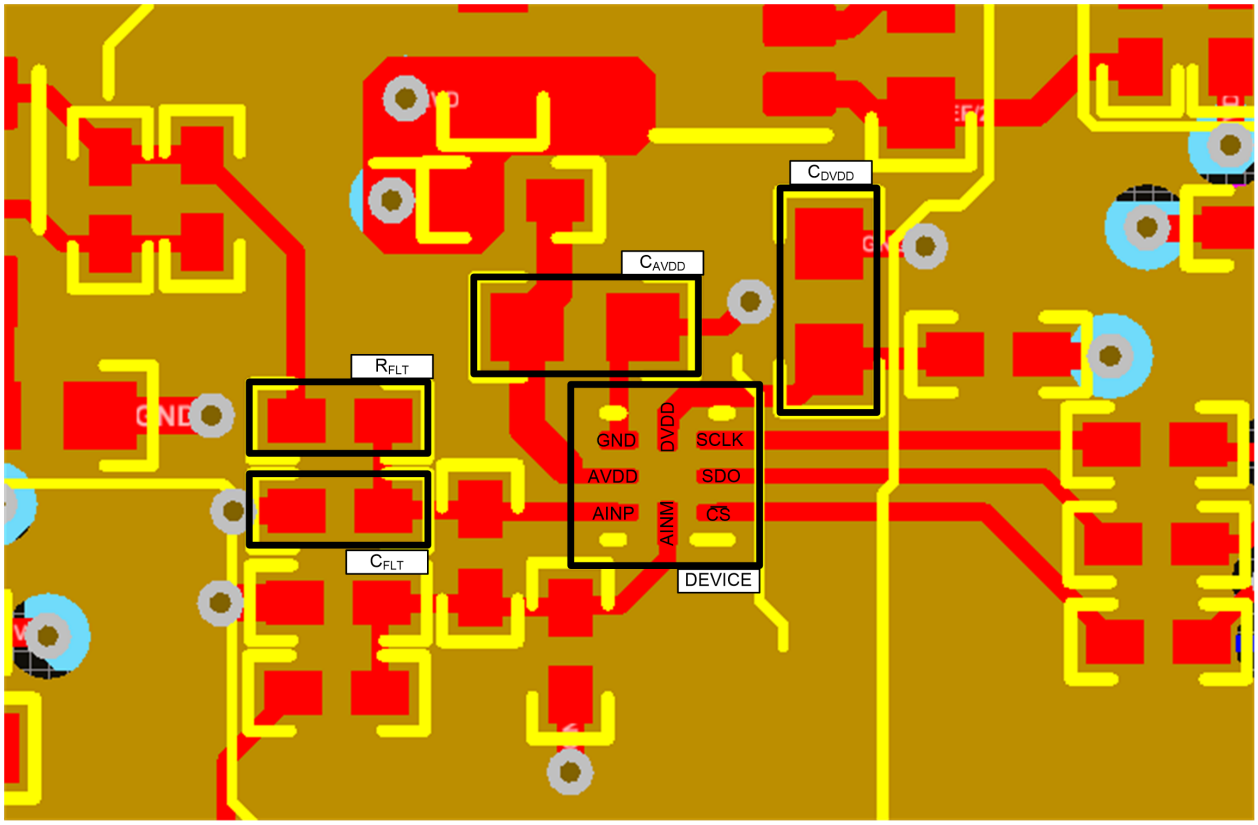


Figure 53. Example Layout

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档请参阅以下部分：

- *《OPAx836 极低功耗、轨至轨输出、负轨输入、电压反馈运算放大器》*
- *《REF19xx 低漂移、低功率、双路输出、V_{REF} 和 V_{REF}/2 电压基准》*
- *《OPAx365 50MHz、零交叉、低失真、高 CMRR、RRI/O、单电源运算放大器》*
- *《具有集成 ADC 驱动器缓冲器的 REF61xx 高精度电压基准》*
- *《THS4281 极低功耗、高速、轨至轨输入和输出电压反馈运算放大器》*
- *《ADS7042 超低功耗、超小尺寸、12 位、1MSPS、SAR ADC》*
- *《ADS7049-Q1 小型低功耗 12 位、2MSPS SAR ADC》*

12.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商标

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12.5 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

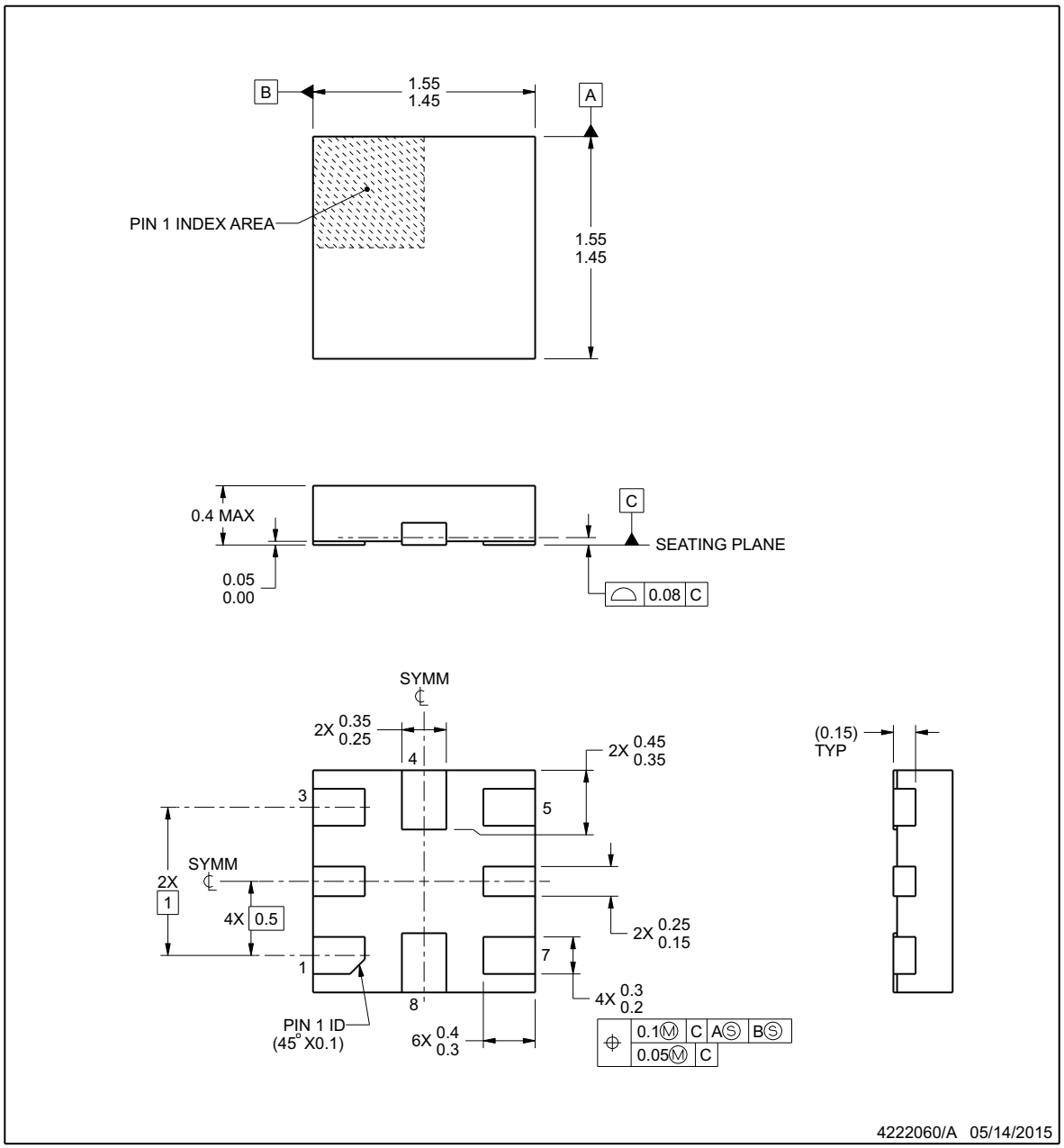
以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OUTLINE

RUG0008A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



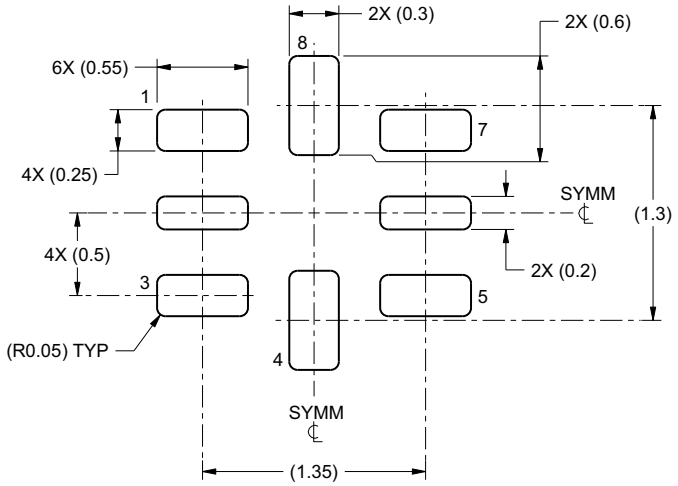
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

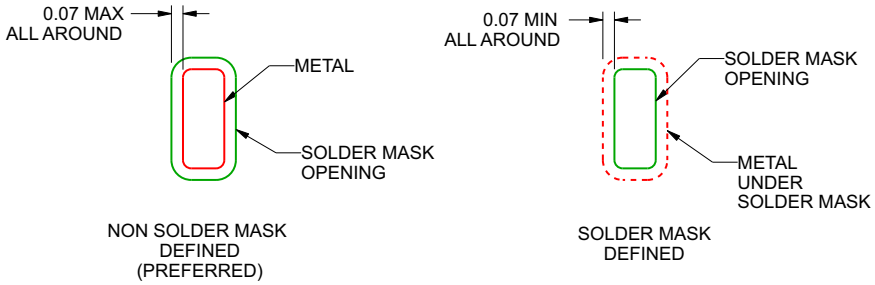
EXAMPLE BOARD LAYOUT

RUG0008A — **X2QFN - 0.4 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

4222060/A 05/14/2015

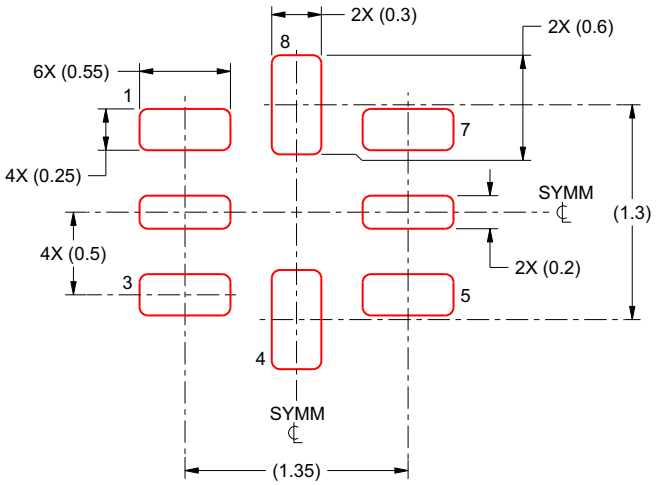
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUG0008A — **X2QFN - 0.4 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE:25X

4222060/A 05/14/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7056IRUGR	ACTIVE	X2QFN	RUG	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	5I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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