ADS1018-Q1 具有内部基准和温度传感器的汽车类、低功耗、兼容 SPI™ 的 12 位模数转换器

1 特性

- 符合汽车类应用标准
- 具有符合 AEC-Q100 的下列结果：
  - 温度等级 1：-40°C 至 +125°C
  - 人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 组件充电模式 (CDM) ESD 分类等级 C6
- 12 位无噪声分辨率
- 宽电源电压范围：2V 至 5.5V
- 低流耗：
  - 连续模式时：只有 150μA
  - 单次模式：自动断电
- 可编程数据传输速率范围：128SPS 至 3300SPS
- 单周期稳定
- 内部低漂移电压基准
- 内部温度传感器：
  2°C 误差（最大值）
- 内部振荡器
- 内部可编程增益放大器 (PGA)
- 四个单端或两个差分输入

2 应用

- 电池管理系统
- 车用传感器
  - 热电偶
  - 电阻式温度检测器 (RTD)
  - 电化学气体传感器
  - 颗粒物传感器

3 说明

ADS1018-Q1 是一款精密的低功耗 12 位无噪声模数转换器 (ADC)，其具备测量最常见传感器信号所需的全部功能。 ADS1018-Q1 集成了可编程增益放大器 (PGA)、电压基准、振荡器以及高精度温度传感器。 凭借这些功能以及 2V 至 5.5V 的宽电源电压范围，ADS1018-Q1 非常适用于功率及空间受限型传感器测量应用。

ADS1018-Q1 以高达 3300 次/秒 (SPS) 的采样数据传输速率进行转换。 PGA 的输入范围为 ±256mV 至 ±6.144V，支持以高分辨率测量大信号和小信号。 该器件通过输入复用器 (MUX) 测量双路差分输入或四路单端输入。 高精度温度传感器用于监控系统级温度或对热电偶进行冷结点补偿。

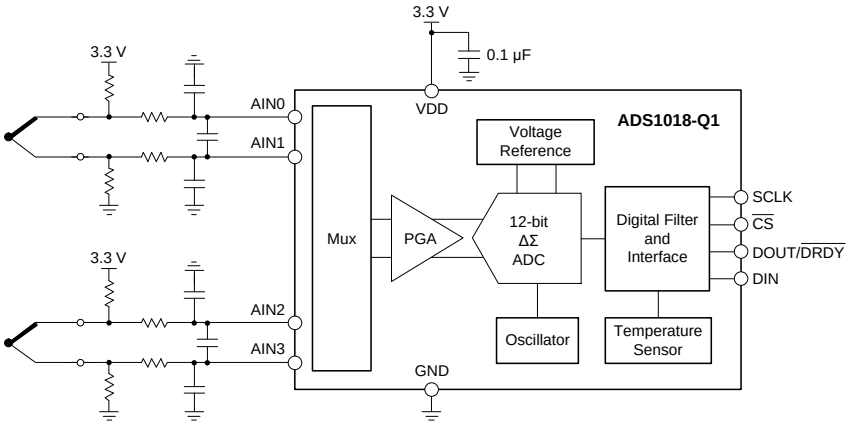
ADS1018-Q1 可选择以连续转换模式或单次模式运行。该器件在单次模式下完成一次转换后便会自动断电。 在空闲状态下，单次模式会显著降低流耗。 所有数据均通过串行外设接口 (SPI™) 进行传输。 ADS1018-Q1 的额定工作温度范围 -40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
ADS1018-Q1	VSSOP (10)	3.00mm × 3.00mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

K 型热电偶测量
使用集成温度传感器进行冷结点补偿



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4 修订历史记录

Changes from Original (October 2015) to Revision A **Page**

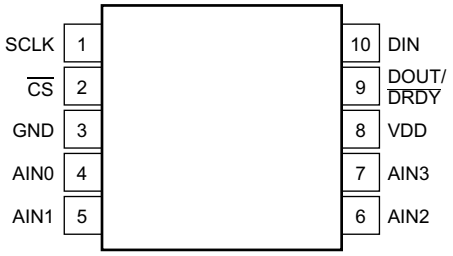
- 已从“产品预览”更改为“量产数据” ... 1

5 Device Comparison Table

DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS Differential (Single-Ended)	PGA	INTERFACE	SPECIAL FEATURES
ADS1118-Q1	16	860	2 (4)	Yes	SPI	Temperature sensor
ADS1018-Q1	12	3300	2 (4)	Yes	SPI	Temperature sensor
ADS1115-Q1	16	860	2 (4)	Yes	I^2C	Comparator
ADS1015-Q1	12	3300	2 (4)	Yes	I^2C	Comparator

6 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SCLK	Digital input	Serial clock input
2	$\overline{CS}$	Digital input	Chip select; active low. Connect to GND if not used.
3	GND	Supply	Ground
4	AIN0	Analog input	Analog input 0. Leave unconnected or tie to VDD if not used.
5	AIN1	Analog input	Analog input 1. Leave unconnected or tie to VDD if not used.
6	AIN2	Analog input	Analog input 2. Leave unconnected or tie to VDD if not used.
7	AIN3	Analog input	Analog input 3. Leave unconnected or tie to VDD if not used.
8	VDD	Supply	Power supply. Connect a 0.1-µF power supply decoupling capacitor to GND.
9	DOUT/$\overline{DRDY}$	Digital output	Serial data output combined with data ready; active low
10	DIN	Digital input	Serial data input

7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	5.5	V
Analog input voltage	AIN0, AIN1, AIN2, AIN3	GND – 0.3	VDD + 0.3	V
Digital input voltage	DIN, DOUT/$\overline{DRDY}$, SCLK, $\overline{CS}$	GND – 0.3	VDD + 0.3	V
Input current, continuous	Any pin except power supply pins	–10	10	mA
Temperature	Junction, T_J	–40	150	°C
	Storage, T_{stg}	–60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Power supply	VDD to GND	2		5.5	V
ANALOG INPUTS(1)						
FSR	Full-scale input voltage(2)	$V_{IN} = V_{(AINP)} - V_{(AINN)}$	See Table 1			
$V_{(AINx)}$	Absolute input voltage		GND		VDD	V
DIGITAL INPUTS						
	Input voltage		GND		VDD	V
TEMPERATURE						
T_A	Operating ambient temperature		–40		125	°C

(1) AINP and AINN denote the selected positive and negative inputs. AINx denotes one of the four available analog inputs.
(2) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.

7.4 Thermal Information

THERMAL METRIC(1)		ADS1018-Q1 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	186.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	108.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	106.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Maximum and minimum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at VDD = 3.3 V and FSR = ±2.048 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
	Common-mode input impedance	FSR = ±6.144 V(1)		8		MΩ
		FSR = ±4.096 V(1), FSR = ±2.048 V		6		
		FSR = ±1.024 V		3		
		FSR = ±0.512 V, FSR = ±0.256 V		100		
	Differential input impedance	FSR = ±6.144 V(1)		22		MΩ
		FSR = ±4.096 V(1)		15		
		FSR = ±2.048 V		4.9		
		FSR = ±1.024 V		2.4		
		FSR = ±0.512 V, FSR = ±0.256 V		710		kΩ
SYSTEM PERFORMANCE						
	Resolution (no missing codes)			12		Bits
DR	Data rate			128, 250, 490, 920, 1600, 2400, 3300		SPS
	Data rate variation	All data rates	–10%		10%	
INL	Integral nonlinearity	DR = 128 SPS, FSR = ±2.048 V(2)			0.5	LSB
	Offset error	FSR = ±2.048 V, differential inputs		0	±0.5	LSB
		FSR = ±2.048 V, single-ended inputs		±0.25		
	Offset drift	FSR = ±2.048 V		0.002		LSB/°C
	Offset channel match	Match between any two inputs		0.25		LSB
	Gain error(3)	FSR = ±2.048 V, T_A = 25°C		0.05%	0.25%	
	Gain drift(3)(4)	FSR = ±0.256 V		7		ppm/°C
		FSR = ±2.048 V		5	40	
		FSR = ±6.144 V(1)		5		
	Gain match(3)	Match between any two gains		0.02%	0.1%	
	Gain channel match	Match between any two inputs		0.05%	0.1%	
TEMPERATURE SENSOR						
	Temperature range		–40		125	°C
	Temperature resolution			0.125		°C/LSB
	Accuracy	T_A = 0°C to 70°C		0.25	±1	°C
		T_A = –40°C to +125°C		0.5	±2	
		vs supply		0.125	±1	°C/V

(1) This parameter expresses the full-scale range of the ADC scaling. No more than VDD + 0.3 V or 5.5 V (whichever is smaller) must be applied to this device.
(2) Best-fit INL; covers 99% of full-scale.
(3) Includes all errors from onboard PGA and voltage reference.
(4) Maximum value specified by characterization.

Electrical Characteristics (continued)

Maximum and minimum specifications apply from T_A = –40°C to +125°C. Typical specifications are at T_A = 25°C. All specifications are at VDD = 3.3 V and FSR = ±2.048 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS/OUTPUTS						
V_{IH}	High-level input voltage		0.7 VDD		VDD	V
V_{IL}	Low-level input voltage		GND		0.2 VDD	V
V_{OH}	High-level output voltage	I_{OH} = 1 mA	0.8 VDD			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	GND		0.2 VDD	V
I_H	Input leakage, high	V_{IH} = 5.5 V	–10		10	µA
I_L	Input leakage, low	V_{IL} = GND	–10		10	µA
POWER SUPPLY						
I_{VDD}	Supply current	Power-down, T_A = 25°C		0.5	2	µA
		Power-down			5	
		Operating, T_A = 25°C		150	200	
		Operating			300	
P_D	Power dissipation	VDD = 5 V		0.9		mW
		VDD = 3.3 V		0.5		
		VDD = 2 V		0.3		

7.6 Timing Requirements: Serial Interface

over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
t_{CSSC}	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge(1)	100		ns
t_{SCCS}	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge	100		ns
t_{CSH}	Pulse duration, $\overline{CS}$ high	200		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	Pulse duration, SCLK high	100		ns
t_{SPWL}	Pulse duration, SCLK low(2)	100		ns
			28	ms
t_{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t_{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

(1) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
(2) Holding SCLK low longer than 28 ms resets the SPI interface.

7.7 Switching Characteristics: Serial Interface

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CSDOD}	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	DOUT load = 20 pF || 100 kΩ to GND			100	ns
t_{DOPD}	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF || 100 kΩ to GND	0		50	ns
t_{CSDOZ}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20 pF || 100 kΩ to GND			100	ns

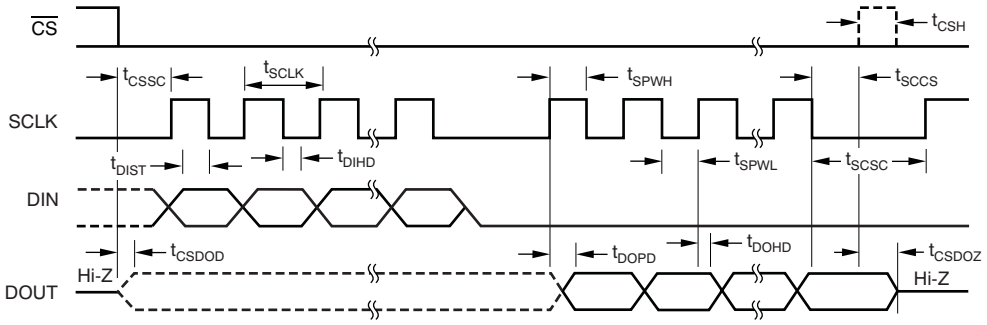


Figure 1. Serial Interface Timing

7.8 Typical Characteristics

at T_A = 25°C, VDD = 3.3 V, and FSR = ±2.048 V (unless otherwise noted)

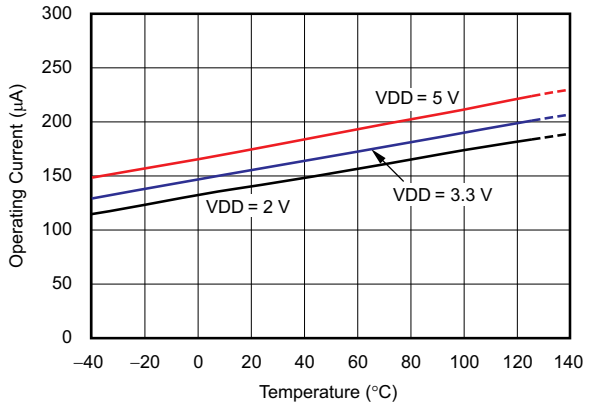


Figure 2. Operating Current vs Temperature

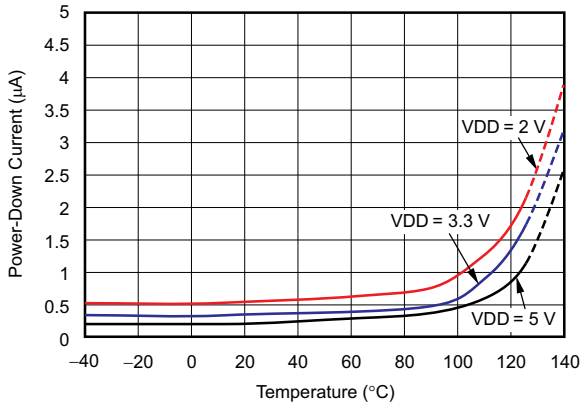


Figure 3. Power-Down Current vs Temperature

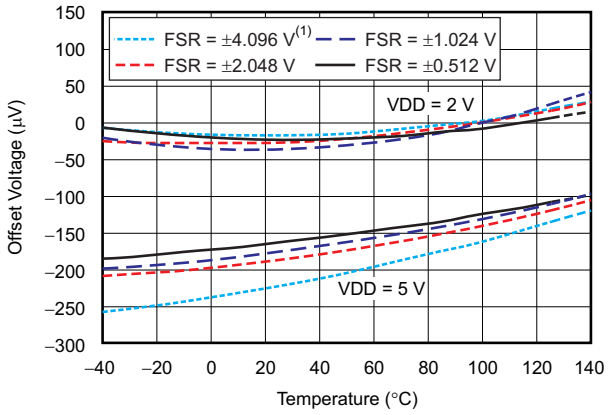


Figure 4. Single-Ended Offset Voltage vs Temperature

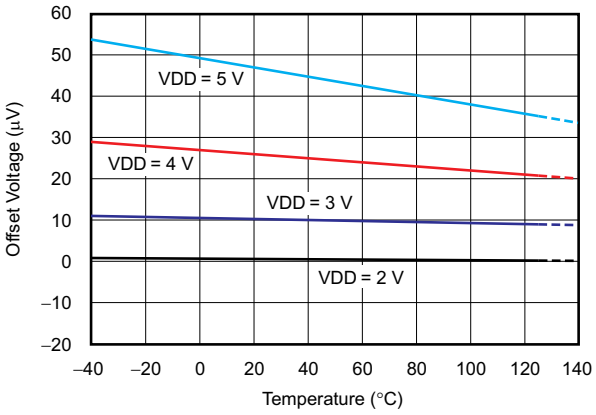


Figure 5. Differential Offset Voltage vs Temperature

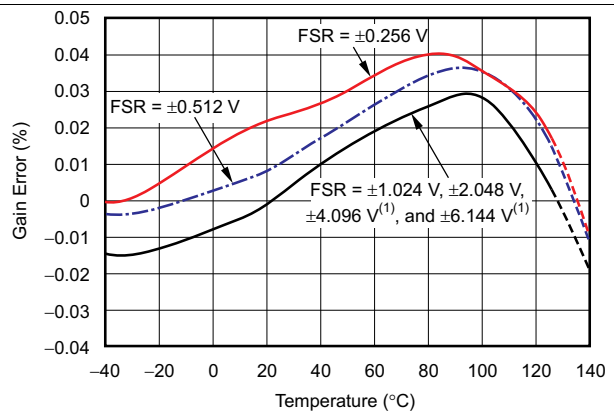


Figure 6. Gain Error vs Temperature

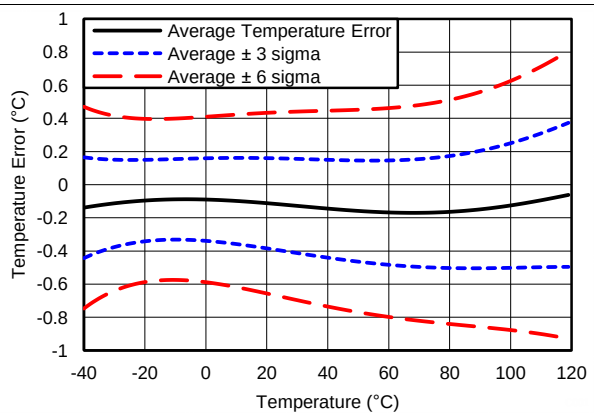


Figure 7. Temperature Sensor Error vs Temperature

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

8 Detailed Description

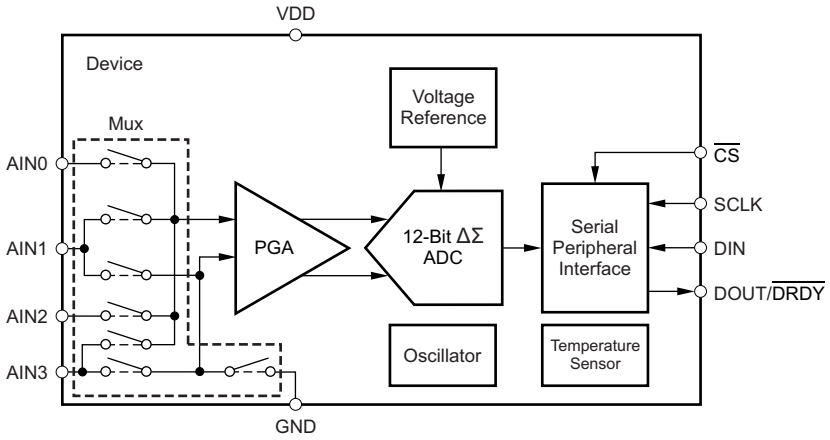
8.1 Overview

The ADS1018-Q1 is a very small, low-power, noise-free, 12-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1018-Q1 consists of a ΔΣ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an SPI. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. The *Functional Block Diagram* section shows the ADS1018-Q1 functional block diagram.

The ADS1018-Q1 ADC core measures a differential signal, V_{IN}, that is the difference of $V_{(AINP)}$ and $V_{(AINN)}$. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1018-Q1 has two available conversion modes: single-shot and continuous-conversion. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal conversion register. The device then enters a power-down state. This mode is intended to provide significant power savings in systems that require only periodic conversions or when there are long idle periods between conversions. In continuous-conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Multiplexer

The ADS1018-Q1 contains an input multiplexer (mux), as shown in Figure 8. Either four single-ended or two differential signals can be measured. Additionally, AIN0, AIN1, and AIN2 can be measured differentially to AIN3. The multiplexer is configured by bits MUX[2:0] in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

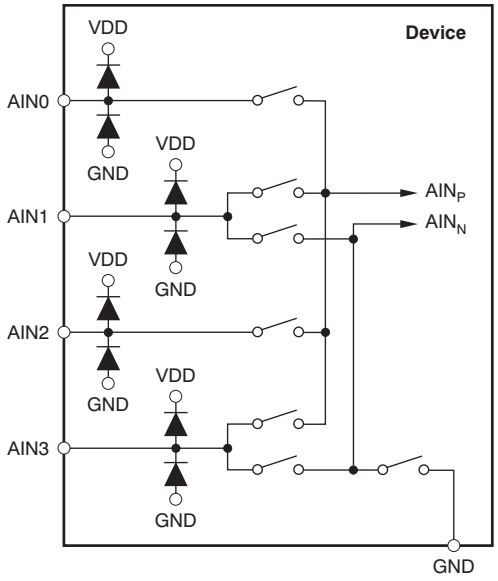


Figure 8. Input Multiplexer

When measuring single-ended inputs, the device does not output negative codes. These negative codes indicate negative differential signals; that is, $(V_{(AINP)} – V_{(AINN)}) < 0$. Electrostatic discharge (ESD) diodes to VDD and GND protect the ADS1018-Q1 inputs. To prevent the ESD diodes from turning on, keep the absolute voltage on any input within the range given in Equation 1:

$$GND – 0.3\ V < V_{(AINx)} < VDD + 0.3\ V \quad (1)$$

If the voltages on the input pins can possibly violate these conditions, use external Schottky diodes and series resistors to limit the input current to safe values (see the *Absolute Maximum Ratings* table).

Also, overdriving one unused input on the ADS1018-Q1 may affect conversions currently taking place on other input pins. If overdriving unused inputs is possible, clamp the signal with external Schottky diodes.

Feature Description (continued)

8.3.2 Analog Inputs

The ADS1018-Q1 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. This frequency at which the input signal is sampled is called the sampling frequency or the modulator frequency ($f_{(MOD)}$). The ADS1018-Q1 has a 1 MHz internal oscillator which is further divided by a factor of 4 to generate the modulator frequency at 250 kHz. The capacitors used in this input stage are small, and to external circuitry, the average loading appears resistive. This structure is shown in Figure 9. The resistance is set by the capacitor values and the rate at which they are switched. Figure 10 shows the setting of the switches illustrated in Figure 9. During the sampling phase, switches S_1 are closed. This event charges C_{A1} to $V_{(AINP)}$, C_{A2} to $V_{(AINN)}$, and C_B to ($V_{(AINP)} – V_{(AINN)}$). During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7 V and C_B discharges to 0 V. This charging draws a very small transient current from the source driving the ADS1018-Q1 analog inputs. The average value of this current can be used to calculate the effective impedance (Z_{eff}), where $Z_{eff} = V_{IN} / I_{AVERAGE}$.

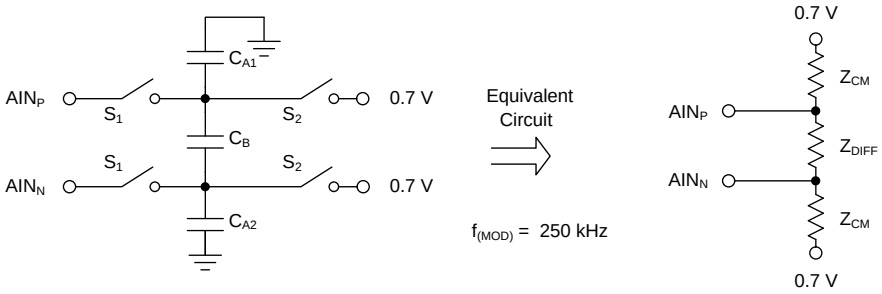


Figure 9. Simplified Analog Input Circuit

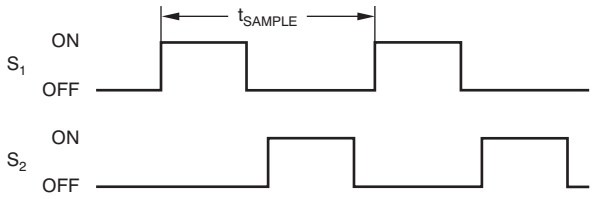


Figure 10. S_1 and S_2 Switch Timing

Common-mode input impedance is measured by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the full-scale range, but is approximately 6 MΩ for the default full-scale range. In Figure 9, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the full-scale range. In Figure 9, the differential input impedance is Z_{DIFF}.

Make sure to consider the typical value of the input impedance. Unless the input source has a low impedance, the ADS1018-Q1 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Active buffers introduce noise, and also introduce offset and gain errors. Consider all of these factors in high-accuracy applications.

The clock oscillator frequency drifts slightly with temperature; therefore, the input impedances also drift. For most applications, this input impedance drift is negligible, and can be ignored.

Feature Description (continued)

8.3.3 Full-Scale Range (FSR) and LSB Size

A programmable gain amplifier (PGA) is implemented in front of the ADS1018-Q1 ΔΣ ADC core. The full-scale range is configured by bits PGA[2:0] in the Config register, and can be set to ±6.144 V, ±4.096 V, ±2.048 V, ±1.024 V, ±0.512 V, or ±0.256 V.

Table 1 shows the FSR together with the corresponding LSB size. Calculate the LSB size from the full-scale voltage by the formula shown in Equation 2. However, make sure that the analog input voltage never exceeds the analog input voltage range limit given in the *Electrical Characteristics*. If VDD greater than 4 V is used, the ±6.144-V full-scale range allows input voltages to extend up to the supply. Note though that in this case, or whenever the supply voltage is less than the full-scale range (for example, VDD = 3.3 V and full-scale range = ±4.096 V), a full-scale ADC output code cannot be obtained. This inability means that some dynamic range is lost.

$$LSB = FSR / 2^{12} \quad (2)$$

Table 1. Full-Scale Range and Corresponding LSB Size

FSR	LSB SIZE
±6.144 V(1)	3 mV
±4.096 V(1)	2 mV
±2.048 V	1 mV
±1.024 V	0.5 mV
±0.512 V	0.25 mV
±0.256 V	0.125 mV

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

8.3.4 Voltage Reference

The ADS1018-Q1 has an integrated voltage reference. An external reference cannot be used with this device. Errors associated with the initial voltage reference accuracy and the reference drift with temperature are included in the gain error and gain drift specifications in the *Electrical Characteristics*.

8.3.5 Oscillator

The ADS1018-Q1 has an integrated oscillator running at 1 MHz. No external clock is required to operate the device. Note that the internal oscillator drifts over temperature and time. The output data rate scales proportionally with the oscillator frequency.

8.3.6 Temperature Sensor

The ADS1018-Q1 offers an integrated precision temperature sensor. To enable the temperature sensor mode, set bit TS_MODE = 1 in the Config register. Temperature data are represented as a 12-bit result that is left-justified within the 16-bit conversion result. Data are output starting with the most significant byte (MSB). When reading the two data bytes, the first 12 bits are used to indicate the temperature measurement result. One 12-bit LSB equals 0.125°C. Negative numbers are represented in binary twos complement format, as shown in Table 2.

Table 2. 12-Bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	0 100 0000 0000	400
127.875	0 011 1111 1111	3FF
100	0 011 0010 0000	320
80	0 010 1000 0000	280
75	0 010 0101 1000	258
50	0 001 1001 0000	190
25	0 000 1100 1000	0C8
0.25	0 000 0000 0010	002
0	0 000 0000 0000	000
–0.25	1 111 1111 1110	FFE
–25	1 111 0011 1000	F38
–40	1 110 1100 0000	EC0

8.3.6.1 Converting from Temperature to Digital Codes

For positive temperatures:

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 12-bit, left justified format with the MSB = 0 to denote the positive sign.

Example: 50°C / (0.125°C/count) = 400 = 190h = 0001 1001 0000

For negative temperatures:

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then, denote the negative sign with the MSB = 1.

Example: |–25°C| / (0.125/count) = 200 = 0C8h = 0000 1100 1000

Twos complement format: 1111 0011 01111 + 1 = 1111 0011 1000

8.3.6.2 Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a 0 or a 1. If the MSB is a 0, simply multiply the decimal code by 0.125°C to obtain the result. If the MSB = 1, subtract 1 from the result and complement all of the bits. Then, multiply the result by –0.125°C.

Example: The device reads back 258h: 258h has an MSB = 0.

258h × 0.125°C = 600 × 0.125°C = +75°C

Example: The device reads back F38h: F38h has an MSB = 1.

Subtract 1 and complement the result: F38h → C8h

C8h × (–0.125°C) = 200 × (–0.125°C) = –25°C

8.4 Device Functional Modes

8.4.1 Reset and Power-Up

When the ADS1018-Q1 powers up, the device resets. As part of the reset process, the ADS1018-Q1 sets all bits in the Config register to the respective default settings. By default, the ADS1018-Q1 enters a power-down state at start-up. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS1018-Q1 relieves systems with tight power-supply requirements from encountering a surge during power-up.

8.4.2 Operating Modes

The ADS1018-Q1 operates in one of two modes: continuous-conversion or single-shot. The MODE bit in the Config register selects the respective operating mode.

8.4.2.1 Single-Shot Mode and Power-Down

When the MODE bit in the Config register is set to 1, the ADS1018-Q1 enters a power-down state, and operates in single-shot mode. This power-down state is the default state for the ADS1018-Q1 when power is first applied. Although powered down, the device still responds to commands. The ADS1018-Q1 remains in this power-down state until a 1 is written to the single-shot (SS) bit in the Config register. When the SS bit is asserted, the device powers up, resets the SS bit to 0, and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a 1 to the SS bit while a conversion is ongoing has no effect. To switch to continuous-conversion mode, write a 0 to the MODE bit in the Config register.

8.4.2.2 Continuous-Conversion Mode

In continuous-conversion mode (MODE bit set to 0), the ADS1018-Q1 continuously performs conversions. When a conversion completes, the ADS1018-Q1 places the result in the Conversion register and immediately begins another conversion. To switch to single-shot mode, write a 1 to the MODE bit in the Config register, or reset the device.

8.4.3 Duty Cycling for Low Power

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator are averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the ADS1018-Q1 supports duty cycling that can yield significant power savings by periodically requesting high data-rate readings at an effectively lower data rate.

For example, an ADS1018-Q1 in power-down state with a data rate set to 3300 SPS can be operated by a microcontroller that instructs a single-shot conversion every 7.8 ms (128 SPS). A conversion at 3300 SPS only requires approximately 0.3 ms; therefore, the ADS1018-Q1 enters power-down state for the remaining 7.5 ms. In this configuration, the ADS1018-Q1 consumes approximately 1/25th the power that is otherwise consumed in continuous-conversion mode. The duty cycling rate is completely arbitrary and is defined by the master controller. The ADS1018-Q1 offers lower data rates that do not implement duty cycling and also offers improved noise performance, if required.

8.5 Programming

8.5.1 Serial Interface

The SPI-compatible serial interface consists of either four signals ($\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$), or three signals (SCLK, DIN, and DOUT/$\overline{DRDY}$, with $\overline{CS}$ tied low). The interface is used to read conversion data, read from and write to registers, and control device operation.

8.5.2 Chip Select ($\overline{CS}$)

The chip select pin ($\overline{CS}$) selects the ADS1018-Q1 for SPI communication. This feature is useful when multiple devices share the same serial bus. Keep $\overline{CS}$ low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT/$\overline{DRDY}$ enters a high-impedance state. In this state, DOUT/$\overline{DRDY}$ cannot provide data-ready indication. In situations where multiple devices are present and DOUT/$\overline{DRDY}$ must be monitored, lower $\overline{CS}$ periodically. At this point, the DOUT/$\overline{DRDY}$ pin either immediately goes high to indicate that no new data are available, or immediately goes low to indicate that new data are present in the Conversion register and are available for transfer. New data can be transferred at any time without concern of data corruption. When a transmission starts, the current result is locked into the output shift register and does not change until the communication completes. This system avoids any possibility of data corruption.

8.5.3 Serial Clock (SCLK)

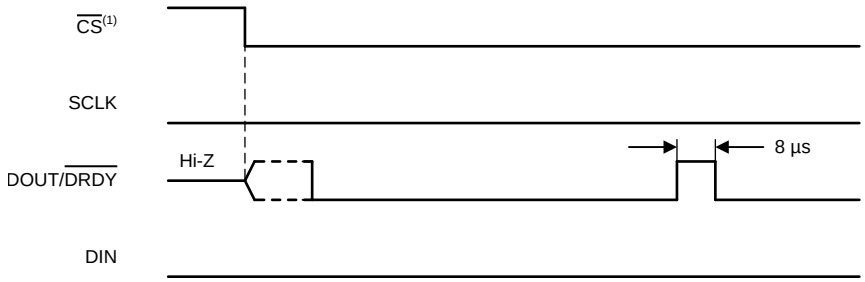
The serial clock pin (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT/$\overline{DRDY}$ pins into and out of the ADS1018-Q1. Even though the input has hysteresis, keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. To reset the serial interface, hold SCLK low for 28 ms, and the next SCLK pulse starts a new communication cycle. Use this time-out feature to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

8.5.4 Data Input (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADS1018-Q1. The device latches data on DIN at the SCLK falling edge. The ADS1018-Q1 never drives the DIN pin.

8.5.5 Data Output and Data Ready (DOUT/$\overline{DRDY}$)

The data output and data ready pin (DOUT/$\overline{DRDY}$) is used with SCLK to read conversion and register data from the ADS1018-Q1. Data on DOUT/$\overline{DRDY}$ are shifted out on the SCLK rising edge. DOUT/$\overline{DRDY}$ is also used to indicate that a conversion is complete and new data are available. This pin transitions low when new data are ready for retrieval. DOUT/$\overline{DRDY}$ is also able to trigger a microcontroller to start reading data from the ADS1018-Q1. In continuous-conversion mode, DOUT/$\overline{DRDY}$ transitions high again 8 µs before the next data ready signal (DOUT/$\overline{DRDY}$ low) if no data are retrieved from the device. This transition is shown in Figure 11. Complete the data transfer before DOUT/$\overline{DRDY}$ returns high.



(1) $\overline{CS}$ can be held low if the ADS1018-Q1 does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 11. DOUT/$\overline{DRDY}$ Behavior Without Data Retrieval in Continuous-Conversion Mode

When $\overline{CS}$ is high, DOUT/$\overline{DRDY}$ is configured by default with a weak internal pullup resistor. This feature reduces the risk of DOUT/$\overline{DRDY}$ floating near midsupply and causing leakage current in the master device. To disable this pullup resistor and place the device into a high-impedance state, set the PULL_UP_EN bit to 0 in the Config register.

Programming (continued)

8.5.6 Data Format

The ADS1018-Q1 provides 12 bits of data in binary twos complement format that is left justified within the 16-bit data word. A positive full-scale (+FS) input produces an output code of 7FF0h and a negative full-scale (–FS) input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 3 summarizes the ideal output codes for different input signals. Figure 12 shows code transitions versus input voltage.

Table 3. Input Signal versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE(1)
≥ +FS (2^{11} – 1) / 2^{11}	7FF0h
+FS / 2^{11}	0010h
0	0
–FS / 2^{11}	FFF0h
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

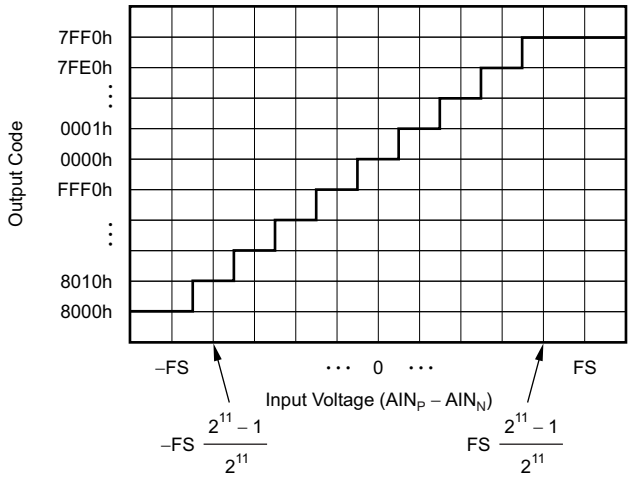


Figure 12. Code Transition Diagram

8.5.7 Data Retrieval

Data is written to and read from the ADS1018-Q1 in the same manner for both single-shot and continuous conversion modes, without having to issue any commands. The operating mode for the ADS1018-Q1 is selected by the MODE bit in the Config register.

Set the MODE bit to 0 to put the device in continuous-conversion mode. In continuous-conversion mode, the device is constantly starting new conversions even when $\overline{CS}$ is high.

Set the MODE bit to 1 for single-shot mode. In single-shot mode, a new conversion only starts by writing a 1 to the SS bit.

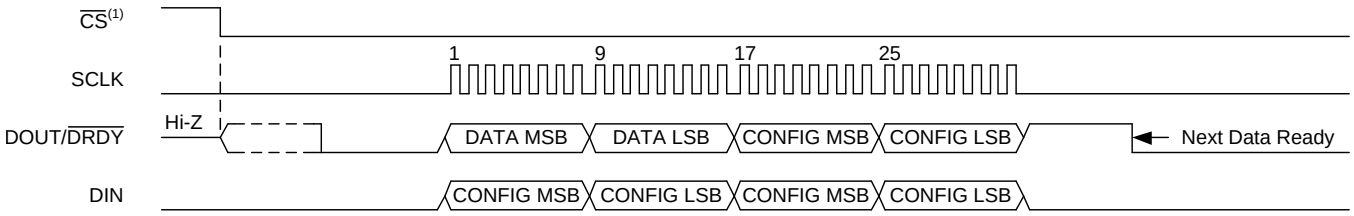
The conversion data are always buffered, and retain the current data until replaced by new conversion data. Therefore, data can be read at any time without concern of data corruption. When DOUT/$\overline{DRDY}$ asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/$\overline{DRDY}$. The MSB of the data (bit 15) on DOUT/$\overline{DRDY}$ is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out of DOUT/$\overline{DRDY}$, new Config register data are latched on DIN on the SCLK falling edge.

The ADS1018-Q1 also offers the possibility of direct readback of the Config register settings in the same data transmission cycle. One complete data transmission cycle consists of either 32 bits (when the Config register data readback is used) or 16 bits (only used when the $\overline{CS}$ line can be controlled and is not permanently tied low).

8.5.7.1 32-Bit Data Transmission Cycle

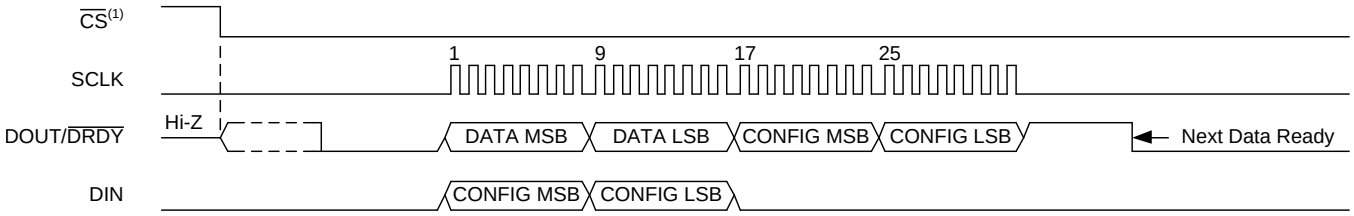
The data in a 32-bit data transmission cycle consist of four bytes: two bytes for the conversion result, and an additional two bytes for the Config register readback. The device always reads the MSB first.

Write the same Config register setting twice during one transmission cycle as shown in Figure 13. If convenient, write the Config register setting once during the first half of the transmission cycle, and then hold the DIN pin either low (as shown in Figure 14) or high during the second half of the cycle. If no update to the Config register is required, hold the DIN pin either low or high during the entire transmission cycle. The Config register setting written in the first two bytes of a 32-bit transmission cycle is read back in the last two bytes of the same cycle.



(1) $\overline{CS}$ can be held low if the ADS1018-Q1 does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 13. 32-Bit Data Transmission Cycle With Config Register Readback



(1) $\overline{CS}$ can be held low if the ADS1018-Q1 does not share the serial bus with another device. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 14. 32-Bit Data Transmission Cycle: DIN Held Low

8.5.7.2 16-Bit Data Transmission Cycle

If Config register data are not required to be read back, the ADS1018-Q1 conversion data can be clocked out in a short 16-bit data transmission cycle, as shown in Figure 15. Take $\overline{CS}$ high after the 16th SCLK cycle to reset the SPI interface. The next time $\overline{CS}$ is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/$\overline{DRDY}$ is low when data retrieval starts, the conversion buffer is already updated with a new result. Otherwise, if DOUT/$\overline{DRDY}$ is high, the same result from the previous data transmission cycle is read.

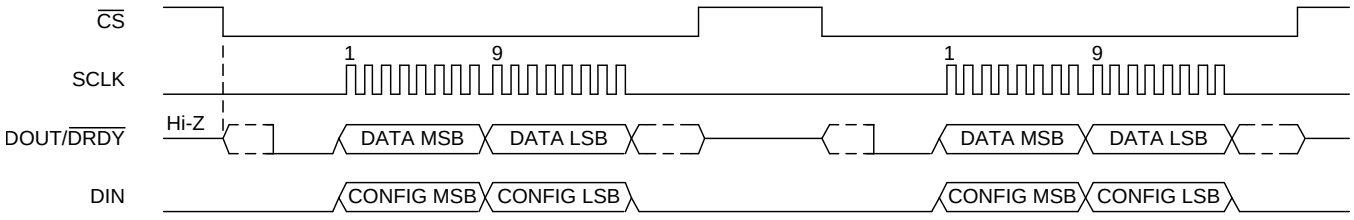


Figure 15. 16-Bit Data Transmission Cycle

8.6 Register Maps

The ADS1018-Q1 has two registers that are accessible through the SPI. The Conversion register contains the result of the last conversion. The Config register allows the user to change the ADS1018-Q1 operating modes and query the status of the devices.

8.6.1 Conversion Register [reset = 0000h]

The 16-bit Conversion register contains the result of the last conversion in binary twos complement format. Following power up, the Conversion register is cleared to 0, and remains 0 until the first conversion is complete. The register format is shown in Figure 16.

Figure 16. Conversion Register

15	14	13	12	11	10	9	8
D11	D10	D9	D8	D7	D6	D5	D4
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
D3	D2	D1	D0	Reserved			
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 4. Conversion Register Field Descriptions

Bit	Field	Type	Reset	Description
15:4	D[11:0]	R	000h	12-bit conversion result
3:0	Reserved	R	0h	Always Reads back 0h

8.6.2 Config Register [reset= 058Bh]

The 16-bit Config register can be used to control the ADS1018-Q1 operating mode, input selection, data rate, full-scale range, and temperature sensor mode. The register format is shown in Figure 17.

Figure 17. Config Register

15	14	13	12	11	10	9	8
SS	MUX[2:0]			PGA[2:0]			MODE
R/W-0h	R/W-0h			R/W-2h			R/W-1h
7	6	5	4	3	2	1	0
DR[2:0]			TS_MODE	PULL_UP_EN	NOP[1:0]		Reserved
R/W-4h			R/W-0h	R/W-1h	R/W-1h		R-1h

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 5. Config Register Field Descriptions

Bit	Field	Type	Reset	Description
15	SS	R/W	0h	**Single-shot conversion start** This bit is used to start a single conversion. SS can only be written when in power-down state and has no effect when a conversion is ongoing. When writing: 0 = No effect 1 = Start a single conversion (when in power-down state) Always reads back as 0 (default).

Table 5. Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
14:12	MUX[2:0]	R/W	0h	**Input multiplexer configuration** These bits configure the input multiplexer. 000 = AIN_P is AIN0 and AIN_N is AIN1 (default) 001 = AIN_P is AIN0 and AIN_N is AIN3 010 = AIN_P is AIN1 and AIN_N is AIN3 011 = AIN_P is AIN2 and AIN_N is AIN3 100 = AIN_P is AIN0 and AIN_N is GND 101 = AIN_P is AIN1 and AIN_N is GND 110 = AIN_P is AIN2 and AIN_N is GND 111 = AIN_P is AIN3 and AIN_N is GND
11:9	PGA[2:0]	R/W	2h	**Programmable gain amplifier configuration** These bits configure the programmable gain amplifier. 000 = FSR is ±6.144 V(1) 001 = FSR is ±4.096 V(1) 010 = FSR is ±2.048 V (default) 011 = FSR is ±1.024 V 100 = FSR is ±0.512 V 101 = FSR is ±0.256 V 110 = FSR is ±0.256 V 111 = FSR is ±0.256 V
8	MODE	R/W	1h	**Device operating mode** This bit controls the ADS1018-Q1 operating mode. 0 = Continuous-conversion mode 1 = Power-down and single-shot mode (default)
7:5	DR[2:0]	R/W	4h	**Data rate** These bits control the data-rate setting. 000 = 128 SPS 001 = 250 SPS 010 = 490 SPS 011 = 920 SPS 100 = 1600 SPS (default) 101 = 2400 SPS 110 = 3300 SPS 111 = Not Used
4	TS_MODE	R/W	0h	**Temperature sensor mode** This bit configures the ADC to convert temperature or input signals. 0 = ADC mode (default) 1 = Temperature sensor mode
3	PULL_UP_EN	R/W	1h	**Pullup enable** This bit enables a weak internal pullup resistor on the DOUT/$\overline{DRDY}$ pin only when $\overline{CS}$ is high. When enabled, an internal 400-kΩ resistor connects the bus line to supply. When disabled, the DOUT/$\overline{DRDY}$ pin floats. 0 = Pullup resistor disabled on DOUT/$\overline{DRDY}$ pin 1 = Pullup resistor enabled on DOUT/$\overline{DRDY}$ pin (default)
2:1	NOP[1:0]	R/W	1h	**No operation** The NOP[1:0] bits control whether data are written to the Config register or not. For data to be written to the Config register, the NOP[1:0] bits must be 01. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register. 00 = Invalid data; do not update the contents of the Config register 01 = Valid data; update the Config register (default) 10 = Invalid data; do not update the contents of the Config register 11 = Invalid data; do not update the contents of the Config register
0	Reserved	R	1h	**Reserved** Always write 1h Reads back either 0h or 1h

(1) This parameter expresses the full-scale range of the ADC scaling. Do not apply more than VDD + 0.3 V to this device.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ADS1018-Q1 is a precision, 12-bit ΔΣ ADC that offers many integrated features to ease the measurement of the most common sensor types including various type of temperature and bridge sensors. The following sections give example circuits and suggestions for using the ADS1018-Q1 in various situations.

9.1.1 Serial Interface Connections

The principle serial interface connections for the ADS1018-Q1 are shown in Figure 18.

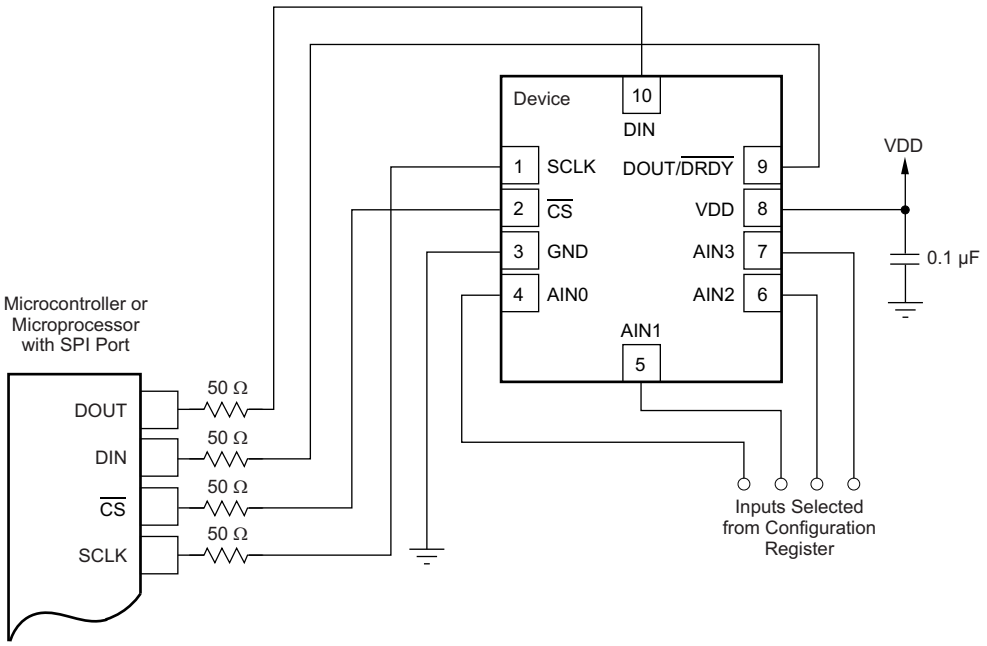


Figure 18. Typical Connections

Most microcontroller SPI peripherals operate with the ADS1018-Q1. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1, SCLK idles low, and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the ADS1018-Q1 can be found in the *Timing Requirements: Serial Interface* section.

It is a good practice to place 50-Ω resistors in the series path to each of the digital pins to provide some short-circuit protection. Take care to still meet all SPI timing requirements because these additional series resistors along with the bus parasitic capacitances present on the digital signal lines slews the signals.

The fully-differential input of the ADS1018-Q1 is ideal for connecting to differential sources (such as thermocouples and thermistors) with a moderately low source impedance. Although the ADS1018-Q1 can read fully-differential signals, the device cannot accept negative voltages on either of its inputs because of ESD protection diodes on each pin. When an input exceeds supply or drops below ground, these diodes turn on to prevent any ESD damage to the device.

Application Information (continued)

9.1.2 GPIO Ports for Communication

Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an SPI controller is not available, the ADS1018-Q1 can be connected to GPIO pins and the SPI bus protocol can be simulated. Using GPIO pins to generate the SPI interface requires only that the pins be configured as push or pull inputs or outputs. Furthermore, if the SCLK line is held low for more than 28 ms, communication times out. This condition means that the GPIO ports must be capable of providing SCLK pulses with no more than 28 ms between pulses.

9.1.3 Analog Input Filtering

Analog input filtering serves two purposes: first, to limit the effect of aliasing during the sampling process and second, to reduce external noise from being a part of the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the *Nyquist frequency*). These frequency components fold back and show up in the actual frequency band of interest below half the sampling frequency. The filter response of the digital filter repeats at multiples of the sampling frequency, also known as modulator frequency $f_{(MOD)}$, as shown in Figure 19. Signals or noise up to a frequency where the filter response repeats are attenuated to a certain amount by the digital filter depending on the filter architecture. Any frequency components present in the input signal around the modulator frequency or multiples thereof are not attenuated and alias back into the band of interest, unless attenuated by an external analog filter.

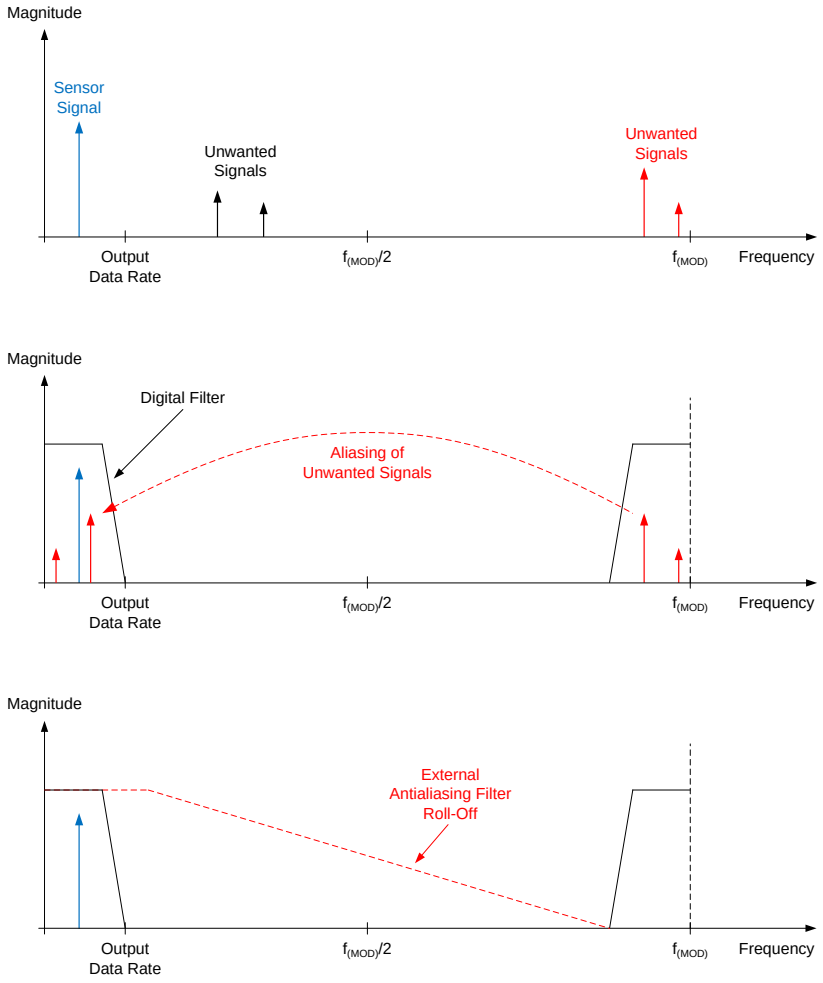


Figure 19. Effect of Aliasing

Application Information (continued)

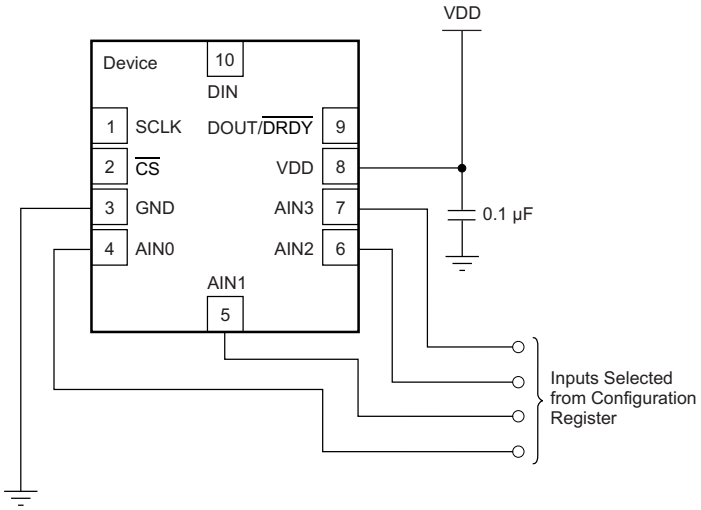
Many sensor signals are inherently band-limited; for example, the output of a thermocouple has a limited rate of change. In this case the sensor signal does not alias back into the pass-band when using a ΔΣ ADC. However, any noise pickup along the sensor wiring or the application circuitry can potentially alias into the pass band. Power line-cycle frequency and harmonics are one common noise source. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source typically exists on the printed-circuit-board (PCB) itself in the form of clocks and other digital signals. Analog input filtering helps remove unwanted signals from affecting the measurement result.

A first-order, resistor-capacitor (RC) filter is, in most cases, sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond $f_{(MOD)}$ / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1018-Q1 attenuates signals to a certain degree. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or ten times higher is generally a good starting point for a system design.

9.1.4 Single-Ended Inputs

Although the ADS1018-Q1 has two differential inputs, the device can measure four single-ended signals. Figure 20 shows a single-ended connection scheme. The ADS1018-Q1 is configured for single-ended measurement by configuring the mux to measure each channel with respect to ground. Data are then read out of one input based on the selection in the Config register. The single-ended signal can range from 0 V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to this circuit because the ADS1018-Q1 can only accept positive voltages with respect to ground. The ADS1018-Q1 does not loose linearity within the input range.

The ADS1018-Q1 offers a differential input voltage range of ±FS. The single-ended circuit shown in Figure 20, however, only uses the positive half of the ADS1018-Q1 FS input voltage range because differentially negative inputs are not produced. Because only half of the FS range is used, one bit of resolution is lost. For optimal noise performance, use differential configurations whenever possible. Differential configurations maximize the dynamic range of the ADC and provide strong attenuation of common-mode noise.



NOTE: Digital pin connections omitted for clarity.

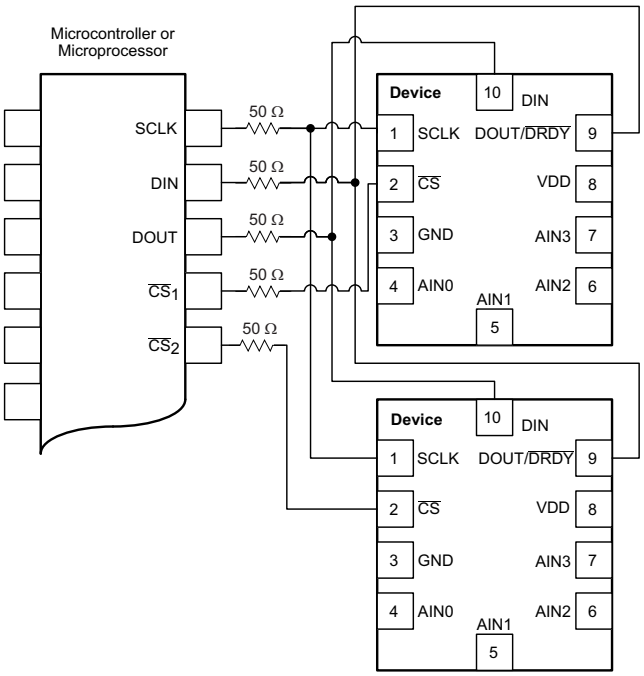
Figure 20. Measuring Single-Ended Inputs

The ADS1018-Q1 also allows AIN3 to serve as a common point for measurements by adjusting the mux configuration. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration, the ADS1018-Q1 operates with inputs where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because negative differential voltages are allowed when GND < $V_{(AIN3)}$ < VDD; however, common-mode noise attenuation is not offered.

Application Information (continued)

9.1.5 Connecting Multiple Devices

When connecting multiple ADS1018-Q1 devices to a single SPI bus, SCLK, DIN, and DOUT/$\overline{\text{DRDY}}$ can be safely shared by using a dedicated chip-select ($\overline{\text{CS}}$) for each SPI-enabled device. By default, when $\overline{\text{CS}}$ goes high for the ADS1018-Q1, DOUT/$\overline{\text{DRDY}}$ is pulled up to VDD by a weak pullup resistor. This feature prevents DOUT/$\overline{\text{DRDY}}$ from floating near midrail and causing excess current leakage on a microcontroller input. If the PULL_UP_EN bit in the Config register is set to 0, the DOUT/$\overline{\text{DRDY}}$ pin enters a 3-state mode when $\overline{\text{CS}}$ transitions high. The ADS1018-Q1 cannot issue a data-ready pulse on DOUT/$\overline{\text{DRDY}}$ when $\overline{\text{CS}}$ is high. To evaluate when a new conversion is ready from the ADS1018-Q1 when using multiple devices, the master can periodically drop $\overline{\text{CS}}$ to the ADS1018-Q1. When $\overline{\text{CS}}$ goes low, the DOUT/$\overline{\text{DRDY}}$ pin immediately drives either high or low. If the DOUT/$\overline{\text{DRDY}}$ line drives low on a low $\overline{\text{CS}}$, new data are currently available for clocking out at any time. If the DOUT/$\overline{\text{DRDY}}$ line drives high, no new data are available and the ADS1018-Q1 returns the last read conversion result. Valid data can be retrieved from the ADS1018-Q1 at anytime without concern of data corruption. If a new conversion becomes available during data transmission, that conversion is not available for readback until a new SPI transmission is initiated.



NOTE: Power and input connections omitted for clarity.

Figure 21. Connecting Multiple ADS1018-Q1s

Application Information (continued)

9.1.6 Pseudo Code Example

The flow chart in Figure 22 shows a pseudo-code sequence with the required steps to set up communication between the device and a microcontroller to take subsequent readings from the ADS1018-Q1. As an example, the default Config register settings are changed to set up the device for FSR = ±0.512 V, continuous-conversion mode, and a 920-SPS data rate.

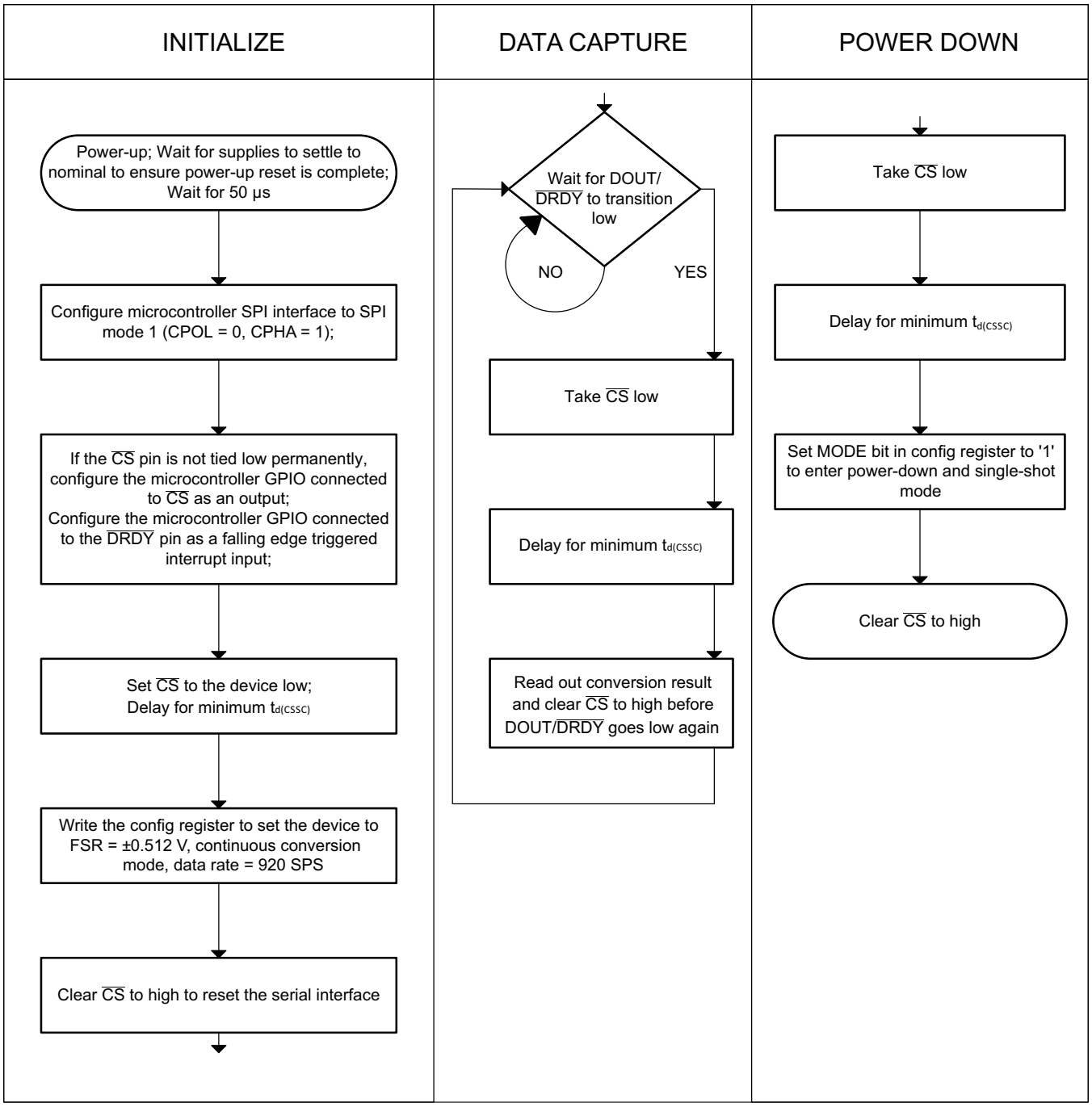


Figure 22. Pseudo-Code Example Flowchart

9.2 Typical Application

Figure 23 shows the basic connections for an independent, two-channel thermocouple measurement system when using the internal high-precision temperature sensor for cold-junction compensation. Apart from the thermocouples, the only external circuitry required are biasing resistors; first-order, low-pass, antialiasing filters; and a power-supply decoupling capacitor.

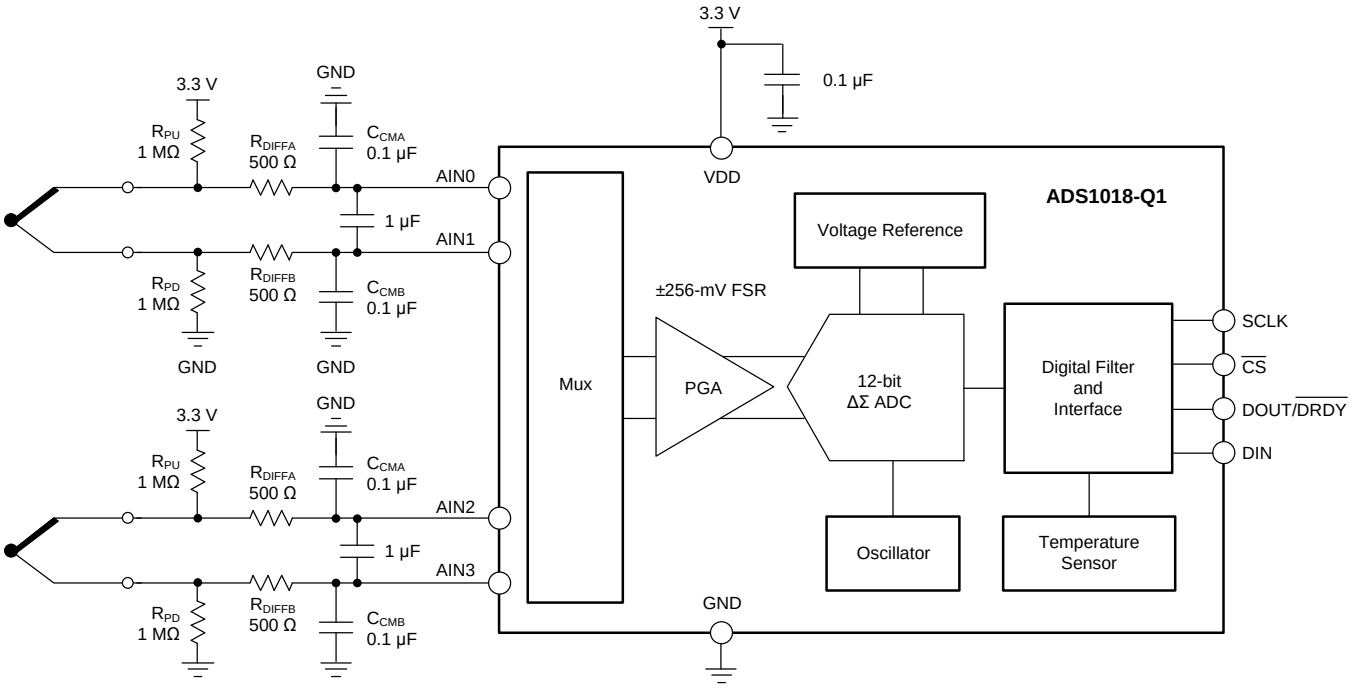


Figure 23. Two-Channel Thermocouple Measurement System

9.2.1 Design Requirements

Table 6 shows the design parameters for this application.

Table 6. Design Parameters

DESIGN PARAMETER	VALUE
Supply voltage	3.3 V
Full-scale range	±0.256 V
Update rate	≥ 100 readings per second
Thermocouple type	K
Temperature measurement range	–200°C to +1250°C
Measurement accuracy at T_A = 25°C(1)	±2.7°C

(1) With offset calibration, and no gain calibration. Measurement does not account for thermocouple inaccuracy.

9.2.2 Detailed Design Procedure

The biasing resistors (R_{PU} and R_{PD}) serve two purposes. The first purpose is to set the common-mode voltage of the thermocouple to within the specified voltage range of the device. The second purpose is to offer a weak pullup and pulldown to detect an open thermocouple lead. When one of the thermocouple leads fails open, the positive input is pulled to VDD and the negative input is pulled to GND. The ADC consequently reads a full-scale value that is outside the normal measurement range of the thermocouple voltage to indicate this failure condition. When choosing the values of the biasing resistors, take care so that the biasing current does not degrade measurement accuracy. The biasing current flows through the thermocouple and can cause self-heating and additional voltage drops across the thermocouple leads. Typical values for the biasing resistors range from 1 MΩ to 50 MΩ.

Although the device digital filter attenuates high-frequency components of noise, provide a first-order, passive RC filter at the inputs to further improve performance. The differential RC filter formed by R_{DIFFA}, R_{DIFFB}, and the differential capacitor C_{DIFF} offers a cutoff frequency that is calculated using Equation 3. While the digital filter of the ADS1018-Q1 strongly attenuates high-frequency components of noise, provide a first-order, passive RC filter to further suppress high-frequency noise and avoid aliasing. Care must be taken when choosing the filter resistor values because the input currents flowing into and out of the device cause a voltage drop across the resistors. This voltage drop shows up as an additional offset error at the ADC inputs. Limit the filter resistor values to below 1 kΩ for best performance.

$$f_C = 1 / [2\pi \cdot (R_{DIFFA} + R_{DIFFB}) \cdot C_{DIFF}] \quad (3)$$

Two common-mode filter capacitors (C_{CMA} and C_{CMB}) are also added to offer attenuation of high-frequency, common-mode noise components. Differential capacitor C_{DIFF} must be at least an order of magnitude (10x) larger than these common-mode capacitors because mismatches in the common-mode capacitors can convert common-mode noise into differential noise.

The highest measurement resolution is achieved when the largest potential input signal is slightly lower than the FSR of the ADC. From the design requirement, the maximum thermocouple voltage (V_{TC}) occurs at a thermocouple temperature (T_{TC}) of 1250°C. At this temperature, V_{TC} = 50.644 mV, as defined in the tables published by the National Institute of Standards and Technology (NIST) using a cold-junction temperature (T_{CJ}) of 0°C. A thermocouple produces an output voltage that is proportional to the temperature difference between the thermocouple tip and the cold junction. If the cold junction is at a temperature below 0°C, the thermocouple produces a voltage larger than 50.644 mV. The isothermal block area is constrained by the operating temperature range of the device. Therefore, the isothermal block temperature is limited to –40°C. A K-type thermocouple at T_{TC} = 1250°C produces an output voltage of V_{TC} = 50.644 mV – (–1.527 mV) = 52.171 mV when referenced to a cold-junction temperature of T_{CJ} = –40°C. The device offers a full-scale range of ±0.256 V and that is what is used in this application example.

The device integrates a high-precision temperature sensor that can be used to measure the temperature of the cold junction. The temperature sensor mode is enabled by setting bit TS_MODE = 1 in the Config register. The accuracy of the overall temperature sensor depends on how accurately the ADS1018-Q1 can measure the cold junction, and hence, careful component placement and PCB layout considerations must be employed for designing an accurate thermocouple system. The ADS1118 Evaluation Module provides a good starting point and offers an example to achieve good cold-junction compensation performance. The ADS1118 Evaluation Module uses the same schematic as shown in Figure 23, except with only one thermocouple channel connected. Refer to the application note, *Precision Thermocouple Measurement With the ADS1118*, SBAA189, for details on how to optimize your component placement and layout to achieve good cold-junction compensation performance.

The calculation procedure to achieve cold-junction compensation can be done in several ways. A typical way is to interleave readings between the thermocouple inputs and the temperature sensor. That is, acquire one on-chip temperature result, T_{CJ}, for every thermocouple ADC voltage measured, V_{TC}. To account for the cold junction, first convert the temperature sensor reading within the ADS1018-Q1 to a voltage (V_{CJ}) that is proportional to the thermocouple currently being used. This process is generally accomplished by performing a reverse lookup on the table used for the thermocouple voltage-to-temperature conversion. Adding these two voltages yields the thermocouple-compensated voltage (V_{Actual}), where $V_{Actual} = V_{CJ} + V_{TC}$. V_{Actual} is then converted to a temperature (T_{Actual}) using the same NIST lookup table. A block diagram showing this process is given in Figure 24. Refer to the application note, *Precision Thermocouple Measurement With the ADS1118*, SBAA189, for a detailed explanation of this method.

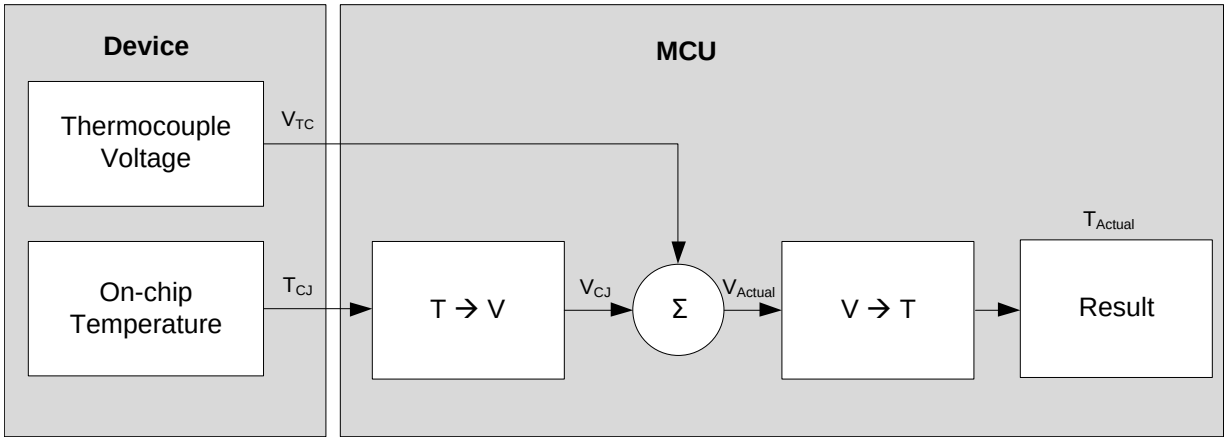


Figure 24. Software-Flow Block Diagram

Figure 25 and Figure 26 show the expected measurement results. A system offset calibration is performed at T_{TC} = 25°C that equates to V_{TC} = 0 V when T_{CJ} = 25°C. The dashed blue lines in Figure 25 show the maximum error guard band due to ADC gain and nonlinearity error. The dashed blue lines in Figure 26 show the corresponding temperature measurement error guard band calculated from the data in Figure 25 using the NIST tables. The dashed red lines in Figure 26 include the guard band for the temperature sensor inaccuracy (±1°C), in addition to the device gain and nonlinearity error. Note that the results in Figure 25 and Figure 26 do not account for the thermocouple inaccuracy that must also be considered while designing a thermocouple measurement system.

9.2.3 Application Curves

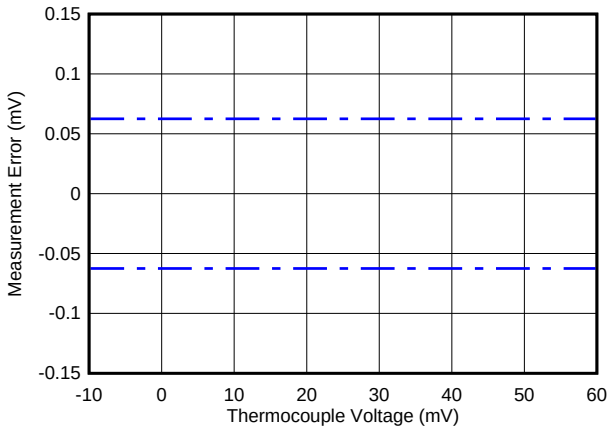


Figure 25. Voltage Measurement Error vs V_{TC}

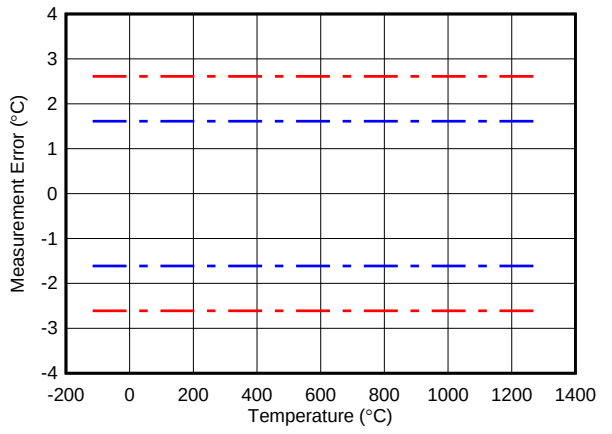


Figure 26. Temperature Measurement Error vs T_{TC}

10 Power-Supply Recommendations

The device requires a single power supply, VDD, to power both the analog and digital circuitry of the device.

10.1 Power-Supply Sequencing

Wait approximately 50 µs after VDD is stabilized before communicating with the device to allow the power-up reset process to complete.

10.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. VDD must be decoupled with at least a 0.1-µF capacitor, as shown in Figure 27. The 0.1-µF bypass capacitor supplies the momentary bursts of extra current required from the supply when the ADS1018-Q1 is converting. Place the bypass capacitor as close to the power-supply pin of the device as possible using low-impedance connections. For best performance, use multilayer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

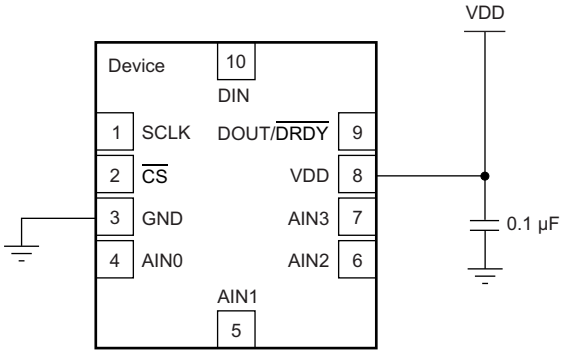


Figure 27. Power Supply Decoupling

11 Layout

11.1 Layout Guidelines

Use best design practices when laying out a printed-circuit-board (PCB) for both analog and digital components. This recommendation generally means that the layout separates analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog muxes] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 28. Although Figure 28 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog component.

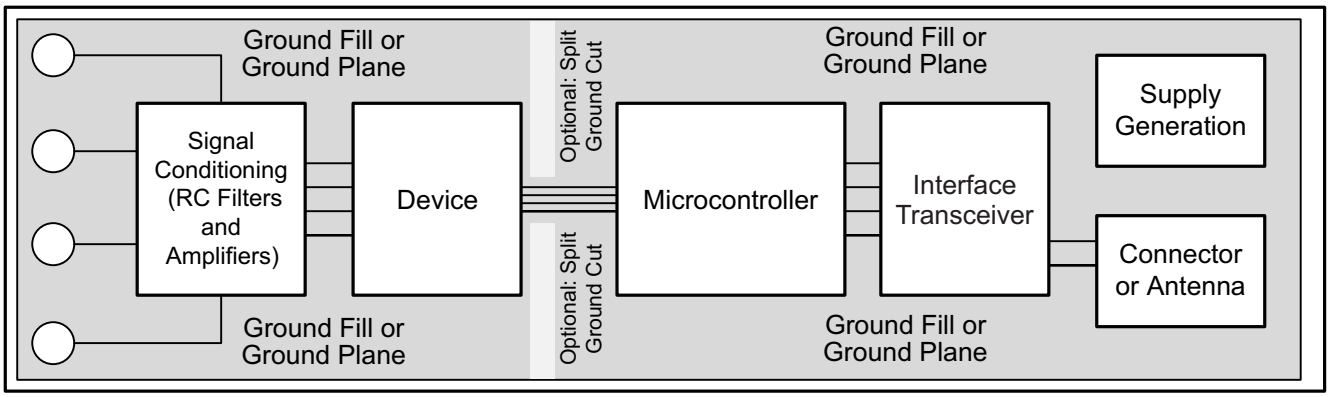


Figure 28. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, TI generally recommends that the ground planes be connected together as close to the device as possible. A two-layer board is possible using common grounds for both analog and digital grounds. Additional layers can be added to simplify PCB trace routing. Ground fill may also reduce EMI and RFI issues.

For best system performance, keep digital components, especially RF portions, as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid placing these traces near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature-sensing functions are much more significant than for ADC functions.

Bypass supply pins to ground with a low-ESR ceramic capacitor. The optimum placement of the bypass capacitors is as close as possible to the supply pins. The ground-side connections of the bypass capacitors must be low-impedance connections for optimum performance. The supply current flows through the bypass capacitor terminal first and then to the supply pin to make the bypassing most effective.

Analog inputs with differential connections must have a capacitor placed differentially across the inputs. Use high-quality differential capacitors. The best ceramic-chip capacitors are C0G (NPO), with stable properties and low-noise characteristics. Thermally isolate a copper region around the thermocouple input connections to create a thermally-stable cold junction. Obtaining acceptable performance with alternate layout schemes is possible as long as the above guidelines are followed.

11.2 Layout Example

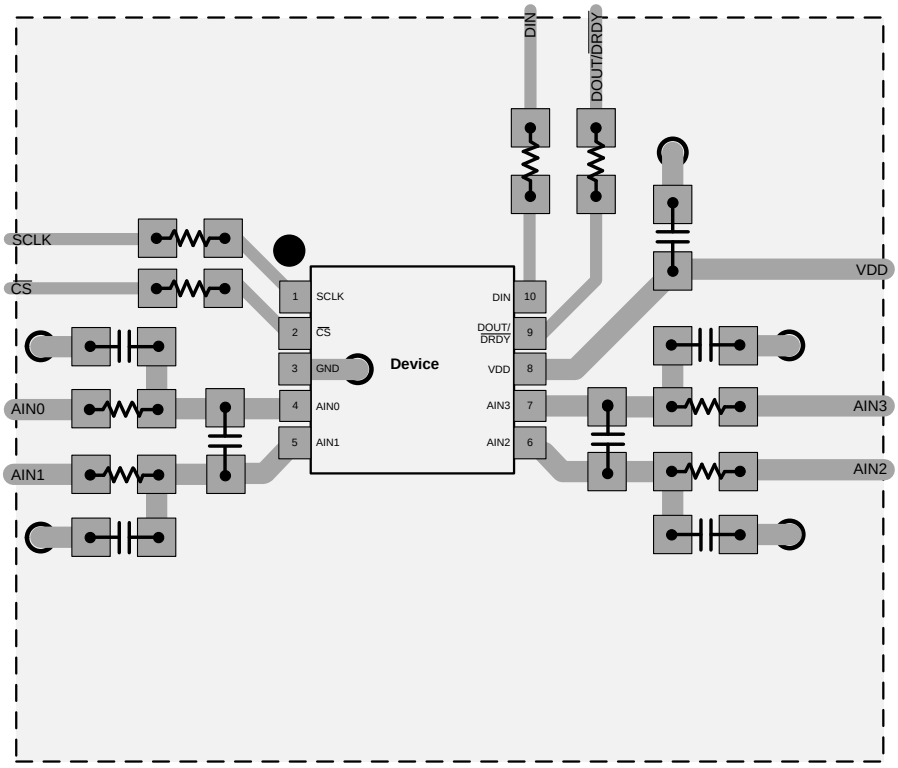


Figure 29. VSSOP Package

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

- 《使用 ADS1118 进行精密热电偶测量》，SBAA189
- 《ADS1118EVM 用户指南》，SBAU184
- 《430BOOST-ADS1118 BoosterPack 用户指南》，SBAU207
- 《ADS1118 Boosterpack》，SLYU013
- 《模数转换规范及性能特性术语表》，SBAA147

12.2 社区资源

下列链接提供到 TI 社区资源的连接。 链接的内容由各个分销商“按照原样”提供。 这些内容并不构成 TI 技术规范和标准且不一定反映 TI 的观点；请见 TI 的使用条款。

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1018QDGSRQ1	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZFOV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

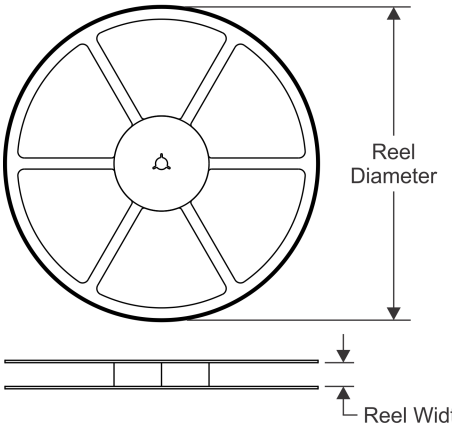
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

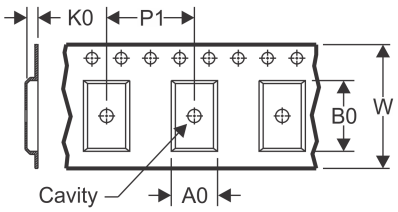
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

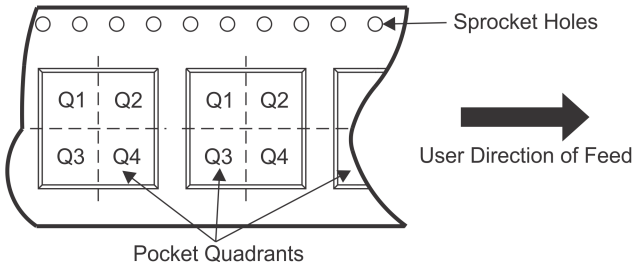


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

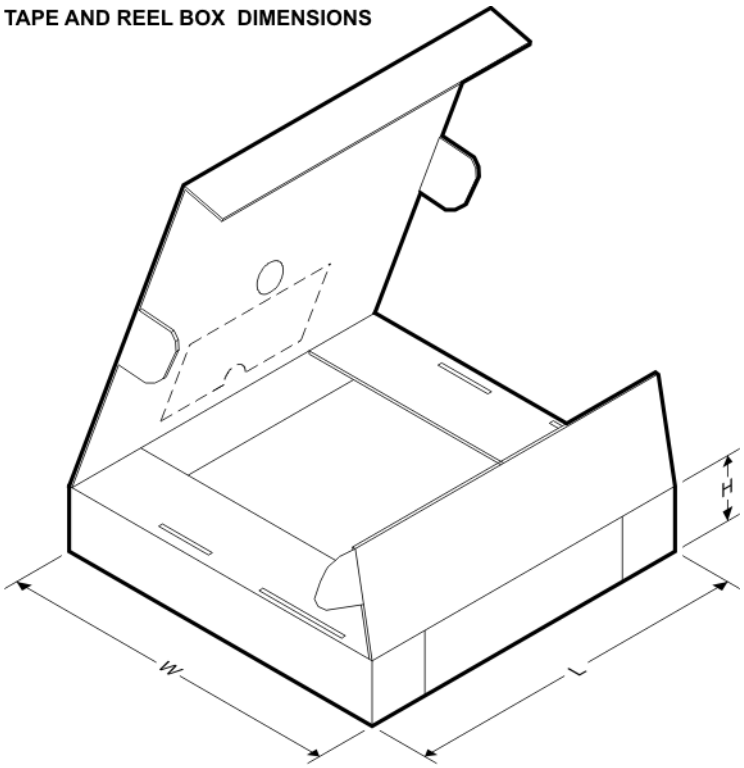
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1018QDGSRQ1	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

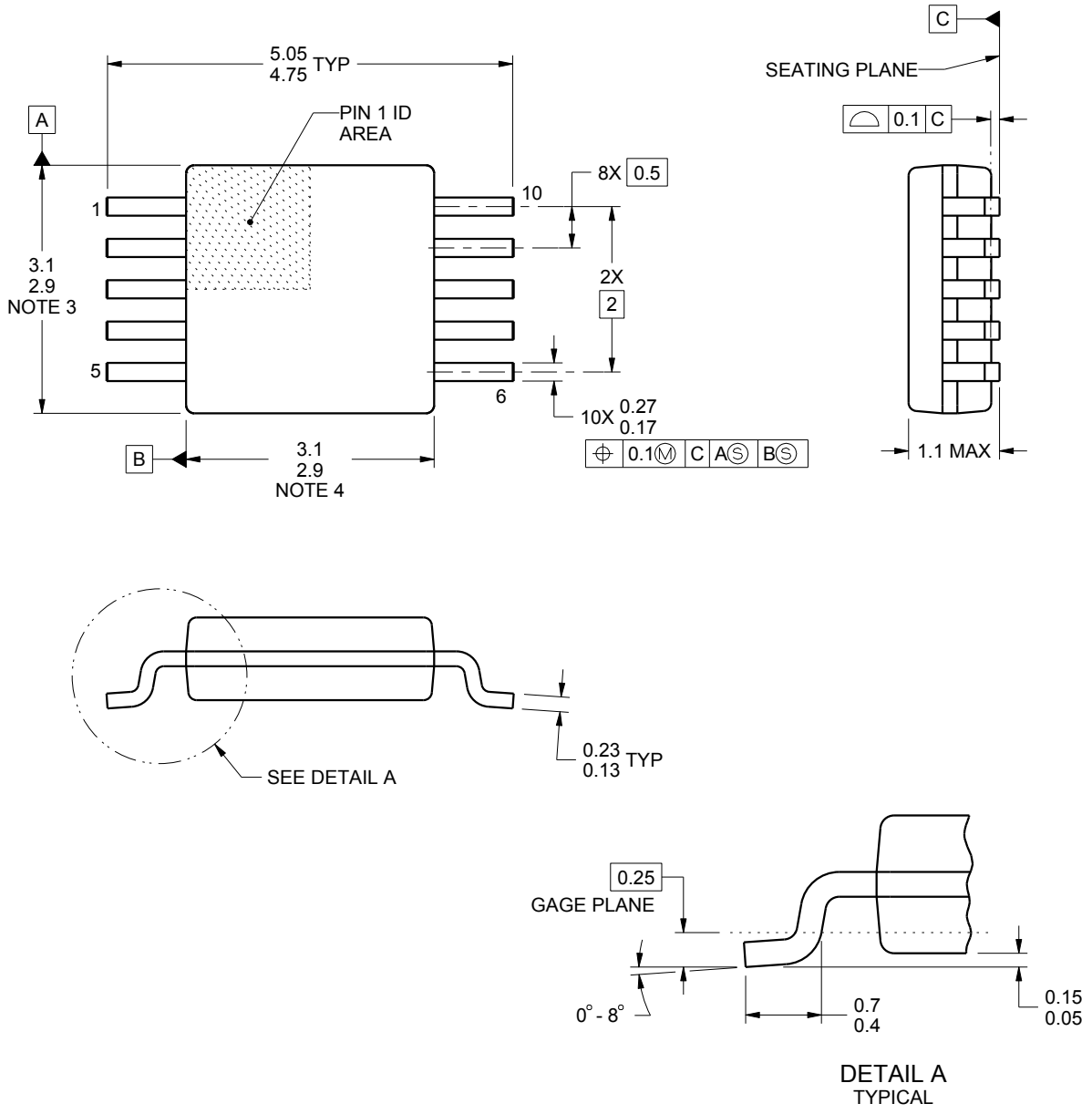
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1018QDGSRQ1	VSSOP	DGS	10	2500	366.0	364.0	50.0

PACKAGE OUTLINE

DGS0010A

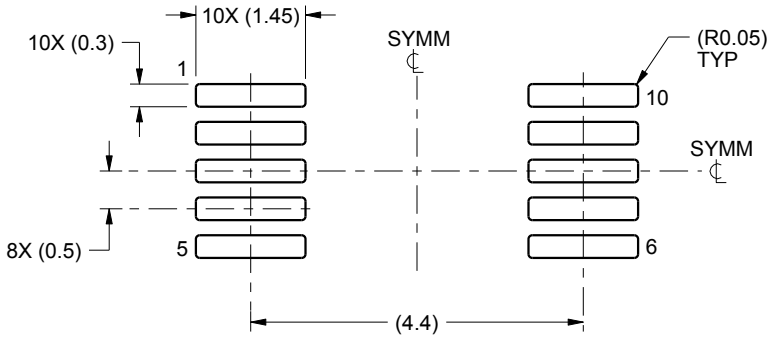
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

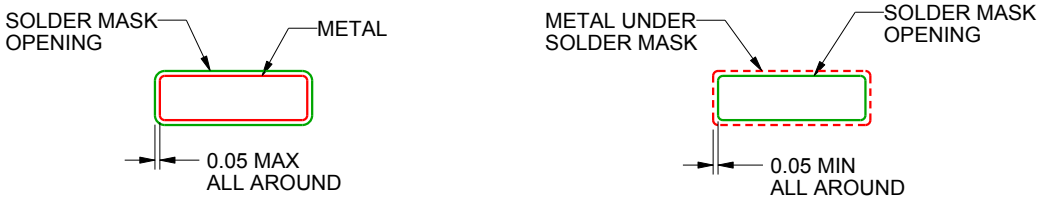


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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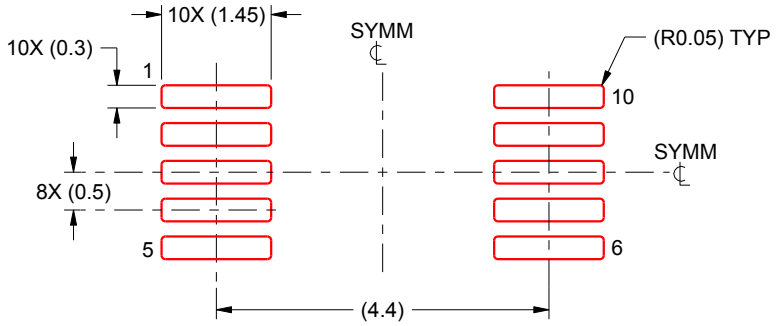
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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