

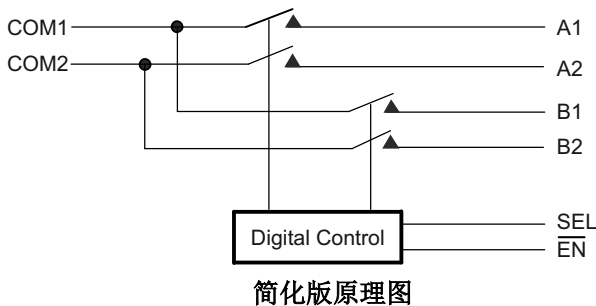
具有断电隔离功能的 TMUX136 6GHz 2 通道 2:1 开关

1 特性

- V_{CC} 范围为 2.3V 至 4.8V
- 高性能开关特性：
 - 带宽 (- 3dB) : 6.1GHz
 - R_{ON} (典型值) : 5.7 Ω
 - C_{ON} (典型值) : 1.6pF
- 电流消耗 : 30 μ A (典型值)
- 特殊特性：
 - I_{OFF} 保护可防止在断电状态下产生泄漏电流
 - 1.8V 兼容控制输入 (SEL、 \overline{EN})
- 静电放电 (ESD) 性能：
 - 5kV 人体放电模型 (A114B , II 类)
 - 1kV 带电器件模型 (C101)
- 紧凑型 10 引脚 UQFN 封装
(1.5mm \times 2mm , 间距为 0.5mm)

2 应用

- 手持终端：智能手机
- 笔记本电脑
- 平板电脑：多媒体
- 电子销售终端
- 现场仪器
- 便携式监视器



3 说明

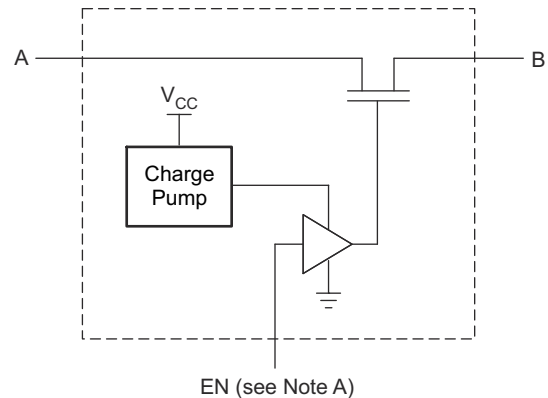
TMUX136 器件是一款高性能 6GHz 2 通道 2:1 开关，同时支持差动和单端信号。该器件具有 2.3V 至 4.8V 的较宽 V_{CC} 范围，支持断电保护功能，当 V_{CC} 引脚断电时，强制所有 I/O 引脚进入高阻抗模式。TMUX136 的部分引脚支持 1.8V 控制电压，允许它们直接与低电压处理器的通用 I/O (GPIO) 相连。

TMUX136 采用小型 10 引脚 UQFN 封装，尺寸仅为 1.5mm \times 2mm，非常适合 PCB 面积有限的情况。

器件信息

器件型号 (1)	封装	封装尺寸 (标称值)
TMUX136	UQFN (10)	1.50mm \times 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



Note A: EN is the internal enable signal applied to the switch.

功能方框图



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4 Revision History

Changes from Revision C (July 2018) to Revision D (August 2020)	Page
• Added new specification limits to support added temperature range $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	4

Changes from Revision B (November 2017) to Revision C (July 2018)	Page
• Changed pin 6 To: $\overline{\text{EN}}$, pin 7 To: COM2, and pin 8 To: COM1 in 图 11-2	18

Changes from Revision A (October 2017) to Revision B (November 2017)	Page
• Changed Pin 7 From: COM1 To: COM2.....	3
• Changed Pin 8 From: COM2 To: COM1.....	3

Changes from Revision * (August 2017) to Revision A (October 2017)	Page
• Changed the HBM value From: ± 3500 To: ± 5000 in the <i>ESD Ratings</i> table.....	4

5 Pin Configuration and Functions

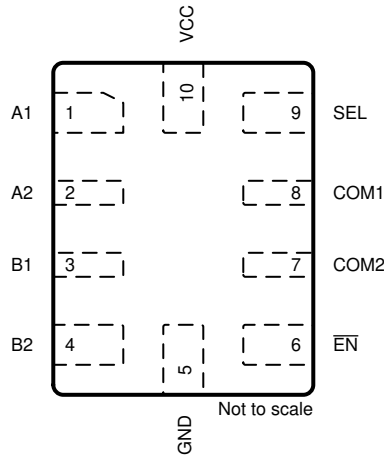


图 5-1. RSE Package 10 Pin (UQFN) Top View

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A1	I/O	Signal path A1
2	A2	I/O	Signal path A2
3	B1	I/O	Signal path B1
4	B2	I/O	Signal path B2
5	GND	—	Ground
6	EN	I	Enable (Active Low)
7	COM2	I/O	Common signal path 2
8	COM1	I/O	Common signal path 1
9	SEL	I	Switch select (Logic Low = COM to A PORT Logic High = COM to B PORT)
10	VCC	—	Supply Voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽²⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽³⁾		- 0.3	5.5	V
V _{I/O}	Input-output DC voltage ⁽³⁾		- 0.3	5.5	V
V _{SEL} , V _{EN}	Digital input voltage (SEL, \bar{EN})		- 0.3	5.5	V
I _K	Input-output port diode current	V _{I/O} < 0	- 50		mA
I _{IK}	Digital logic input clamp current ⁽³⁾	V _I < 0	- 50		mA
I _{CC}	Continuous current through VCC			100	mA
I _{GND}	Continuous current through GND		- 100		mA
T _{stg}	Storage temperature		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±5000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{CC}	Supply voltage		2.3	4.8	V
V _{I/O}	Analog voltage		0	3.6	V
V _{SEL} , V _{EN}	Digital input voltage (SEL, \bar{EN})		0	V _{CC}	V
T _{RAMP} (V _{CC})	Power supply ramp time requirement (V _{CC})		100	1000	μs/V
I _{I/O}	Continuous current through I/O signal path (COMx, Ax, Bx) T _A = - 40°C to +85°C			±20	mA
I _{I/O}	Continuous current through I/O signal path (COMx, Ax, Bx) T _A = - 40°C to +125°C			±10	mA
T _A	Operating free-air temperature		- 40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TMUX136	UNIT
		RSE (UQFN)	
		10 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	191.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	94.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	117.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ _{JB}	Junction-to-board characterization parameter	117.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

T_A = -40°C to +85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
A PORT SWITCH						
R _{ON} ON-state resistance	V _{CC} = 2.7 V	V _{I/O} = 1.65 V, I _{ON} = -8 mA	5.7	9		Ω
	V _{CC} = 2.3 V	V _{I/O} = 1.65 V, I _{ON} = -8 mA	5.7	9.5		
	V _{CC} = 2.7 V	V _{I/O} = 1.65 V, I _{ON} = -8 mA T _A = -40°C to +125°C		13		
	V _{CC} = 2.3 V	V _{I/O} = 1.65 V, I _{ON} = -8 mA T _A = -40°C to +125°C		13		
ΔR _{ON} ON-state resistance match between signal path 1 and 2	V _{CC} = 2.3 V	V _{I/O} = 1.65 V, I _{ON} = -8 mA	0.1			Ω
R _{ON (FLAT)} ON-state resistance flatness	V _{CC} = 2.3 V	V _{I/O} = 1.65 V to 3.45 V, I _{ON} = -8 mA		1		Ω
I _{OZ} OFF leakage current	V _{CC} = 4.8 V	Switch OFF, V _B = 1.65 V to 3.45 V, V _{COM} = 0 V	-2		2	μA
		Switch OFF, V _B = 1.65 V to 3.45 V, V _{COM} = 0 V T _A = -40°C to +125°C	-15		15	
I _{OFF} Power-off leakage current	V _{CC} = 0 V	Switch ON or OFF, V _B = 1.65 V to 3.45 V, V _{COM} = NC	-10		10	μA
		Switch ON or OFF, V _B = 1.65 V to 3.45 V, V _{COM} = NC T _A = -40°C to +125°C	-50		50	
I _{ON} ON leakage current	V _{CC} = 4.8 V	Switch ON, V _B = 1.65 V to 3.45 V, V _{COM} = NC	-2		2	μA
		Switch ON, V _B = 1.65 V to 3.45 V, V _{COM} = NC T _A = -40°C to +125°C	-15		15	
	V _{CC} = 2.3 V	Switch ON, V _B = 1.65 V to 3.45 V, V _{COM} = NC	-	125	125	
		Switch ON, V _B = 1.65 V to 3.45 V, V _{COM} = NC T _A = -40°C to +125°C	-175		175	
B PORT SWITCH						
R _{ON} ON-state resistance	V _{CC} = 2.3 V	V _{I/O} = 0.4 V, I _{ON} = -8 mA	4.6	7.5		Ω
		V _{I/O} = 0.4 V, I _{ON} = -8 mA		12		
		T _A = -40°C to +125°C				

T_A = -40°C to +85°C, Typical values are at V_{CC} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔR _{ON}	ON-state resistance match between signal path 1 and 2	V _{CC} = 2.3 V	V _{I/O} = 0.4 V, I _{ON} = -8 mA		0.1		Ω
R _{ON} (FLAT)	ON-state resistance flatness	V _{CC} = 2.3 V	V _{I/O} = 0 V to 0.4 V, I _{ON} = -8 mA		1		Ω
I _{OZ}	OFF leakage current	V _{CC} = 4.8 V	Switch OFF, V _A = 0 V to 3.6 V, V _{COM} = 0 V	-2		2	μA
			Switch OFF, V _A = 0 V to 3.6 V, V _{COM} = 0 V T _A = -40°C to +125°C	-15		15	
I _{OFF}	Power-off leakage current	V _{CC} = 0 V	Switch ON or OFF, V _A = 0 V to 3.6 V, V _{COM} = NC	-10		10	μA
			Switch ON or OFF, V _A = 0 V to 3.6 V, V _{COM} = NC T _A = -40°C to +125°C	-50		50	
I _{ON}	ON leakage current	V _{CC} = 4.8 V	Switch ON, V _A = 0 V to 3.6 V, V _{D±} = NC	-2		2	μA
		V _{CC} = 4.8 V	Switch ON, V _A = 0 V to 3.6 V, V _{D±} = NC T _A = -40°C to +125°C	-15		15	
		V _{CC} = 2.3 V	Switch ON, V _A = 0 V to 3.6 V, V _B = NC	-125		125	
		V _{CC} = 2.3 V	Switch ON, V _A = 0 V to 3.6 V, V _B = NC T _A = -40°C to +125°C	-175		175	
DIGITAL CONTROL INPUTS (SEL, EN)							
V _{IH}	Input logic high	V _{CC} = 2.3 V to 4.8 V T _A = -40°C to +125°C		1.3			V
V _{IL}	Input logic low	V _{CC} = 2.3 V to 4.8 V T _A = -40°C to +125°C				0.6	V
I _{IN}	Input leakage current	V _{CC} = 4.8 V, V _{I/O} = 0 V to 3.6 V, V _{IN} = 0 to 4.8 V		-10		10	μA

6.6 Dynamic Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C _{ON}	PORT B ON capacitance	V _{CC} = 3.3 V, V _{I/O} = 0 or 3.3 V, f = 240 MHz	Switch ON		1.6	2	pF
	PORT A ON capacitance	V _{CC} = 3.3 V, V _{I/O} = 0 or 3.3 V, f = 240 MHz	Switch ON		1.4	2	pF
C _{OFF}	PORT B OFF capacitance	V _{CC} = 3.3 V, V _{I/O} = 0 or 3.3 V, f = 240 MHz	Switch OFF		1.4	2	pF
	PORT A OFF capacitance	V _{CC} = 3.3 V, V _{I/O} = 0 or 3.3 V, f = 240 MHz	Switch OFF		1.6	2	pF
C _I	Digital input capacitance	V _{CC} = 3.3 V, V _I = 0 or 2 V			2.2		pF
O _{ISO}	OFF Isolation	V _{CC} = 2.3 V to 4.8 V, R _L = 50 Ω, f = 240 MHz	Switch OFF		- 34		dB
X _{TALK}	Crosstalk	V _{CC} = 2.3 V to 4.8 V, R _L = 50 Ω, f = 240 MHz	Switch ON		- 37		dB
BW	- 3-dB bandwidth	V _{CC} = 2.3 V to 4.8 V, R _L = 50 Ω,	Switch ON		6.1		GHz
SUPPLY							
V _{CC}	Power supply voltage			2.3		4.8	V
I _{CC}	Positive supply current	V _{CC} = 4.8 V, V _{IN} = V _{CC} or GND, V _{I/O} = 0 V, Switch ON or OFF			30	50	μA
		V _{CC} = 4.8 V, V _{IN} = V _{CC} or GND, V _{I/O} = 0 V, Switch ON or OFF T _A = - 40°C to +125°C				70	
I _{CC, HZ}	Power supply current in high-Z mode	V _{CC} = 4.8 V, V _{IN} = V _{CC} or GND, V _{I/O} = 0 V, Switch ON or OFF, \overline{OE} = H			5	10	μA
		V _{CC} = 4.8 V, V _{IN} = V _{CC} or GND, V _{I/O} = 0 V, Switch ON or OFF, \overline{OE} = H T _A = - 40°C to +125°C				20	

6.7 Timing Requirements

			MIN	NOM	MAX	UNIT	
t _{pd}	Propagation delay	R _L = 50 Ω, C _L = 5 pF, V _{CC} = 2.3 V to 4.8 V		100		ps	
t _{switch}	Switching time (SEL to output)				600	ns	
t _{ZH, ZL}	Enable time (\overline{EN} to output)		V _{I/O} = 3.3 V or 0 V		100		μs
t _{HZ, LZ}	Disable time (\overline{EN} to output)				200		ns
t _{SK(P)}	Skew of opposite transitions of same output				20		ps

6.8 Typical Characteristics

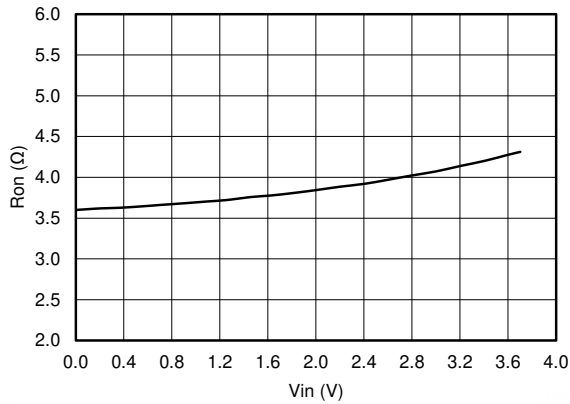


图 6-1. ON-Resistance vs $V_{I/O}$

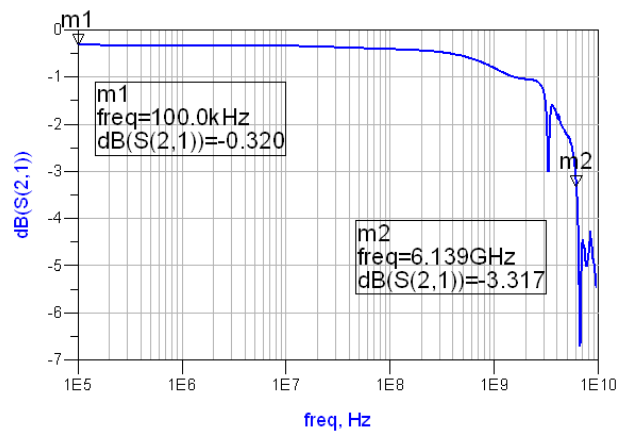


图 6-2. Bandwidth

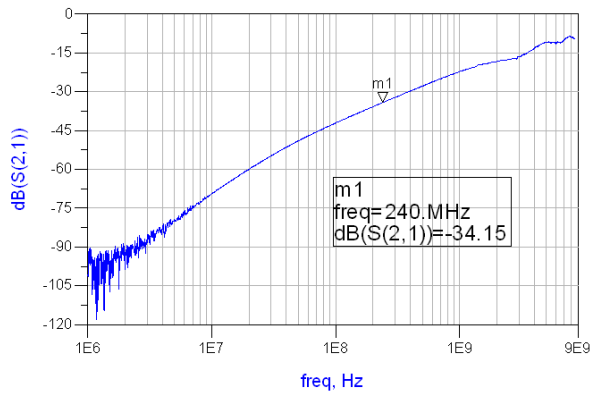


图 6-3. Off Isolation

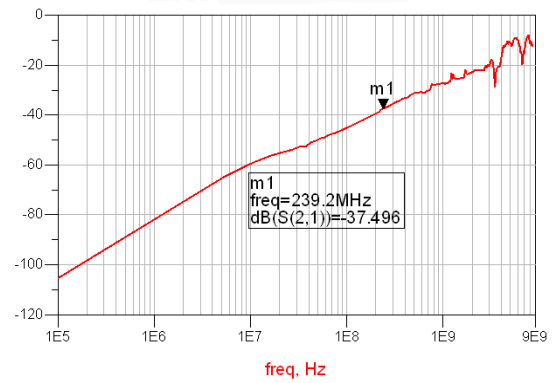
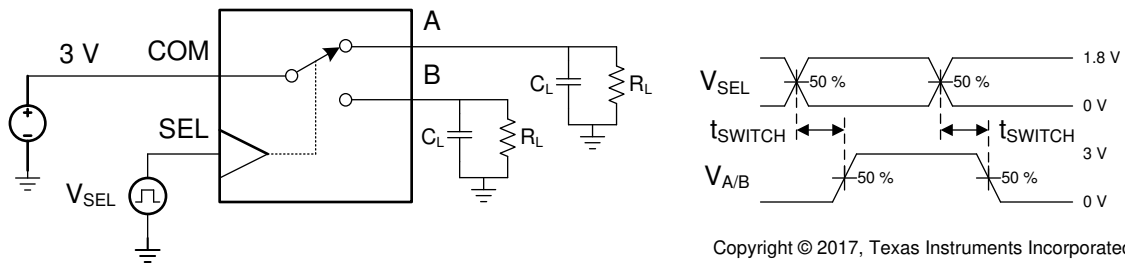


图 6-4. Cross Talk

7 Parameter Measurement Information



- A. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$, $t_r < 5$ ns, $t_f < 5$ ns.
B. C_L includes probe and jig capacitance.

图 7-1. Timing Diagram

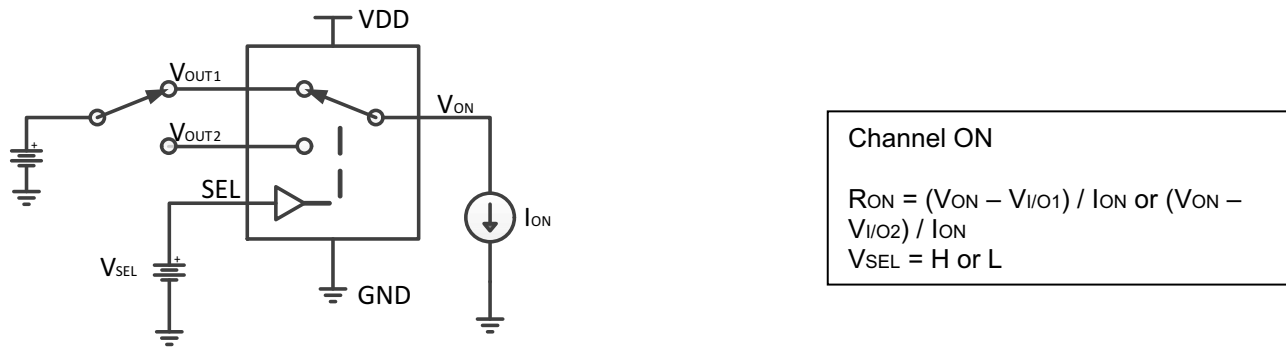


图 7-2. ON-State Resistance (R_{ON})

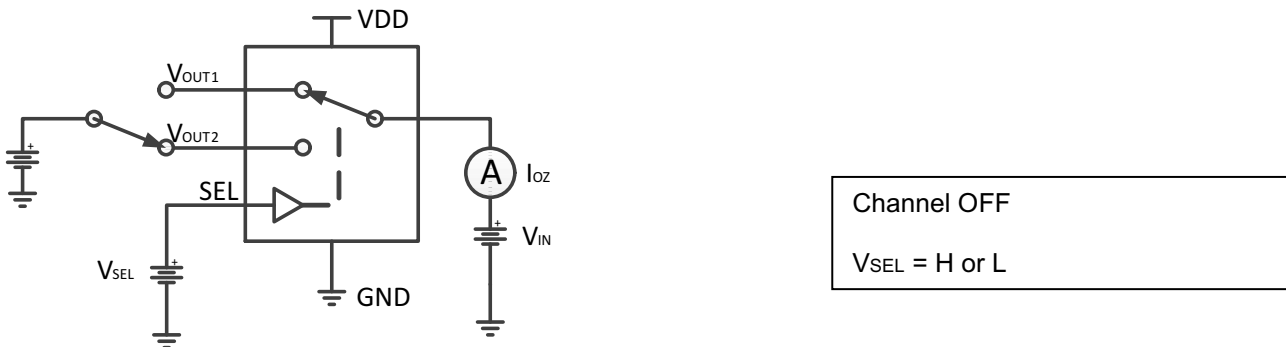
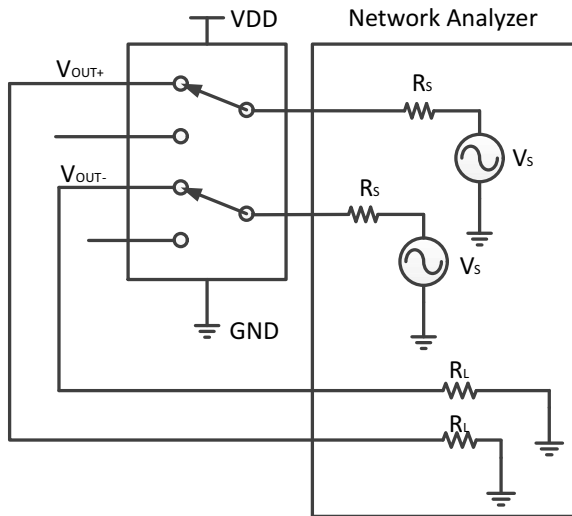


图 7-3. OFF Leakage Current (I_{OZ})



Channel ON
 $V_{SEL} = H$ or L
 $R_S = R_L = 50\Omega$

图 7-4. Bandwidth (BW)

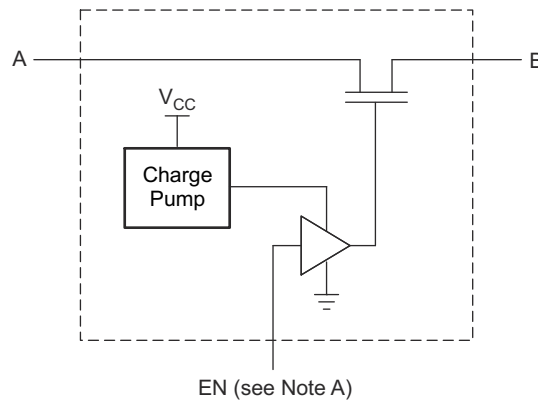
8 Detailed Description

8.1 Overview

The TMUX136 device is a 2-channel, 2:1, switch specifically designed for the switching of high-speed signals in handset and consumer applications, such as cell phones, tablets, and notebooks but may be used for any high speed application. The wide bandwidth (6.1 GHz) of this switch allows signals to pass with minimum edge and phase distortion. The switch is bidirectional and offers little or no attenuation of the high-speed signals at the outputs and will support both single-ended and differential signals. The device also has a low power mode that reduces the power consumption to 5 μ A for portable applications with a battery or limited power budget.

The TMUX136 device integrates ESD protection cells on all pins, is available in a tiny UQFN package (1.5 mm \times 2 mm) and is characterized over the free-air temperature range from -40°C to +125°C.

8.2 Functional Block Diagram



Note A: EN is the internal enable signal applied to the switch.

8.3 Feature Description

8.3.1 Low Power Mode

The TMUX136 has a low power mode that reduces the power consumption to 5 μ A while the device is not in use. To put the device in low power mode and disable the switch, the bus-switch enable pin $\overline{\text{EN}}$ must be supplied with a logic High signal.

8.4 Device Functional Modes

8.4.1 High Impedance Mode

The TMUX136 has a high impedance mode that places all the signal paths in a Hi-Z state while the device is not in use. To put the device in high impedance mode and disable the switch, the bus-switch enable pin $\overline{\text{EN}}$ must be supplied with a logic *High* signal as shown in [表 8-1](#).

表 8-1. Function Table

SEL	EN	SWITCH STATUS
X	High	Both A PORT and B PORT switches in High-Z
Low	Low	COM to A PORT
High	Low	COM to B PORT

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

There are many applications in which microprocessors or controllers have a limited number of I/Os. The TMUX136 solution can effectively expand the limited I/Os by switching between multiple buses in order to interface them to a single microprocessor or controller.

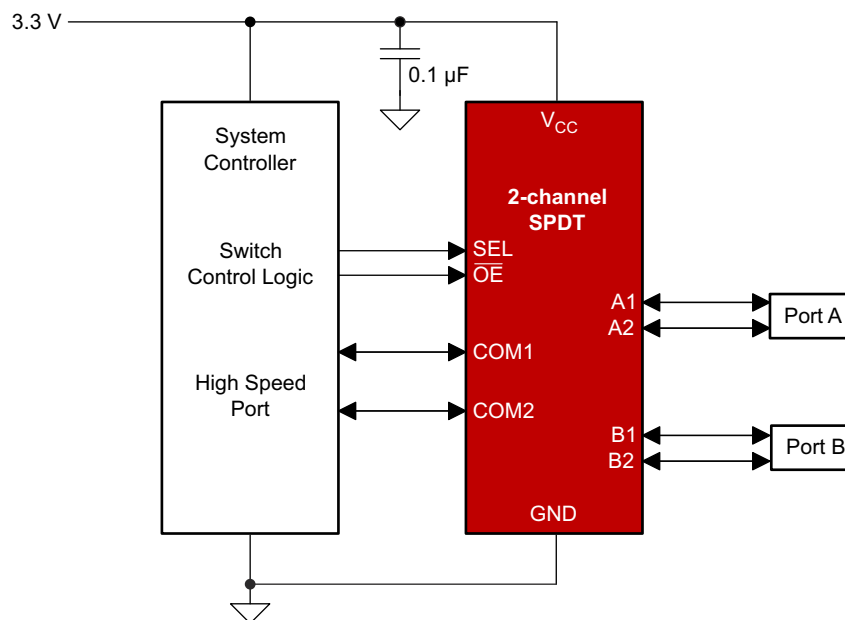


图 9-1. Typical Application

9.2.1 Design Requirements

The TMUX136 has internal 6-M Ω pull-down resistors on SEL and \overline{EN} , so no external resistors are required on the logic pins. The internal pull-down resistor on SEL ensures PORT A channel is selected by default. The internal pull-down resistor on \overline{EN} enables the switch when power is applied to VCC.

9.2.1.1 Detailed Design Procedure

The TMUX136 can operate without any external components; however, TI recommends that unused pins must be connected to ground through a 50- Ω resistor to prevent signal reflections back into the device.

9.2.2 Application Curves

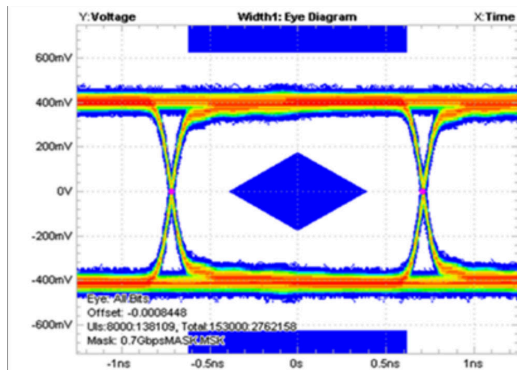


图 9-2. Eye Pattern: 0.7 Gbps with No Device

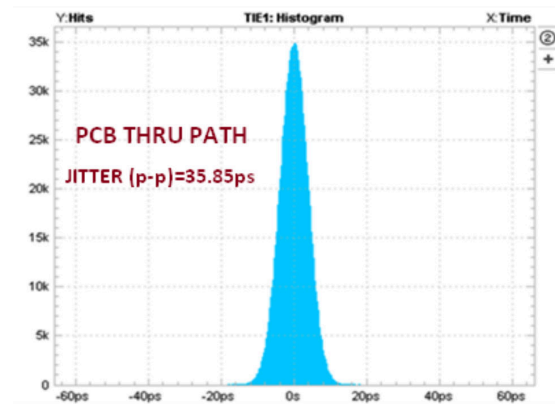
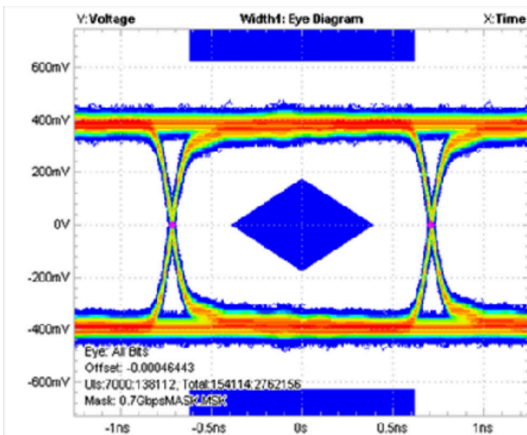
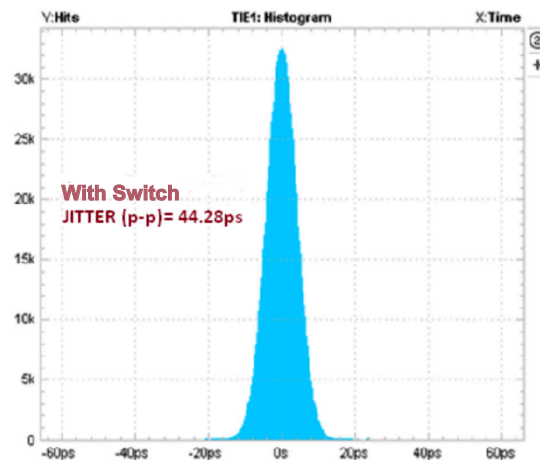


图 9-3. Time Interval Error Histogram: 0.7 Gbps with No Device



The TMUX136 contributes only 8.4 ps of peak-to-peak jitter for 0.7-Gbps data rate

图 9-4. Eye Pattern: 0.7 Gbps with Switch



The TMUX136 contributes only 8.4 ps of peak-to-peak jitter for 0.7-Gbps data rate

图 9-5. Time Interval Error Histogram: 0.7 Gbps with Switch

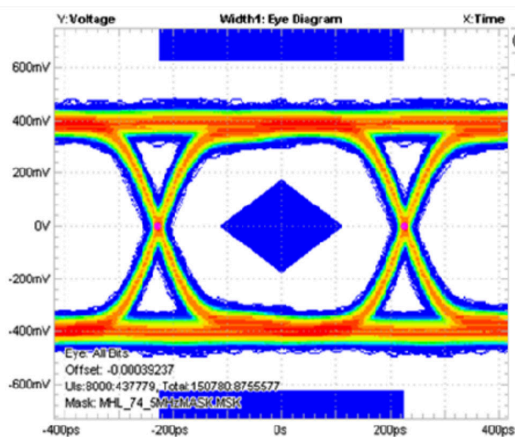


图 9-6. Eye Pattern: 2.2 Gbps with No Device

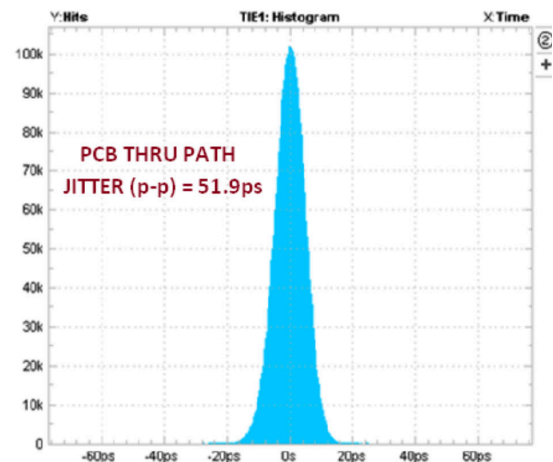
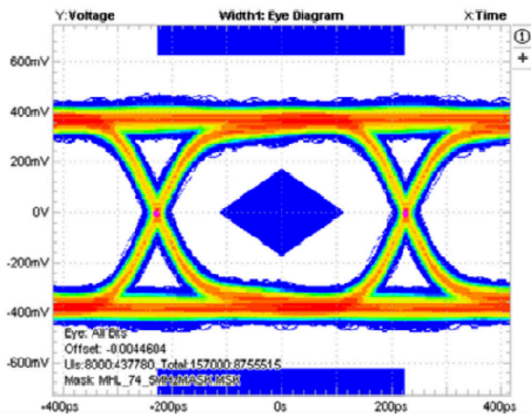
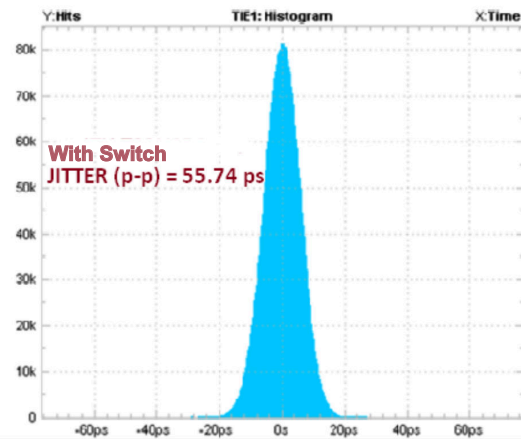


图 9-7. Time Interval Error Histogram: 2.2 Gbps with No Device



The TMUX136 contributes only 3.8 ps of peak-to-peak jitter for 2.2-Gbps data rate

图 9-8. Eye Pattern: 2.2 Gbps with Switch



The TMUX136 contributes only 3.8 ps of peak-to-peak jitter for 2.2-Gbps data rate

图 9-9. Time Interval Error Histogram: 2.2 Gbps with Switch

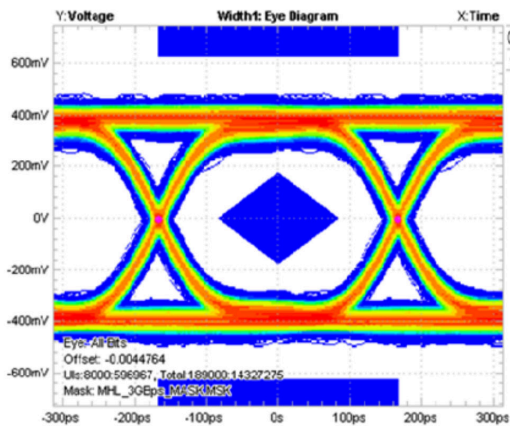


图 9-10. Eye Pattern: 3 Gbps with No Device

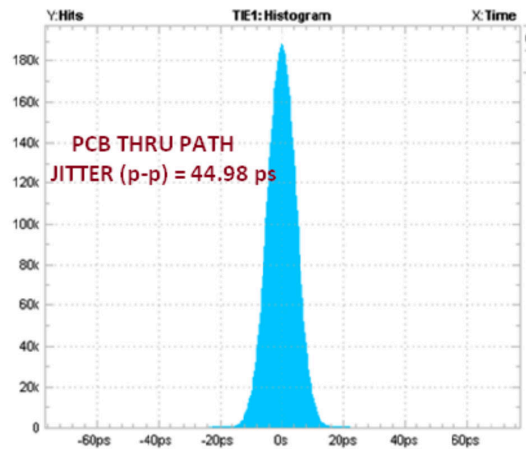
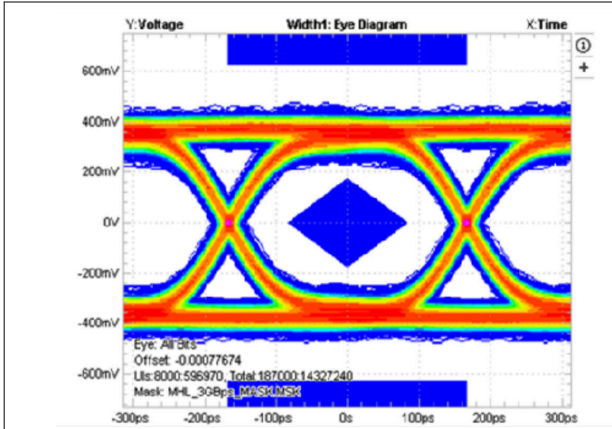
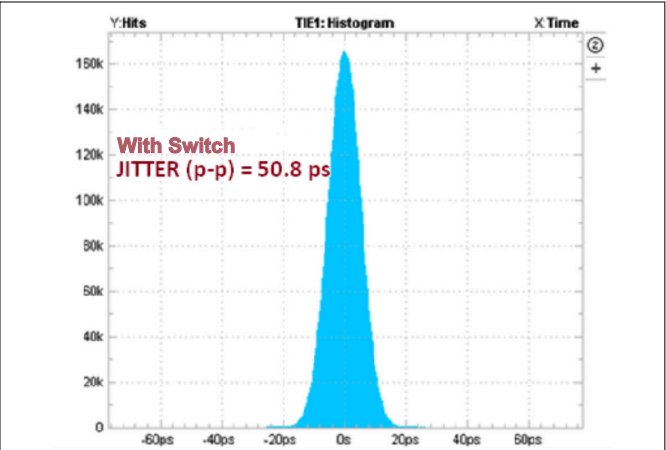


图 9-11. Time Interval Error Histogram: 3 Gbps with No Device



The TMUX136 contributes only 5.8 ps of peak-to-peak jitter for 3-Gbps data rate

图 9-12. Eye Pattern: 3 Gbps with Switch



The TMUX136 contributes only 5.8 ps of peak-to-peak jitter for 3-Gbps data rate

图 9-13. Time Interval Error Histogram: 3 Gbps with Switch

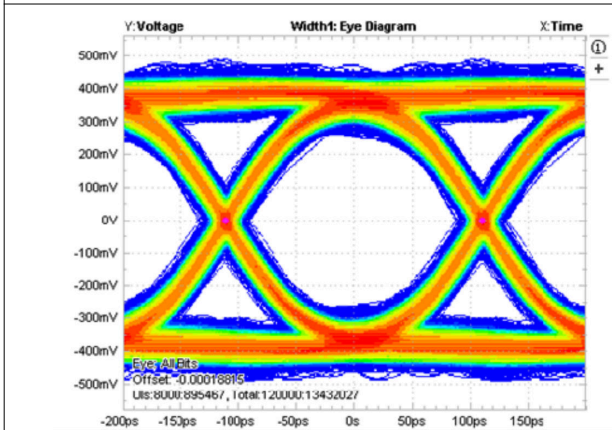


图 9-14. Eye Pattern: 4.5 Gbps with No Device

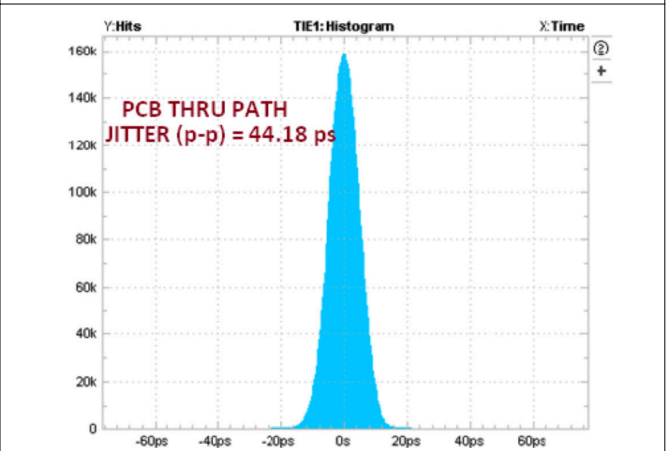
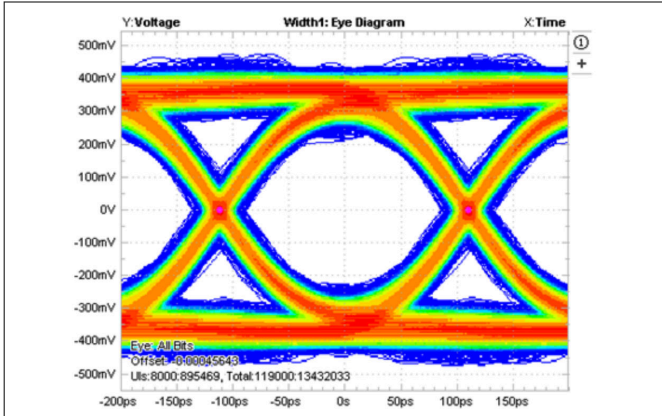
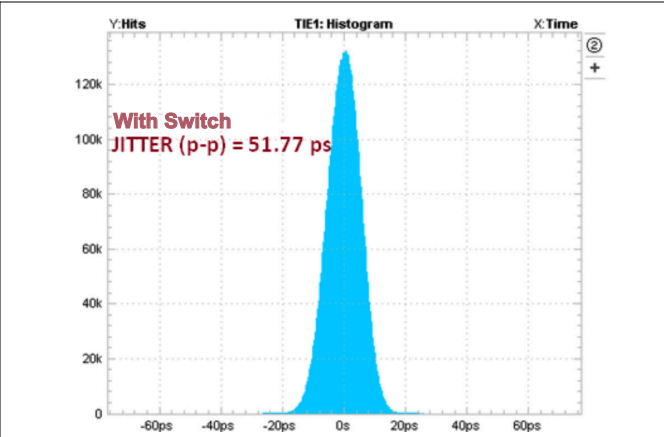


图 9-15. Time Interval Error Histogram: 4.5 Gbps with No Device



The TMUX136 contributes only 7.6 ps of peak-to-peak jitter for 4.5-Gbps data rate

图 9-16. Eye Pattern: 4.5 Gbps with Switch



The TMUX136 contributes only 7.6 ps of peak-to-peak jitter for 4.5-Gbps data rate

图 9-17. Time Interval Error Histogram: 4.5 Gbps with Switch

10 Power Supply Recommendations

TI recommends placing a bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

11 Layout

11.1 Layout Guidelines

Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the high speed traces.

The high-speed signalpaths must should be no more than 4 inches long; otherwise, the eye diagram performance may be degraded.

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed signals traces because they cause signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.

Route all high-speed signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in [图 11-1](#).

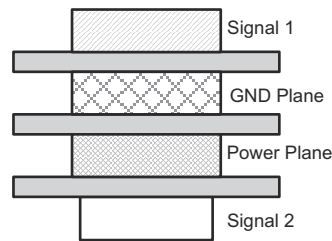


图 11-1. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

11.2 Layout Example

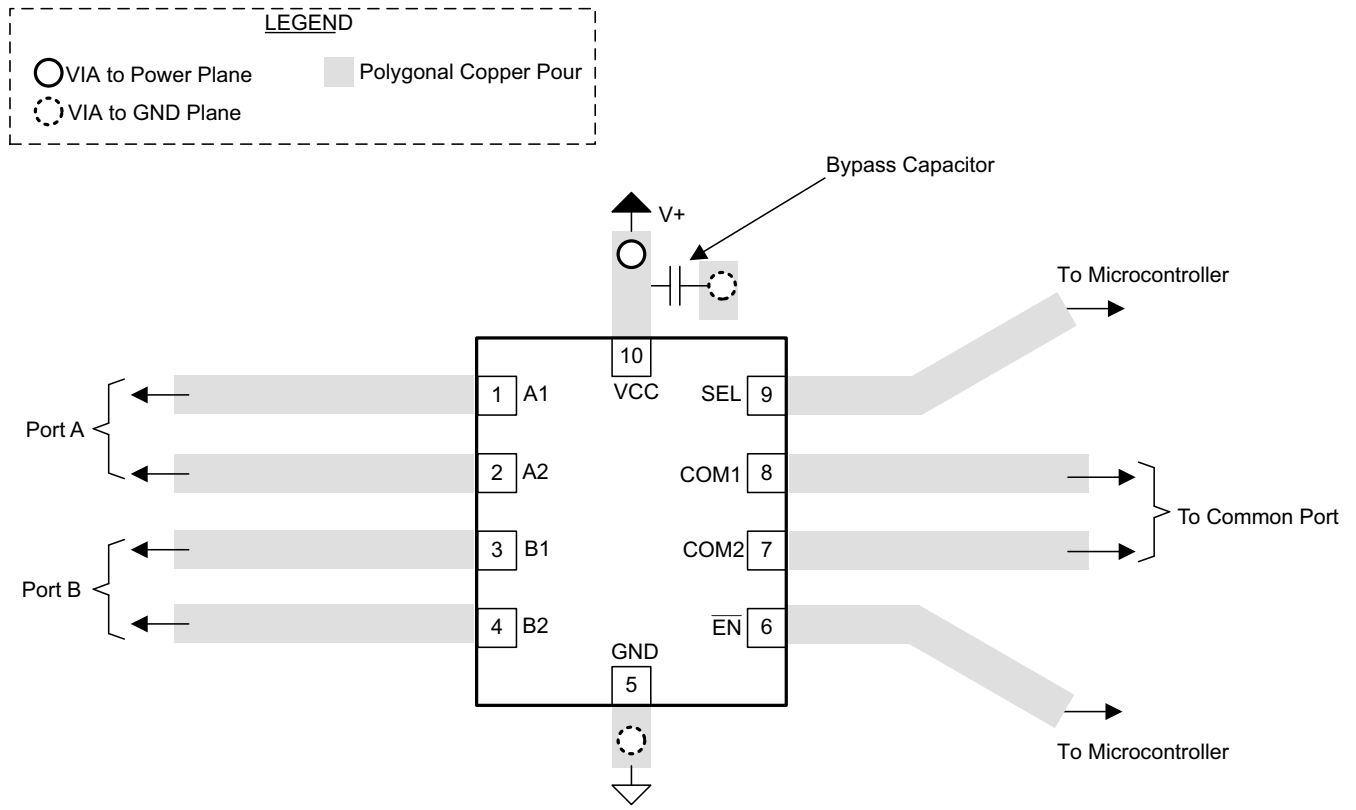


图 11-2. Package Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- [High-Speed Layout Guidelines Application Report](#)
- [High-Speed Interface Layout Guidelines](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX136MRSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	19H	Samples
TMUX136RSER	ACTIVE	UQFN	RSE	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	19G	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

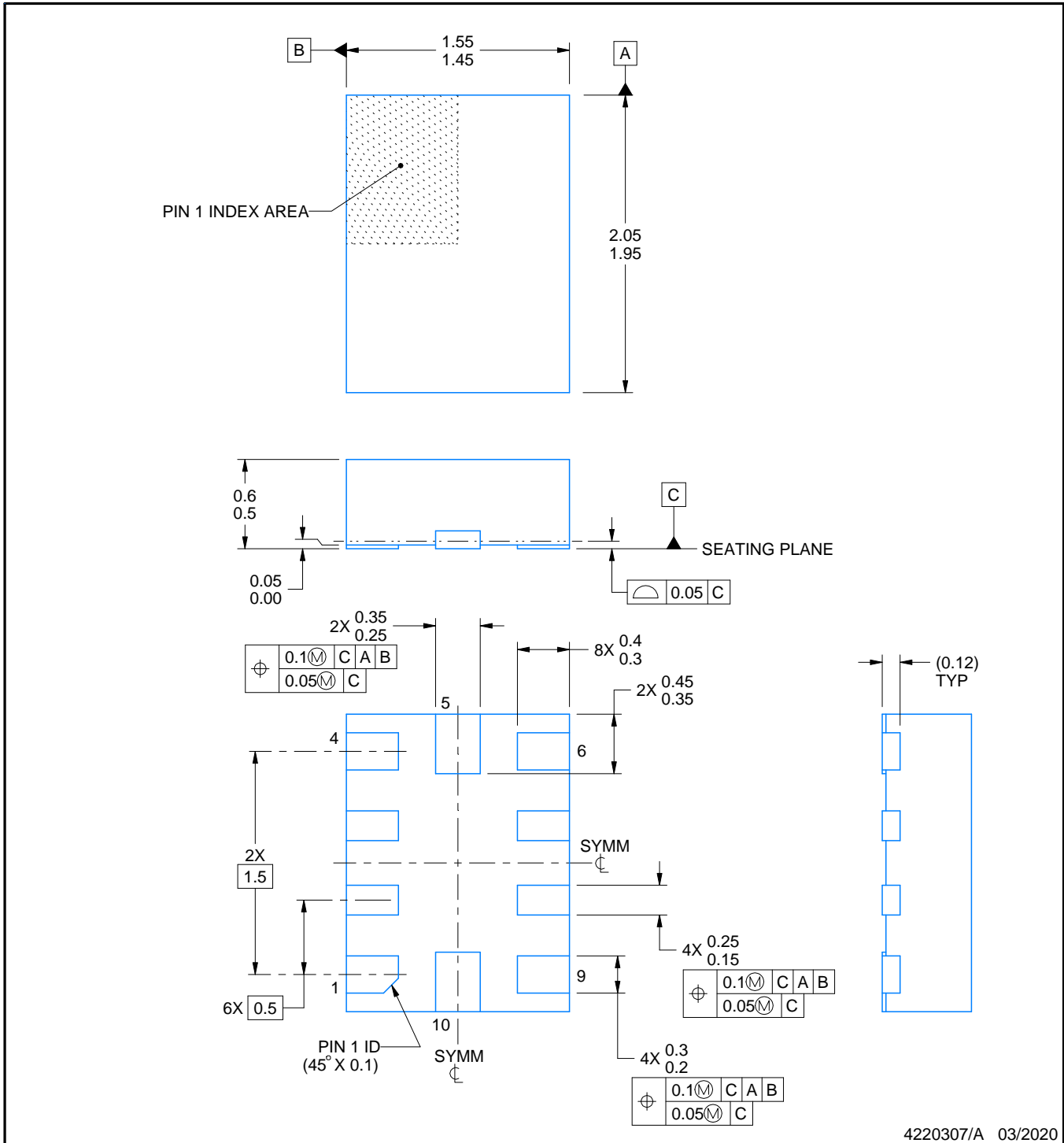
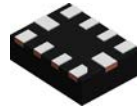

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX136MRSER	UQFN	RSE	10	3000	180.0	9.5	2.2	1.8	0.75	4.0	8.0	Q3
TMUX136RSER	UQFN	RSE	10	3000	180.0	9.5	1.7	2.2	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX136MRSER	UQFN	RSE	10	3000	189.0	185.0	36.0
TMUX136RSER	UQFN	RSE	10	3000	189.0	185.0	36.0



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NOTES:

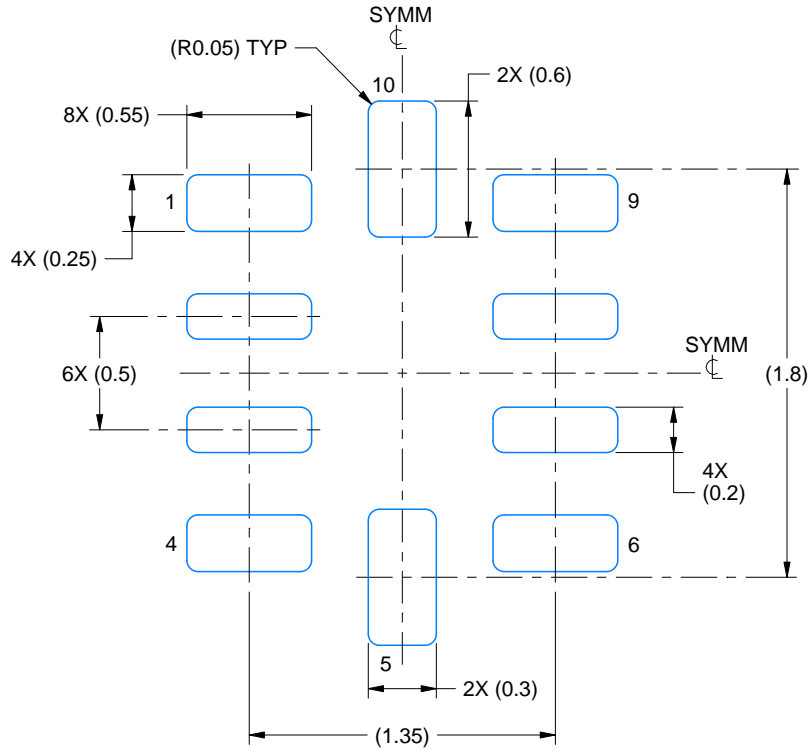
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

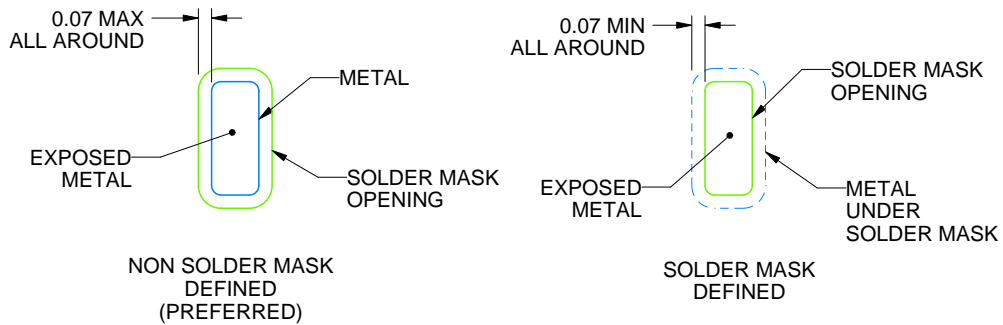
RSE0010A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4220307/A 03/2020

NOTES: (continued)

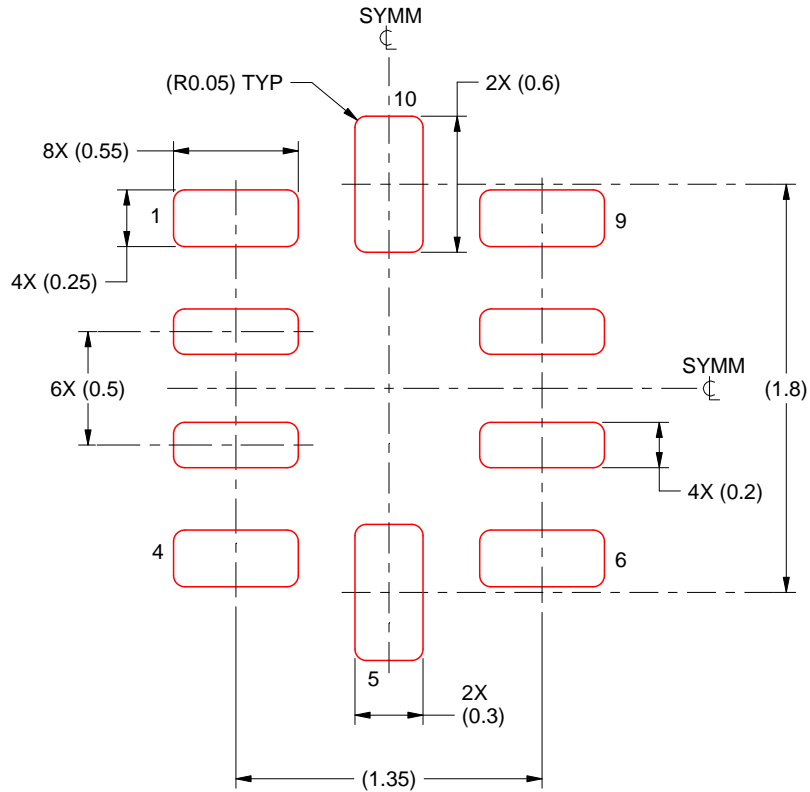
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RSE0010A

UQFN - 0.6 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

4220307/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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