

## TMDS171/I 3.4Gbps TMDS 重定时器

### 1 特性

- 高清多媒体接口 (HDMI) 输入端口与输出端口间具有时钟和数据恢复 (CDR) 电路, 支持高达 3.4Gbps 的数据传输速率
- 兼容 HDMI1.4b 电气参数。
- 支持 4k2k30p 和高达 WUXGA 12 位色深或 1080p, 具有更高的刷新率™
- 对输入流重新定时以补偿随机抖动
- 自适应接收器均衡器或可编程固定均衡器
- I<sup>2</sup>C 和引脚设置可编程
- 5+ 位对内偏移补偿
- 包括眼图的链路调试工具, 位于 RX 均衡器之后
- 支持单端模式 ARC
- 48 引脚 7mm x 7mm 0.5mm 间距超薄型四方扁平无引线 (VQFN) 封装
- 扩展商业温度范围为 0°C 至 85°C (TMDS171)
- 工业温度范围为 -40°C 至 85°C (TMDS171I)

### 2 应用

- 数字电视
- 数字投影仪
- 音频/视频设备
- 蓝光 (Blu-Ray) DVD
- 监视器
- 台式机/一体化计算机
- 有源线缆

### 3 说明

TMDS171 是一款数字视频接口 (DVI) 或高清多媒体接口 (HDMI) 重定时器。TMDS171 支持四条 TMDS 通道, 音频返回通道 (SPDIF\_IN/ARC\_OUT)、热插拔检测 (HPD) 和数字显示控制 (DDC) 接口。TMDS171 支持高达 3.4Gbps 的信号传输速率, 可实现最高分辨率达 4k2k30p 24 位/像素和高达 WUXGA 12 位色深或 1080p, 并且具有较高的刷新率。TMDS171 在低于 1Gbps 的数据速率下会自动配置为重驱动器, 而在高于该速率时会自动配置为重定时器。

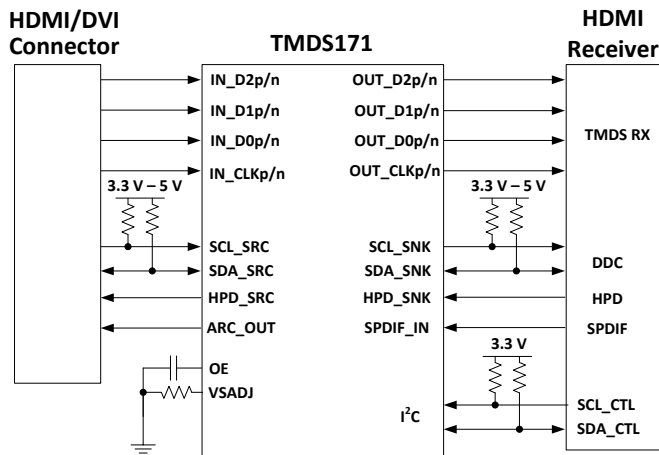
TMDS171 支持双电源轨 (VDD 为 1.2V, VCC 为 3.3V), 有助于降低功耗。该器件采用多种电源管理方法来降低整体功耗。TMDS171x 通过 I<sup>2</sup>C 或引脚设置支持固定的 EQ 增益或自适应 EQ 控制, 以补偿不同长度的输入电缆或电路板走线。

#### 器件信息<sup>(1)</sup>

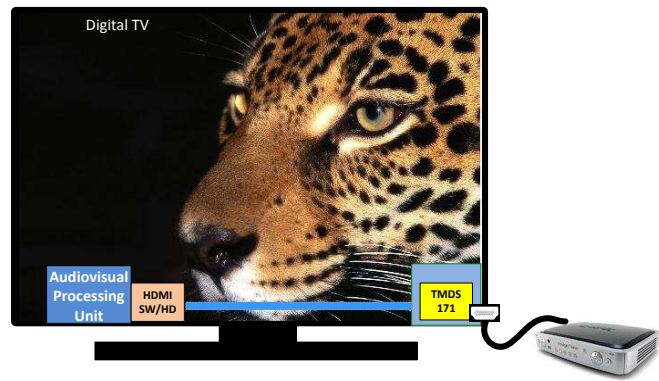
器件型号	封装	封装尺寸 (标称值)
TMDS171	(VQFN) 48 引脚	7.00mm x 7.00mm
TMDS171I		

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

简化电路原理图



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## 4 修订历史记录

Changes from Revision D (August 2016) to Revision E	Page
• Added Note 3 to the <i>Electrical Characteristics</i> table .....	8
• Deleted text "which is needed for certain HDMI CTS test." from the second paragraph in the <i>Overview</i> section .....	20
• Changed section: <i>Input Signal Detect Block</i> .....	25
• Changed H to X in the first row of the HPD_SNK column in <a href="#">Table 36</a> .....	51
• Changed the IN_Dx column in <a href="#">Table 36</a> .....	51

Changes from Revision C (April 2016) to Revision D	Page
• <a href="#">Recommended Operating Conditions</a> , Changed the CONTROL PINS section .....	7
• <a href="#">Electrical Characteristics</a> Changed the DDC and I2C section .....	9

Changes from Revision B (February 2016) to Revision C	Page
• Changed pin 36 Description From: TX_TERM_CTL = L: 150 - 300 Ω To: TX_TERM_CTL = L: Reserved in the <i>Pin Functions</i> table .....	6
• Added OE to V <sub>IL</sub> "Low-level input voltage" in the <a href="#">Recommended Operating Conditions</a> table .....	7
• Added OE to V <sub>IH</sub> "High-level input voltage" in the <a href="#">Recommended Operating Conditions</a> table .....	7
• Changed <a href="#">Figure 23</a> .....	22
• Deleted the VDD_ramp and VCC_ramp MIN values in <a href="#">Table 1</a> .....	23
• Changed TX_TERM_CTL = L to Reserved in <a href="#">Table 3</a> .....	25
• Changed text "address 22h through the I <sup>2</sup> C interface" To: "address 0Bh through the I <sup>2</sup> C interface" <a href="#">DDC Functional Description</a> .....	29
• Added Note to 11–400-kbps in <a href="#">Table 8</a> .....	32
• Added Note to 11–400-kbps in <a href="#">Table 10</a> .....	34

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**Changes from Revision A (December 2015) to Revision B** **Page**

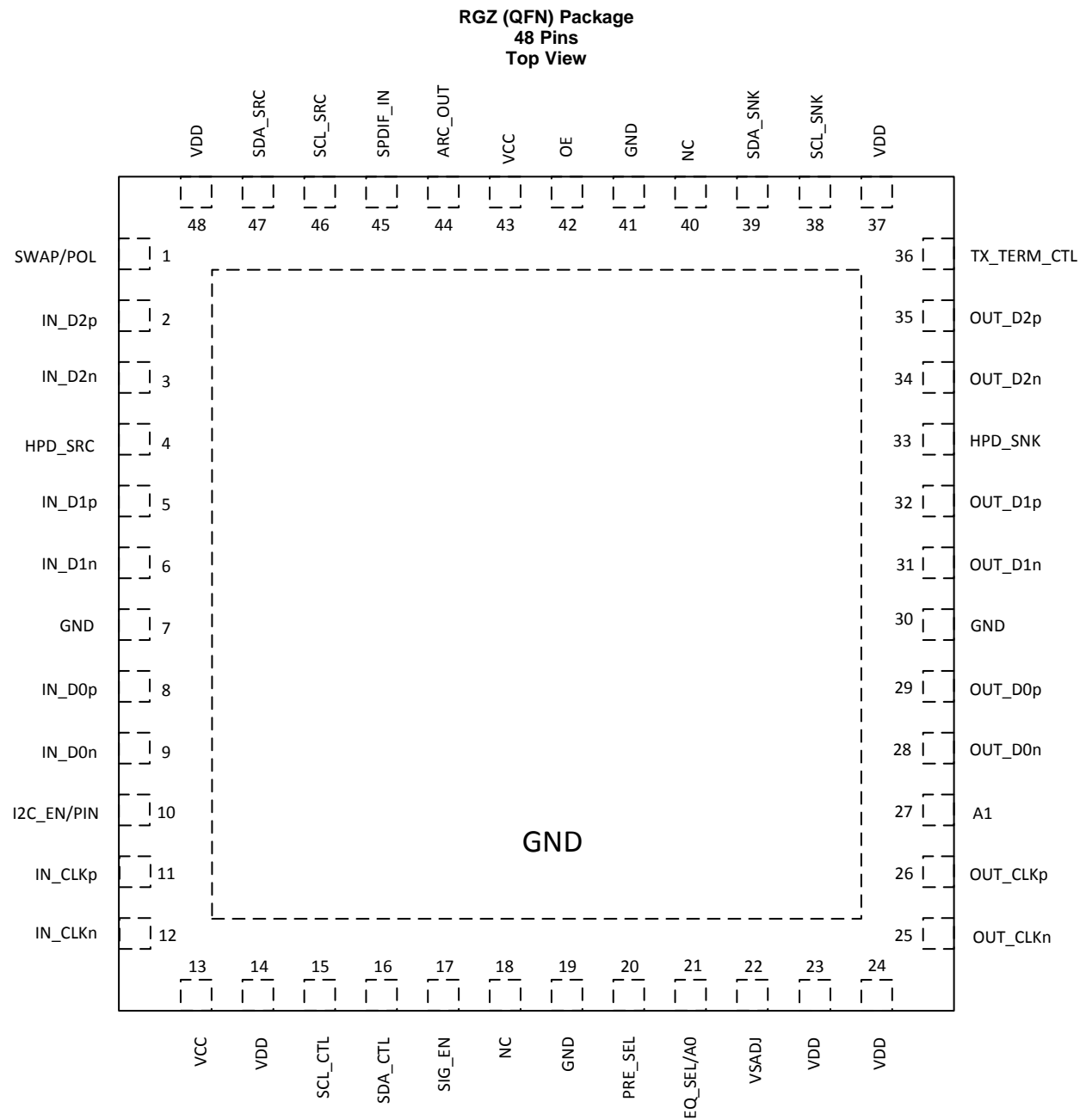
- Changed Pin 44 From: AUX\_SRCn To: ARC\_OUT Pin 45 From: AUX\_SRCn To: SPDIF\_IN in the [Pin Configuration and Functions](#) image ..... 4
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**Changes from Original (October 2015) to Revision A** **Page**

- 已将器件状态从“产品预览”更改为“量产数据” ..... 1
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## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
VCC	13, 43	P	3.3 V Power Supply
VDD	14, 23, 24, 37, 48	P	1.2 V Power Supply
GND	7, 19, 41, 30	G	Ground
Thermal Pad		G	Ground
<b>MAIN LINK INPUT PINS (FAIL SAFE)</b>			
IN_D2p/n	2, 3	I	Channel 2 Differential Input
IN_D1p/n	5, 6	I	Channel 1 Differential Input
IN_D0p/n	8, 9	I	Channel 0 Differential Input
IN_CLKp/n	11, 12	I	Clock Differential Input
<b>MAIN LINK OUTPUT PINS (FAIL SAFE)</b>			
OUT_D2n/p	34, 35	O	TMDS Data 2 Differential Output
OUT_D1n/p	31, 32	O	TMDS Data 1 Differential Output
OUT_D0n/p	28, 29	O	TMDS Data 0 Differential Output
OUT_CLKn/p	25, 26	O	TMDS Clock Differential Output
<b>HOT PLUG DETECT PINS</b>			
HPD_SRC	4	O	Hot Plug Detect Output to source side
HPD_SNK	33	I	Hot Plug Detect Input from sink side
<b>AUDIO RETURN CHANNEL and DDC PINS</b>			
SPDIF_IN	45	I	SPDIF signal input
ARC_OUT	44	O	Audio return channel output
SDA_SRC	47	I/O	Source Side TMDS Port Bidirectional DDC Data line
SCL_SRC	46	I/O	Source Side TMDS Port Bidirectional DDC Clock line
SDA_SNK	39	I/O	Sink Side TMDS Port Bidirectional DDC Data Line
SCL_SNK	38	I/O	Sink Side TMDS Port Bidirectional DDC Clock Line
<b>CONTROL PINS<sup>(2)</sup></b>			
OE	42	I	Operation Enable/Reset Pin OE = L: Power Down Mode OE = H: Normal Operation Internal weak pull up: Resets device when transitions from H to L
SIG_EN	17	I	Signal detector circuit enable SIG_EN = L: Signal Detect Circuit Disabled: Term resistors always connected (Default) SIG_EN = H: Signal Detect Circuit Enabled: When no valid clock device enters Standby Mode. Internal weak pull down
PRE_SEL	20	I 3-Level	De-emphasis Control when I2C_EN/PIN = Low. PRE_SEL = L: -2 dB PRE_SEL = No Connect: 0 dB PRE_SEL = H: Reserved When I2C_EN/PIN = High; De-emphasis is controlled through I <sup>2</sup> C
EQ_SEL/A0	21	I	Input Receive Equalization pin strap when I2C_EN/PIN = Low EQ_SEL = L: Fixed EQ at 7.5 dB EQ_SEL = No Connect: Adaptive EQ EQ_SEL = H: Fixed at 14 dB When I2C_EN/PIN = High Address Bit 1 Note: 3 level for pin strap programming but 2 level when I <sup>2</sup> C address
I2C_EN/PIN	10	I	I2C_EN/PIN = High; Puts Device into I2C Control Mode I2C_EN/PIN = Low; Puts Device into Pin Strap Mode
SCL_CTL	15	I/O	I <sup>2</sup> C Clock Signal when I <sup>2</sup> C_EN/PIN = High. Note: When I2C_EN = Low; Pin strapping takes priority and those functions cannot be changed by I <sup>2</sup> C
SDA_CTL	16	I/O	I <sup>2</sup> C Data Signal when I <sup>2</sup> C_EN/PIN = High Note: When I2C_EN = Low; Pin strapping takes priority and those functions cannot be changed by I <sup>2</sup> C
VSadj	22	I	TMDS Output Voltage Swing Control; Nominal 7.06 kΩ Resistor to GND

(1) (1) G = Ground, I = Input, O = Output, P = Power

(2) (H) Logic High (Pin strapped to VCC through 65 kΩ resistor); (L) Logic Low (Pin strapped to GND through 65 kΩ resistor); (Mid-Level = No connect)

**Pin Functions (continued)**

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A1	27	I	High address bit 2 for I <sup>2</sup> C programming Weak internal pull down. Note: When I2C_EN/PIN = Low for Pin Strapping Mode leave this pin as No connect
TX_TERM_CTL	36	I 3-Level	Transmit Termination Control TX_TERM_CTL = H: No transmit Termination TX_TERM_CTL = L: Reserved TX_TERM_CTL = No Connect: Automatically selects the termination impedance 2 Gbps > DR ≤ 3.4 Gbps – 150 - 300 Ω differential near end termination DR < 2 Gbps – no termination Note: If left floating; the device will be in Automatic Select Mode. DR stands for Data Rate
SWAP/POL	1	I 3-Level	Receive Polarity Swap and Receive Lane Swap control pin SWAP/POL = H: Receive Lanes Polarity Swap (Retimer Mode Only) SWAP/POL = L: Receive Lanes (Retimer and Redriver Mode) Swap SWAP/POL = No Connect, Normal Operation
NC	18, 40	–	No connect

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) <sup>(1)(2)(3)</sup>

		MIN	MAX	UNIT
Supply Voltage Range	VCC	–0.3	4	
	VDD	–0.3	1.4	
Voltage Range	Main Link Input Differential Voltage (IN_Dx, IN_CLKx); I <sub>IN</sub> = 15mA	V <sub>CC</sub> - 0.75 V	V <sub>CC</sub> + 0.3 V	V
	TMDS Outpus ( OUT_Dx)	–0.3	4	
	HPD_SRC, Vsadj, SDA_CTL, SCL_CTL, OE, A1, PRE_SEL, EQ_SEL/A0, I2C_EN/PIN, SIG_EN, TX_TERM_CTL,	–0.3	4	
	HDP_SNK, SDA_SNK, SCL_SNK, SDA_SRC, SCL_SRC	–0.3	6	
Input Current I <sub>IN</sub>	Main Link Input Differential Voltage (IN_Dx, IN_CLKx);		15	mA
Continuous power dissipation		See <a href="#">Thermal Information</a>		
Storage temperature, T <sub>stg</sub>		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-B

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply Voltage Nominal Value 3.3 V	3.135	3.3	3.465	V
V <sub>DD</sub>	Supply Voltage Nominal Value 1.2 V	1.1	1.2	1.27	V
T <sub>STG</sub>	Storage temperature	-65		150	°C
T <sub>CASE</sub>	Case temperature			92.7	°C
T <sub>A</sub>	Operating free-air temperature (TMDS171)	0		85	°C
	Operating free-air temperature (TMDS1711)	-40		85	°C
<b>MAIN LINK DIFFERENTIAL PINS</b>					
V <sub>ID(PP)</sub>	Peak-to-peak input differential voltage	75		1560	mVpp
V <sub>IC</sub>	Input Common Mode Voltage	VCC - 0.4		VCC + 0.1	V
d <sub>R</sub>	Data rate	0.25		3.4	Gbps
R <sub>(VSADJ)</sub>	TMDS compliant swing voltage bias resistor 1%		7.06		KΩ
<b>CONTROL PINS</b>					
V <sub>I(DC)</sub>	DC Input Voltage	-0.3		3.6	V
V <sub>IL</sub> <sup>(1)</sup>	Low-level input voltage OE			0.8	V
	Low-level input voltage at PRE_SEL, EQ_SEL/A0, TX_TERM_CTL, SWAP/POL pins only <sup>(1)</sup>			0.3	V
V <sub>IM</sub> <sup>(1)</sup>	Mid-Level input voltage at PRE_SEL, EQ_SEL/A0, TX_TERM_CTL, SWAP/POL pins only <sup>(1)</sup>	1	1.2	1.4	V
V <sub>IH</sub> <sup>(1)</sup>	High-level input voltage at PRE_SEL, EQ_SEL/A0, TX_TERM_CTL, SWAP/POL, OE <sup>(2)</sup> pins only <sup>(1)</sup>	2.6			V
V <sub>OL</sub>	Low-level output voltage			0.4	V
V <sub>OH</sub>	High-level output voltage	2.4			V
I <sub>IH</sub>	High level input current	30		30	μA
I <sub>IL</sub>	Low level input current	-25		25	μA
I <sub>OS</sub>	Short circuit output current	-50		50	mA
I <sub>OZ</sub>	High impedance output current			10	μA
R <sub>(OEPU)</sub>	Pull up resistance on OE pin	150		250	KΩ

- (1) These values are based upon a microcontroller driving the control pins. The pull up/down/floating resistor configuration will set control pins properly which will have a different value than shown due to internal biasing.
- (2) This value is based upon a microcontroller driving the OE pin. A passive reset circuit using an external capacitor and the internal pullup resistor will set OE pin properly, but may have a different value than shown due to internal biasing.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		RGZ (QFN)	UNIT
		48 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	31.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	18.2	
R <sub>θJB</sub>	Junction-to-board thermal resistance	8.1	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	8.1	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.2	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

The Maximum rating is simulated at 3.465 V  $V_{CC}$  and 1.27 V  $V_{DD}$  and at 85°C temperature. The Typical rating is simulated at 3.3  $V_{CC}$  and 1.2 V  $V_{DD}$  and at 27°C temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Power Supply</b>						
$P_{(D1)}$ <sup>(1)(2)</sup>	Device power Dissipation (Retimer Operation)	OE = H, $V_{CC}$ = 3.3 V / 3.465 V, $V_{DD}$ = 1.2 V / 1.27 V IN_Dx: VID_PP = 1200 mV, I2C_EN/PIN = L, PRE_SEL = H, EQ_CTL = H, SDA_CTL/CLK_CTL = 0 V		675	875	mW
$P_{(D2)}$ <sup>(1)(2)</sup>	Device power Dissipation (Redriver Operation)	3.4 Gbps TMDS pattern, $V_I$ = 3.3 V; VSADJ = 7.06 k $\Omega$		400	600	mW
$P_{(SD1)}$ <sup>(1)(2)(3)</sup>	Device power in Standby	OE = H, $V_{CC}$ = 3.3 V / 3.465 V $V_{DD}$ = 1.2 V / 1.27 V, HPD = H, No Valid input Signal		50	100	mW
$P_{(SD2)}$ <sup>(1)(2)(3)</sup>	Device power in PowerDown	OE = L, $V_{CC}$ = 3.3 V / 3.465 V $V_{DD}$ = 1.2 V / 1.27 V		10	30	mW
$I_{CC1}$ <sup>(1)(2)</sup>	$V_{CC}$ Supply current (TMDS 3.4 Gbps Retimer Mode)	OE = H, $V_{CC}$ = 3.3 V / 3.465 V $V_{DD}$ = 1.2 V / 1.27 V		80	140	mA
$I_{DD1}$ <sup>(1)(2)</sup>	$V_{DD}$ Supply current (TMDS 3.4 Gbps Retimer Mode)	IN_Dx: VID_PP = 1200 mV, 3.4 Gbps TMDS pattern I2C_EN/PIN = L, PRE_SEL = H, EQ_CTL = H, SDA_CTL/CLK_CTL = 0 V, SLEW_CTL = H		286	325	mA
$I_{CC2}$ <sup>(1)(2)</sup>	$V_{CC}$ Supply current (TMDS 3.4 Gbps Redriver Mode)	OE = H, $V_{CC}$ = 3.3 V / 3.465 V $V_{DD}$ = 1.2 V / 1.27 V		51		mA
$I_{DD2}$ <sup>(1)(2)</sup>	$V_{DD}$ Supply current (TMDS 3.4 Gbps Redriver Mode)	IN_Dx: VID_PP = 1200 mV, 3.4 Gbps TMDS pattern I2C_EN/PIN = L, PRE_SEL = H, EQ_CTL = H, SDA_CTL/CLK_CTL = 0V, SLEW_CTL = H		188		mA
$I_{(SD1)}$ <sup>(3)</sup>	Standby current	OE = H, $V_{CC}$ = 3.3 V / 3.465 V $V_{DD}$ = 1.2 V / 1.27 V HPD = H: No valid signal on IN_CLK	3.3V Rail <sup>(1)</sup>	6	15	mA
			1.2V Rail	40	50	
$I_{(SD2)}$ <sup>(3)</sup>	PowerDown current	OE = L, $V_{CC}$ = 3.3 V / 3.465 V $V_{DD}$ = 1.2 V / 1.27 V	3.3V Rail <sup>(1)</sup>	2	5	mA
			1.2V Rail	3.5	15	
<b>TMDS Differential Input</b>						
$D_{(R\_RX\_DATA)}$	TMDS data lanes data rate		0.25		3.4	Gbps
$D_{(R\_RX\_CLK)}$	TMDS clock lanes clock rate		25		340	MHz
$t_{RX\_DUTY}$	Input clock duty circle		40%	50%	60%	
$t_{CLK\_JIT}$	Input clock jitter tolerance				0.3	Tbit
$t_{DATA\_JIT}$	Input data jitter tolerance	Test the TTP2 See <a href="#">Figure 11</a>			150	ps
$t_{RX\_INTRA}$	Input intra-pair skew tolerance	Test at TTP2 when DR = 1.6 Gbps See <a href="#">Figure 11</a>	112			ps
$t_{RX\_INTER}$	Input inter-pair skew tolerance				1.8	ns
$E_{QH(D)}$	Fixed EQ gain for data lane IN_D(0,1,2)n/p	EQ_SEL/A0=H; Fixed EQ gain, test at 3.4 Gbps		14		dB
$E_{QL(D)}$	Fixed EQ gain for data lane IN_D(0,1,2)n/p	EQ_SEL/A0=L; Fixed EQ gain, test at 3.4 Gbps		7.5		
$E_{OZ(D)}$	Adaptive EQ gain for data lane IN_D(0,1,2)n/p	EQ_SEL/A0=NC; adaptive EQ	2		14	
$E_{Q(C)}$	EQ gain for clock lane IN_CLKn/p	EQ_SEL/A0=H,LNC		0		
$R_{(INT)}$	Input differential termination impedance		90	100	115	$\Omega$
<b>TMDS Differential Output</b>						
$V_{OH}$	Single-ended high level output voltage	PRE_SEL = NC; TX_TERM_CTL = H; OE = H; DR = 750 Mbps; VSadj = 7.06 k $\Omega$	$V_{CC}$ - 10mV		$V_{CC}$ + 10mV	V
		PRE_SEL = NC; TX_TERM_CTL = H; OE = NC; DR = 2.97 Gbps; VSadj = 7.06 k $\Omega$	$V_{CC}$ - 200mV		$V_{CC}$ + 10mV	
$V_{OL}$	Single-ended low level output voltage No Pre-emphasis, Load is 50 $\Omega$ pull ups to 3.135 V and 3.465 V	PRE_SEL = NC; TX_TERM_CTL = H; OE = H; DR = 750 Mbps; VSadj = 7.06 k $\Omega$	$V_{CC}$ - 600mV		$V_{CC}$ - 400mV	
		PRE_SEL = NC; TX_TERM_CTL = H; OE = NC; DR = 2.97 Gbps; VSadj = 7.06 k $\Omega$	$V_{CC}$ - 700mV		$V_{CC}$ - 400mV	

(1)  $I_{CC}$  is a direct result of the source design as the TMDS171 integrated receive termination resistor accounts for 85 mA to 100 mA.

(2)  $I_{DD}$  is impacted by ARC usage. Connecting a 500 k $\Omega$  resistor to GND at SPDIF reduces the value by more than 20 mA.

(3) The measurements were made with no active source connected.



## Electrical Characteristics (continued)

The Maximum rating is simulated at 3.465 V  $V_{CC}$  and 1.27 V  $V_{DD}$  and at 85°C temperature. The Typical rating is simulated at 3.3 V  $V_{CC}$  and 1.2 V  $V_{DD}$  and at 27°C temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SWING\_DA)}$	Single-ended output voltage swing on data lane	PRE_SEL = NC; TX_TERM_CTL = H/NC; OE = NC; DR = $\leq 3.4$ Gbps; VSadj = 7.06 k $\Omega$	400	500	600	mV
$V_{(SWING\_CLK)}$	Single-ended output voltage swing on clock lane	PRE_SEL = NC; TX_TERM_CTL = H/NC; OE = NC; DR = $\leq 3.4$ Gbps; VSadj = 7.06 k $\Omega$	400	500	600	
$\Delta V_{(SWING)}$	Change in single-end output voltage swing per 100 $\Omega$ $\Delta V_{Sadj}$			20		
$\Delta V_{OCM(SS)}$	Change in steady state output common mode voltage between logic levels		-5		5	
$V_{OD(PP)}$	Initial output differential voltage before steady state when pre-emphasis or de-emphasis is implemented	VSadj = 7.06 k $\Omega$ ; PRE_SEL = NC, See <a href="#">Figure 8</a>	800		1200	
$V_{OD(SS)}$	Steady state output differential voltage	VSadj = 7.06 k $\Omega$ ; PRE_SEL = L, See <a href="#">Figure 9</a>	600		1075	
$I_{OS}$	Short circuit current limit	Main link output shorted to GND			50	mA
$I_{LEAK}$	Failsafe condition leakage current	$V_{CC} = 0$ V; $V_{DD} = 0$ V; TMDS Outputs pulled to 3.3V through 50 $\Omega$ resistor			45	$\mu$ A
$R_{(TERM)}$	Source Termination resistance		150		300	$\Omega$
<b>DDC and I2C</b>						
$V_{I-DC}$	SCL/SDA_SNK, SCL/SDA_SRC DC input voltage		-0.3		5.5	V
	SCL/SDA_CTL, DC input voltage		-0.3		3.6	V
$V_{IL}$	SCL/SDA_SNK, SCL/SDA_SRC Low level input voltage				$0.3 \times V_{CC}$	V
	SCL/SDA_CTL Low level input voltage				$0.3 \times V_{CC}$	V
$V_{IH}$	SCL/SDA_SNK, SCL/SDA_SRC high level input voltage		3			V
	SCL/SDA_CTL high level input voltage		$0.7 \times V_{CC}$			V
$V_{OL}$	SCL/SDA_CTL, SCL/SDA_SRC low level output voltage	$I_O = 3$ mA and $V_{CC} > 2$ V			0.4	V
		$I_O = 3$ mA and $V_{CC} < 2$ V			$0.2 \times V_{CC}$	V
$f_{SCL}$	SCL clock frequency fast I2C mode for local I2C control				400	kHz
$C_{bus}$	Total capacitive load for each bus line (DDC and local I2C pins)				400	pF
<b>HPD</b>						
$V_{IH}$	High-level input voltage	HPD_SNK	2.1			V
$V_{IL}$	Low-level input voltage	HPD_SNK			0.8	
$V_{OH}$	High-level output voltage	$I_{OH} = -500$ $\mu$ A; HPD_SRC	2.4		3.6	
$V_{OL}$	Low-level output voltage	$I_{OL} = -500$ $\mu$ A; HPD_SRC	0		0.1	
$I_{LEAK}$	Failsafe condition leakage current	$V_{CC} = 0$ V; $V_{DD} = 0$ V; HPD_SNK = 5 V			40	$\mu$ A
$I_{H(HPD)}$	High level input current	Device powered; $V_{IH} = 5$ V; $I_{H(HPD)}$ includes $R_{pd(HPD)}$ resistor current			40	
		Device powered; $V_{IL} = 0.8$ V; $I_{H(HPD)}$ includes $R_{pd(HPD)}$ resistor current			30	
$R_{pd(HPD)}$	HPD input termination to GND;	$V_{CC} < 0$ V	150	190	220	k $\Omega$
<b>SPDIF and ARC</b>						
$V_{(EL)}$	Operating DC voltage for single mode ARC output	Test at ARC_OUT, see <a href="#">Figure 19</a>	0		5	V

## Electrical Characteristics (continued)

The Maximum rating is simulated at 3.465 V  $V_{CC}$  and 1.27 V  $V_{DD}$  and at 85°C temperature. The Typical rating is simulated at 3.3 V  $V_{CC}$  and 1.2 V  $V_{DD}$  and at 27°C temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN(DC)}$	Operating DC voltage for SPDIF input				0.05	V
$V_{(SP\_SW)}$	Signal amplitude of SPDIF input		0.2	0.5	0.6	V
$V_{(EISWING)}$	Signal amplitude on the ARC output	Test at ARC_OUT, 75 $\Omega$ external termination resistor, see <a href="#">Figure 19</a>	0.4	0.5	0.6	V
$CLK_{(ARC)}$	Signal frequency on ARC	Test at ARC_OUT, see <a href="#">Figure 19</a>	3.687	5.645±0.1%	13.517	MHz
Duty Cycle	Output Clock Duty cycle		45%	50%	55%	
Data Rate	SPDIF Input DR		7.373	11.29	27.034	Mbps
$t_{EDGE}$	The rise/fall time for ARC output	From 10% to 90% voltage level, see <a href="#">Figure 19</a>			0.4	UI
$R_{(IN\_SPDIF)}$	The Input Termination resistance for SPDIF			75		$\Omega$
$R_{(EST)}$	Single mode Output Termination resistance	0.1 MHz to 128 times the maximum frame rate	36	55	75	$\Omega$

## 6.6 Switching Characteristics

The Maximum rating is simulated at 3.465 V  $V_{CC}$  and 1.27 V  $V_{DD}$  and at 85°C temperature. The Typical rating is simulated at 3.3 V  $V_{CC}$  and 1.2 V  $V_{DD}$  and at 27°C temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>TMDS Redriver Mode</b>						
$D_R$	Data rate (Redriver mode)		250		3400	Mbps
$t_{PLH}$	Propagation delay time (low to high)		250		600	ps
$t_{PHL}$	Propagation delay time (high to low)		250		800	
$t_{T1}$	Transition time (rise and fall time); measured at 20% and 80% levels for Data Lanes.	$TX\_TERM\_CTL=L$ ; $PRE\_SEL=NC$ ; Data Rate 3.4 Gbps; Clock 340 MHz	75			
$t_{SK1(T)}$	Intra-pair output skew	$TX\_TERM\_CTL=NC$ ; $PRE\_SEL=NC$ ;			40	
$t_{SK2(T)}$	Inter-pair output skew	$TX\_TERM\_CTL=NC$ ; $PRE\_SEL=NC$ ;			100	
$t_{JTD1}$	Total output data jitter	$DR = 750$ Mbps, $PRE\_SEL = NC$ , $EQ\_SEL/A0 = NC$ . See <a href="#">Figure 5</a> at TTP3			0.2	Tbit
$t_{JTC1}$	Total output clock jitter				0.25	
<b>TMDS Retimer Mode</b>						
$D_R$	Data rate (retimer mod )		1.2		3.4	Gbps
$d_{(XVR)}$	Automatic redriver to Retimer Cross-Over	Measured with input signal applied from 0 to 200 mV <sub>PP</sub>	0.75	1.00	1.25	Gbps
$f_{(CROSSOVER)}$	Crossover frequency hysteresis			250		MHz
$PLL_{(BW)}$	Data Retimer PLL bandwidth	Default loop bandwidth setting		0.4	1	MHz
$t_{ACQ}$	Input Clock Frequency Detection and Retimer Acquisition Time			180		$\mu$ s
$I_{JT1}$	Input Clock Jitter Tolerance	Tested when data rate > 1.0 Gbps			0.3	Tbit
$t_{T1}$	Transition time (rise and fall time); measured at 20% and 80% levels for Data Lanes. TMDS		75			ps
$t_{DCD}$	OUT_CLK $\pm$ duty cycle		40%	50%	60%	
$t_{SK\_INTER}$	Inter-pair output skew	Default setting for internal inter-pair skew adjust, $PRE\_SEL = NC$ ; $TX\_TERM\_CTL = NC$ , $DR \leq 3.4$ Gbps; See <a href="#">Figure 6</a>			0.2	Tch

## Switching Characteristics (continued)

The Maximum rating is simulated at 3.465 V  $V_{CC}$  and 1.27 V  $V_{DD}$  and at 85°C temperature. The Typical rating is simulated at 3.3 V  $V_{CC}$  and 1.2 V  $V_{DD}$  and at 27°C temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SK\_INTRA}$ Intra-pair output skew	Default setting for internal intra-pair skew adjust, PRE_SEL = NC; TX_TERM_CTL = NC, DR ≤ 3.4 Gbps; See <a href="#">Figure 6</a>			0.15	Tbit
$t_{JITC2}$ Total output clock jitter	CLK Rate ≤ 340 MHz			0.25	Tbit
$t_{JITD2}$ Total output data jitter	DR ≤ 3.4 Gbps; See <a href="#">Figure 11</a>			0.2	Tbit
<b>HPD</b>					
$t_{PD(HPD)}$ Propagation delay from HPD_SNK to HPD_SRC; rising edge and falling edge <sup>(1)</sup>	see <a href="#">Figure 13</a> ; not valid during switching time		40	120	ns
$t_{T(HPD)}$ HPD logical disconnected timeout	see <a href="#">Figure 14</a>		2		ms
<b>DDC and I2C</b>					
$t_r$ Rise time of both SDA and SCL signals	$V_{CC} = 3.3\text{ V}$			300	ns
$t_f$ Fall time of both SDA and SCL signals				300	
$t_{HIGH}$ Pulse duration, SCL high		0.6			μs
$t_{LOW}$ Pulse duration, SCL low		1.3			μs
$t_{SU1}$ Setup time, SDA to SCL		100			
$t_{ST\_STA}$ Setup time, SCL to start condition		0.6			
$t_{HD\_STA}$ Hold time, start condition to SCL		0.6			
$t_{ST\_STO}$ Setup time, SCL to stop condition		0.6			μs
$t_{(BUF)}$ Bus free time between stop and start condition		1.3			
$t_{PLH1}$ Propagation delay time, low-to-high-level output	Source to Sink: 100 kbps pattern; $C_{b(Sink)} = 400\text{ pF}^{(2)}$ ; see <a href="#">Figure 17</a>		360		ns
$t_{PHL1}$ Propagation delay time, high-to-low-level output			230		
$t_{PLH2}$ Propagation delay time, low-to-high-level output	Sink to Source: 100 kbps pattern; $C_{b(Source)} = 100\text{ pF}^{(2)}$ ; see <a href="#">Figure 18</a>		250		
$t_{PHL2}$ Propagation delay time, high-to-low-level output			200		

(1) The Maximum rating is simulated at 3.465 V  $V_{CC}$  and 1.27 V  $V_{DD}$

(2)  $C_b$  = total capacitance of one bus line in pF.

### 6.7 Typical Characteristics

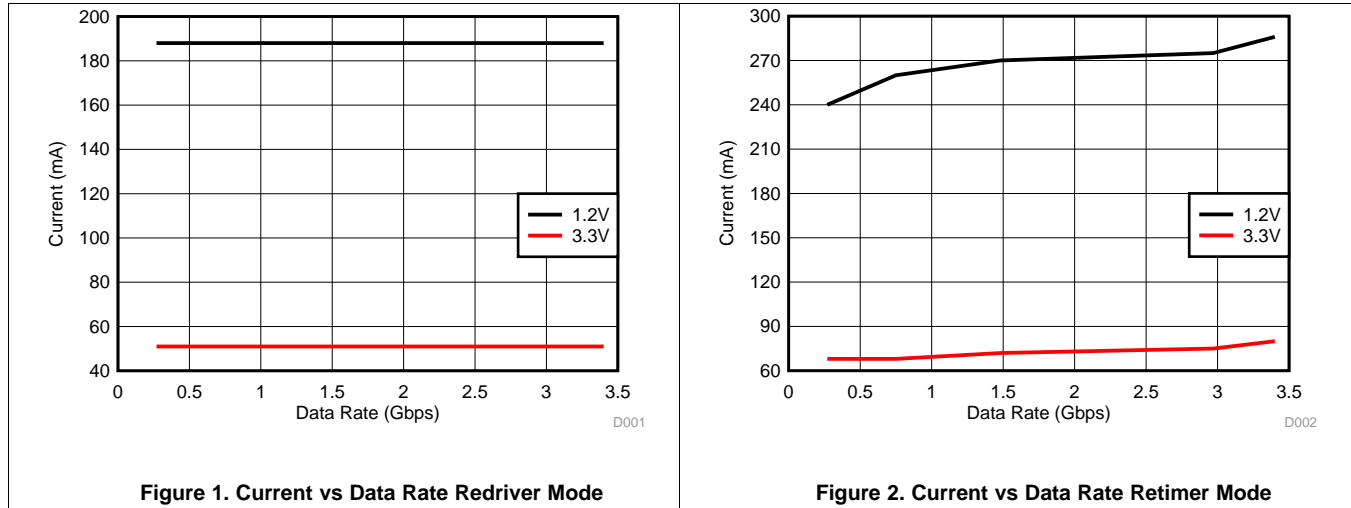


Figure 1. Current vs Data Rate Redriver Mode

Figure 2. Current vs Data Rate Retimer Mode

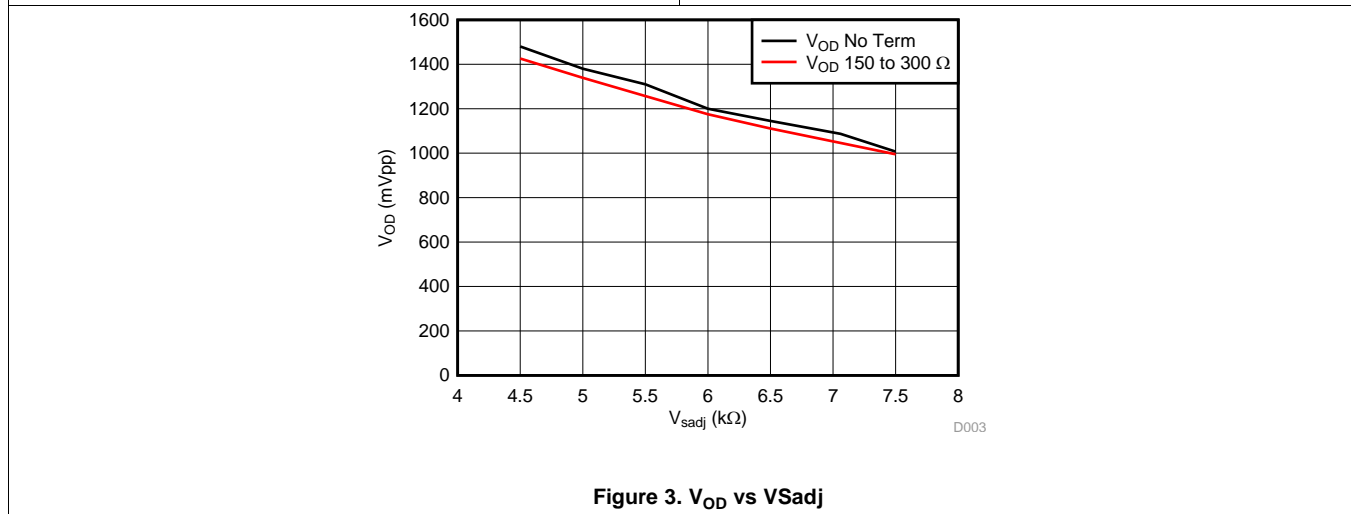


Figure 3. V<sub>OD</sub> vs V<sub>Sadj</sub>

### 7 Parameter Measurement Information

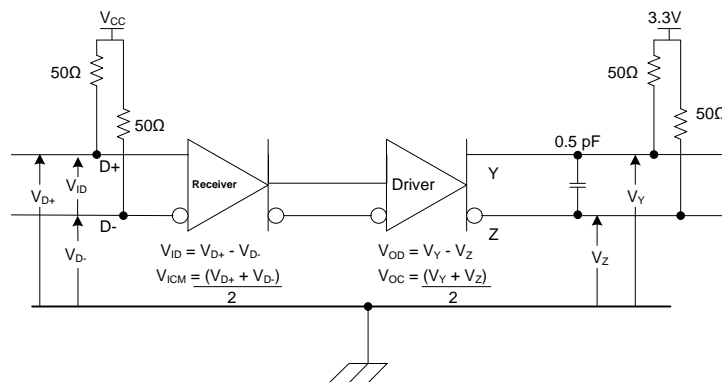


Figure 4. TMDS Main Link Test Circuit

Parameter Measurement Information (continued)

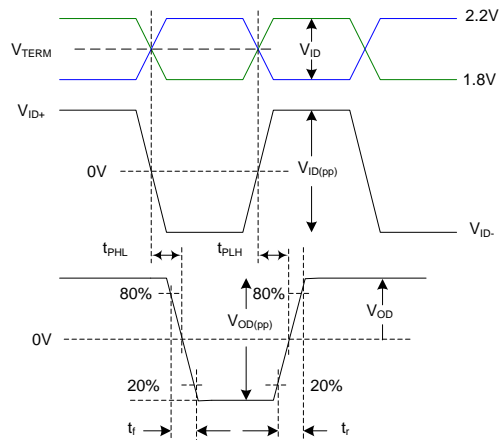


Figure 5. Input/Output Timing Measurements

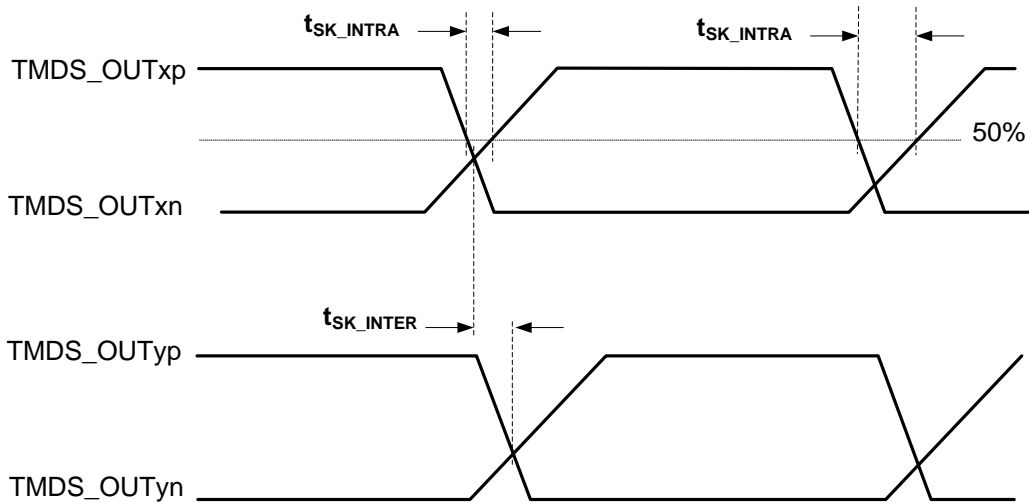


Figure 6. TMDS Output Skew Measurements

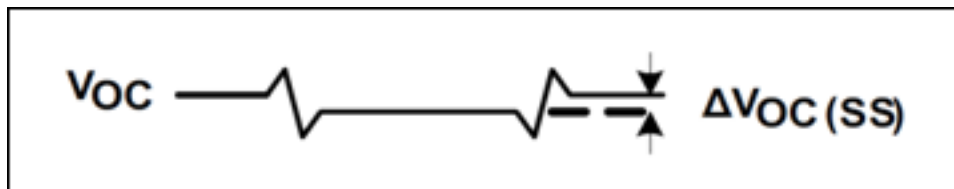


Figure 7. HDMI/DVI TMDS Output Common Mode Measurement

Parameter Measurement Information (continued)

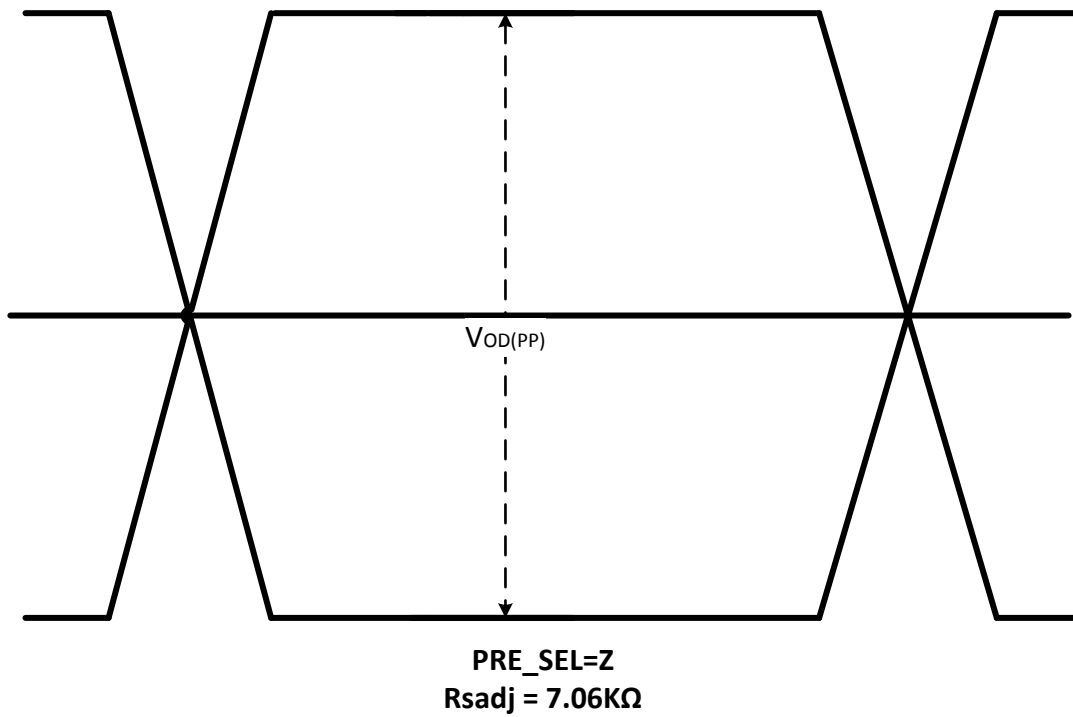


Figure 8. Output Differential Waveform

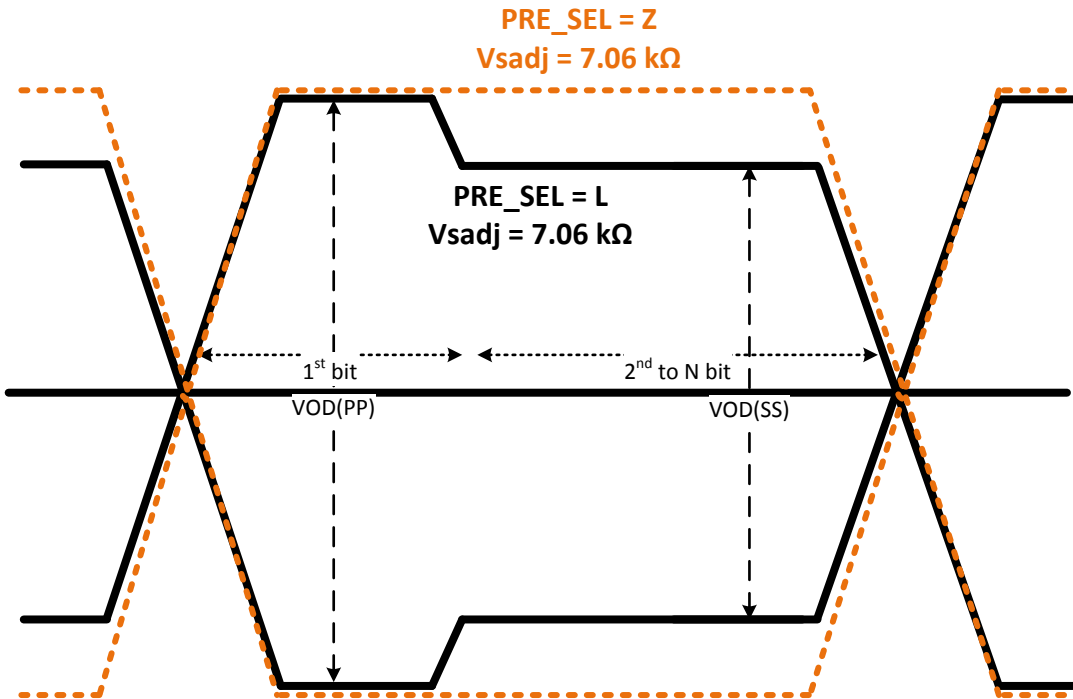
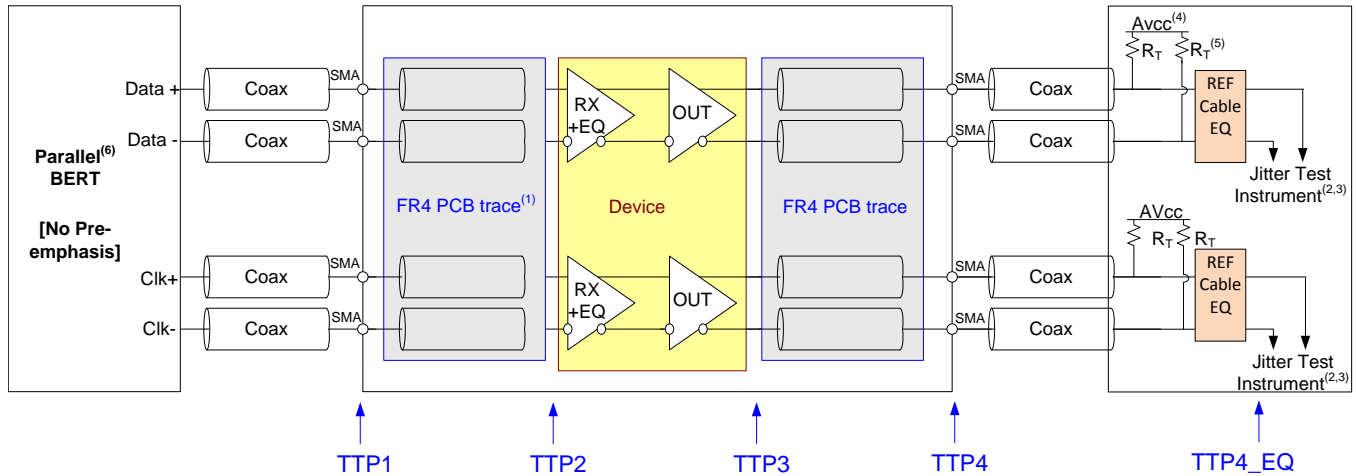


Figure 9. Output De-emphasis Waveform

Parameter Measurement Information (continued)



- (1) The FR4 trace between TTP1 and TTP2 is designed to emulate 1-8" of FR4, connector and another 1-8" of FR4. Trace width – 4 mils. 100 Ω differential impedance.
- (2) All Jitter is measured at a BER of  $10^{-9}$
- (3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1
- (4) AVCC = 3.3 V
- (5)  $R_T = 50 \Omega$
- (6) The input signal from parallel Bert does not have any pre-emphasis. Refer to *Recommended Operating Conditions*.

Figure 10. Jitter Measurement Circuit

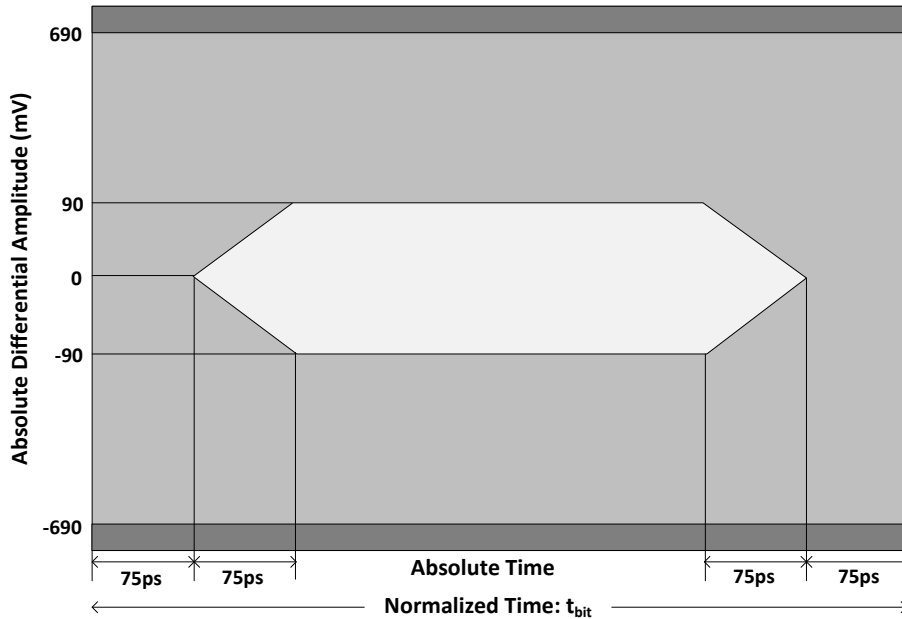
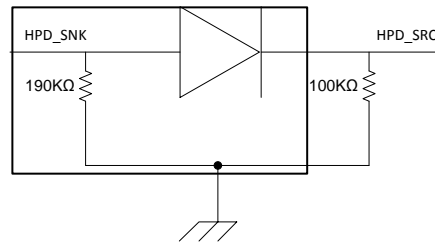
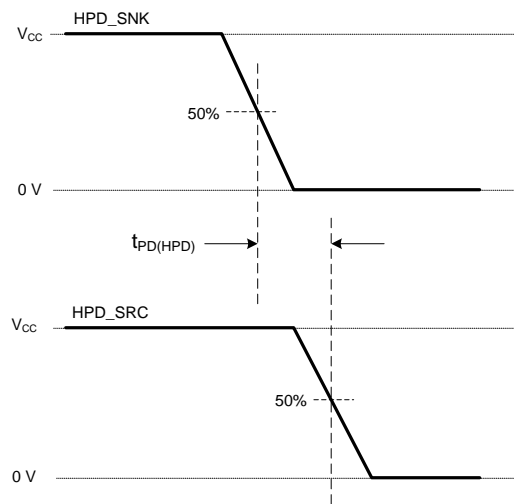


Figure 11. HDMI Output Jitter Measurement

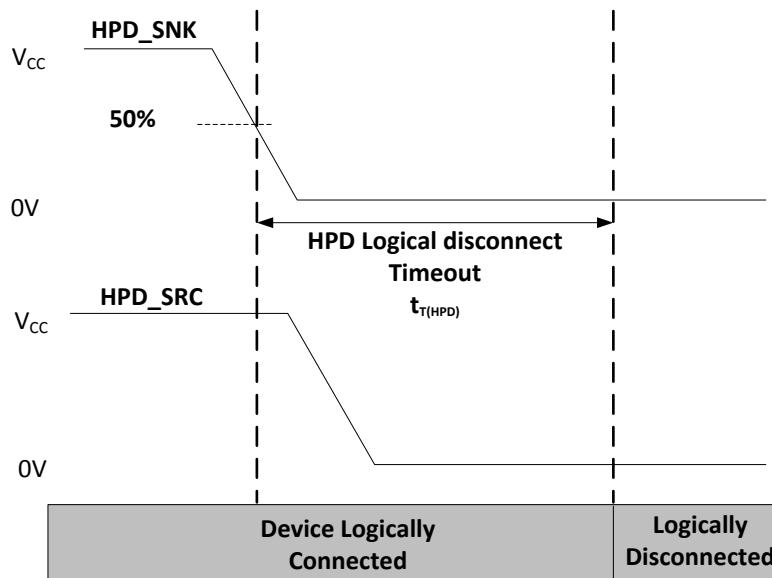
**Parameter Measurement Information (continued)**



**Figure 12. HPD Test Circuit**



**Figure 13. HPD Timing Diagram No. 1**



**Figure 14. HPD Logic Disconnect Timeout**



Parameter Measurement Information (continued)

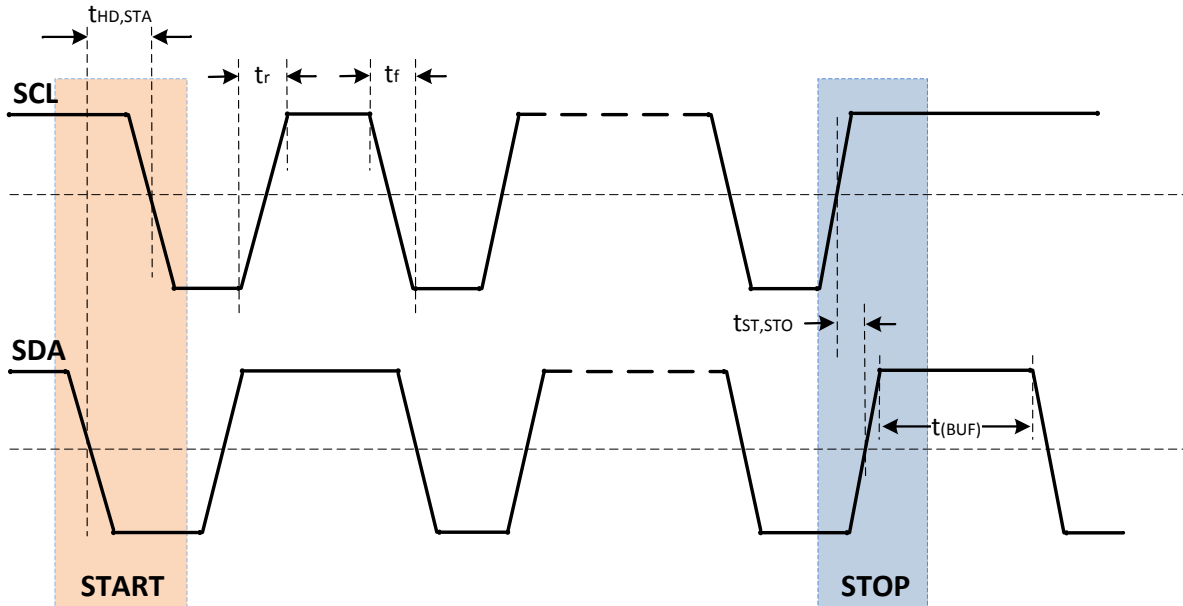


Figure 15. Start and Stop Condition Timing

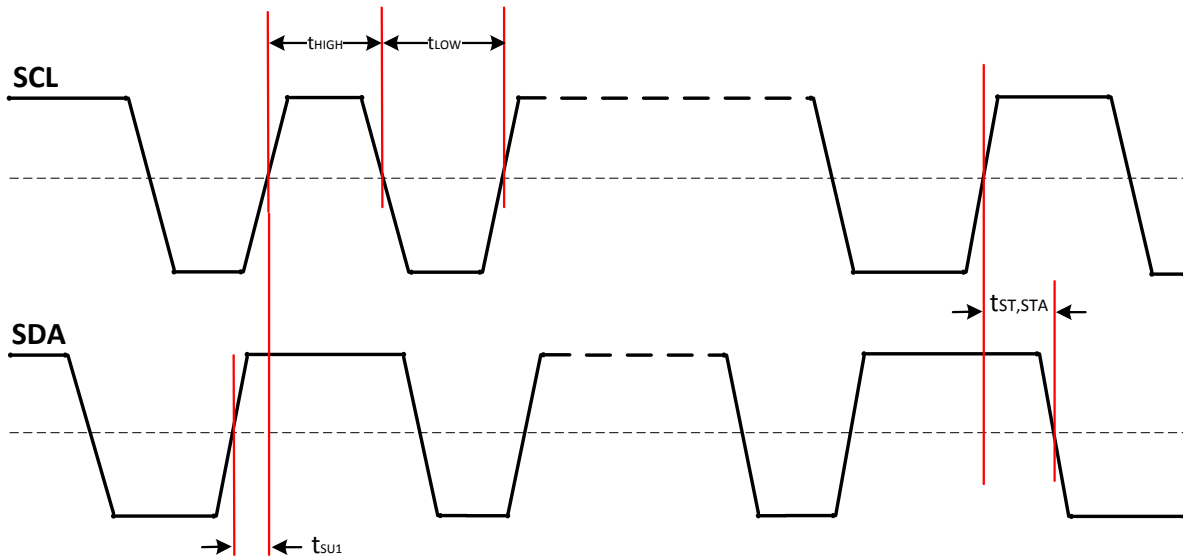
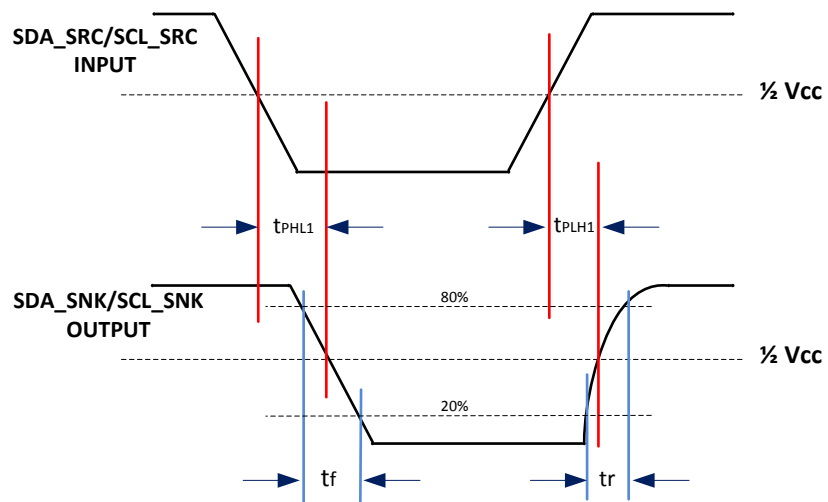
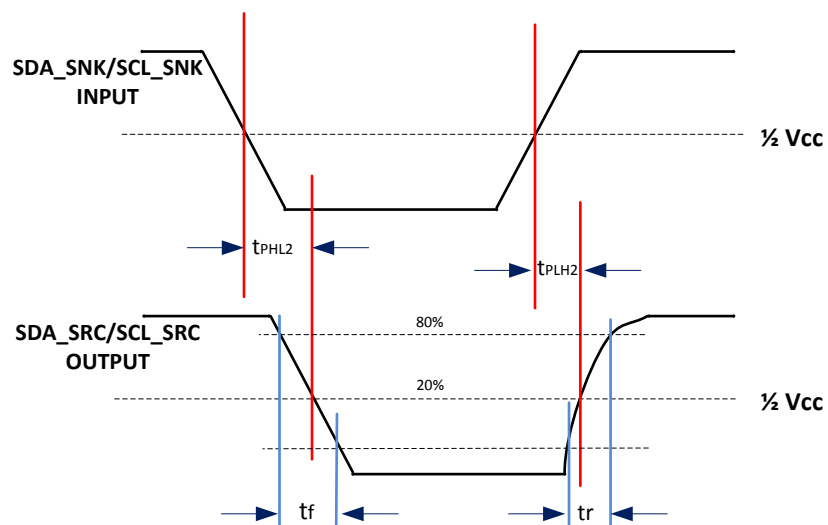


Figure 16. SCL and SDA Timing

**Parameter Measurement Information (continued)**

**Figure 17. DDC Propagation Delay – Source to Sink**

**Figure 18. DDC Propagation Delay – Sink to Source**

Parameter Measurement Information (continued)

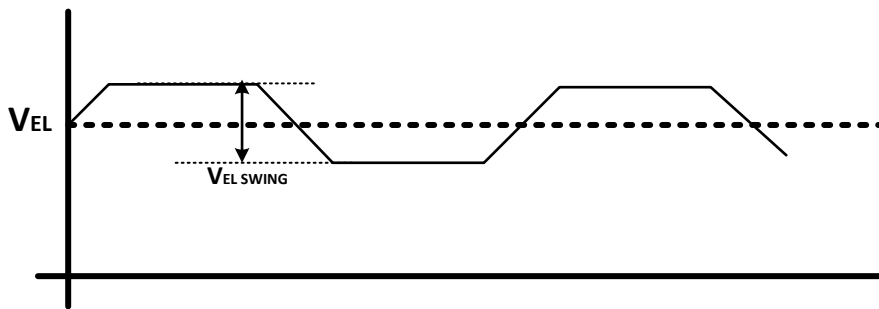
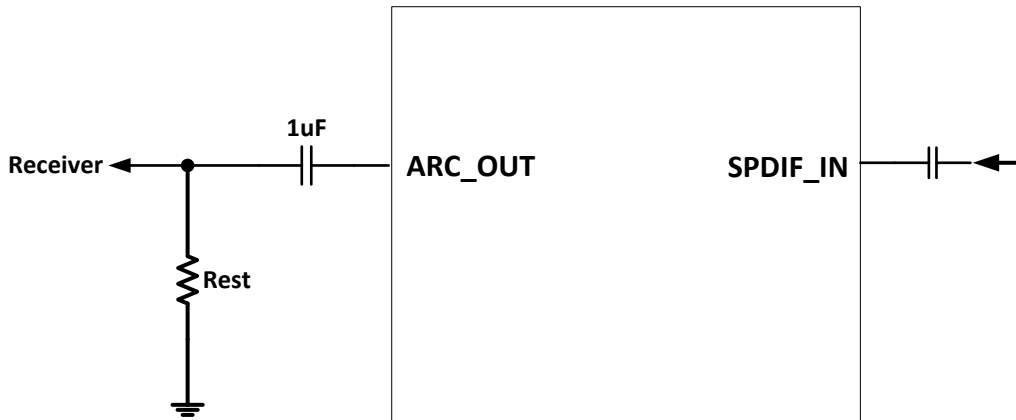


Figure 19. ARC Output

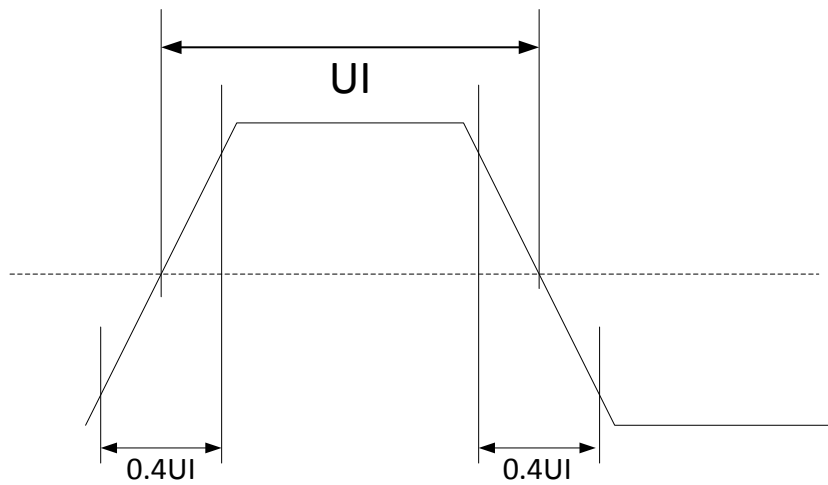


Figure 20. Rise/Fall Time of ARC

## 8 Detailed Description

### 8.1 Overview

The TMDS171 is a digital video interface (DVI) or high-definition multimedia interface (HDMI) retimer. The TMDS171 supports four TMDS channels, Audio Return Channel (SPDIF\_IN/ARC\_OUT), Hot Plug Detect, and a Digital Display Control (DDC) interfaces. The TMDS171 supports signaling rates up to 3.4 Gbps to allow for the highest resolutions of 4k2k30p 24 bits per pixel and up to WUXGA 12-bit color depth or 1080p with higher refresh rates. The TMDS171 can automatically configure itself as a re-driver at low data rate (< 1 Gbps) or as a re-timer above this data rate. For passing compliance and reducing system level design issues several features have been included such as TMDS output amplitude adjust using an external resistor on the VSADJ pin and source termination selection control. Device operation and configuration can be programmed by pin strapping or I<sup>2</sup>C. Four TMDS171s can be used on one I<sup>2</sup>C bus when I2C\_EN enable and device address set by A0/A1.

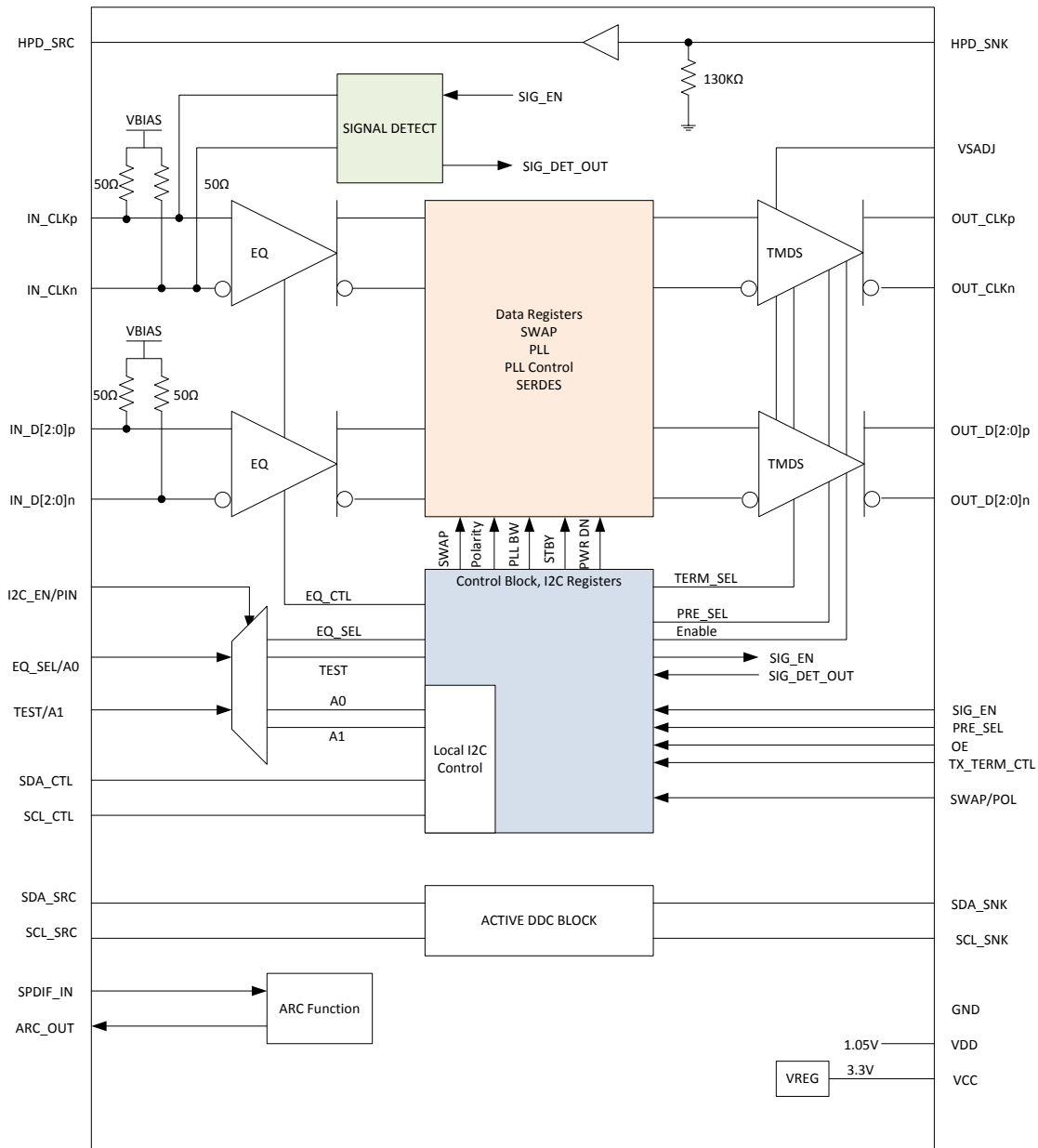
To reduce active power the TMDS171 supports dual power supply rails of 1.2 V on V<sub>DD</sub> and 3.3 V on V<sub>CC</sub>. The TMDS171 supports several methods of power management. It can enter power down mode using three methods; (1) HPD is low; (2) Writing an 1 to register 09h[3]; or (3) de-asserting OE. If using OE, the device must be reprogrammed via I<sup>2</sup>C if it was originally programmed this way. The SIG\_EN pin enables the signal detect circuit that provides an automatic power-management feature during normal operation. When no valid signal is present on the inputs the device enters Stand by mode. By disabling the detect circuit the receiver block is always on. DDC bridge supports 100 Kbps data rate default and 400 kbps adjustable by software.

TMDS171 supports both fixed EQ gain control or adaptive equalization to compensate for different lengths of input cables or board traces. The EQ gain can be software adjusted by I<sup>2</sup>C control or selection between two fixed values or adaptive equalization by pin strapping EQ\_SEL pin. Implementers can use the TX\_TERM\_CTL pin to change the transmitter termination impedance for better output performance when working in HDMI1.4b or leave it floating. When floating the TMDS171 in conjunction with the rate detect will automatically change its output termination to be compatible with HDMI1.4b requirements.

The TMDS171 supports single ended mode audio return channel. To assist in ease of implementation the TMDS171 supports receive lane swapping and receive polarity swap. When swapping the input lanes IN\_CLK and IN\_D2 swap and IN\_D1 and IN\_D0 swap with each other. Swap works in both retimer and re-driver mode. Polarity swap will swap the receive pins n and p channel polarity in each lane and is only available during retimer mode. Both lane swap and polarity swap can be implemented at the same time in retimer mode using I<sup>2</sup>C control.

Two versions of the device are offered to support extended commercial temperature range 0°C to 85°C (TMDS171) or industrial operational temperature range from -40°C to 85°C (TMDS171I).

## 8.2 Functional Block Diagram



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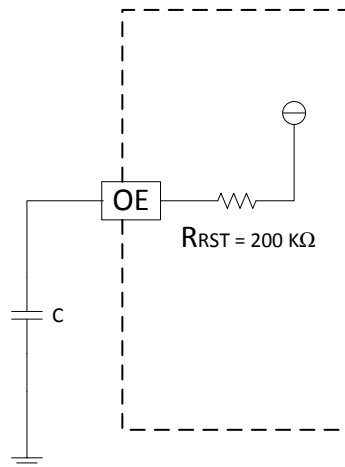
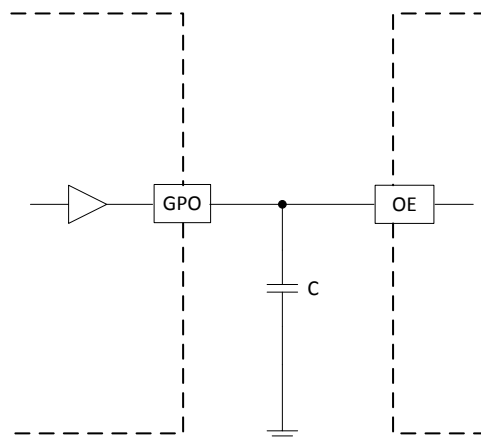
## 8.3 Feature Description

### 8.3.1 Reset Implementation

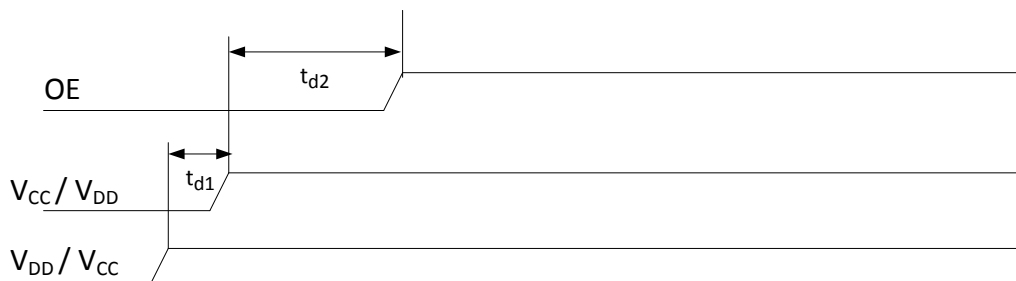
When OE is de-asserted, control signal inputs are ignored; the HDMI inputs and outputs are high impedance. It is critical to transition the OE from a low level to high after the  $V_{CC}$  supply has reached the minimum recommended operating voltage. This is achieved by a control signal to the OE input, or by an external capacitor connected between OE and GND. To insure the TMDS171 is properly reset, the OE pin must be de-asserted for at least 100  $\mu$ s before being asserted. When OE is re-asserted the TMDS171 will have to be reprogrammed if it

**Feature Description (continued)**

was programmed by I<sup>2</sup>C and not pin strapping. When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the V<sub>CC</sub> supply, where a slower ramp-up results in a larger value external capacitor. Refer to the latest reference schematic for TMDS171; consider approximately 200 nF capacitor as a reasonable first estimate for the size of the external capacitor. Both OE implementations are shown in [Figure 21](#) and [Figure 22](#).


**Figure 21. External Capacitor Controlled OE**

**Figure 22. OE Input from Active controller**
**8.3.2 Operation Timing**

TMDS171 starts to operate after the OE signal is properly set after power up timing complete. See [Figure 23](#), [Figure 24](#), [Table 1](#). If OE is held low until V<sub>DD</sub> and V<sub>CC</sub> become stable there is no rail sequence requirement.


**Figure 23. Power up Timing for TMDS171**

Feature Description (continued)

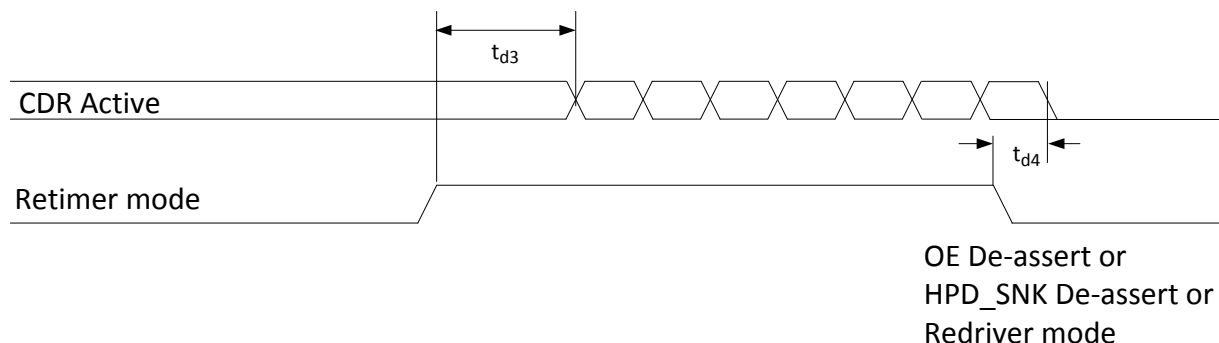


Figure 24. CDR Timing for TMDS171

Table 1. Power Up and Operation Timing Requirements

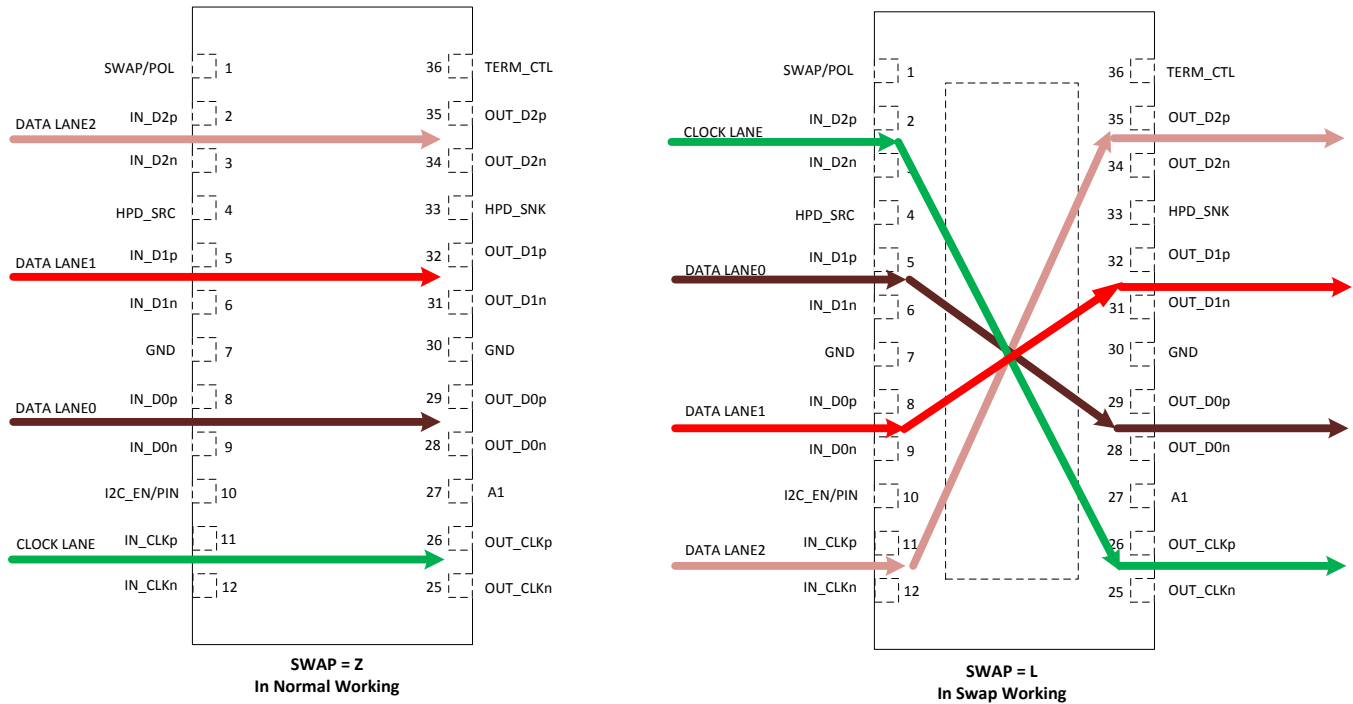
	DESCRIPTION	MIN	TYP	MAX	UNIT
$t_{d1}$	$V_{DD}$ Stable before $V_{CC}$	0		200	$\mu$ s
$t_{d2}$	$V_{DD}$ and $V_{CC}$ stable before OE de-assertion	100			$\mu$ s
$t_{d3}$	CDR active operation after retimer mode initiated			15	ms
$t_{d4}$	CDR turn off time after retimer mode de-assert			120	ns
$V_{DD(ramp)}$	$V_{DD}$ supply ramp up requirements			100	ms
$V_{CC(ramp)}$	$V_{CC}$ supply ramp up requirements			100	ms

8.3.3 Swap and Polarity Working (Retimer Mode Only)

TMDS171 incorporates swap function which can set the input lanes in swap mode. The IN\_D2 will route to the OUT\_CLK position by swapping with IN\_CLK. The IN\_D1 swaps with IN\_D0. The Swap function only changes the input pins. The EQ setup follows the new mapping, see Figure 25. This function can be used with the SWAP/POL pin 1 and control the register 0x09h bit 7 for SWAP enable. The Swap function works in both redriver and retimer mode. The TMDS171 can also swap the input polarity signals. When SWAP/POL is high the n and p pins on each lane will swap. Polarity swap only works when in retimer mode. When this function is enabled and the device is in automatic cross over mode between redriver and retimer modes, care must be taken to avoid losing polarity swap. When the data rate drops to the redriver level, the polarity swap is lost.

Table 2. SWAP Pin Mapping

Normal Op	SWAP = L or CSR 0x09h bit 7 is 1'b1
IN_D2 → OUT_D2	IN_D2 → OUT_CLK
IN_D1 → OUT_D1	IN_D1 → OUT_D0
IN_D0 → OUT_D0	IN_D0 → OUT_D1
IN_CLK → OUT_CLK	IN_CLK → OUT_D2


**Figure 25. TMDS171 Swap Function**

### 8.3.4 TMDS Inputs

Standard TMDS terminations are integrated on all TMDS inputs. External terminations are not required. Each input data channel contains an adaptive or fixed equalizer to compensate for Inter-Symbol Interference (ISI) due to cable, connector, and/or board trace losses. The voltage at the TMDS input pins must be limited under the absolute maximum ratings. TMDS input pins have incorporated failsafe circuits. An unused input channel can be externally biased to prevent output oscillation by connecting the N input pin to be grounded through a 1-kΩ resistor and the other pin left open. The input pins can be polarity changed through local I<sup>2</sup>C register when in retimer mode.

### 8.3.5 TMDS Inputs Debug Tools

There are two methods for debugging a system to make sure the inputs to the TMDS171 are valid. A TMDS error checker is implemented to provide a rough Bit Error Rate per data lane. This allows the system implementer to determine how the link between the source and TMDS171 is performing on all three data lanes. See *CSR BIT FIELD DEFINITIONS – RX PATTERN VERIFIER CONTROL/STATUS* register.

If a high error count is evident the TMDS171 has a way to view the general receiver eye quality. A tool is available that uses the I<sup>2</sup>C link to download the data that can be plotted for an eye diagram. This is available per data lane. This tool also provides a method to turn on an internal PRBS generator that will transmit a data signal on the data pins. A clock at the proper frequency is required on the IN\_CLK pins to generate the expected output data rate.

### 8.3.6 Receiver Equalizer

The equalizer used to clean up inter-symbol interference (ISI) jitter/loss from the bandwidth-limited board traces or cables. TMDS171 supports fixed receiver equalizer and adaptive equalizer by setting the EQ\_SEL/A0 pin or through I<sup>2</sup>C. When EQ\_SEL/A0 is high, the EQ gain is fixed to 10 dB and when set low the EQ gain is set to 7.5 dB. TMDS171 operates in adaptive equalizer mode when EQ\_SEL/A0 pin is left floating. The EQ gain will be automatically adjusted based on the data rate to compensate for trace or cable loss. Implementers can enable the various EQ settings through local I<sup>2</sup>C control.



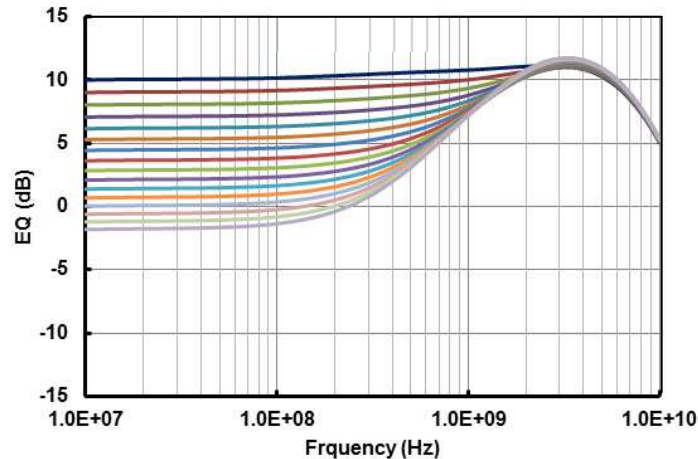


Figure 26. Adaptive EQ Gain Curve

### 8.3.7 Input Signal Detect Block

When SIG\_EN is enabled, the TMDS looks for a valid TMDS clock signal input. The terminations on the TMDS data lines are connected and the device is fully functional when a valid signal is detected. If no valid TMDS clock signal is detected, the device enters standby mode waiting for a valid signal at the clock input. The internal CDR is shut down and all of the TMDS outputs are in high-Z status. TMDS signal detect circuit can be set as enable by SIG\_EN pin or through local I<sup>2</sup>C control but is default disabled. Designers are recommended to activate this function in normal operation for power saving.

### 8.3.8 Audio Return Channel

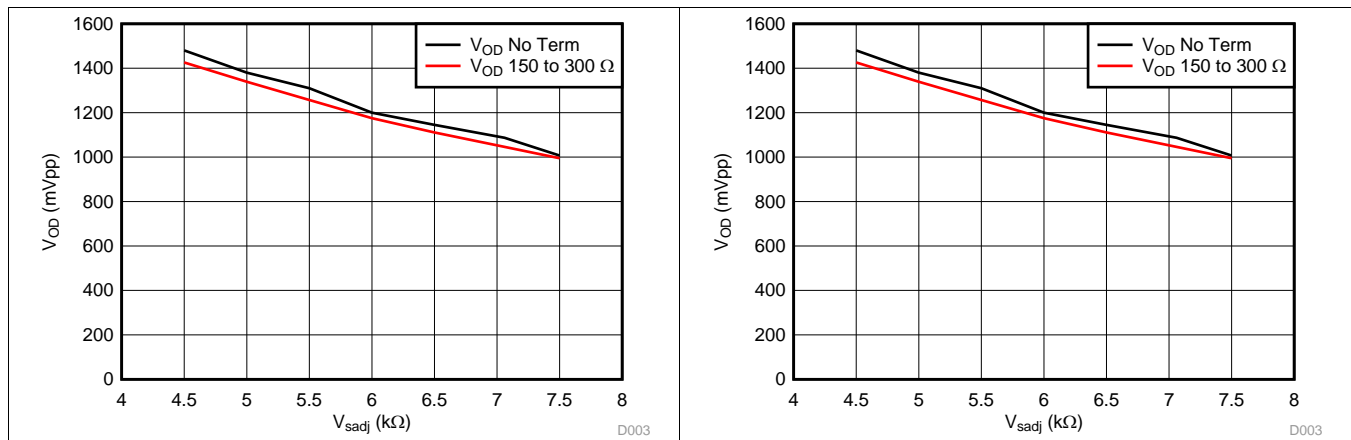
The Audio Return Channel in TMDS171 enables a TV, via a single HDMI cable, to send audio data “upstream” to an A/V receiver or surround audio controller, increasing user flexibility and eliminating the need for any separate S/PDIF audio connection. The TMDS171 supports single mode audio return channel. Implementers can send the S/PDIF signal to SPDIF\_IN. The signal from ARC\_OUT is sent to HDMI connectors and is passed through the general HDMI cable to audio receiver. By I<sup>2</sup>C control, customer can disable ARC\_OUT by register. Enabled by default after initialization.

### 8.3.9 Transmitter Impedance Control

Source termination is disabled at data rates < 2 Gbps. When the data rate is between 2 Gbps and 3.4 Gbps, the output signal may be better if the termination value around 150 Ω to 300 Ω depending upon system implementation. TMDS171 supports two different source termination impedances for ease of implementation. Pin 36, TX\_TERM\_CTL, offers a selection option to choose the output termination impedance value.

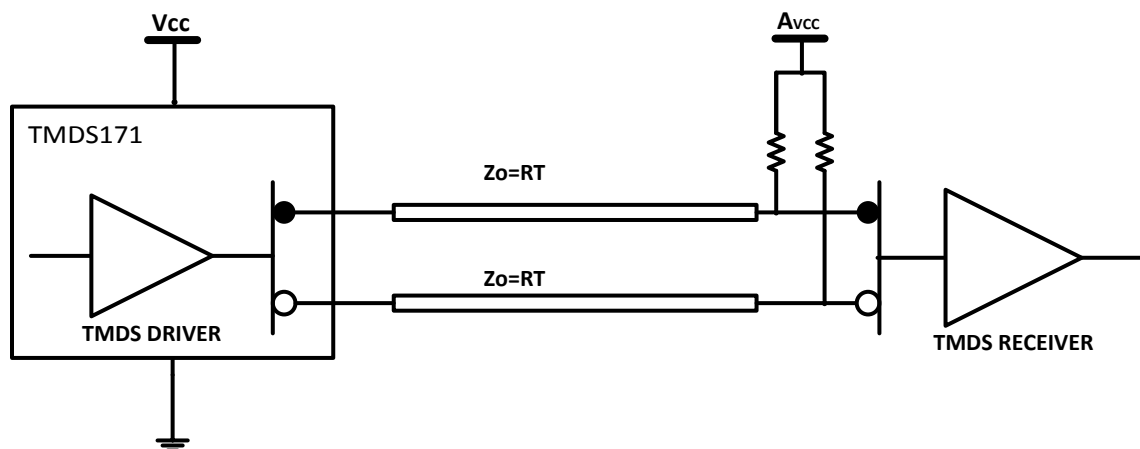
Table 3. TX Termination Control

Control Pin 36	DESCRIPTION
TX_TERM_CTL = H	The transmit Termination is disabled
TX_TERM_CTL = L	Reserved
TX_TERM_CTL = Z	Automatic select the impedance <ul style="list-style-type: none"> <li>2 Gbps &gt; DR &lt; 3.4 Gbps – 150 - 300 Ω differential near end termination</li> <li>DR &lt; 2 Gbps – no termination</li> </ul>



### 8.3.10 TMDS Outputs

A 1% precision resistor, 7.06 k $\Omega$ , connected from VSADJ to ground is recommended to allow the differential output swing to comply with TMDS signal levels. The differential output driver provides a typical 10 mA current sink capability, which provides a typical 500 mV voltage drop across a 50  $\Omega$  termination resistor.



**Figure 27. TMDS Driver and Termination Circuit**

In [Figure 27](#), if  $V_{CC}$  (TMDS171 supply) and  $AVCC$  (sink termination supply) are both powered, the TMDS output signals are high impedance when  $OE = high$ . Both supplies being active are the normal operating condition. Again refer to [Figure 27](#), if  $V_{CC}$  is on and  $AVCC$  is off, the TMDS outputs source a typical 5 mA current through each termination resistor to ground. A total of 33 mW of power is consumed by the terminations independent of the OEB logical selection. When  $AVCC$  is powered on, normal operation ( $OE$  controls output impedance) is resumed. When the power source of the device is off and the power source to termination is on, the  $IO(off)$ , output leakage current, specification ensures the leakage current is limited to 45  $\mu A$  or less. The  $PRE\_SEL$  pin provides  $-2$  dB de-emphasis gain, allowing output signal pre-conditioning to offset interconnect losses from the TMDS171 outputs to a TMDS receiver. De-emphasis is recommended to be set at 0 dB while connecting to a receiver through short PCB route. The  $V_{OD}$  of the data lanes and clock lane can be adjusted through I<sup>2</sup>C. See [Table 11](#) for detail. [Figure 1](#) shows the different output voltages based on the different VSADJ settings.

### 8.3.11 Pre-Emphasis/De-Emphasis

The TMDS171 provides de-emphasis as a way to compensate for ISI loss between the TMDS171 outputs and a TMDS receiver. There are two methods to implement this function. When in pin strapping mode the PRE\_SEL pin controls this function. The PRE\_SEL pin provides - 2 dB or 0 dB de-emphasis, which allows the output signal pre-conditioning. De-emphasis is recommended to be set at 0-dB while connecting to a receiver through short PCB traces. When pulled to ground through a 65 kΩ resistor - 2 dB can be realized, see Figure 9. When using I<sup>2</sup>C, reg0Ch[1:0] is used to make these adjustments.

As there are times that true pre-emphasis may be the best solution there are two methods to accomplish this. If pin strapping is being used the best method is to reduce the VSADJ resistor value thus increasing the V<sub>OD</sub> swing and then pulling the PRE\_SEL pin to ground using a 65 kΩ resistor, see Figure 28. If using I<sup>2</sup>C there are two methods to accomplish this. The first is similar to pin strapping but reducing VSADJ resistor value and then implementing - 2 db de-emphasis through I<sup>2</sup>C, reg0Ch[1:0] = 01. The second method is to increase the VOD swing by setting reg0Ch[7:5] = 011 and reg0Ch[1:0] = 01 which will accomplish the same pre-emphasis value, see Figure 29. Note: De-emphasis is only implement able during retimer mode. In redriver mode this function is not available.

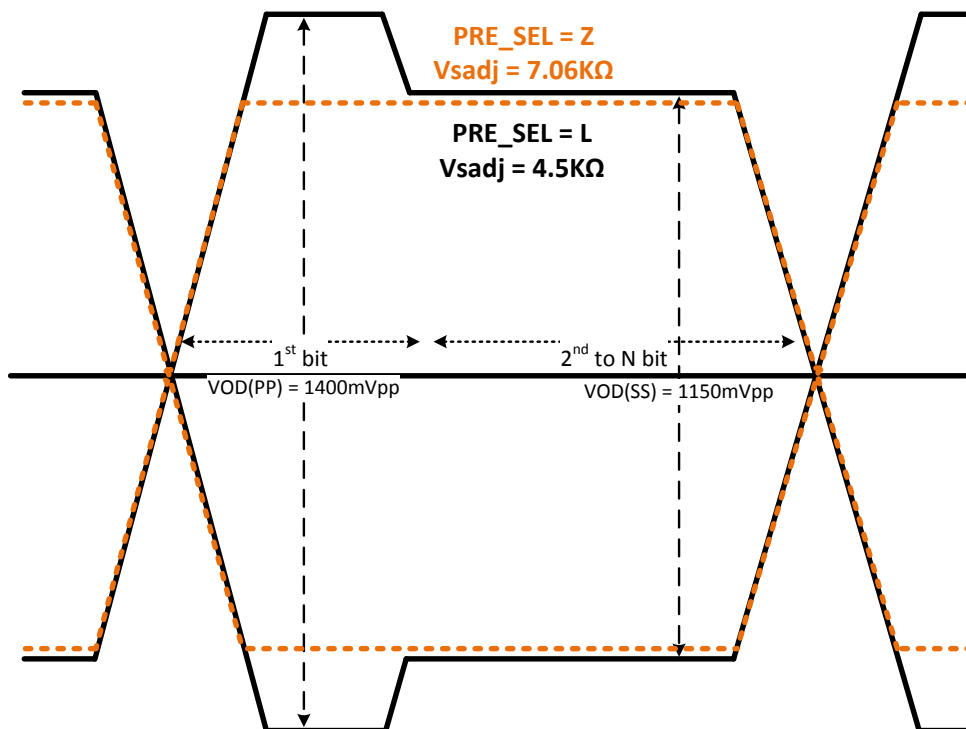
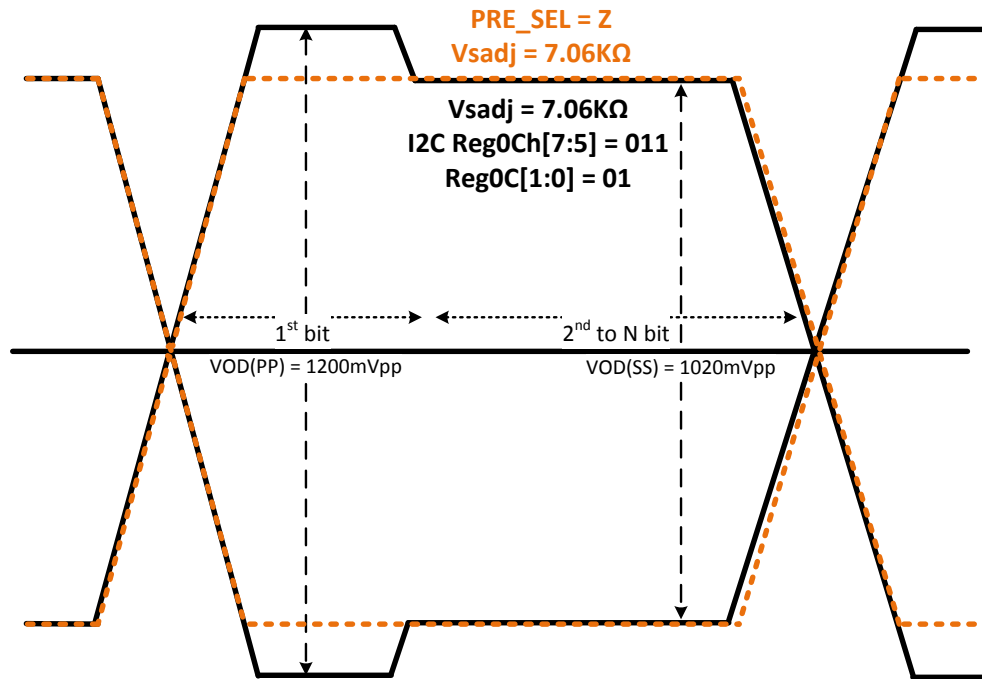


Figure 28. Pre-emphasis Using Pin Strapping


**Figure 29. Pre-emphasis Using I<sup>2</sup>C**

## 8.4 Device Functional Modes

### 8.4.1 Retimer Mode

Clock and Data Recovery Circuits (CDR) are used to track, sample and retimer the equalized data bit streams. The CDRs are designed with loop bandwidth to minimize the amount of jitter transfer from the video source to the TMDS outputs. Input jitter within the CDR's PLL bandwidth, < 1 MHz, is transferred to the TMDS outputs. Higher frequency jitter above the CDR loop bandwidth is attenuated, providing a jitter cleaning function to reduce the amount of high frequency jitter from the video source. The retimer is automatically activated at pixel clock above approximately 100 MHz when jitter cleaning is needed for robust operation. The retimer operates at about 100 MHz – 340 MHz pixel clock (1 – 3.4 Gbps). At pixel clock below about 100 MHz, the TMDS171 automatically bypasses the internal retimer, and operates as a redriver. When the video source changes resolution, the internal retimer starts the acquisition process to determine the input clock frequency and acquire lock to the new data bit streams. During the clock frequency detection period and the retimer acquisition period that last approximately 7 ms, the TMDS drivers can be kept active (default) or programmed to be disabled to avoid sending invalid clock or data to the downstream receiver. The TMDS171 can support retimer mode across the full data rate range of 250 Mbps - 3.4 Gbps by setting DEV\_FUNC\_MODE bits at reg0Ah[1:0], See [Table 9](#). For compliance testing such as JTOL for 480 Mbps the PLL must be forced to lock.

### 8.4.2 Redriver Mode

The TMDS171 can function as a redriver which compensates for ISI channel loss. In this mode, power is reduced as the CDR and PLL are turned off. When in automatic mode, the TMDS171 is in redriver mode for data rates < 1.0 Gbps. By using I<sup>2</sup>C the device can be put in Redriver mode for the complete data rate range of 250 Mbps to 3.4 Gbps. This is done by writing a 00 to register 0Ah[1:0]. If the link has excessive random jitter then retimer mode is the best operating mode. If the link has excessive random jitter, the retimer mode is the best operating mode. When in redriver mode, the device compensates for ISI loss only. When in redriver mode compliance is not ensured as skew compensation and retiming functions are disabled. If a significant amount of random jitter is present, the system may not pass compliance at the connector.

## Device Functional Modes (continued)

### 8.4.3 DDC Functional Description

The TMDS171 solves sink/source level issues by implementing a master/slave control mode for the DDC bus. When the TMDS171 detects the start condition on the DDC bus from the SDA\_SRC/SCL\_SRC, it transfers the data or clock signal to the SDA\_SNK/SCL\_SNK with little propagation delay. When SDA\_SNK detects the feedback from the downstream device, the TMDS171 pulls up or pulls down the SDA\_SRC bus and delivers the signal to the source.

The DDC link defaults to 100 kbps but can be set to various values including 400 kbps by setting the correct value to address 0Bh through the I<sup>2</sup>C interface. The DDC lines are 5 V tolerant when the device is powered off. The HPD goes to high impedance when VCC is under low power conditions < 1.5 V.

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#### NOTE

The TMDS171 utilizes clock stretching for DDC transactions. As there are sources and sinks that do not perform this function correctly as system may not work correctly as DDC transactions are incorrectly transmitted/received. To overcome this a snoop configuration can be implemented where the SDA/SCL from the source is connected directly to the SDA/SCL sink. The TMDS171 will need its SDA\_SNK and SCL\_SNK pins connected to this link.

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### 8.4.4 Mode Selection Functional Description

Mode Selection Definition: reg0Ah[7] is the mode select register, see [Table 9](#). This bit lets the receiver know where the device is located in a system for the purpose of centering the AEQ point. The TMDS171 is targeting sink or dock applications so the default value is 1 which centers the EQ at 12 dB to 13 dB, see [Table 12](#). If the TMDS171 is in a source application the value should be changed to a 0 which centers the EQ at 6.5 dB to 7.5 dB.

## 8.5 Register Maps

### 8.5.1 Local I<sup>2</sup>C Overview

The TMDS171 local I<sup>2</sup>C interface is enabled when I2C\_EN/PIN is high. The SCL\_CTL and SDA\_CTL terminals are used for I<sup>2</sup>C clock and I<sup>2</sup>C data respectively. The TMDS171 I<sup>2</sup>C interface conforms to the two-wire serial interface defined by the I<sup>2</sup>C Bus Specification, Version 2.1 (January 2000), and supports the fast mode transfer up to 400 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for TMDS171 decides by the combination of EQ\_SEL/A0 and A1. Table 4 clarifies the TMDS171 target address.

**Table 4. TMDS171 I2C Device Address Description**

TMDS171 I2C Device Address									
A1/A0	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)	HEX
00	1	0	1	1	1	1	0	0/1	BC/BD
01	1	0	1	1	1	0	1	0/1	BA/BB
10	1	0	1	1	1	0	0	0/1	B8/B9
11	1	0	1	1	0	1	1	0/1	B6/B7

The typical source application of the TMDS171 is as a retimer in a TV connecting the HDMI input connector and an internal HDMI receiver through flat cables. The register setup can adjust by source side. When TMDS171 used in sink side application, it received data from input connector and transmit to receiver. The local I<sup>2</sup>C is not 5 V tolerant and only support 3.3 V. Local I2C buses run at 400 kHz supporting fast-mode I<sup>2</sup>C operation.

The following procedure is followed to write to the TMDS171 I<sup>2</sup>C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TMDS171 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The TMDS171 acknowledges the address cycle
3. The master presents the sub-address (I<sup>2</sup>C register within TMDS171) to be written, consisting of one byte of data, MSB-first
4. The TMDS171 acknowledges the sub-address cycle
5. The master presents the first byte of data to be written to the I<sup>2</sup>C register
6. The TMDS171 acknowledges the sub-address cycle
7. TMDS171 acknowledges the byte transfer
8. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TMDS171
9. The master terminates the write operation by generating a stop condition (P)

The following procedure is followed to read the TMDS171 I<sup>2</sup>C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TMDS171 7-bit address and a one-value “W/R” bit to indicate a read cycle
2. The TMDS171 acknowledges the address cycle
3. The TMDS171 transmit the contents of the memory registers MSB-first starting at register 00h.
4. The TMDS171 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I<sup>2</sup>C master acknowledges reception of each data byte transfer
5. If an ACK is received, the TMDS171 transmits the next byte of data
6. The master terminates the read operation by generating a stop condition (P)

#### NOTE

Nno sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I<sup>2</sup>C master terminates the read operation.

Refer to [Table 4](#) for TMDS171 local I<sup>2</sup>C register descriptions. Reads from reserved fields not described return zeros, and writes are ignored.

### 8.5.1.1 BIT Access Tag Conventions

A table of bit descriptions is typically included for each register description that indicates the bit field name, field description, and the field access tags. The field access tags are described in [Table 5](#).

**Table 5. Access Tags**

ACCESS TAG	NAME	DESCRIPTION
R	Read	The field shall be read by software
W	Write	The field shall be written by software
S	Set	The field shall be set by a write of one. Writes of Zero to the field have no effect
C	Clear	The field shall be cleared by a write of one. Writes of Zero to the field have no effect
u	Update	Hardware may autonomously update this field
NA	No Access	Not accessible or not applicable

### 8.5.2 CSR Bit Field Definitions, DEVICE\_ID (offset: 00000000 ≈ 00000111) (reset:00h ≈ 07h)

**Figure 30. CSR Bit Field Definitions, DEVICE\_ID (00h ≈ 07h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 6. CSR Bit Field Definitions, DEVICE\_ID (00h ≈ 07h)**

Bit	Field	Type	Reset	Description
7:0	DEVICE_ID	R	00h ≈ 07h	These fields return a string of ASCII characters "TMDS171" preceded by one space characters. TMDS171: 0x00 – 0x07 = { - 0x54"T", 0x4D"M", 0x44"D", 0x53"S", 0x31"1", 0x37"7", 0x31"1", 0x20},

### 8.5.3 CSR Bit Field Definitions, REV\_ID (offset: 00001000) (reset: 01h)

**Figure 31. CSR Bit Field Definitions, REV\_ID (08h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 7. CSR Bit Field Definitions, REV\_ID (08h)**

Bit	Field	Type	Reset	Description
7:0	REV_ID	R	01h	This field identifies the device revision. 0000001– TMDS171 Revision 1

**8.5.4 CSR BIT Field Definitions – Misc Control (offset: 00001001) (reset: 02h)**
**Figure 32. CSR Bit Field Definitions – Misc Control (09h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	0
R/W/U	R/W/U	R	R/W/U	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 8. CSR Bit Field Definitions – Misc Control (09h)**

Bit	Field	Type	Reset	Description
7	Lane_SWAP	R/W/U	1'b0	This field Swaps the input lanes as per <a href="#">Figure 25</a> . 0 --- Disable (default) No Lane Swap 1 --- enable: Swaps input lanes (Redriver and Retimer Mode) Note: field is loaded from SWAP/POL pin; Writes are ignored when I2C_EN/PIN = 0
6	LANE_POLARITY	R/W/U	1'b0	Swaps the input Data and Clock lanes polarity. 0 – Disabled: No polarity swap 1 – Swaps the input Data and Clock lane polarity (Retimer Mode Only) Note: field is loaded from SWAP/POL pin; Writes are ignored when I2C_EN/PIN = 0
5	Reserved	R	1'b0	Reserved
4	SIG_EN	R/W/U	1'b0	This field enable the clock lane activity detect circuitry. 0 – Disable(Default) Clock detector circuit closed and receiver always works in normal operation. 1 – Enable , Clock detector circuit will make receiver automatic enter the standby state when no valid data detect. Note: field is loaded from SIG_EN pin; Writes are ignored when I2C_EN/PIN = 0
3	PD_EN	R/W	1'b0	0 – Normal working (default) 1 – Forced Power down by I <sup>2</sup> C, Lowest Power state
2	HPD_AUTO_PWRDWN_DISABLE	R/W	1'b0	0 – Automatically enters power down mode based on HPD_SNK (default) 1 – Will not automatically enter power down mode
1:0	I2C_DR_CTL	R/W	2'b10	I <sup>2</sup> C data rate supported for configuring device. 00 – 5 Kbps 01 – 10 Kbps 10 – 100 Kbps(default) 11 – 400 Kbps (Note: HPD_AUTO_PWRDWN_DISABLE must be set before enabling 400 Kbps mode)



**8.5.5 CSR BIT Field Definitions – Misc Control (offset: 00001010) (reset: B1h)**
**Figure 33. CSR Bit Field Definitions – Misc Control (0Ah)**

7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	1
R/W	R/W	R/W	R/W	R	W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 9. CSR Bit Field Definitions – Misc Control (0Ah)**

Bit	Field	Type	Reset	Description
7	Application Mode Selection	R/W	1'b1	See <i>Mode Selection</i> TMDS171 0 – Source 1 – Sink (Default)
6	HPDSNK_GATE_EN	R/W	1'b0	Swaps the input Data and Clock lanes polarity. The field set the HPD_SNK signal pass through to HPD_SRC or not and HPD_SRC whether held in the de-asserted state. 0 – HPD_SNK passed through to the HPD_SRC ( default ) 1 – HPD_SNK will not pass through to the HPD_SRC.
5	EQ_ADA_EN	R/W	1'b1	This field enable the equalizer functioning state; Writes are ignored when I2C_EN/PIN = 0 0 – Fixed EQ 1 – Adaptive EQ (default)
4	EQ_EN	R/W	1'b1	This field enable the Equalizer; Writes are ignored when I2C_EN/PIN = 0 0 -- EQ disable 1 – EQ enable (default)
3	Reserved	R	1'b0	Reserved
2	APPLY_RXTX_CHANGES	W	1'b0	Self-clearing write-only bit. Writing a 1 to this bit will apply new TX_TERM, HDMI_TWPST1, EQ_EN, EQ_ADA_EN, VSWING, Fixed EQ value settings to the clock and data lanes. Writes to the respective registers do not take immediate effect. This bit does not need to be written if I <sup>2</sup> C configuration occurs while OE or HPD_SNK are low, I2C PD_EN=1 or there is no HDMI clock applied and SIG_EN is high.
1:0	DEV_FUNC_MODE.	R/W	2'b01	This field selects the Device Working Function Mode. 00 – Redriver Mode across full range 250 Mbps – 3.4 Gbps 01 - Automatic Redriver to Retimer Cross Over at 1.0 Gbps (default) 10 - Reserved 11 - Retimer Mode across full range 250 Mbps – 3.4 Gbps When changing crossover point, need to toggle PD_EN or toggle external HPD_SNK.

**8.5.6 CSR BIT Field Definitions – Misc Control (offset: 00001011) (reset: 00h)**
**Figure 34. CSR Bit Field Definitions – Misc Control (0Bh)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R/W/U	R/W/U	R/W	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 10. CSR Bit Field Definitions – Misc Control (0Bh)**

Bit	Field	Type	Reset	Description
7:5	Reserved	R	2'b000	Reserved
4:3	TX_TERM_CTL	RWU	2'b00	Controls termination for HDMI TX; Writes are ignored when I2C_EN/PIN = 0 00 – No termination 01 – 150 to 300 Ω 10 – Reserved. 11 – Reserved
2	DDC_DR_SEL	R/W	1'b0	Defines the DDC output speed for both DDC bridge and AUX-DDC Bridge. 0 = 100 kbps (default) 1 = 400 kbps (Note: HPD_AUTO_PWRDWN_DISABLE must be set before enabling 400 Kbps mode)
1:0	Reserved	R	2'b00	Reserved

**8.5.7 CSR BIT Field Definitions – Misc Control (offset: 00001100) (reset: 00h)**
**Figure 35. CSR Bit Field Definitions – Misc Control (0Ch)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W/U	R/W/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 11. CSR Bit Field Definitions – Misc Control (0Ch)**

Bit	Field	Type	Reset	Description
7:5	VSWING_DATA	R/W	3'b000	Data Output Swing Control (Need Design input on what is available) 000 – Vsadj set (default) 001 – Increase by 7% 010 – Increase by 13% 011 – Increase by 18% 100 – Decrease by 30% 101 – Decrease by 22% 110 – Decrease by 15% 111 – Decrease by 7%
4:2	VSWING_CLK	R/W	13'b000	Clock Output Swing Control: Default is set by DR which means standard based swing values but this allows for the swing to be overridden by selecting one of the following values. 000 – Set by Data Rate 001 – Increase by 7% 010 – Increase by 13% 011 – Increase by 18% 100 – Decrease by 30% 101 – Decrease by 22% 110 – Decrease by 15% 111 – Decrease by 7%
1:0	HDMI_TWPST1[1:0]	R/W/U	2'b00	HDMI pre-emphasis FIR post-cursor-1 signed tap weight. 00 – No pre-emphasis 01 – 2 dB pre-emphasis. 10 – Reserved 11 – Reserved Note: Reflects value of PRE_SEL pin; Writes are ignored when I2C_EN/PIN = 0

**8.5.8 CSR BIT Field Definitions – Equalization Control Register (offset: 00001101) (reset: 01h)**
**Figure 36. CSR BIT Field Definitions – Equalization Control Register (0Dh)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1
R	R	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 12. CSR BIT Field Definitions – Equalization Control Register (0Dh)**

Bit	Field	Type	Reset	Description
7:6	Reserved	R	2'b00	Reserved
5:3	Data Lane EQ	R/W	1'b000	Sets Fixed EQ Values 000 – 0 dB 001 – 4.5 dB 010 – 6.5 dB 011 – 8.5 dB 100 – 10.5 dB 101 – 12 dB 110 – 14 dB 111 – 16.5 dB
2:1	Clock Lane EQ	R/W	13'b000	- Sets Fixed EQ Values. 00 – 0 dB 01 – 1.5 dB 10 – 3 dB 011 – RSVD
0	Reserved	R	1'b1	Reserved

**8.5.9 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00001110) (reset: 00h)**
**Figure 37. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (0Eh)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 13. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (0Eh)**

Bit	Field	Type	Reset	Description
7:4	PV_SYNC[3:0]	R/W	4'b0000	Pattern timing pulse. This field is updated for 8UI once every cycle of the PRBS generator. 1 bit per lane.
3:0	PV_LD[3:0]	R/W	4'b0000	Load pattern-verifier controls into RX lanes. When asserted high, the PV_TO, PV_SEL, PV_LEN, PV_CP20, and PV_CP values are enabled into the corresponding RX lane. These values are then latched and held when PV_LD[n] is subsequently de-asserted low. 1 bit per lane.

**8.5.10 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00001111) (reset: 00h)**
**Figure 38. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (0Fh)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/U	R/U	R/U	R/U	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 14. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (0Fh)**

Bit	Field	Type	Reset	Description
7:4	PV_SYNC[3:0]	R/U	4'b0000	Pattern verification mismatch detected. 1 bit per lane.
3:0	PV_LD[3:0]	R/U	4'b0000	Pattern search/training in progress. 1 bit per lane.

**8.5.11 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00010000) (reset: 00h)**
**Figure 39. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (10h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 15. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (10h)**

Bit	Field	Type	Reset	Description
7	PV_CP20	R/W	1'b0	Customer pattern length 20/16 bits. 0 – 16 bits 1 – 20 bits
6	Reserved	R	1'b0	Reserved
5:3	PV_LEN[2:0]	R,W	3'b000	JPRBS pattern length 000 – PRBS7 001 – PRBS11 010 – PRBS23 011 – PRBS31 100 – PRBS15 101 – PRBS15 110 – PRBS20 111 – PRBS20
2:0	PV_SEL[24:0]	R/W	3'b000	Pattern select control 000 – Disabled 001 – PRBS 010 - Clock 011 - Custom 1xx – Timing only mode with sync pulse spacing defined by PV_LEN

**8.5.12 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00010001) (reset: 00h)**
**Figure 40. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (11h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 16. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (11h)**

Bit	Field	Type	Reset	Description
7	PV_CP[7:0]	R/W	'h00	Custom pattern data.

**8.5.13 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00010010) (reset: 00h)**
**Figure 41. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (12h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 17. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (12h)**

Bit	Field	Type	Reset	Description
7	PV_CP[15:8]	R/W	'h00	Custom pattern data.

**8.5.14 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00010011) (reset: 00h)**
**Figure 42. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (13h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 18. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (13h)**

Bit	Field	Type	Reset	Description
7:4	Reserved	R	4'b0000	Reserved
3:0	PV_CP[19:16]	R/W	4'b0000	Custom pattern data. Used when PV_CP20 = 1'b1.

**8.5.15 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00010100) (reset: 00h)**
**Figure 43. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (14h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 19. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (14h)**

Bit	Field	Type	Reset	Description
7:3	Reserved	R	5'b00000	Reserved
2:0	PV_THR[2:0]	R/W	3'b000	Pattern-verifier retain threshold.

**8.5.16 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00010101) (reset: 00h)**
**Figure 44. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (15h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R/S/U	R/S/U	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 20. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (15h)**

Bit	Field	Type	Reset	Description
7	DESKEW_CMPLT	R	1'b0	Indicates that TMDS lane deskew has completed when high.
6:5	Reserved	R	2'b00	Reserved
4	BERT_CLR	R/S/U	1'b0	Clear BERT counter (on rising edge).
3	TST_INTQ_CLR	R/S/U	1'b0	Clear latched interrupt flag.
2:0	TST_SEL[2:0]	R/W	3'b000	Test interrupt source select.

**8.5.17 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00010110) (reset: 00h)**
**Figure 45. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (16h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 21. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (16h)**

Bit	Field	Type	Reset	Description
7:4	PV_DP_EN[3:0]	R/W	4'b0000	Enable datapath verified based on DP_TST_SEL, 1 bit per lane
3	Reserved	R	1'b0	Reserved
2:0	DP_TST_SEL[2:0]	R/W	3'b000	Selects pattern reported by BERT_CNT[11:0], TST_INT[0] and TST_INTQ[0] and PV_DP_EN is non-zero. 000 – TMDS disparity or data errors 001 – FIFO errors 010 – FIFO overflow errors 011 – FIFO underflow errors 100 – TMDS deskew status 101,110,111 – Reserved.

**8.5.18 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00010111) (reset: 00h)**
**Figure 46. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (17h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/U	R/U	R/U	R/U	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 22. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (17h)**

Bit	Field	Type	Reset	Description
7:4	TST_INTQ[3:0]	R/U	4'b0000	Latched interrupt flag. 1 bit per lane
3:0	RTST_INT[3:0]	R/U	4'b0000	Test interrupt flag. 1 bit per lane.

**8.5.19 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00011000) (reset: 00h)**
**Figure 47. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (18h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/U	R/U	R/U	R/U	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 23. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (18h)**

Bit	Field	Type	Reset	Description
7:0	BERT_CNT[7:0]	R/U	'h00	BERT error count. Lane 0

**8.5.20 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00011001) (reset: 00h)**
**Figure 48. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (19h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 24. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (19h)**

Bit	Field	Type	Reset	Description
7:4	Reserved	R	4'b0000	Reserved
3:0	BERT_CNT[11:8]	R/U	4'b0000	BERT error count. Lane 0

**8.5.21 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00011010) (reset: 00h)**
**Figure 49. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Ah)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/U	R/U	R/U	R/U	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 25. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Ah)**

Bit	Field	Type	Reset	Description
7:0	BERT_CNT[19:12].	R/U	'h00	BERT error count. Lane 1

**8.5.22 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00011011) (reset: 00h)**
**Figure 50. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Bh)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 26. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Bh)**

Bit	Field	Type	Reset	Description
7:4	Reserved	R	4'b0000	Reserved
3:0	BERT_CNT[23:20]	R/U	4'b0000	BERT error count. Lane 1

**8.5.23 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00011100) (reset: 00h)**
**Figure 51. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Ch)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/U	R/U	R/U	R/U	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 27. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Ch)**

Bit	Field	Type	Reset	Description
7:0	BERT_CNT[31:24]	R/U	'h00	BERT error count. Lane 2



**8.5.24 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00011101) (reset: 00h)**
**Figure 52. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Dh)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 28. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Dh)**

Bit	Field	Type	Reset	Description
7:4	Reserved	R	4'b0000	Reserved
3:0	BERT_CNT[35:32]	R/U	4'b0000	BERT error count. Lane 2

**8.5.25 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00011110) (reset: 00h)**
**Figure 53. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Eh)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R/U	R/U	R/U	R/U	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 29. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Eh)**

Bit	Field	Type	Reset	Description
7:0	BERT_CNT[19:12]	R/U	'h00	BERT error count. Lane 3

**8.5.26 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00011111) (reset: 00h)**
**Figure 54. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Fh)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R	R	R/U	R/U	R/U	R/U

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 30. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (1Fh)**

Bit	Field	Type	Reset	Description
7:4	Reserved	R	4'b0000	Reserved
3:0	BERT_CNT[23:20]	R/U	4'b0000	BERT error count. Lane 3

**8.5.27 CSR BIT Field Definitions – RX Pattern Verifier Control/Status (offset: 00100000) (reset: 00h)**
**Figure 55. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (20h)**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
R	R	R/W	R/W	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset, S= Set, U = autonomously update

**Table 31. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (20h)**

Bit	Field	Type	Reset	Description
7	PWR_DWN_STATUS	R	1'b0	Power Down Status Bit. 0 = Normal Operation (default) 1 = Device in Power Down Mode

**Table 31. CSR BIT Field Definitions – RX Pattern Verifier Control/Status (20h) (continued)**

Bit	Field	Type	Reset	Description
6	STB_STATUS	R	1'b0	Standby Status Bit 0 = Normal Operation (default) 1 = Device in Standby Mode
5:0	Reserved	R	6'b000000	Reserved

## 9 Application and Implementation

### NOTE

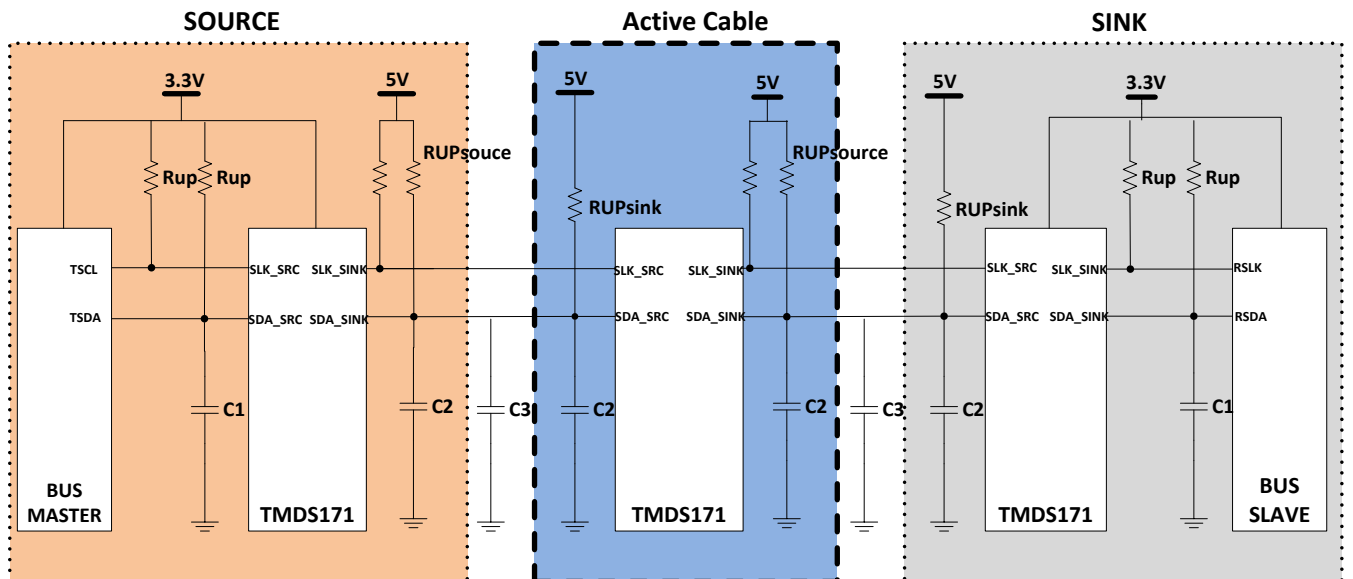
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TMDS171 was defined to work in many applications. This includes source applications like a Blu-Ray DVD player or AVR. The adaptive receive equalizer makes it ideal for sink applications like HDTV, monitors and projectors where cable length can be widely varied. The TMDS171 is also capable of working as an active cable to extend the cable length even further.

#### 9.1.1 Application Chain Showing DDC Connections

The DDC circuitry inside the TMDS171 allows multiple stage operation as shown in Figure 56. The retimer devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time of flight considerations for the maximum bus speed requirements.



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Figure 56. Typical Series Application

#### 9.1.2 DDC Pull Up Resistors

This section is for information only and subject to change depending upon system implementation. The pull-up resistor value is determined by two requirements.

1. The maximum sink current of the I<sup>2</sup>C buffer: The maximum sink current is 3 mA or slightly higher for an I<sup>2</sup>C driver supporting standard-mode I<sup>2</sup>C operation.

$$R_{up(min)} = \frac{V_{CC}}{I_{sink}} \quad (1)$$

2. The maximum transition time on the bus:

The maximum transition time, T, of an I<sup>2</sup>C bus is set by an RC time constant, where R is the pull-up resistor value, and C is the total load capacitance. The parameter, k, can be calculated from Equation 2 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. Table 32 summarizes the possible values of k under different threshold combinations.

**Application Information (continued)**

$$T = k \times RC \tag{2}$$

$$V(t) = V_{DD} \times \left( 1 - e^{-\frac{t}{RC}} \right) \tag{3}$$

**Table 32. Value k upon Different Input Threshold Voltages**

V <sub>th</sub> -V <sub>th+</sub>	0.7 V <sub>CC</sub>	0.65 V <sub>CC</sub>	0.6 V <sub>CC</sub>	0.55 V <sub>CC</sub>	0.5 V <sub>CC</sub>	0.45 V <sub>CC</sub>	0.4 V <sub>CC</sub>	0.35 V <sub>CC</sub>	0.3 V <sub>CC</sub>
0.1 V <sub>CC</sub>	1.0986	0.9445	0.8109	0.6931	0.5878	0.4925	0.4055	0.3254	0.2513
0.15 V <sub>CC</sub>	1.0415	0.8873	0.7538	0.6360	0.5306	0.4353	0.3483	0.2683	0.1942
0.2 V <sub>CC</sub>	0.9808	0.8267	0.6931	0.5754	0.4700	0.3747	0.2877	0.2076	0.1335
0.25 V <sub>CC</sub>	0.9163	0.7621	0.6286	0.5108	0.4055	0.3102	0.2231	0.1431	0.0690
0.3 V <sub>CC</sub>	0.8473	0.6931	0.5596	0.4418	0.3365	0.2412	0.1542	0.0741	

From Equation 1,  $R_{up(min)} = 5.5 \text{ V} / 3 \text{ mA} = 1.83 \text{ k}\Omega$  to operate the bus under a 5-V pull-up voltage and provide less than 3 mA when the I<sup>2</sup>C device is driving the bus to a low state. If a higher sink current, for example 4 mA, is allowed,  $R_{up(min)}$  can be as low as 1.375 k $\Omega$ .

If DDC working at standard mode of 100 Kbps, the maximum transition time T is fixed, 1  $\mu$ s, and using the k values from Table 32, the recommended maximum total resistance of the pull-up resistors on an I<sup>2</sup>C bus can be calculated for different system setups. If DDC working at fast mode of 400 Kbps, the transition time should be set at 300 ns according to I<sup>2</sup>C specification.

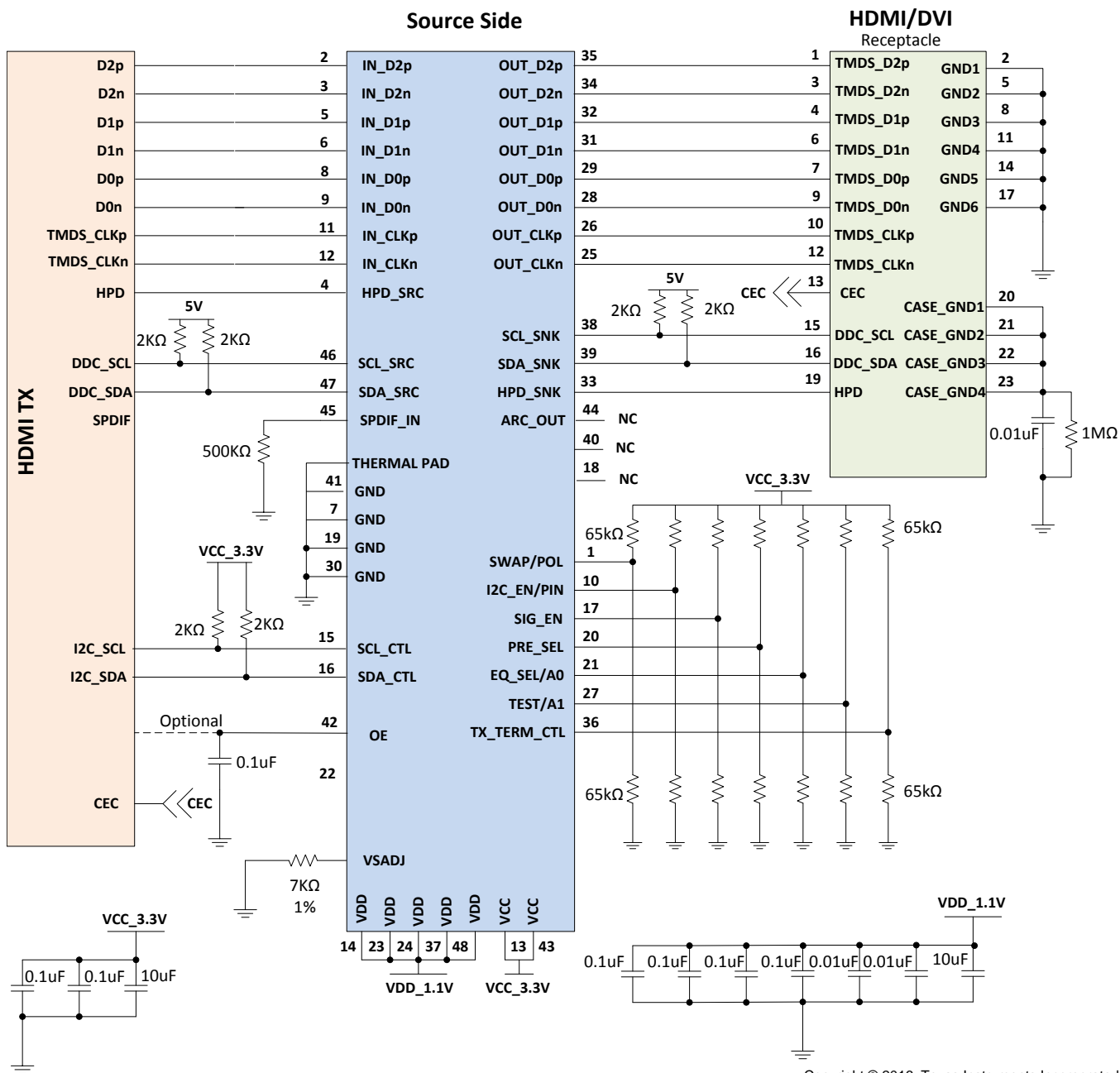
To support the maximum load capacitance specified in the HDMI spec,  $C_{cable(max)} = 700 \text{ pF} / C_{(source)} = 50 \text{ pF} / C_i = 50 \text{ pF}$ , R(max) can be calculated as shown in Table 33.

**Table 33. Pull-Up Resistor Upon Different Threshold Voltages and 800-pF Loads**

V <sub>th</sub> -V <sub>th+</sub>	0.7 V <sub>CC</sub>	0.65 V <sub>CC</sub>	0.6 V <sub>CC</sub>	0.55 V <sub>CC</sub>	0.5 V <sub>CC</sub>	0.45 V <sub>CC</sub>	0.4 V <sub>CC</sub>	0.35 V <sub>CC</sub>	0.3 V <sub>CC</sub>	UNIT
0.1 V <sub>CC</sub>	1.14	1.32	1.54	1.8	2.13	2.54	3.08	3.84	4.97	K $\Omega$
0.15 V <sub>CC</sub>	1.2	1.41	1.65	1.97	2.36	2.87	3.59	4.66	6.44	K $\Omega$
0.2 V <sub>CC</sub>	1.27	1.51	1.8	2.17	2.66	3.34	4.35	6.02	9.36	K $\Omega$
0.25 V <sub>CC</sub>	1.36	1.64	1.99	2.45	3.08	4.03	5.6	8.74	18.12	K $\Omega$
0.3 V <sub>CC</sub>	1.48	1.8	2.23	2.83	3.72	5.18	8.11	16.87	—	K $\Omega$

To accommodate the 3 mA drive current specification, a narrower threshold voltage range is required to support a maximum 800 pF load capacitance for a standard-mode I<sup>2</sup>C bus.

### 9.2 Source Side Application



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Figure 57. TMDS171 in Source Side Application

## Source Side Application (continued)

### 9.2.1 Design Requirements

The TMDS171 can be designed into many different applications. In all the applications there are certain requirements for the system to work properly. Two voltage rails are required in order to support lowest power consumption possible. OE pin must have a 200 nF capacitor to ground. This pin can be driven by a processor but the pin needs to change states after voltage rails have stabilized. The best way to configure the device is by using I<sup>2</sup>C but pin strapping is also provided as I<sup>2</sup>C is not available in all cases. As sources may have many different naming conventions it is necessary to confirm that the link between the source and the TMDS171 are correctly mapped. A Swap function is provide for the input pins incase signaling if reversed between source and device. [Table 34](#) provides information on expected values in order to perform properly.

**Table 34. Design Parameters**

PARAMETER	VALUE
V <sub>CC</sub>	3.3 V
V <sub>DD</sub>	1.2 V
Main Link Input Voltage	V <sub>ID</sub> = 75 mV <sub>PP</sub> to 1.4 V <sub>PP</sub>
Control Pin Max Voltage for Low	65 kΩ pulldown
Control Pin Voltage Range Mid	Left Not Connected/Floating
Control Pin Min Voltage for High	65 kΩ pullup
R <sub>(VSADJ)</sub> Resistor	7.06 kΩ 1%

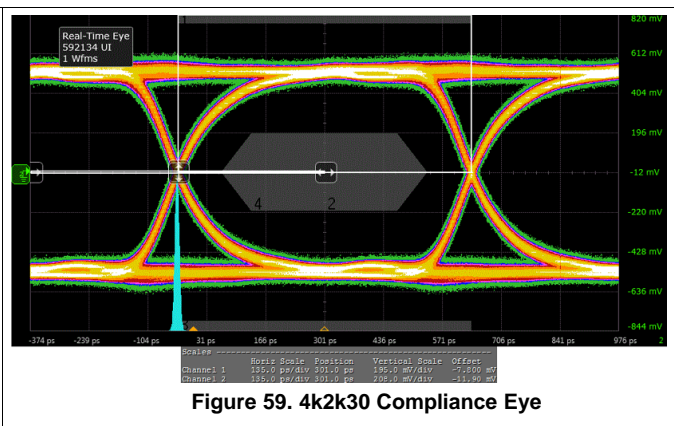
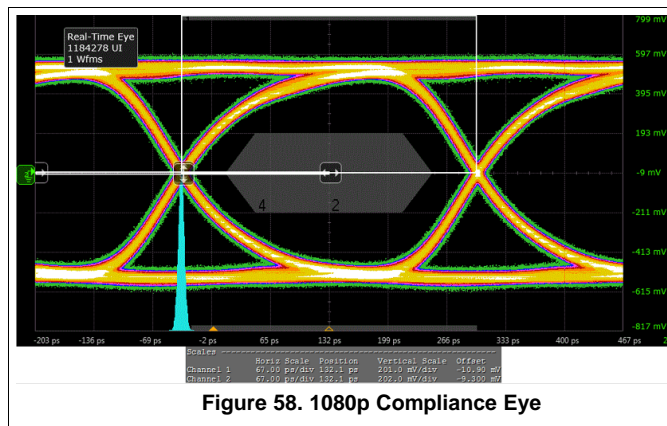
### 9.2.2 Detailed Design Procedure

The TMDS171 is a signal conditioning device that provides several forms of signal conditioning in order to support compliance for HDMI or DVI at a source connector. These forms of signal conditioning are accomplished using receive equalization, retiming, and output driver configurability. The transmitter will drive 2-3" of board trace and connector when compliance is required at the connector.

To design in the TMDS171 the following need to be understood for a source side application:

- Determine the loss profile between the GPU/chipset and the HDMI/DVI connector.
- Based upon this loss profile and signal swing determine optimal location for the TMDS171, in order to pass source electrical compliance. Usually within 2"-3" of the connector
- Use the typical application [Figure 57](#) for information on control pin resistors.
- The TMDS171 has a receiver adaptive equalizer but can also be configured using EQ\_SEL control pin.
- Set the VOD, Pre-emphasis, termination, and edge rate levels appropriately to support compliance by using the appropriate VSADJ resistor value and setting PRE\_SEL, and TX\_TERM\_CTL control pins.
- The thermal pad must be connected to ground.
- See [Figure 57](#) for recommended decouple capacitors from V<sub>CC</sub> and V<sub>DD</sub> pins to Ground

### 9.2.3 Application Curves



### 9.2.4 Sink Side Application

For a sink side application HPD needs consideration. The TMDS171 drives the HPD signal to 3.3V which meetings requirements but if 5 V HPD signaling is required the two circuits shown in Figure 60 are required. As sources are not consistent in implementing all aspects of the DDC link it is recommended to configure the TMDS171 as per Figure 60. Another consideration in relationship to how HPD is implemented is the architecture and behavior of the HDMI RX/Scalar.

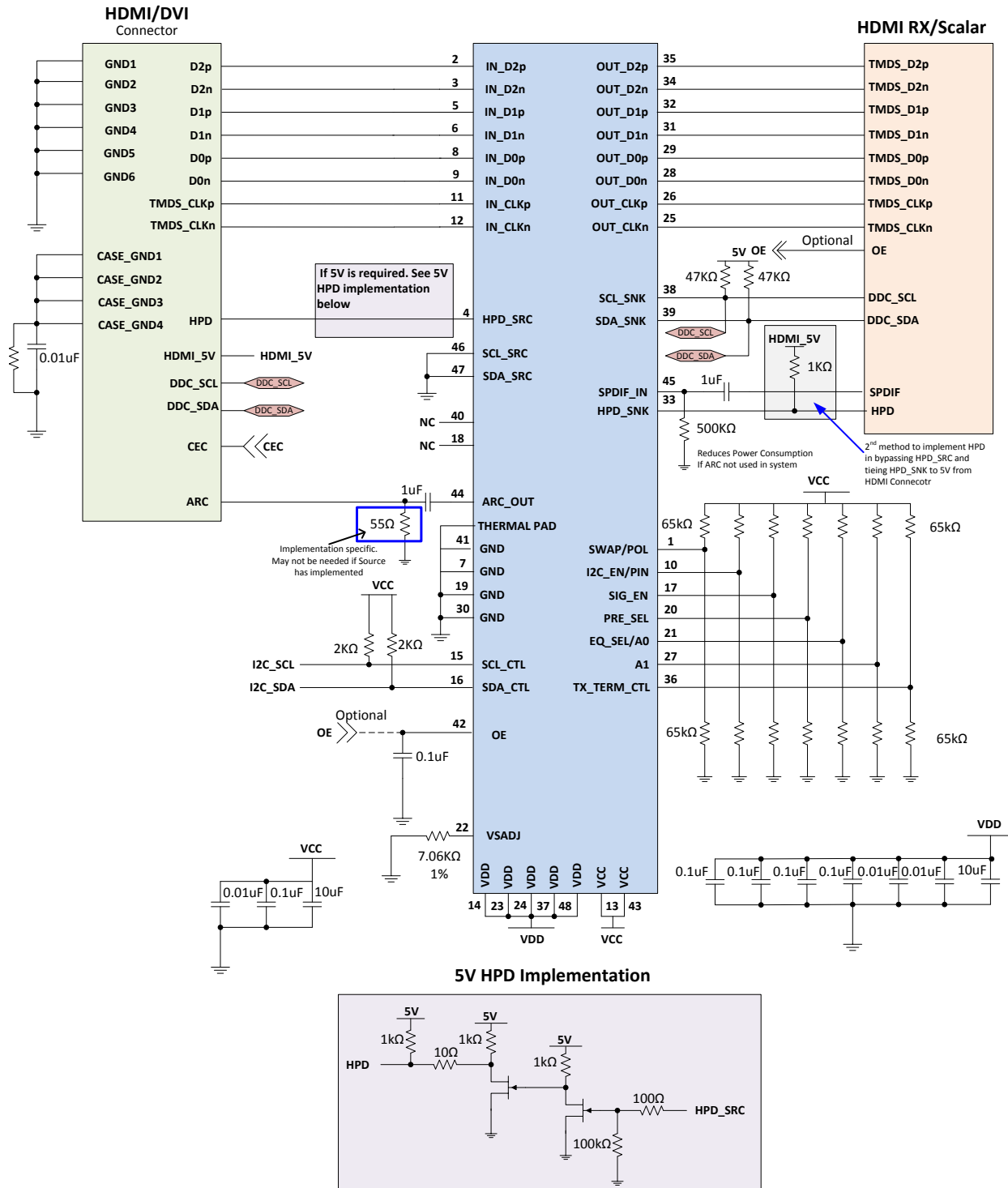


Figure 60. TMDS171 in Sink Side Application, 5 V HPD Implementation

### 9.2.4.1 Design Requirements

See [Table 35](#) for the Sink Side design example parameters.

**Table 35. Design Parameters**

PARAMETER	VALUE
$V_{CC}$	3.3 V
$V_{DD}$	1.2 V
Main Link Input Voltage	$V_{ID} = 75 \text{ mV}_{PP}$ to $1.4 \text{ V}_{PP}$
Control Pin Max Voltage for Low	65 k $\Omega$ pulldown
Control Pin Voltage Range Mid	Left Not Connected/Floating
Control Pin Min Voltage for High	65 k $\Omega$ pullup
$R_{(VSADJ)}$ Resistor	7.06 k $\Omega$ 1%

### 9.2.4.2 Detailed Design Procedure

To design in the TMDS171 the following need to be understood for a source side application.

- Determine the loss profile between the RX/chipset and the HDMI/DVI connector.
- Based upon this loss profile and signal swing determine optimal location for the TMDS171, in order to pass sink electrical compliance.
- Use the typical application [Figure 56](#) for information on control pin resistors.
- The TMDS171 has a receiver adaptive equalizer but can also be configured using EQ\_SEL control pin.
- Set the VOD, Pre-emphasis, termination, and edge rate levels appropriately to support link between TMDS171 and HDMI RX/Chipset by using the appropriate VSADJ resistor value and setting PRE\_SEL and TX\_TERM\_CTL control pins.
- The thermal pad must be connected to ground.
- See [Figure 60](#) for recommended decouple caps from  $V_{CC}$  and  $V_{DD}$  pins to Ground.



### 9.3 System Examples

Another way to configure sink application is to configure the sink as per Figure 61. This is done as not all sources are supporting clock stretching as per standard.

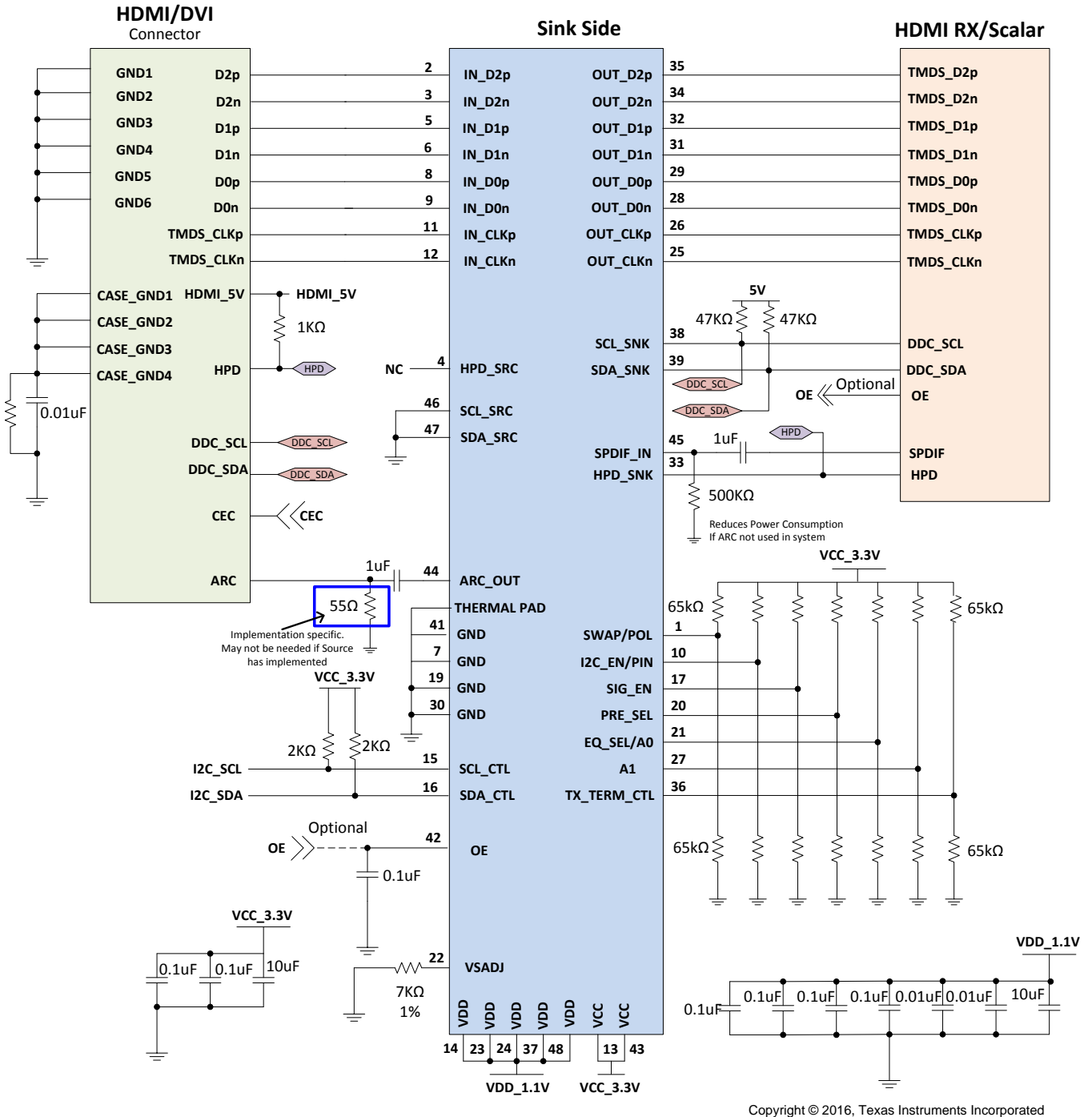


Figure 61. TMDS171 in Sink Side Application

## 10 Power Supply Recommendations

To minimize the power consumption of customer application, TMDS171 used the dual power supply.  $V_{CC}$  is 3.3 V with 5% range to support the I/O voltage. The  $V_{DD}$  is 1.2 V with 1.1 V to 1.27 V range to supply the internal digital control circuit. TMDS171 operates in 3 different working states.

- o Power down Mode:
  - OE = Low puts the device into its lowest power state by shutting down all function blocks.
    - When OE is re-asserted the transitions from L→H will create a reset and if the device is programmed through I<sup>2</sup>C it must to be reprogrammed.
  - Writing a 1 to register 09h[3].
  - OE = High, HPD\_SNK = Low
- Standby Mode: HPD\_SNK = High but no valid clock signal detect on clock lane.
- Normal operation: Working in Redriver or Retimer
- When HPD assert, the device CDR and output will enable based on the signal detector circuit result.
- HPD\_SRC = HPD\_SNK in all conditions.

**Table 36. Power Up and Operation Timing Requirements**

INPUTS					STATUS						
HPD_SNK	OE	SIG_EN	IN_CLK	Device Mode	HPD_SRC	IN_Dx	SDA/ SCL_CTL	OUT_Dx OUT_CLK	DDC	ARC	Mode
X	L	H or L	X	X	H	RX Termination On	Disable	High-Z	Disabled	Disable	Power Down Mode
L	H	H or L	X	X	L	RX Termination On	Active	High-Z	Disabled	Disable	Power Down Mode
H	H	H or L	X	X	H	RX Termination On	Active	High-Z	Disabled	Disable	Power Down Mode by W 1 to 09h[3]
H	H	H	No Valid TMDS Clock	X	H	D0-D2 disabled with RX Termination On, IN_CLK Active	Active	High-Z	Active	Active	Standby Mode (Squelch waiting)
H	H	H or L	No Valid TMDS Clock	Retimer mode	H	D0-D2 disabled with RX Termination On, IN_CLK Active	Active	High-Z	Active	Active	Standby Mode (Squelch waiting)
H	H	H	Valid TMDS Clock	Retimer mode	H	RX Active	Active	TX Active	Active	Active	Normal operation
H	H	H or L	No Valid TMDS Clock	Redriver mode	H	RX Active	Active	TX Active	Active	Active	Normal operation

## 11 Layout

### 11.1 Layout Guidelines

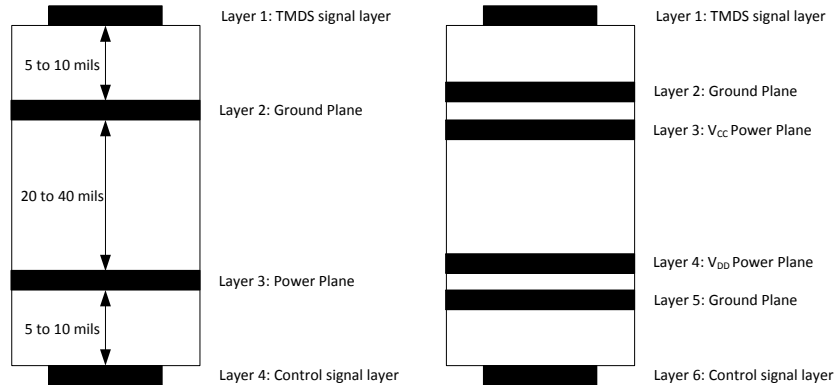
On a high-K board – It is always recommended to solder the PowerPAD™ onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the PowerPAD™ package. On a high-K board the TMDS171 can operate over the full temperature range by soldering the PowerPAD onto the thermal land without vias.

On a low-K board – In order for the device to operate across the temperature range on a low-K board, a 1-oz Cu trace connecting the GND pins to the thermal land must be used. A simulation shows  $R_{\theta JA} = 100.84^{\circ}\text{C/W}$  allowing 545 mW power dissipation at 70°C ambient temperature.

A general PCB design guide for PowerPAD packages is provided in the document SLMA002 - PowerPAD Thermally Enhanced Package.

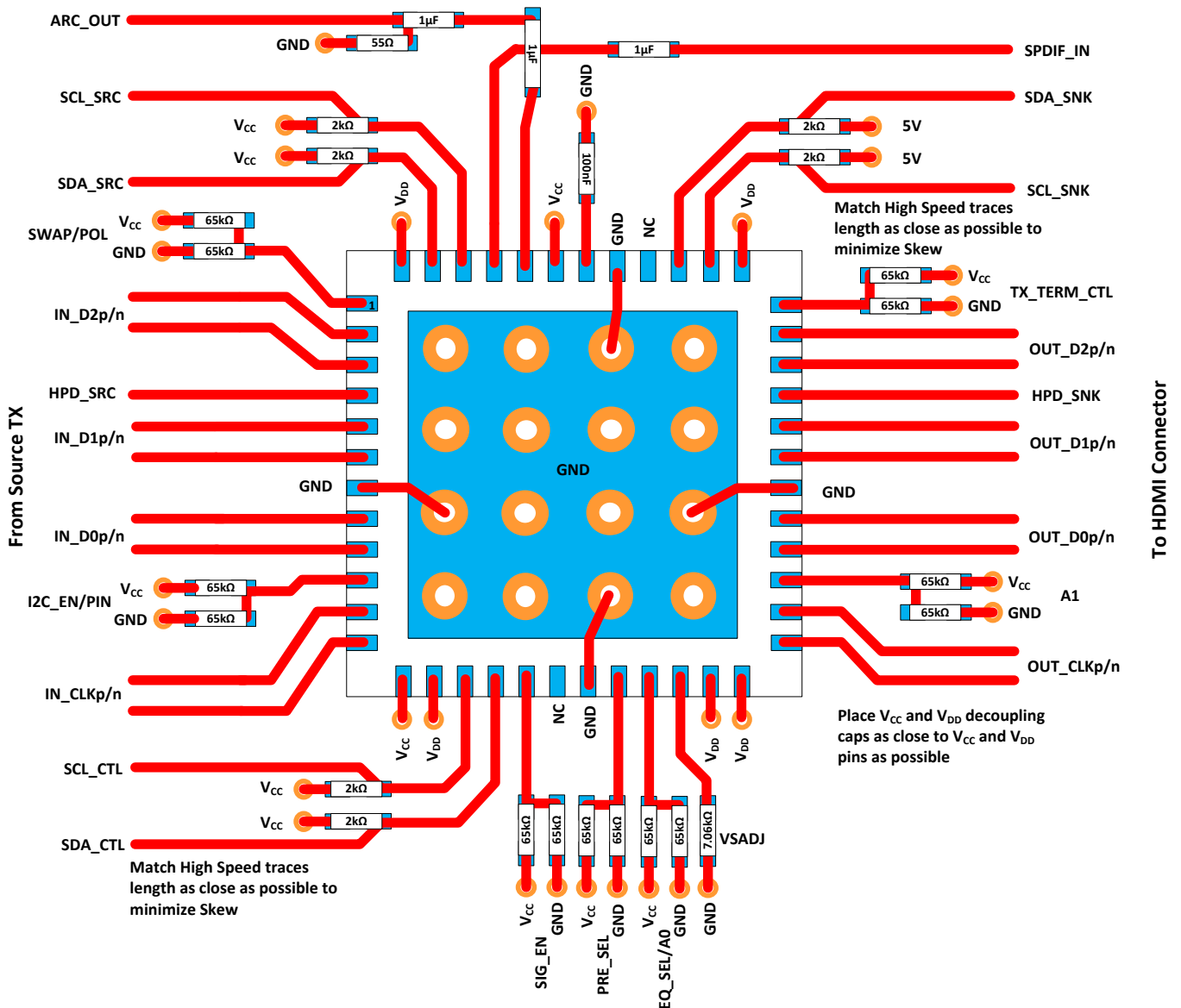
TI recommends six layers as the TMDS171 is a two voltage rail device.

- Routing the high-speed TMDS traces on the top layer avoids the use of vias. (and the introduction of their inductances) and allows for clean interconnects from the HDMI connectors to the retimer inputs and outputs. It is important to match the electrical length of these high speed traces to minimize both inter-pair and intra-pair skew.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission link interconnects and provides an excellent low –inductance path for the return current flow.
- Placing a power plane next to the ground plane creates an additional high-frequency bypass capacitance.
- Routing slower seed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power/ground plane system to the stack to keep symmetry. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be place closer together, thus increasing the high frequency bypass capacitance significantly.



**Figure 62. Recommended 4 or 6 Layer PCB Stack**

### 11.2 Layout Example



- (1) If ARC is not used a 500KΩ resistor should be tied to GND at the SPDIF\_IN pin
- (2) The 55-Ω resistor to GND on the ARC\_OUT pin is implementation specific and may not be needed if it is already implemented elsewhere.

Figure 63. Layout

## 12 器件和文档支持

### 12.1 相关文档

[HDMI] 高清多媒体接口规范版本 1.4b, 2011 年 10 月

[HDMI] 高清多媒体接口 CTS 版本 1.4b, 2011 年 10 月

[I2C] I2C 总线规范版本 2.1, 2000 年 1 月

### 12.2 接收文档更新通知

要接收文档更新通知, 请导航至 [TI.com](http://TI.com) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册, 即可每周接收产品信息更改摘要。有关更改的详细信息, 请查看任何已修订文档中包含的修订历史记录。

### 12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范, 并且不一定反映 TI 的观点; 请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中, 您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 12.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.  
is a trademark of ~HDMI.

### 12.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时, 应将导线一起截短或将装置放置于导电泡棉中, 以防止 MOS 门极遭受静电损伤。

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更, 恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本, 请参阅左侧的导航。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMDS171IRGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TMDS171I	<a href="#">Samples</a>
TMDS171IRGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TMDS171I	<a href="#">Samples</a>
TMDS171RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TMDS171	<a href="#">Samples</a>
TMDS171RGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	TMDS171	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMDS171IRGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TMDS171IRGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TMDS171RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TMDS171RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMDS1711RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TMDS1711RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0
TMDS1711RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TMDS1711RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

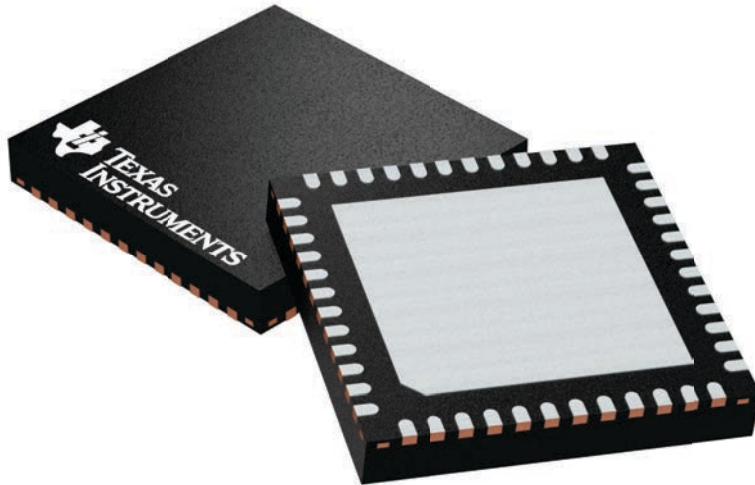
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch

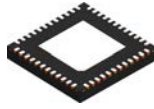
PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224671/A

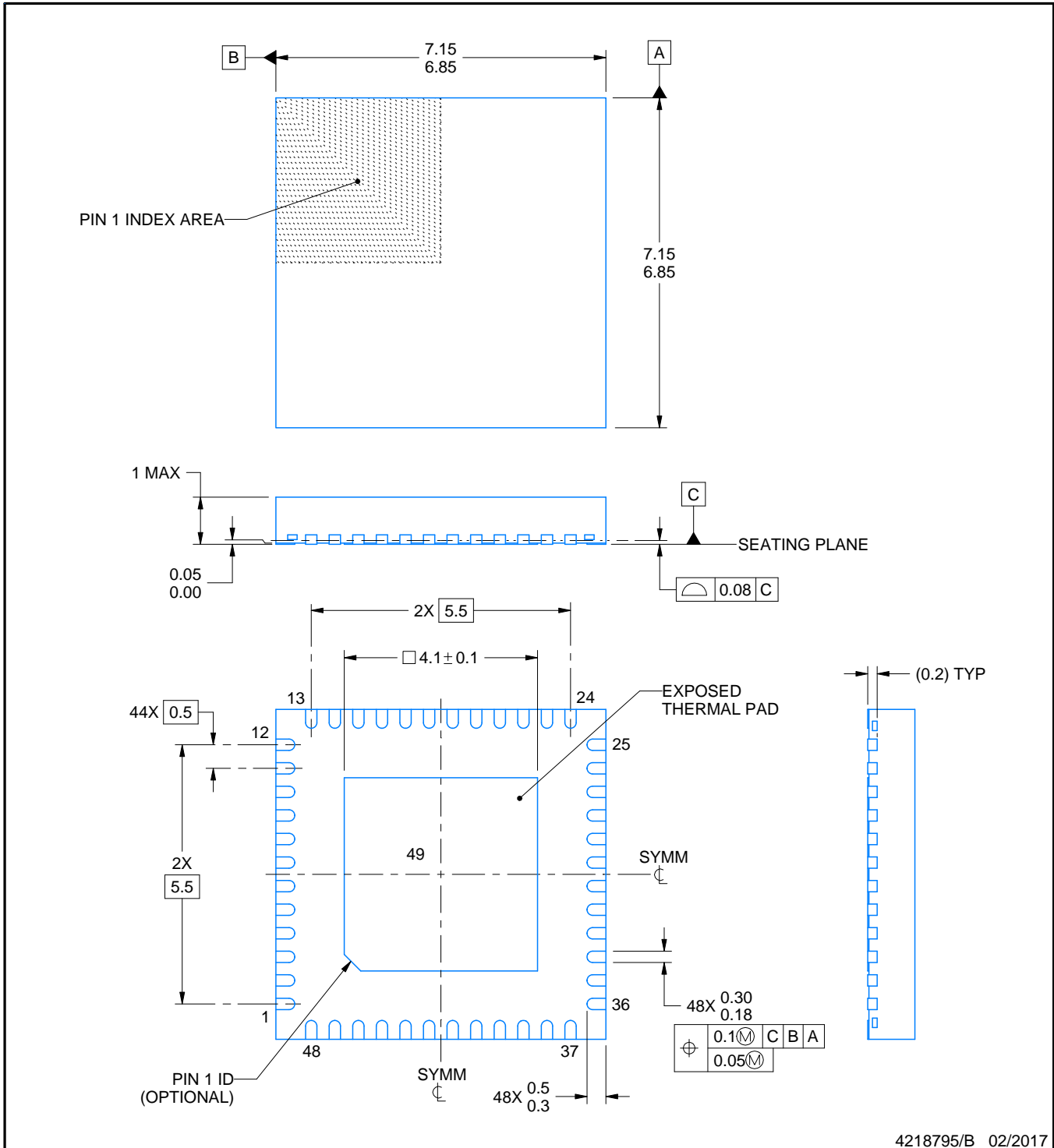
RGZ0048B



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES:

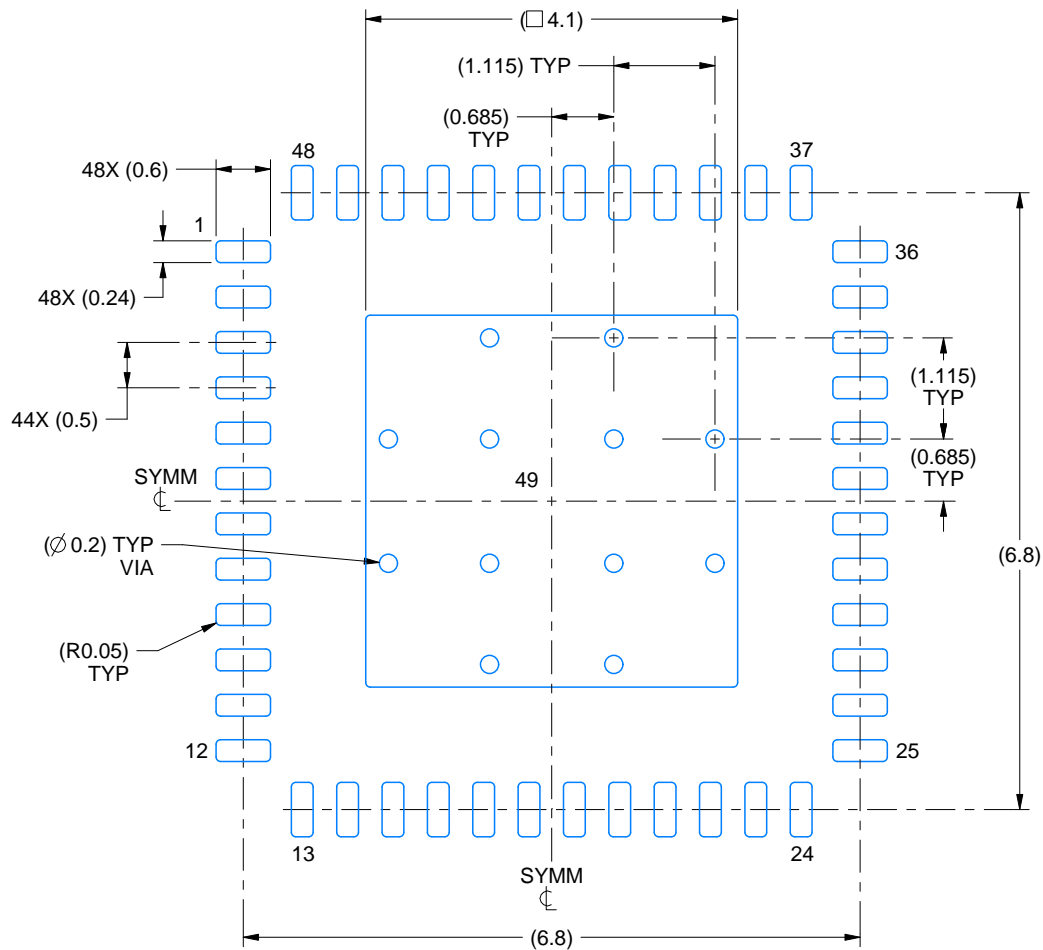
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

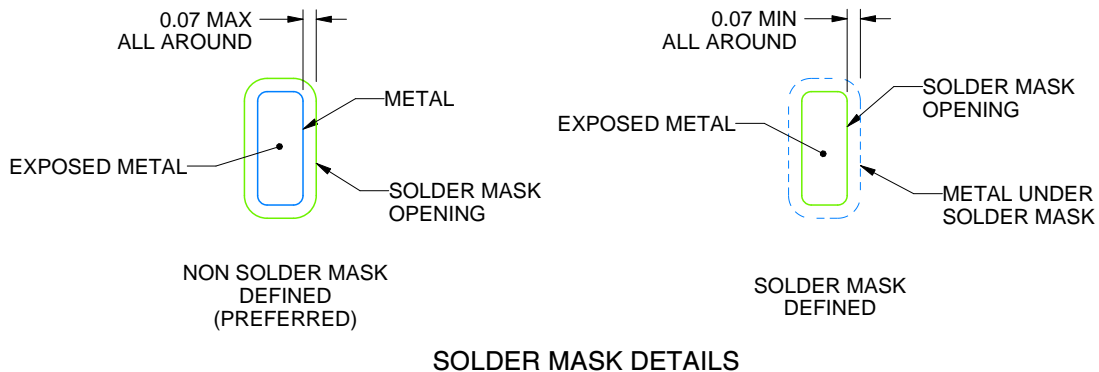
**RGZ0048B**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:12X



**SOLDER MASK DETAILS**

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49  
 73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:12X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要声明和免责声明

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