DSLVDS1047 3.3V LVDS 四通道高速差动线路驱动器

1 特性

- 旨在用于信号传输速率高达 400Mbps 的应用
- 3.3V 电源设计
- 300ps 典型差动偏斜
- 400ps 最大差动偏斜
- 1.7ns 最大传播延迟
- ±350mV 差动信号传输
- 低功耗（3.3V 静态条件下为 13mW）
- 能够与现有 5V LVDS 接收器交互操作
- 在断电模式下，LVDS 输出端具有高阻抗
- 直通引脚排列可简化 PCB 布局
- 符合或超出 TIA/EIA-644 LVDS 标准
- 工业工作温度范围（−40°C 至 +85°C）
- 可采用 TSSOP 封装

2 应用

- 多功能打印机
- 板对板通信
- 测试和测量
- 打印机
- 数据中心互连
- 实验室仪表
- 超声波扫描仪

3 说明

DSLVDS1047 器件是一款四路 CMOS 直通差动线路驱动器，专为需要超低功耗和高数据速率的 应用 而设计。该器件旨在使用低电压差动信号 (LVDS) 技术支持超过 400Mbps (200MHz) 的数据速率。

DSLVDS1047 接受低电压 TTL/CMOS 输入电平，并将其转换为低电压 (350mV) 差动输出信号。
此外，该驱动器支持可用于禁用输出级的 TRI-STAT 功能，可禁用负载电流，从而将器件降至功率为 13mW（典型值）的超低空闲功耗状态。
DSLVDS1047 采用了直通引脚排列，可简化 PCB 布局。

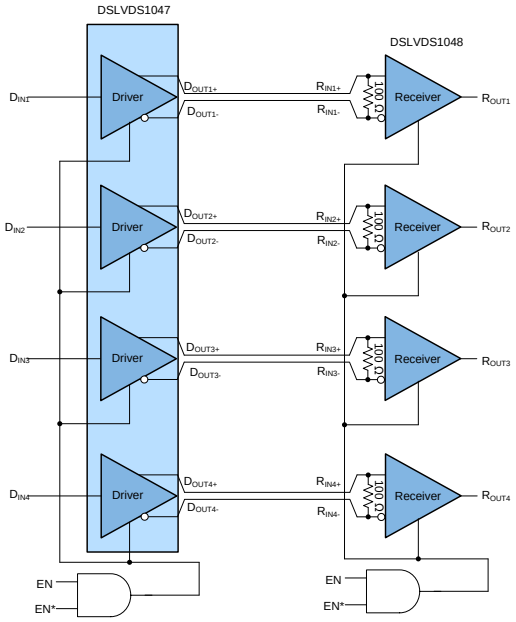
EN 和 EN* 输入将接受 AND 运算并控制 TRI-STATE 输出。这些使能端由四个驱动器共用。 和配套的线路接收器 (DSLVDS1048) 为高速点对点接口应用提供了大功率伪 ECL 器件的替代 产品。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DSLVDS1047	TSSOP (16)	5.00mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

图 1. 703A I2C



目录

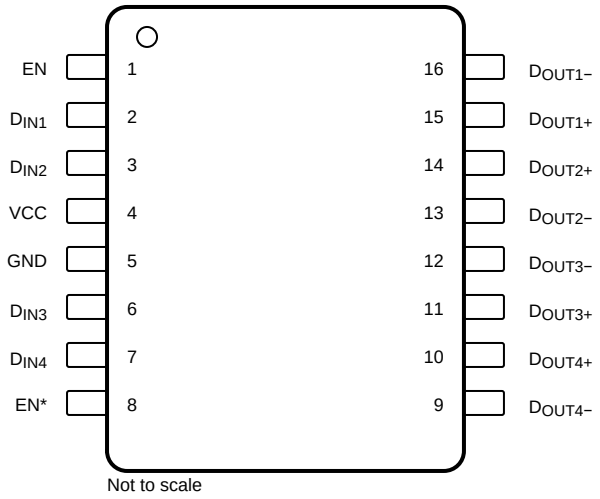
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2018 年 9 月	*	最初发布版本。

5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
2	D_{IN1}	I	Driver input pin, TTL/CMOS compatible
3	D_{IN2}		
6	D_{IN3}		
7	D_{IN4}		
10	D_{OUT4+}	O	Non-inverting driver output pin, LVDS levels
11	D_{OUT3+}		
14	D_{OUT2+}		
15	D_{OUT1+}		
9	D_{OUT4-}	O	Inverting driver output pin, LVDS levels
12	D_{OUT3-}		
13	D_{OUT2-}		
16	D_{OUT1-}		
1	EN	I	Driver enable pin: When EN is low, the driver is disabled. When EN is high and EN* is low or open, the driver is enabled. If both EN and EN* are open circuit, then the driver is disabled.
8	EN*	I	Driver enable pin: When EN* is high, the driver is disabled. When EN* is low or open and EN is high, the driver is enabled. If both EN and EN* are open circuit, then the driver is disabled.
5	GND	—	Ground pin
4	V_{CC}	—	Power supply pin, +3.3 V ± 0.3 V

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

			MIN	MAX	UNIT
Supply voltage (V_{CC})			−0.3	4	V
Input voltage (D_{IN})			−0.3	V_{CC} + 0.3	V
Enable input voltage (EN, EN*)			−0.3	V_{CC} + 0.3	V
Output voltage (D_{OUT+}, D_{OUT-})			−0.3	3.9	V
Short-circuit duration	(D_{OUT+}, D_{OUT-})		Continuous		
Maximum package power dissipation at +25°C	PW0016A package			866	mW
	Derate PW0016A package	above +25°C		6.9	mW/°C
Lead temperature	Soldering (4 s)			260	°C
Maximum junction temperature				150	°C
Storage temperature, T_{stg}			−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±1200	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±200	
		Machine Model	±1200	

(1) ESD Ratings:
HBM (1.5 kΩ, 100 pF)
EIAJ (0 Ω, 200 pF)
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
Operating free air temperature, T_A	−40	25	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		DSLVDS1047 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified(1)(2)(3)

PARAMETER		TEST CONDITIONS	PIN	MIN	TYP	MAX	UNIT
V_{OD1}	Differential output voltage	R_L = 100 Ω (Figure 18)	D_{OUT-} D_{OUT+}	250	310	450	mV
ΔV_{OD1}	Change in magnitude of V_{OD1} for complementary output states				1	35	|mV|
V_{OS}	Offset voltage			1.125	1.17	1.375	V
ΔV_{OS}	Change in magnitude of V_{OS} for complementary output states				1	25	|mV|
V_{OH}	Output high voltage				1.33	1.6	V
V_{OL}	Output low voltage			0.9	1.02		V
V_{IH}	Input high voltage		D_{IN}, EN, EN*	2		V_{CC}	V
V_{IL}	Input low voltage			GND		0.8	V
I_{IH}	Input high current	V_{IN} = V_{CC} or 2.5 V			2	15	µA
I_{IL}	Input low current	V_{IN} = GND or 0.4 V			2	15	µA
V_{CL}	Input clamp voltage	I_{CL} = −18 mA		−1.5	−0.8		V
I_{OS}	Output short-circuit current(4)	ENABLED, D_{IN} = V_{CC}, D_{OUT+} = 0 V or D_{IN} = GND, D_{OUT-} = 0 V	D_{OUT-} D_{OUT+}		−4	−8	mA
I_{OSD}	Differential output short-circuit current(4)	ENABLED, V_{OD} = 0 V			−4.2	−9	mA
I_{OFF}	Power-off leakage	V_{OUT} = 0 V or 3.6 V, V_{CC} = 0 V or Open		−20	±1	20	µA
I_{OZ}	Output TRI-STATE current	EN = 0.8 V and EN* = 2.0 V V_{OUT} = 0 V or V_{CC}		−10	±1	10	µA
I_{CC}	No load supply current drivers enabled	D_{IN} = V_{CC} or GND	V_{CC}		4	8	mA
I_{CCL}	Loaded supply current drivers enabled	R_L = 100 Ω all channels, D_{IN} = V_{CC} or GND (all inputs)			20	30	mA
I_{CCZ}	No load supply current drivers disabled	D_{IN} = V_{CC} or GND, EN = GND, EN* = V_{CC}			2.2	6	mA

(1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except: V_{OD1} and ΔV_{OD1}.
(2) All typicals are given for: V_{CC} = 3.3 V, T_A = +25°C.
(3) The DSLVDS1047 is a current mode device and only functions within datasheet specifications when a resistive load is applied to the driver outputs typical range is (90 Ω to 110 Ω).
(4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

6.6 Switching Characteristics

V_{CC} = +3.3V ± 10%, T_A = −40°C to +85°C(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHLD}	Differential propagation delay high to low	R_L = 100 Ω, C_L = 15 pF (Figure 19 and Figure 20)	0.5	0.9	1.7	ns
t_{PLHD}	Differential propagation delay low to high		0.5	1.2	1.7	ns
t_{SKD1}	Differential pulse skew $\|t_{PHLD} - t_{PLHD}\|$(4)			0.3	0.4	ns
t_{SKD2}	Channel-to-channel skew(5)			0.4	0.5	ns
t_{SKD3}	Differential part-to-part skew(6)		0		1	ns
t_{SKD4}	Differential part-to-part skew(7)		0		1.2	ns
t_{TLH}	Rise time			0.5	1.5	ns
t_{THL}	Fall time			0.5	1.5	ns
t_{PHZ}	Disable time high to Z	R_L = 100 Ω, C_L = 15 pF (Figure 21 and Figure 22)		2	5	ns
t_{PLZ}	Disable time low to Z			2	5	ns
t_{PZH}	Enable time Z to high			3	7	ns
t_{PZL}	Enable time Z to low			3	7	ns
f_{MAX}	Maximum operating frequency(8)		200	250		MHz

(1) All typicals are given for: V_{CC} = 3.3 V, T_A = +25°C.
(2) Generator waveform for all tests unless otherwise specified: f = 1 MHz, Z_O = 50 Ω, t_r ≤ 1 ns, and t_f ≤ 1 ns.
(3) C_L includes probe and jig capacitance.
(4) t_{SKD1} $|t_{PHLD} - t_{PLHD}|$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.
(5) t_{SKD2} is the differential channel-to-channel skew of any event on the same device.
(6) t_{SKD3}, differential part-to-part skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.
(7) t_{SKD4}, part to part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. t_{SKD4} is defined as |Max − Min| differential propagation delay.
(8) f_{MAX} generator input conditions: t_r = t_f < 1 ns (0% to 100%), 50% duty cycle, 0 V to 3 V. Output criteria: duty cycle = 45% / 55%, VOD > 250 mV, all channels switching.

6.7 Typical Characteristics

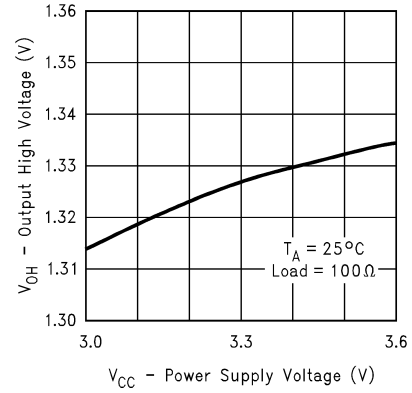


Figure 2. Output High Voltage vs Power Supply Voltage

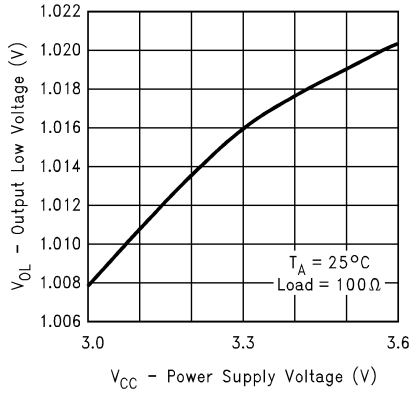


Figure 3. Output Low Voltage vs Power Supply Voltage

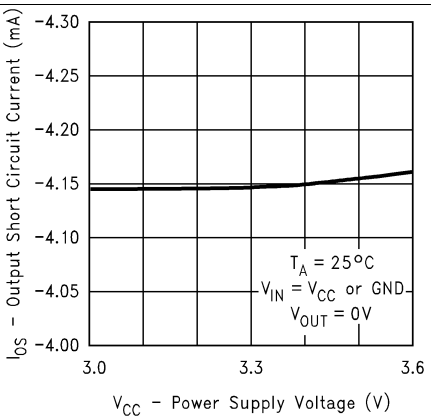


Figure 4. Output Short Circuit Current vs Power Supply Voltage

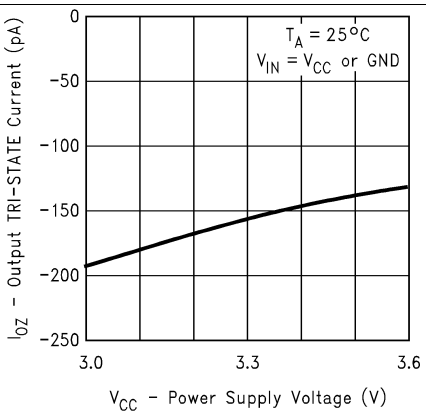


Figure 5. Output TRI-STATE Current vs Power Supply Voltage

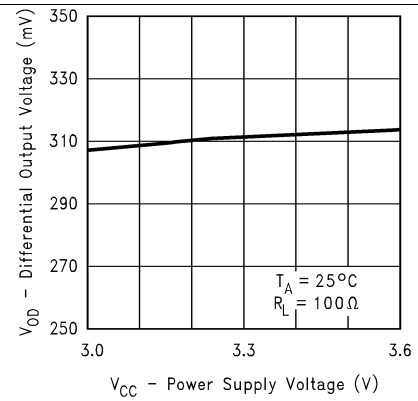


Figure 6. Differential Output Voltage vs Power Supply Voltage

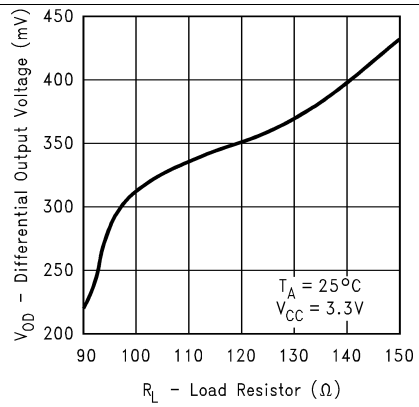


Figure 7. Differential Output Voltage vs Load Resistor

Typical Characteristics (continued)

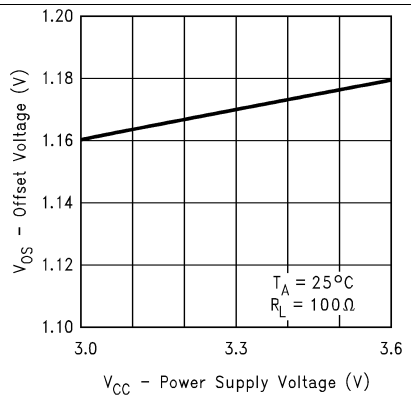


Figure 8. Offset Voltage vs Power Supply Voltage

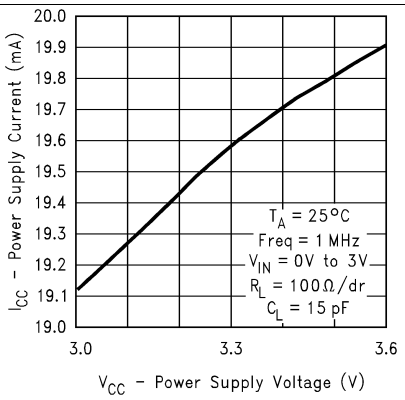


Figure 9. Power Supply Current vs Power Supply Voltage

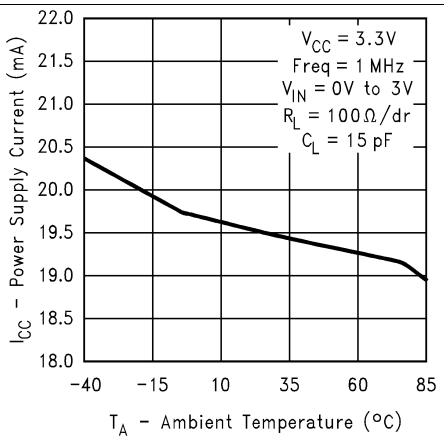


Figure 10. Power Supply Current vs Ambient Temperature

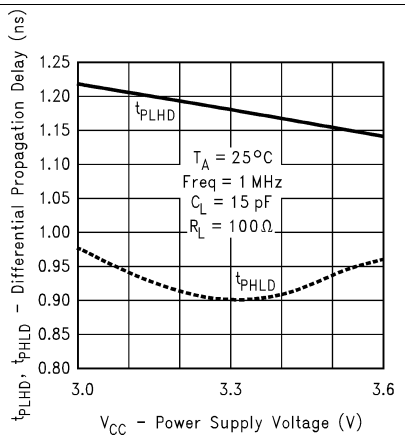


Figure 11. Differential Propagation Delay vs Power Supply Voltage

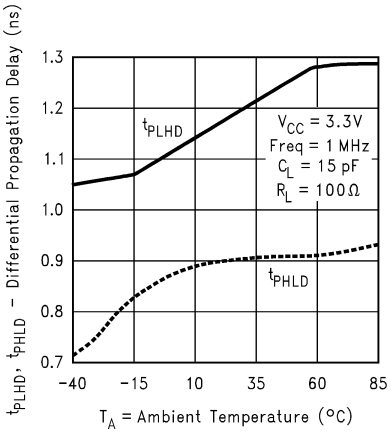


Figure 12. Differential Propagation Delay vs Ambient Temperature

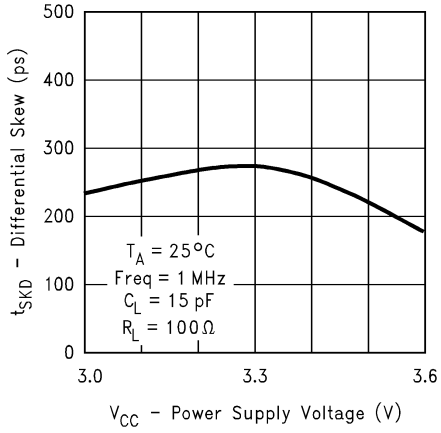


Figure 13. Differential Skew vs Power Supply Voltage

Typical Characteristics (continued)

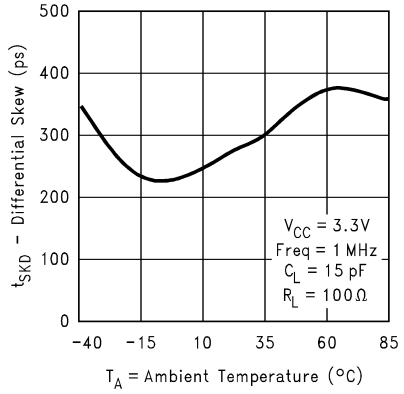


Figure 14. Differential Skew vs Ambient Temperature

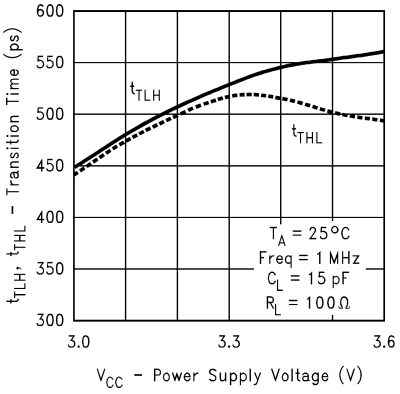


Figure 15. Transition Time vs Power Supply Voltage

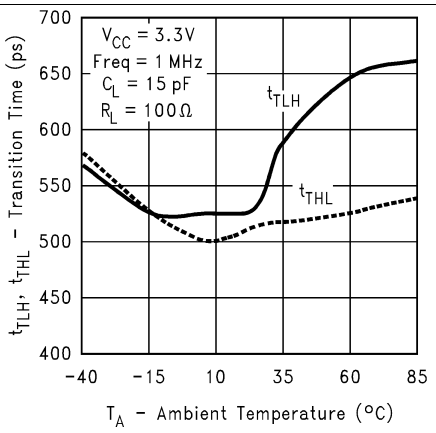


Figure 16. Transition Time vs Ambient Temperature

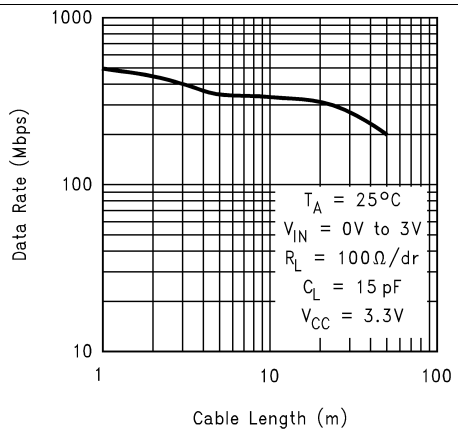


Figure 17. Data Rate vs Cable Length

7 Parameter Measurement Information

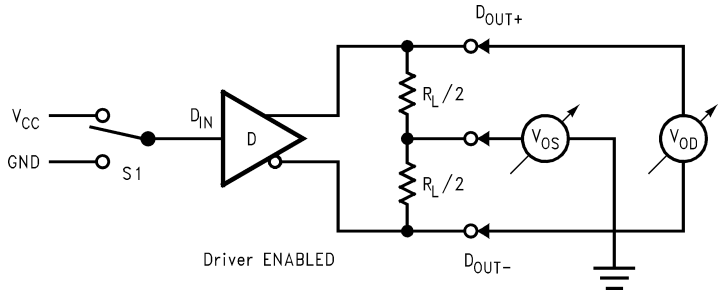


Figure 18. Driver V_{OD} and V_{OS} Test Circuit

Parameter Measurement Information (continued)

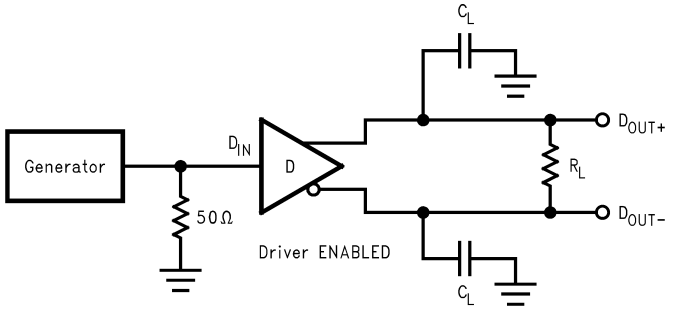


Figure 19. Driver Propagation Delay and Transition Time Test Circuit

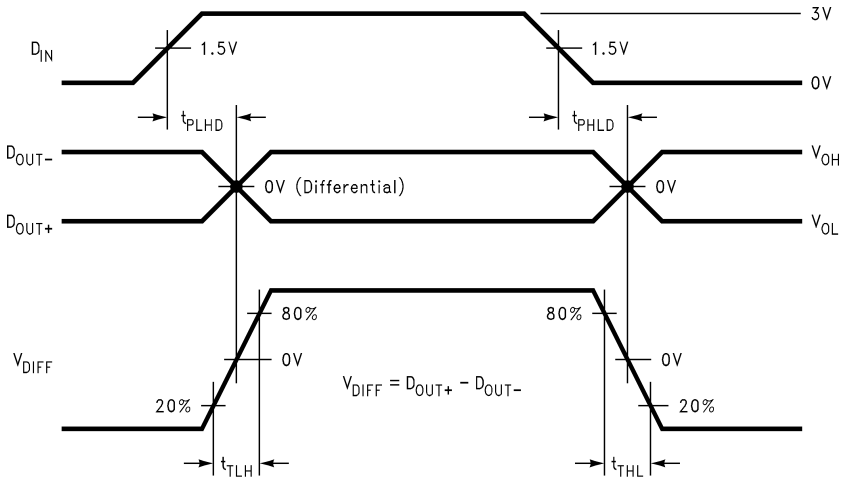


Figure 20. Driver Propagation Delay and Transition Time Waveforms

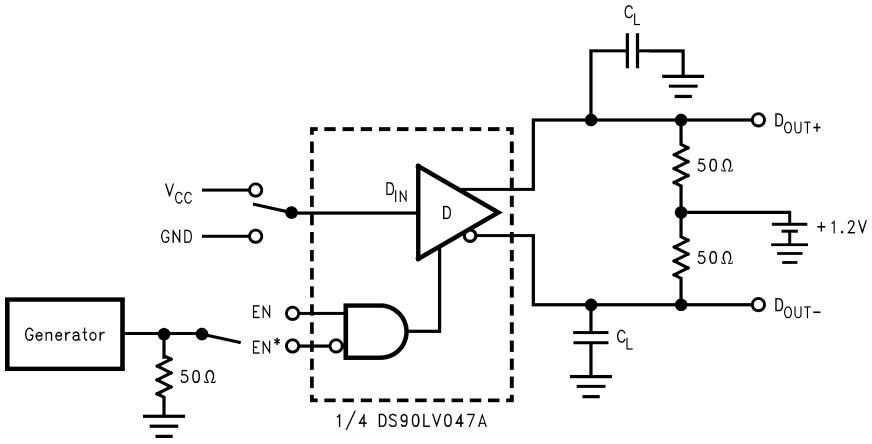


Figure 21. Driver TRI-STATE Delay Test Circuit

Parameter Measurement Information (continued)

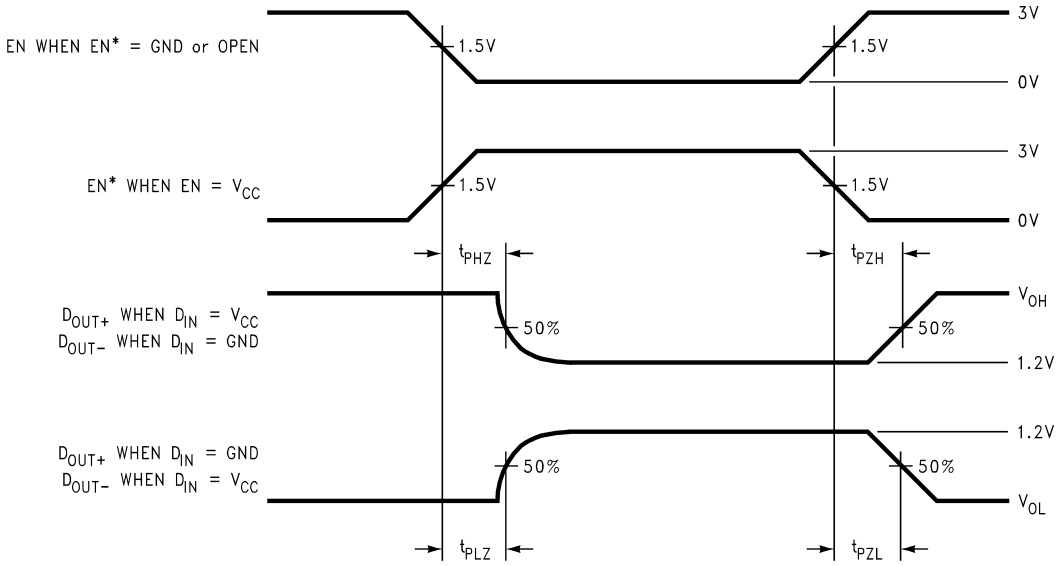


Figure 22. Driver TRI-STATE Delay Waveform

8 Detailed Description

8.1 Overview

LVDS drivers and receivers are intended to be primarily used in an uncomplicated point-to-point configuration as is shown in Figure 24. This configuration provides a clean signaling environment for the fast edge rates of the drivers. The receiver is connected to the driver through a balanced media which may be a standard twisted pair cable, a parallel pair cable, or simply PCB traces. Typically, the characteristic differential impedance of the media is in the range of 100 Ω. A termination resistor of 100 Ω (selected to match the media), and is located as close to the receiver input pins as possible. The termination resistor converts the driver output current (current mode) into a voltage that is detected by the receiver. Other configurations are possible such as a multi-receiver configuration, but the effects of a mid-stream connector(s), cable stub(s), and other impedance discontinuities as well as ground shifting, noise margin limits, and total termination loading must be taken into account.

The DSLVDS1047 differential line driver is a balanced current source design. A current mode driver, generally speaking has a high output impedance and supplies a constant current for a range of loads (a voltage mode driver on the other hand supplies a constant voltage for a range of loads). Current is switched through the load in one direction to produce a logic state and in the other direction to produce the other logic state. The output current is typically 3.1 mA, a minimum of 2.5 mA, and a maximum of 4.5 mA. The current mode driver requires that a resistive termination be employed to terminate the signal and to complete the loop as shown in Figure 24. AC or unterminated configurations are not allowed. The 3.1-mA loop current develops a differential voltage of 310 mV across the 100-Ω termination resistor which the receiver detects with a 250-mV minimum differential noise margin, (driven signal minus receiver threshold (250 mV – 100 mV = 150 mV). The signal is centered around +1.2 V (Driver Offset, V_{OS}) with respect to ground as shown in Figure 23.

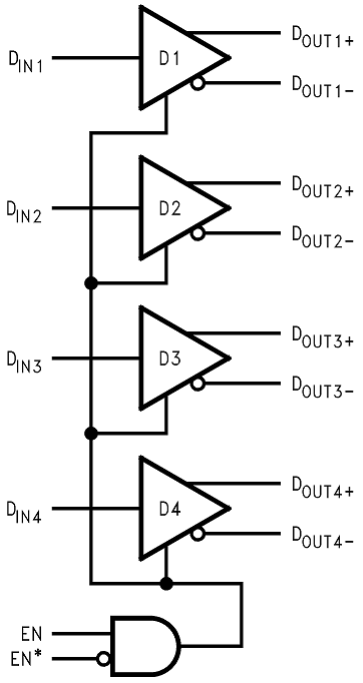
NOTE

The steady-state voltage (V_{SS}) peak-to-peak swing is twice the differential voltage (V_{OD}) and is typically 620 mV.

The current mode driver provides substantial benefits over voltage mode drivers, such as an RS-422 driver. Its quiescent current remains relatively flat versus switching frequency. Whereas the RS-422 voltage mode driver increases exponentially in most case from 20 MHz to 50 MHz. This is due to the overlap current that flows between the rails of the device when the internal gates switch. Whereas the current mode driver switches a fixed current between its output without any substantial overlap current. This is similar to some ECL and PECL devices, but without the heavy static I_{CC} requirements of the ECL/PECL designs. LVDS requires > 80% less current than similar PECL devices. AC specifications for the driver are a tenfold improvement over other existing RS-422 drivers.

The TRI-STATE function allows the driver outputs to be disabled, thus obtaining an even lower power state when the transmission of data is not required.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 LVDS Fail-Safe

This section addresses the common concern of fail-safe biasing of LVDS interconnects, specifically looking at the DSLVDS1047 driver outputs and the DSLVDS1048 receiver inputs.

The LVDS receiver is a high-gain, high-speed device that amplifies a small differential signal (20 mV) to CMOS logic levels. Due to the high gain and tight threshold of the receiver, take care to prevent noise from appearing as a valid signal.

The internal fail-safe circuitry of the receiver is designed to source or sink a small amount of current, providing fail-safe protection (a stable known state of HIGH output voltage) for floating, terminated, or shorted receiver inputs.

1. **Open Input Pins.** The DSLVDS1048 is a quad receiver device, and if an application requires only 1, 2, or 3 receivers, the unused channel(s) inputs must be left OPEN. Do not tie unused receiver inputs to ground or any other voltages. The input is biased by internal high value pullup and pulldown resistors to set the output to a HIGH state. This internal circuitry ensures a HIGH, stable output state for open inputs.
2. **Terminated Input.** If the DSLVDS1047 driver is disconnected (cable unplugged), or if the DSLVDS1047 driver is in a TRI-STATE or power-off condition, the receiver output is again in a HIGH state, even with the end of cable 100-Ω termination resistor across the input pins. The unplugged cable can become a floating antenna which can pick up noise. If the cable picks up more than 10 mV of differential noise, the receiver may see the noise as a valid signal and switch. To insure that any noise is seen as common-mode and not differential, a balanced interconnect must be used. Twisted pair cable offers better balance than flat ribbon cable.
3. **Shorted Inputs.** If a fault condition occurs that shorts the receiver inputs together, thus resulting in a 0-V differential input voltage, the receiver output remains in a HIGH state. Shorted input fail-safe is not supported across the common-mode range of the device (GND to 2.4 V). It is only supported with inputs shorted and no external common-mode voltage applied.

Feature Description (continued)

External lower value pullup and pulldown resistors (for a stronger bias) may be used to boost fail-safe in the presence of higher noise levels. The pullup and pulldown resistors should be in the 5-kΩ to 15-kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point should be set to approximately 1.2 V (less than 1.75 V) to be compatible with the internal circuitry.

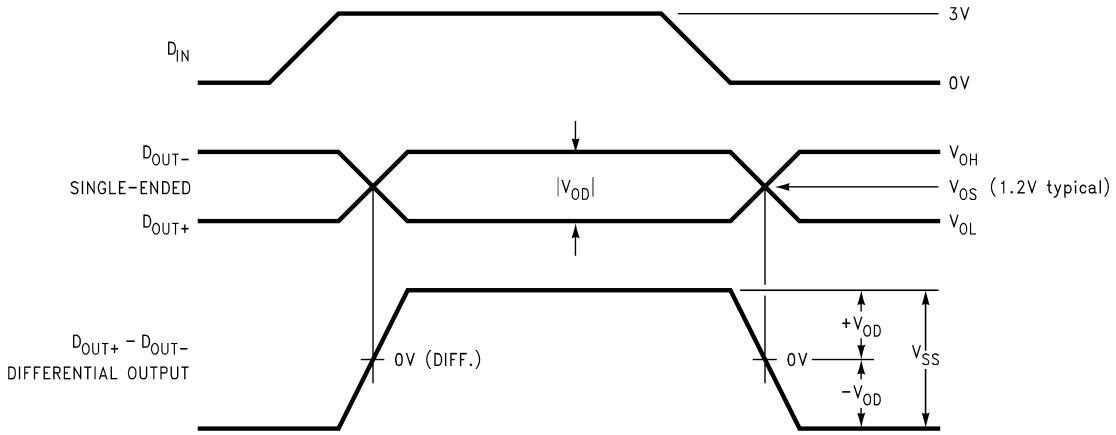


Figure 23. Driver Output Levels

8.4 Device Functional Modes

Table 1 lists the functional modes DSLVDS1047.

Table 1. Truth Table

ENABLES		INPUT	OUTPUTS	
EN	EN*	D_{IN}	D_{OUT+}	D_{OUT-}
H	L or Open	L	L	H
		H	H	L
All other combinations of ENABLE inputs		X	Z	Z

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DSLVDS1047 has a flow-through pinout that allows for easy PCB layout. The LVDS signals on one side of the device easily allows for matching electrical lengths of the differential pair trace lines between the driver and the receiver as well as allowing the trace lines to be close together to couple noise as common-mode. Noise isolation is achieved with the LVDS signals on one side of the device and the TTL signals on the other side.

9.2 Typical Application

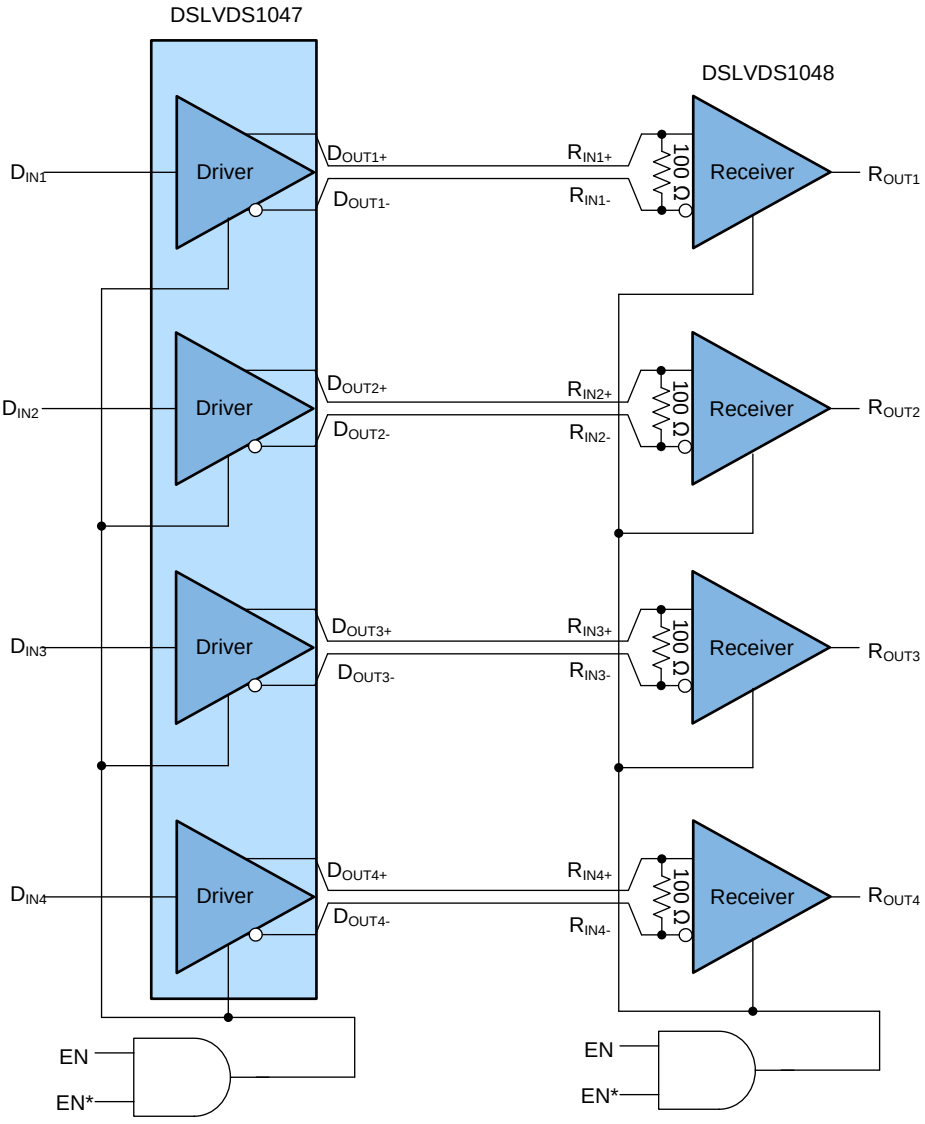


Figure 24. Point-to-Point Application

Typical Application (continued)

9.2.1 Design Requirements

When using LVDS devices, it is important to remember to specify controlled impedance PCB traces, cable assemblies, and connectors. All components of the transmission media should have a matched differential impedance of about 100 Ω. They should not introduce major impedance discontinuities.

Balanced cables (for example, twisted pair) are usually better than unbalanced cables (ribbon cable) for noise reduction and signal quality. Balanced cables tend to generate less EMI due to field canceling effects and also tend to pick up electromagnetic radiation as common-mode (not differential mode) noise which is rejected by the LVDS receiver.

For cable distances < 0.5 M, most cables can be made to work effectively. For distances 0.5 M ≤ d ≤ 10 M, CAT5 (Category 5) twisted pair cable works well, is readily available and relatively inexpensive.

Table 2. Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUE
Driver Supply Voltage (V_{CC})	3.0 to 3.6 V
Driver Input Voltage	0 to 3.6 V
Driver Signaling Rate	DC to 400 Mbps
Interconnect Characteristic Impedance	100 Ω
Termination Resistance	100 Ω
Number of Receiver Nodes	1
Ground shift between driver and receiver	±1 V

9.2.2 Detailed Design Procedure

9.2.2.1 Probing LVDS Transmission Lines

Always use high impedance (> 100 kΩ), low capacitance (< 2 pF) scope probes with a wide bandwidth (1 GHz) scope. Improper probing gives deceiving results.

9.2.2.2 Data Rate vs Cable Length Graph Test Procedure

A pseudo-random bit sequence (PRBS) of 2^9-1 bits was programmed into a function generator (Tektronix HFS9009) and connected to the driver inputs through 50-Ω cables and SMB connectors. An oscilloscope (Tektronix 11801B) was used to probe the resulting eye pattern, measured differentially at the input to the receiver. A 100-Ω resistor was used to terminate the pair at the far end of the cable. The measurements were taken at the far end of the cable, at the input of the receiver, and used for the jitter analysis for this graph (Figure 17). The frequency of the input signal was increased until the measured jitter (t_{tcs}) equaled 20% with respect to the unit interval (t_{tui}) for the particular cable length under test. Twenty percent jitter is a reasonable place to start with many system designs. The data used was NRZ. Jitter was measured at the 0-V differential voltage of the differential eye pattern. The DSLVDS1047 and DSLVDS1048 can be evaluated using the new DS90LV047-048AEVM.

Figure 25 shows very good typical performance that can be used as a design guideline for data rate vs cable length. Increasing the jitter percentage increases the curve respectively, allowing the device to transmit faster over longer cable lengths. This relaxes the jitter tolerance of the system allowing more jitter into the system, which could reduce the reliability and efficiency of the system. Alternatively, decreasing the jitter percentage has the opposite effect on the system. The area under the curve is considered the safe operating area based on the above signal quality criteria. For more information on eye pattern testing, please see *AN-808 Long Transmission Lines and Data Signal Quality* (SNLA028).

9.2.3 Application Curve

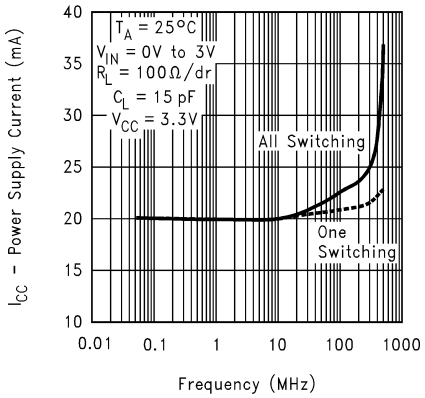


Figure 25. Power Supply Current vs Frequency

10 Power Supply Recommendations

Although the DSLVDS1047 draws very little power while at rest. At higher switching frequencies there is a dynamic current component which increases the overall power consumption. The DSLVDS1047 power supply connection must take this additional current consumption into consideration for maximum power requirements.

11 Layout

11.1 Layout Guidelines

- Use at least 4 PCB layers (top to bottom); LVDS signals, ground, power, TTL signals.
- Isolate TTL signals from LVDS signals, otherwise the TTL may couple onto the LVDS lines. It is best to put TTL and LVDS signals on different layers which are isolated by a power/ground plane(s).
- Keep drivers and receivers as close to the (LVDS port side) connectors as possible.

11.1.1 Power Decoupling Recommendations

Bypass capacitors must be used on power pins. Use high frequency ceramic (surface mount is recommended) 0.1-µF and 0.001-µF capacitors in parallel at the power supply pin with the smallest value capacitor closest to the device supply pin. Additional scattered capacitors over the printed-circuit board improves decoupling. Multiple vias must be used to connect the decoupling capacitors to the power planes. A 10-µF (35-V) or greater solid tantalum capacitor must be connected at the power entry point on the printed-circuit board between the supply and ground.

11.1.2 Differential Traces

Use controlled impedance traces which match the differential impedance of your transmission medium (that is, cable) and termination resistor. Run the differential pair trace lines as close together as possible as soon as they leave the IC (stubs must be < 10 mm long). This helps eliminate reflections and ensure noise is coupled as common-mode. In fact, we have seen that differential signals which are 1 mm apart radiate far less noise than traces 3 mm apart since magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

Match electrical lengths between traces to reduce skew. Skew between the signals of a pair means a phase difference between signals, which destroys the magnetic field cancellation benefits of differential signals and EMI, results.

NOTE

The velocity of propagation, v = c/Er where c (the speed of light) = 0.2997mm/ps or 0.0118 in/ps

Do not rely solely on the autoroute function for differential traces. Carefully review dimensions to match differential impedance and provide isolation for the differential lines. Minimize the number or vias and other discontinuities on the line.

Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels.

Within a pair of traces, the distance between the two traces must be minimized to maintain common-mode rejection of the receivers. On the printed-circuit board, this distance must remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable.

11.1.3 Termination

Use a termination resistor which best matches the differential impedance or your transmission line. The resistor must be between 90 Ω and 130 Ω. Remember that the current mode outputs need the termination resistor to generate the differential voltage. LVDS does not work without resistor termination. Typically, connecting a single resistor across the pair at the receiver end will suffice.

Layout Guidelines (continued)

Surface mount 1% to 2% resistors are best. PCB stubs, component lead, and the distance from the termination to the receiver inputs must be minimized. The distance between the termination resistor and the receiver should be < 10 mm (12 mm maximum).

11.2 Layout Example

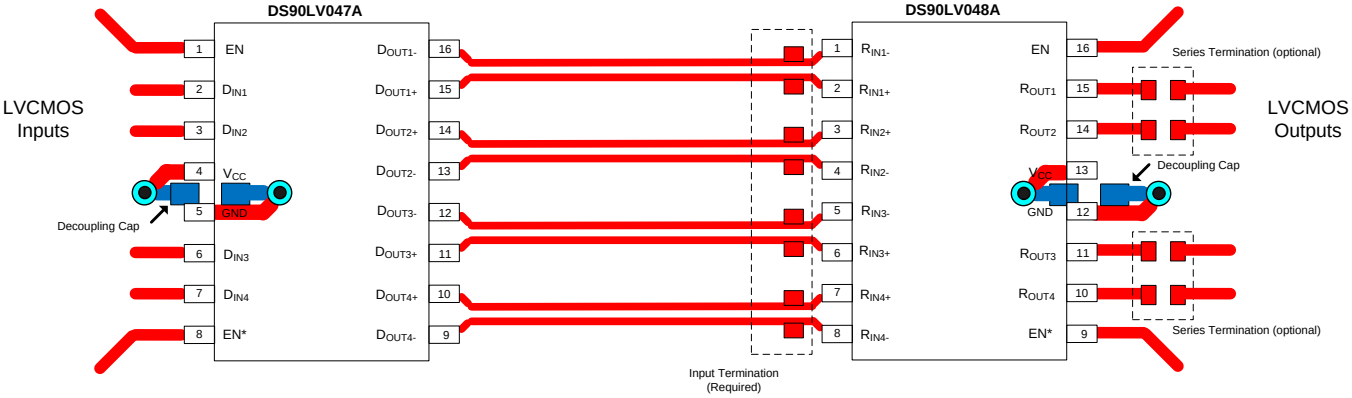


Figure 26. Layout Recommendation

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.3 商标

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12.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DSLVDS1047PWR	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DSLVDS 1047	Samples
DSLVDS1047PWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	DSLVDS 1047	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

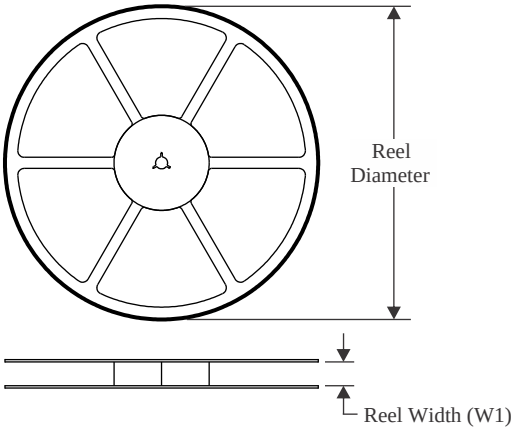
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

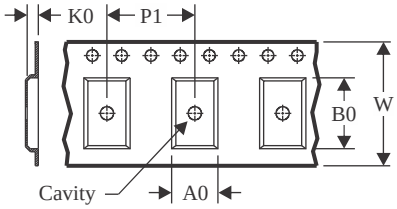
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

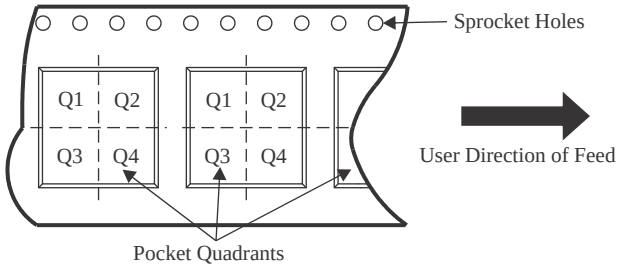


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

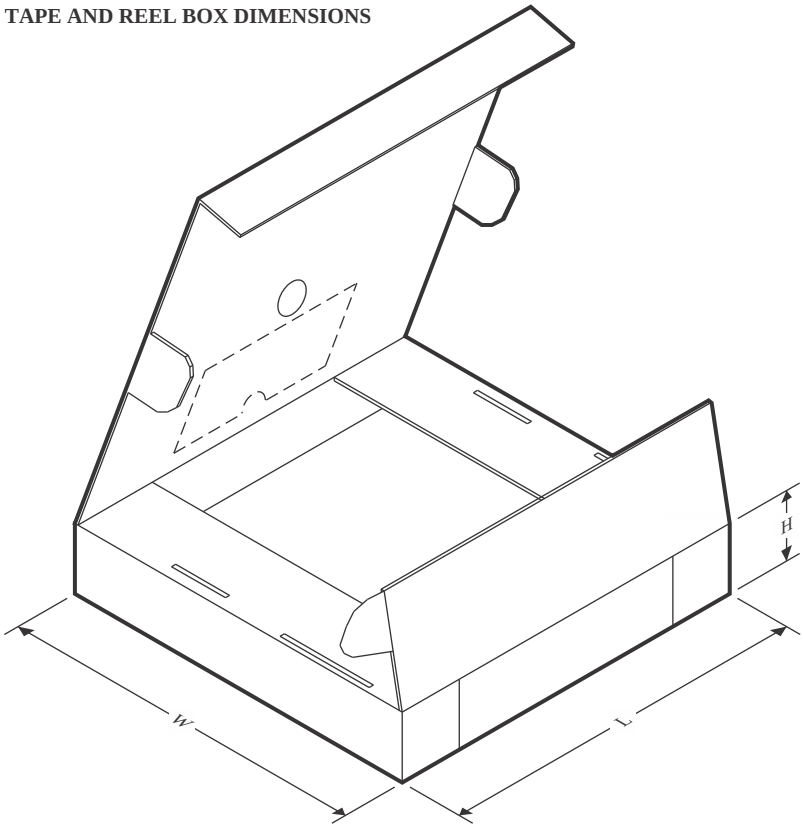
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DSLVDS1047PWR	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1
DSLVDS1047PWT	TSSOP	PW	16	250	178.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

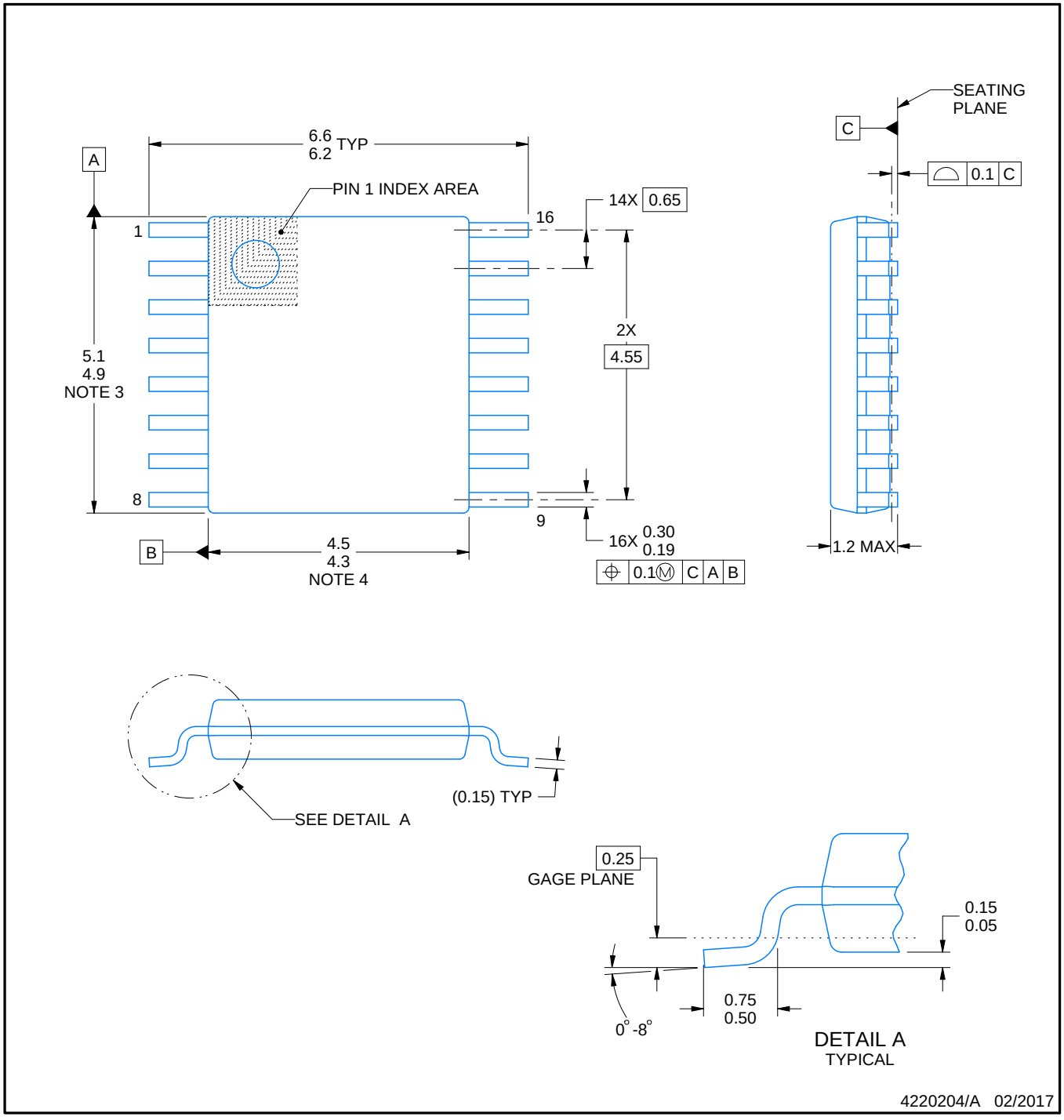
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DSLVDS1047PWR	TSSOP	PW	16	2500	367.0	367.0	35.0
DSLVDS1047PWT	TSSOP	PW	16	250	210.0	185.0	35.0

PACKAGE OUTLINE

PW0016A

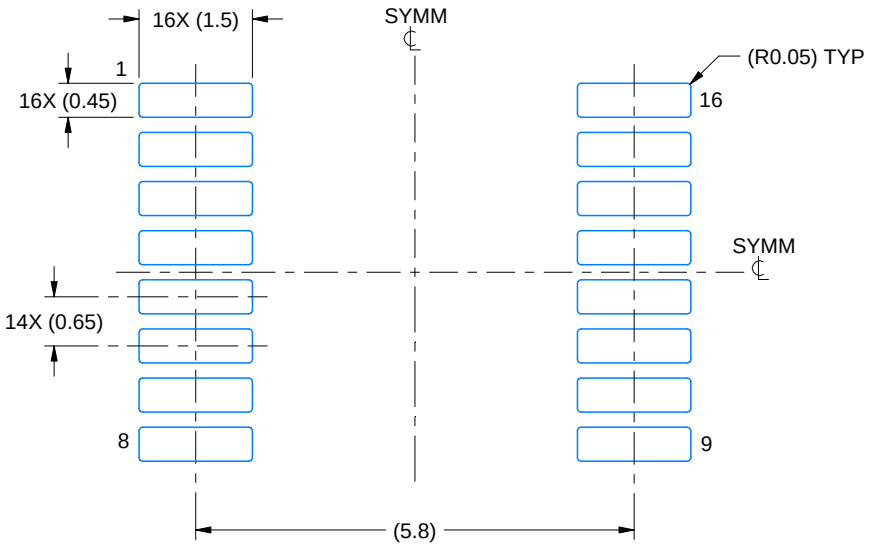
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

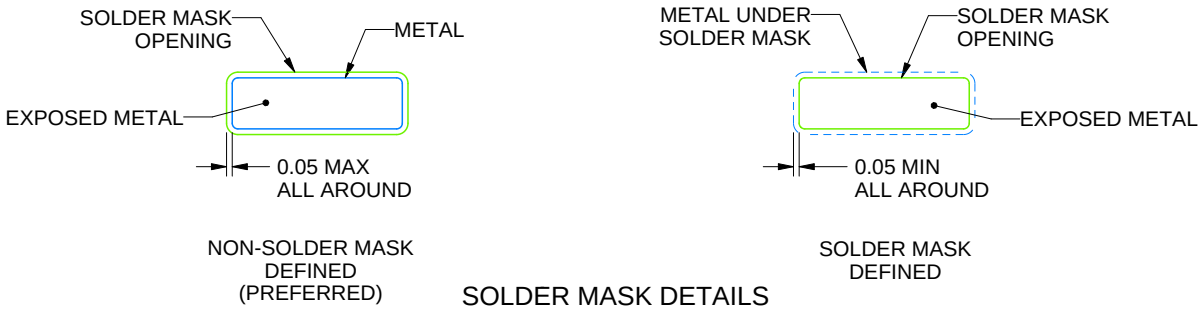


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

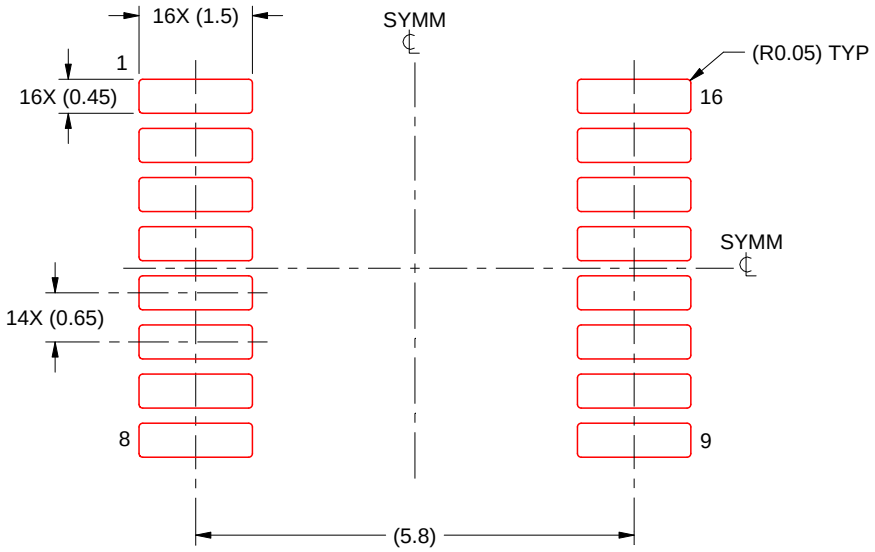


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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