LSF0102-Q1 汽车类 2 通道自动双向多电压电平转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 温度等级 1：–40°C ≤ T_A ≤ 125°C
  - 器件 HBM ESD 分类等级 2
  - CDM ESD 分类等级 C6
- 用无方向引脚提供双向电压转换
- 支持开漏和推挽应用，如 I^2C、SPI、UART、MDIO、SDIO 和 GPIO
- 在不超过 30pF 的容性负载条件下支持最高达 100MHz 的上行转换和超过 100MHz 的下行转换，在 50pF 的容性负载条件下支持高达 40MHz 的上行/下行转换
- 可实现以下电压之间的双向电压电平转换
  - 0.95V ↔ 1.8/2.5/3.3/5 V
  - 1.2V ↔ 1.8/2.5/3.3/5V
  - 1.8V ↔ 2.5/3.3/5V
  - 2.5V ↔ 3.3/5V
  - 3.3V ↔ 5V
- 低待机电流
- 5V 耐受 I/O 端口，可支持 TTL 电压电平
- 低导通电阻，可减少信号失真
- EN = 低电平时为高阻抗 I/O 引脚
- 采用直通引脚排列以简化 PCB 布线
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 信息娱乐系统音响主机
- 图形群集
- ADAS 融合
- ADAS 前置摄像头
- HEV 电池管理系统

3 说明

LSF0102-Q1 器件是一款自动双向电压转换器，无需方向引脚即可在广泛的电源范围内进行转换。当容性负载 ≤ 30pF 时，LSF0102-Q1 支持最高 100MHz 的升压转换和高于 100MHz 的降压转换。此外，当容性负载为 50pF 时，LSF0102-Q1 支持最高 40MHz 的上行和下行转换，因此，LSF0102-Q1 器件可支持汽车中各种常见的标准接口，如 I^2C、SPI、GPIO、SDIO、UART 和 MDIO。

LSF0102-Q1 器件具有 5V 耐受数据输入。因此该器件可兼容 TTL 电压电平。此外，LSF0102-Q1 还支持混合模式电压转换，可在各个通道上升压和降压转换至不同的电源电平。

器件信息(1)

器件型号	封装（引脚）	封装尺寸（标称值）
LSF0102QDCURQ1	VSSOP (8)	2.30mm x 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

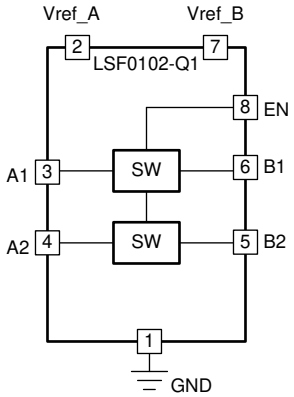


Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (May 2018) to Revision A (April 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated the *Bidirectional Translation* section to include inclusive terminology	11

5 Pin Configuration and Functions

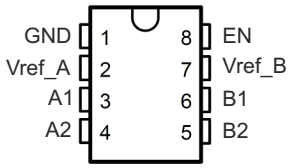


图 5-1. LSF0102-Q1 DCU Package, 8-Pin VSSOP (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	DCU		
A1	3	I/O	Input/Output A port for Channel 1
A2	4	I/O	Input/Output A port for Channel 2
B1	6	I/O	Input/Output B port for Channel 1
B2	5	I/O	Input/Output B port for Channel 2
EN	8	I	I/O enable input; see 图 9-1 for typical setup. Should be tied directly to Vref_B to be enabled or pulled LOW to disable all I/O pins.
GND	1	—	Ground
Vref_A	2	—	A side reference supply voltage; see 节 9 for setup and supply voltage range.
Vref_B	7	—	B side reference supply voltage. Must be connected to supply through 200 kΩ; see 节 9 for setup and supply voltage range.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage(2), V_I		–0.5	7	V
Input/output voltage(2), $V_{I/O}$		–0.5	7	V
Continuous channel current			128	mA
Input clamp current, I_{IK}	$V_I < 0$		–50	mA
Storage temperature range, T_{stg}		–65	150	°C
Operating junction temperature, T_J			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage		5	V
$V_{ref\_A/B/EN}$	Reference voltage		5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LSF0102-Q1 DCU (US8) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	106.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	141.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	141.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = – 18 mA, V_{EN} = 0				– 1.2	V
I_{IH}	I/O input high leakage	V_I = 5 V, V_{EN} = 0				5.0	µA
I_{CCBA}	V_{ref_B} to V_{ref_A} leakage	V_{ref_B} = V_{EN} = 5.5 V, V_{ref_A} = 4.5 V, I_O = 0, V_I = V_{CC} or GND			1		µA
$C_{I(ref\_A/B/EN)}$	Input capacitance	V_I = 3 V or 0			11		pF
$C_{io(off)}$	I/O pin off-state capacitance	V_O = 3 V or 0, V_{EN} = 0			4.0	6.0	pF
$C_{io(on)}$	I/O Pin on-state capacitance	V_O = 3 V or 0, V_{EN} = 3 V			10.5	12.5	pF
r_{on} (2)	On-state resistance	V_I = 0, I_O = 64 mA	V_{ref_A} = 3.3 V; V_{ref_B} = V_{EN} = 5 V		8.0		Ω
			V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 5 V		9.0		
			V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 5 V		10		
		V_I = 0, I_O = 32 mA	V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 5 V		10		Ω
			V_{ref_A} = 2.5 V; V_{ref_B} = V_{EN} = 5 V		15		
		V_I = 1.8 V, I_O = 15 mA	V_{ref_A} = 3.3 V; V_{ref_B} = V_{EN} = 5 V		9.0		Ω
		V_I = 1.0 V, I_O = 10 mA	V_{ref_A} = 1.8 V; V_{ref_B} = V_{EN} = 3.3 V		18		Ω
		V_I = 0 V, I_O = 10 mA	V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 3.3 V		20		Ω
		V_I = 0 V, I_O = 10 mA	V_{ref_A} = 1.0 V; V_{ref_B} = V_{EN} = 1.8 V		30		Ω

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B pins at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) pins.

6.6 Switching Characteristics (Translating Down): V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see 节 7 table)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1.1			0.7			0.3		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1.2			0.8			0.4		

6.7 Switching Characteristics (Translating Down): V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see 节 7 table)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1.2			0.8			0.35		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1.3			1			0.5		

6.8 Switching Characteristics Translating Up): V_{GATE} = 3.3 V

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V and R_L = 300 (unless otherwise noted) (see 节 7 table)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1			0.8			0.4		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1			0.9			0.4		

6.9 Switching Characteristics (Translating Up): V_{GATE} = 2.5 V

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V and R_L = 300 (unless otherwise noted) (see 节 7 table)

PARAMETER		TEST CONDITIONS	C_L = 50 pF			C_L = 30 pF			C_L = 15 pF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high output	From (input) A or B to (output) B or A		1.1			0.9			0.45		ns
t_{PHL}	Propagation delay time, high-to-low output	From (input) A or B to (output) B or A		1.3			1.1			0.6		

6.10 Typical Characteristics

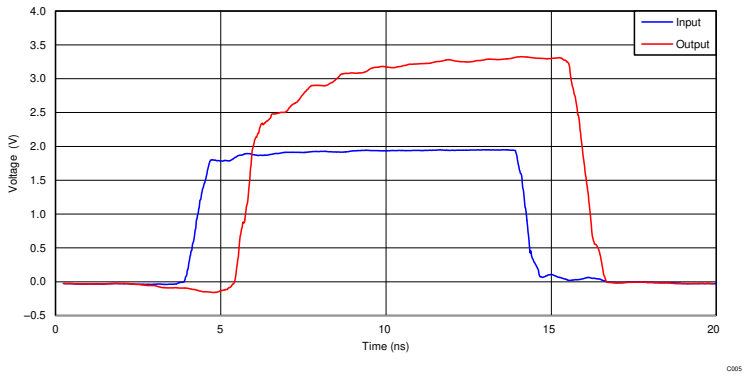
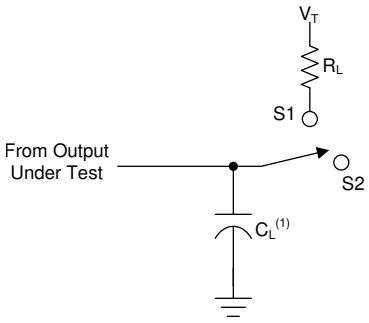


图 6-1. Signal Integrity (1.8 to 3.3 V Translation Up at 50 MHz)

7 Parameter Measurement Information

The outputs are measured one at a time, with one transition per measurement. All input pulses are supplied by generators that have the following characteristics:

- PRR ⩽ 10 MHz
- Z_O = 50 Ω
- t_r ⩽ 2 ns
- t_f ⩽ 2 ns



A. C_L includes probe and jig capactictance.

图 7-1. Load Circuit

USAGE	SWITCH
Translating Up Translating Down	S1 S2

图 7-2. Translating Up and Down Table

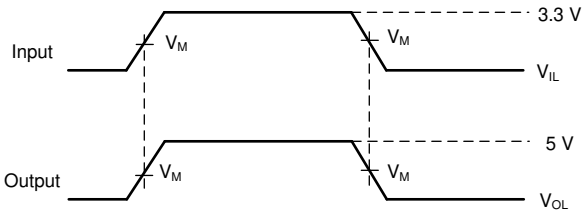


图 7-3. Translating Up

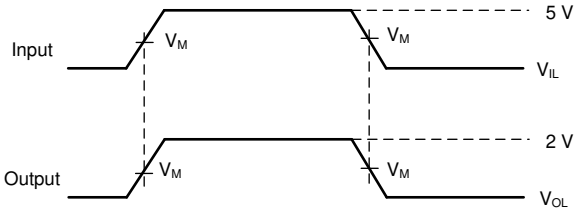


图 7-4. Translating Down

8 Detailed Description

8.1 Overview

The LSF0102-Q1 device can be used in level translation applications for interfacing devices or systems operating at different interface voltages. The LSF0102-Q1 device is ideal for use in applications where an open-drain driver is connected to the data I/Os. With appropriate pull-up resistors and layout, the LSF0102-Q1 device can achieve 100 MHz. The LSF0102-Q1 can also be used in applications where a push-pull driver is connected to the data I/Os.

8.2 Functional Block Diagrams

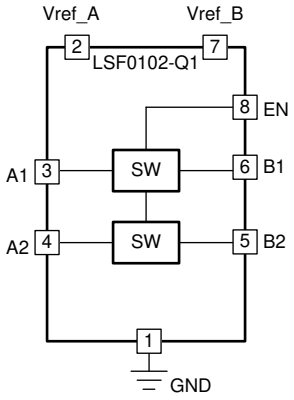


图 8-1. LSF0102-Q1 Functional Block Diagram

8.3 Feature Description

8.3.1 Auto Bidirectional Voltage Translation

The LSF0102-Q1 device is an auto bidirectional voltage level translator that operates from 0.95 to 4.5 V on Vref_A and 1.8 to 5.5 V on Vref_B. This allows bidirectional voltage translation between 0.95 V and 5.5 V without the need for a direction pin in open-drain or push-pull applications. The LSF0102-Q1 device supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 250-Ω pullup resistor with a 30-pF capacitive load.

8.3.2 Output Enable

When EN is HIGH, the translator switch is on, and the An I/O is connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high-impedance state exists between ports. To enable the I/O pins, the EN input should be tied directly to Vref_B. To ensure the high-impedance state during power-up or power-down, EN must be LOW. For additional details on how to use the enable pin, see the *Using the Enable Pin with the LSF Family* video.

表 8-1. Enable Function Table

INPUT EN(1) PIN	FUNCTION
Tied directly to Vref_B	An = Bn
L	Hi-Z

(1) EN is controlled by V_{ref_B} logic levels and should be at least 1 V higher than V_{ref_A} for best translator.

8.3.3 Mixed-Mode Voltage Translation

The supply voltage (Vpu#) for each channel can be individually set up with a pull-up resistor. For example, CH1 can be used in up-translation mode (1.2 V ↔ 3.3 V) and CH2 in down-translation mode (2.5 V ↔ 1.8 V). For additional details on how to use the LSF0102-Q1 for mixed-mode voltage translation, see the *Multi-Voltage Translation with the LSF Family* video.

8.4 Device Functional Modes

When the An or Bn port is LOW, the switch is in the ON-state and a low resistance connection exists between the An and Bn ports. The low R_{on} of the switch allows connections to be made with minimal propagation delay and signal distortion. Assuming the higher voltage is on the Bn port when the Bn port is HIGH, the voltage on the An port is limited to the voltage set by Vref_A. When the An port is HIGH, the Bn port is pulled to the drain pull-up supply voltage ($V_{pu\#}$) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for direction control. For additional details on the functional operation of the LSF0102-Q1, see the *Down Translation with the LSF Family* and *Up Translation with the LSF Family* videos.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The LSF0102-Q1 device is able to perform voltage translation for open-drain or push-pull interfaces such as I^2C, SPI, UART, MDIO, SDIO, and GPIO.

9.2 Typical Application

9.2.1 Bidirectional Translation

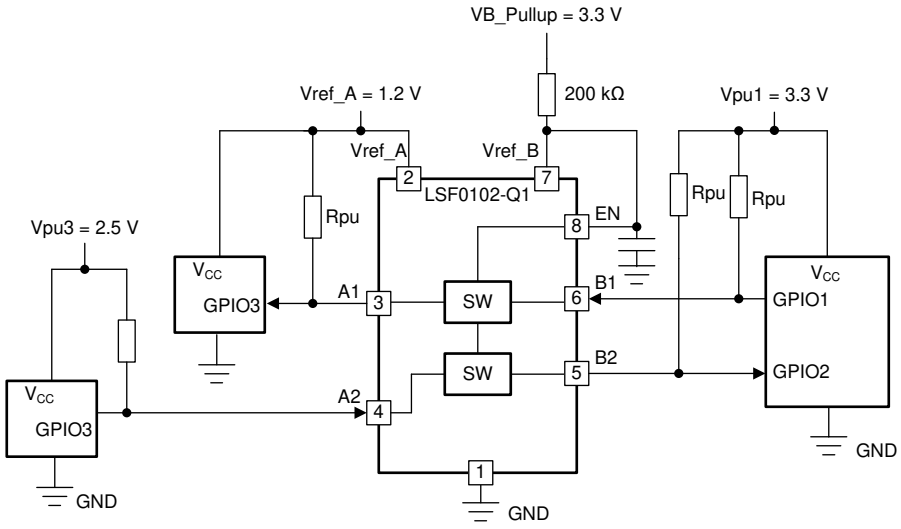


图 9-1. Bidirectional Translation to Multiple Voltage Levels

9.2.1.1 Design Requirements

9.2.1.1.1 Enable, Disable, and Reference Voltage Guidelines

The LSF0102-Q1 device has an EN input that is used to disable the device by setting EN LOW, which places all I/Os in the high-impedance state. Since LSF family is switch-type voltage translator, the power consumption is very low. It is recommended to always enable LSF0102-Q1 device for bidirectional applications by connecting the EN pin to the Vref_B pin, as shown in 图 9-1. For additional details on setting up the Vref_A, Vref_B, and EN pins, see the *Understanding the Bias Circuit for the LSF Family* video.

表 9-1. Application Operating Condition

PARAMETER		MIN	TYP	MAX	UNIT
Vref_A(1)	reference voltage (A)	0.95		4.5	V

表 9-1. Application Operating Condition (continued)

PARAMETER		MIN	TYP	MAX	UNIT
Vref_B	reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	Vref_A + 0.8	Vref_B	5.5	V
Vpu	pull-up supply voltage	0		Vref_B	V

(1) Vref_A is required to be the lowest voltage level across all inputs and outputs.

The 200 kΩ, pull-up resistor is required to allow Vref_B to regulate the EN input. A filter capacitor on Vref_B is recommended. Also Vref_B and $V_{I(EN)}$ are recommended to be 1.0 V higher than Vref_A for best signal integrity.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Bidirectional Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to Vref_B and both pins pulled to HIGH side Vpu through a pull-up resistor (typically 200 kΩ), as shown in 图 9-1. This allows Vref_B to regulate the EN input. A filter capacitor on Vref_B is recommended. The controller output driver can be push-pull or open-drain (pull-up resistors may be required) and the peripheral device output can be push-pull or open-drain (pull-up resistors are required to pull the Bn outputs to Vpu).

If either output is push-pull, data must be unidirectional or the outputs must be tri-state and be controlled by some direction-control mechanism to prevent HIGH-to-LOW contention in either direction. If both outputs are open-drain, no direction control is needed.

In 图 9-1, the reference supply voltage (Vref_A) is connected to the processor core power supply voltage. When Vref_B is connected through a 200 kΩ resistor to a 3.3 V Vpu power supply, and Vref_A is set 1.2 V. The output of A1 has a maximum output voltage equal to Vref_A, and the bidirectional interface on channel 2 has a maximum output voltage equal to Vpu.

9.2.1.2.2 Pull-up Resistor Sizing

To maintain an appropriate output low voltage, the pull-up resistor value should limit the current through the pass transistor when it is in the ON state to less than 15 mA. This ensures a pass voltage of 260 mV to 350 mV. To set the current through each pass transistor at 15 mA, the pull-up resistor value can be calculated using the following equation:

$$Rpu = (Vpu - 0.35\ V) / 0.015\ A \quad (1)$$

The appropriate pull up resistor will depend on the current requirements of the application. 表 9-2 summarizes resistor values, reference voltages, and currents at 15 mA, 10 mA, and 3 mA. The resistor value shown in the +10% column (or a larger value) should be used to ensure that the pass voltage of the transistor is 350 mV or less. The external driver must be able to sink the total current from the resistors on both sides of the LSF0102-Q1 device at 0.175 V, although the 15 mA applies only to current flowing through the LSF0102-Q1.

表 9-2. Pull-up Resistor Values

V_{DPU}	15 mA		10 mA		3 mA	
	NOMINAL (Ω)	+10%(1) (Ω)	NOMINAL (Ω)	+10%(1) (Ω)	NOMINAL (Ω)	+10%(1) (Ω)
5 V	310	341	465	512	1550	1705
3.3 V	197	217	295	325	983	1082
2.5 V	143	158	215	237	717	788
1.8 V	97	106	145	160	483	532
1.5 V	77	85	115	127	383	422
1.2 V	57	63	85	94	283	312

(1) +10% to compensate for V_{DD} range and resistor tolerance

9.2.1.3 Application Curve

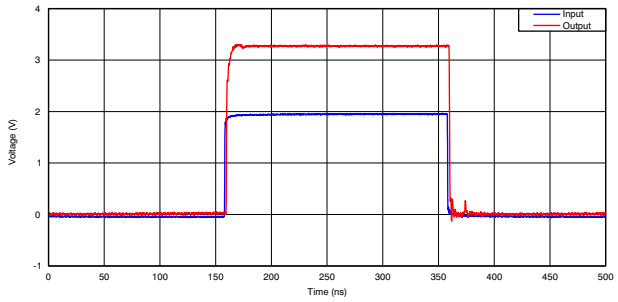


图 9-2. Captured Waveform From Above I²C Set-Up (1.8 V to 3.3 V at 2.5 MHz)

10 Power Supply Recommendations

There are no power sequence requirements for the LSF family. For recommended operating voltages for all supply and input pins, see 表 10-1.

表 10-1. Recommended Operating Voltages

PARAMETER		MIN	TYP	MAX	UNIT
Vref_A(1)	reference voltage (A)	0.95		4.5	V
Vref_B	reference voltage (B)	Vref_A + 0.8		5.5	V
$V_{I(EN)}$	input voltage on EN pin	Vref_A + 0.8		5.5	V
Vpu	pull-up supply voltage	0		Vref_B	V

11 Layout

11.1 Layout Guidelines

Because the LSF0102-Q1 device is a switch-type level translator, the signal integrity is dependent upon the pull-up resistor value and PCB board parasitics. Consider the following recommendations when designing with the LSF0102-Q1.

- Minimize the signal trace length to reduce capacitance
- Avoid using stubs in the signal path to reduce parasitics.
- Place the LSF0102-Q1 device near the high voltage side.
- Select the appropriate pull-up resistor that applies to translation levels and driving capability of transmitter.

11.2 Layout Example

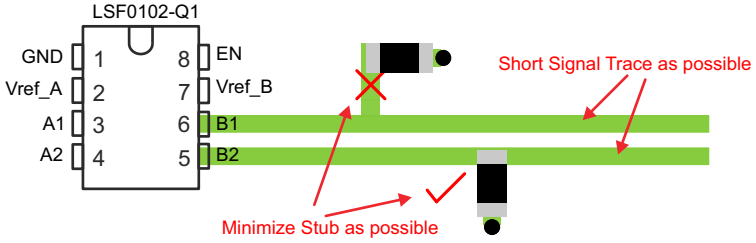


图 11-1. Short Trace Layout

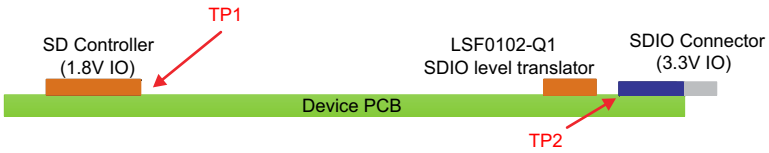


图 11-2. Device Placement

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, TI Logic Minute: *Introduction – Voltage Level Translation with the LSF Family* video
- Texas Instruments, *Voltage-Level Translation with the LSF Family* application report

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LSF0102QDCURQ1	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	NG2SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF LSF0102-Q1 :

- Catalog : LSF0102

NOTE: Qualified Version Definitions:

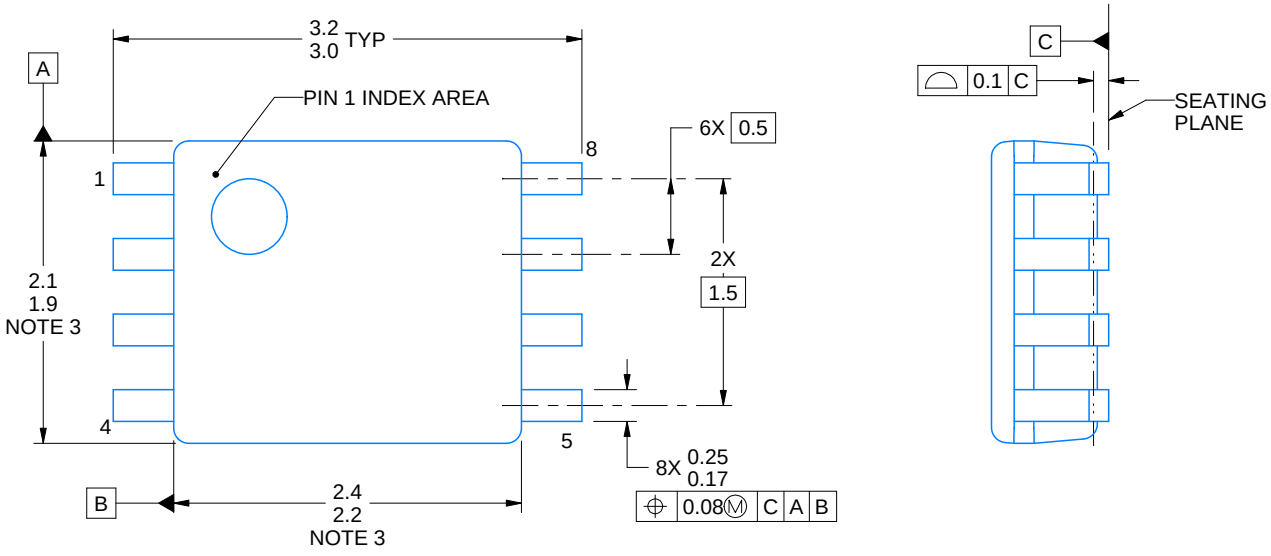
- Catalog - TI's standard catalog product

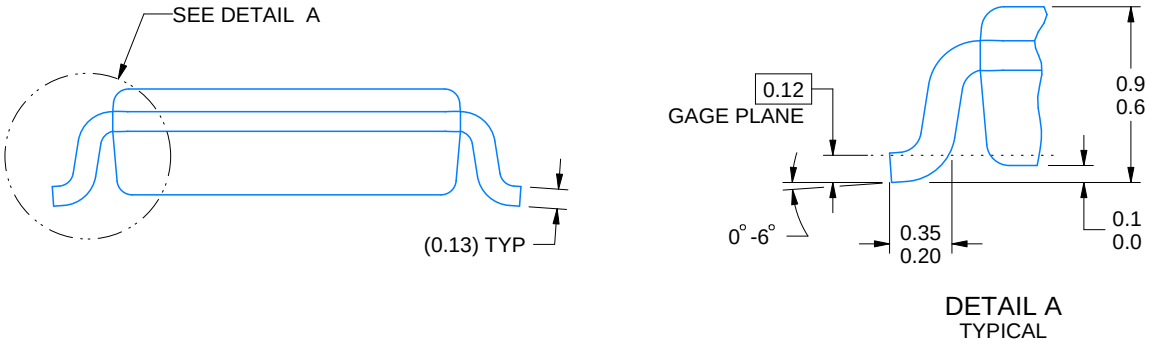
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

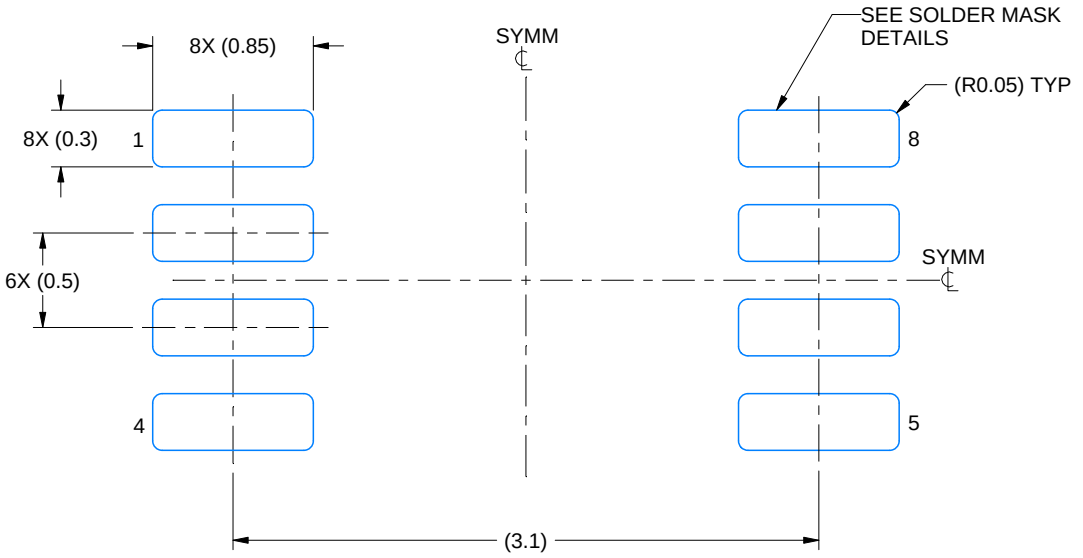




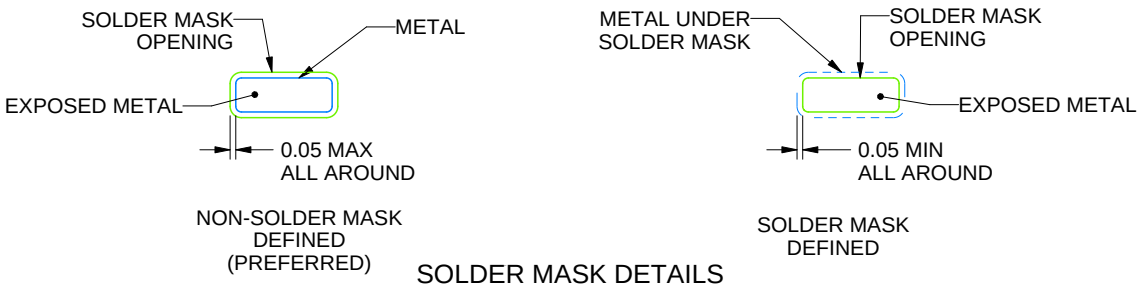
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

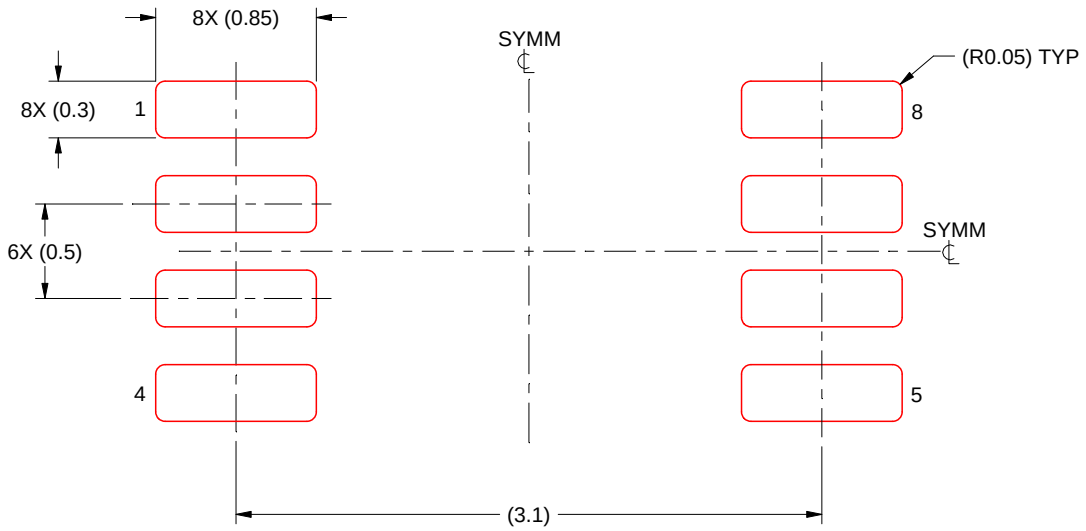


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265