SNx4LV06A Hex Inverter Buffers/Drivers With Open-Drain Outputs

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 6.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Outputs are Disabled During Power Up and Power Down With Inputs Tied to V_{CC}
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Live insertion, Partial Power Down Mode, and Back Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2500-V Human-Body Model (A114-1)
  - 200-V Machine Model (A115-A)
  - 2000-V Charged-Device Mode (C101)

2 Applications

- Servers
- Telecom Infrastructures
- TV Set-Top Boxes
- UPS
- Printers
- Elevators, and Escalators
- EPOS, ECR, and Cash Drawers
- Vending, Payment, Cash Machines

3 Description

These hex inverter buffers/drivers are designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV06A device performs the Boolean function $Y = \overline{A}$ in positive logic.

The open-drain output require pull-up resistors to perform correctly and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV06A	TVSOP (14)	3.60 mm x 4.40 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SOP (14)	10.30 mm x 5.30 mm
	SSOP (14)	6.20 mm x 5.30 mm
	TSSOP (14)	5.00 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

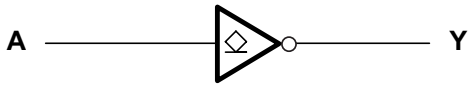


Table of Contents

4 Revision History

Changes from Revision I (February 2015) to Revision J — **Page**

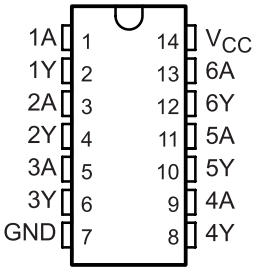
- Added T_J Junction temperature to the *Absolute Maximum Ratings*(1) table ... 4
- Changed Figure 6 ... 10

Changes from Revision H (April 2005) to Revision I — **Page**

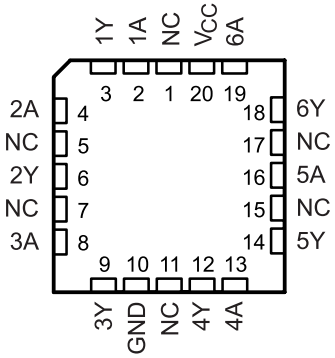
- Added *ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.* ... 1
- Changed datasheet title. ... 1

5 Pin Configuration and Functions

SN54LV06A . . . J OR W PACKAGE
SN74LV06A . . . D, DB, DGV, NS, OR PW PACKAGE
(TOP VIEW)



SN54LV06A . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1A	I	Input 1
2	1Y	O	Output 1
3	2A	I	Input 2
4	2Y	O	Output 2
5	3A	I	Input 3
6	3Y	O	Output 3
7	GND	GND	Ground Pin
8	4Y	O	Output 4
9	4A	I	Input 4
10	5Y	O	Output 5
11	5A	I	Input 5
12	6Y	O	Output 6
13	6A	I	Input 6
14	V_{CC}	—	Power Pin

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	7	V
V_I	Input voltage range(2)		–0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	7	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}		–35	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		–65	150	°C
T_J	Junction Temperature			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54LV06A(2)		SN74LV06A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2		2	5.5	V
V_{IH}	High level input voltage	V_{CC} = 2 V	.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		V_{CC} × 0.7		
V_{IL}	Low level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	5.5	0	5.5	V
I_{OL}	Low level output current	V_{CC} = 2 V		50		20	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
Δt/Δv	Input transition rise and fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).
(2) Product Preview.

6.4 Thermal Information

THERMAL METRIC[1]		SN74LV06A					UNIT
		D	DB	DGV	NS	PW	
		14 PINS	14 PINS	14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.6	112.5	135.2	95.4	128.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.8	65.0	57.9	52.9	57.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.9	59.9	68.3	51.2	70.7	
ψ_{JT}	Junction-to-top characterization parameter	25.0	25.0	9.2	17.9	9.3	
ψ_{JB}	Junction-to-board characterization parameter	54.7	59.3	67.6	53.8	70.0	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN74LV06A			–40°C to 85°C SN74LV06A			–40°C to 125°C SN74LV06A	UNIT
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{OL}	I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	0.1	V
	I_{OL} = 2 mA	2.3 V			0.4			0.4	0.4	
	I_{OL} = 8 mA	3 V			0.44			0.44	0.44	
	I_{OL} = 16 mA	4.5 V			0.55			0.55	0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	±1	µA
I_{OH}	$V_I = V_{IL}$, $V_{OH} = V_{CC}$	5.5 V			±2.5			±2.5	±2.5	µA
I_{CC}	$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			20			20	20	µA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5	5	µA
C_i	$V_I = V_{CC}$ or GND	3.3 V		1.6			1.6		1.6	pF

6.6 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C SN74LV06A		–40°C to 125°C SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5.4[1]	10.4[1]	1[1]	13[1]	1	14	ns
t_{PHL}					7.2[1]	10.4[1]	1[1]	13[1]	1	14	
t_{PLH}	A	Y	C_L = 50 pF		9.7	15.2	1	18	1	19	ns
t_{PHL}	A	Y			9.3	15.2	1	18	1	19	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C SN74LV06A		–40°C to 125°C SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		4.1[1]	7.1[1]	1[1]	8.5[1]	1	9.5	ns
t_{PHL}	A	Y			4.9[1]	7.1[1]	1[1]	8.5[1]	1	9.5	
t_{PLH}	A	Y	C_L = 50 pF		7.1	10.6	1	12	1	13	ns
t_{PHL}	A	Y			6.4	10.6	1	12	1	13	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			–40°C to 85°C SN74LV06A		–40°C to 125°C SN74LV06A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		3(1)	5.5(1)	1(1)	6.5(1)	1	7	ns
t_{PHL}	A	Y			3.3(1)	5.5(1)	1(1)	6.5(1)	1	7	
t_{PLH}	A	Y	C_L = 50 pF		4.8	7.5	1	8.5	1	9	ns
t_{PHL}	A	Y			4.4	7.5	1	8.5	1	9	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.9 Noise Characteristics(1)

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic VOL		–0.1	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

(1) Characteristics are for surface-mount packages only.

6.10 Operating Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	2.6	pF
				5 V	4.7	

6.11 Typical Characteristics

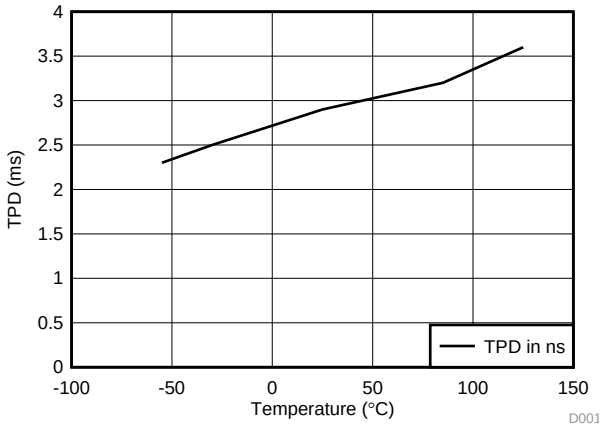


Figure 1. TPD vs Temperature at 5 V

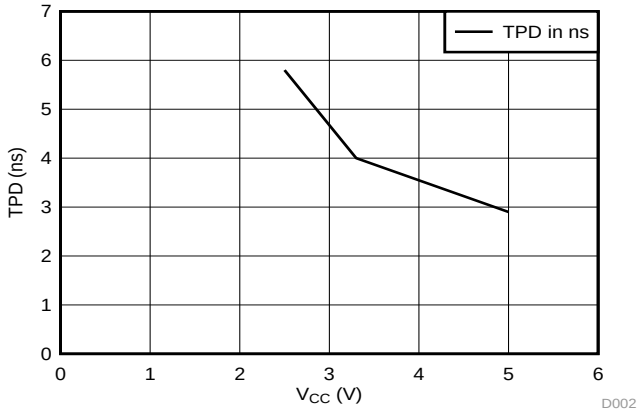
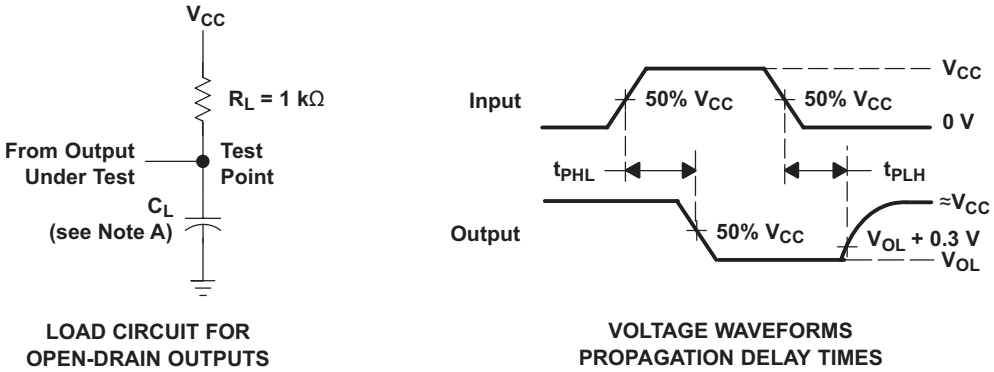


Figure 2. TPD vs V_{CC} at 25°C

7 Parameter Measurement Information



LOAD CIRCUIT FOR OPEN-DRAIN OUTPUTS

VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.

C. The outputs are measured one at a time, with one input transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

These hex inverter buffers/drivers are designed for 2-V to 5.5-V V_{CC} operation.

The SN74LV06A device performs the Boolean function $Y = \overline{A}$ in positive logic.

The open-drain output require pull-up resistors to perform correctly and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current back-flow through the devices when they are powered down.

8.2 Functional Block Diagram

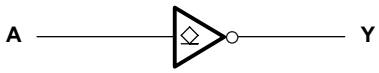


Figure 4. Logic Diagram (Positive Logic)

8.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows up or down voltage translation
  - Inputs and outputs accept voltages to 5.5 V
- I_{off} feature
  - Allows voltages on the inputs and outputs when V_{CC} is 0 V

8.4 Device Functional Modes

Table 1. Function Table (Each Inverter)

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV06A is a low drive Open drain CMOS device that can be used for a multitude of buffer type functions. The inputs are 5.5 V tolerant and the outputs open drain and 5.5 V tolerant allowing it to translate up to 5.5 V or down to any other voltage between GND and 5.5 V.

9.2 Typical Application

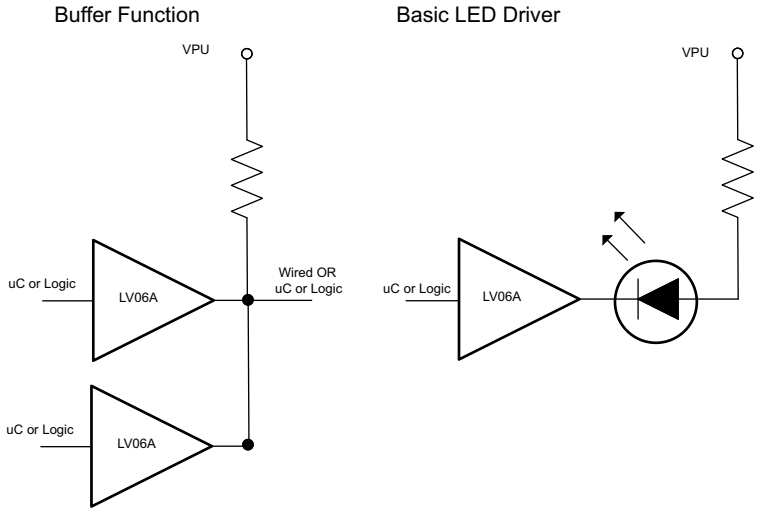


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and is open drain so it has low output drive only. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The parallel output drive can create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifications, see Δt/ΔV in the Recommended Operating Conditions table.
   - For specified high and low levels, see V_{IH} and V_{IL} in the *Recommended Operating Conditions* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommended Output Conditions:
   - Load currents should not exceed 35 mA per output and 50 mA total for the part.

Typical Application (continued)

9.2.3 Application Curves

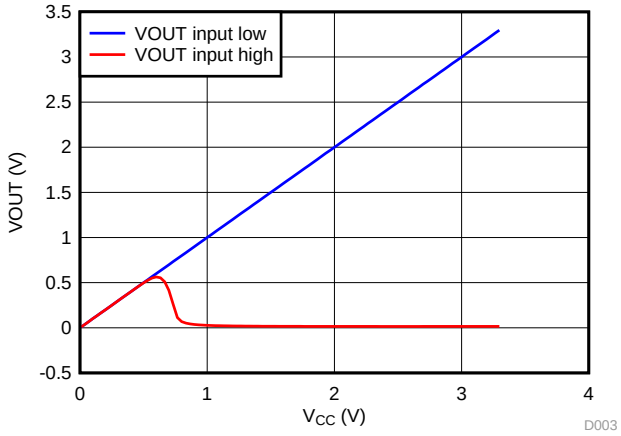


Figure 6. Output During Power Up with 4 k Pull-up at 3.3 V

10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 µF or 0.022 µF capacitor is recommended for each power terminal. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 µF and 1 µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver.

11.2 Layout Example

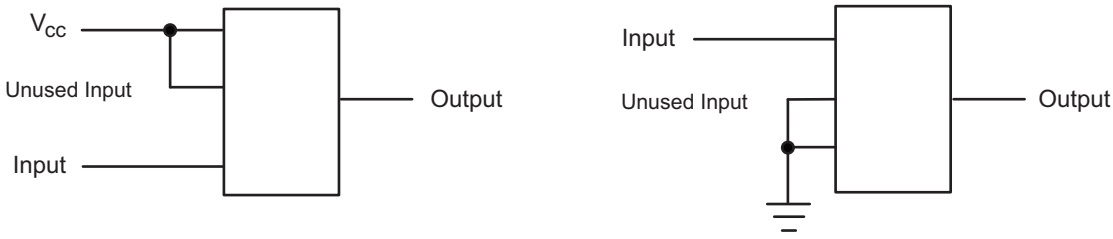


Figure 7. Layout Diagram

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LV06A	Click here	Click here	Click here	Click here	Click here
SN74LV06A	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV06AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06ADRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV06A	Samples
SN74LV06APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples
SN74LV06APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV06A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

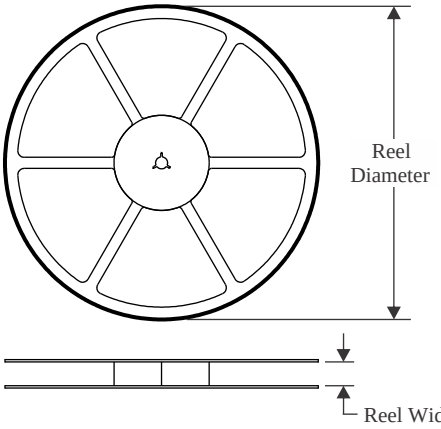
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

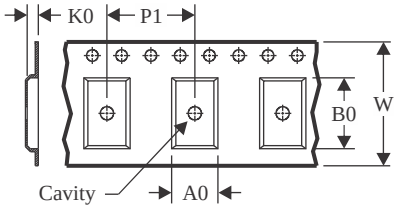
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

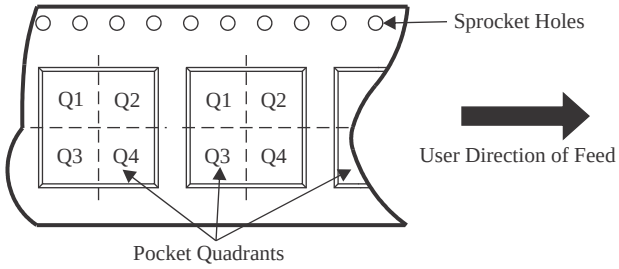


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

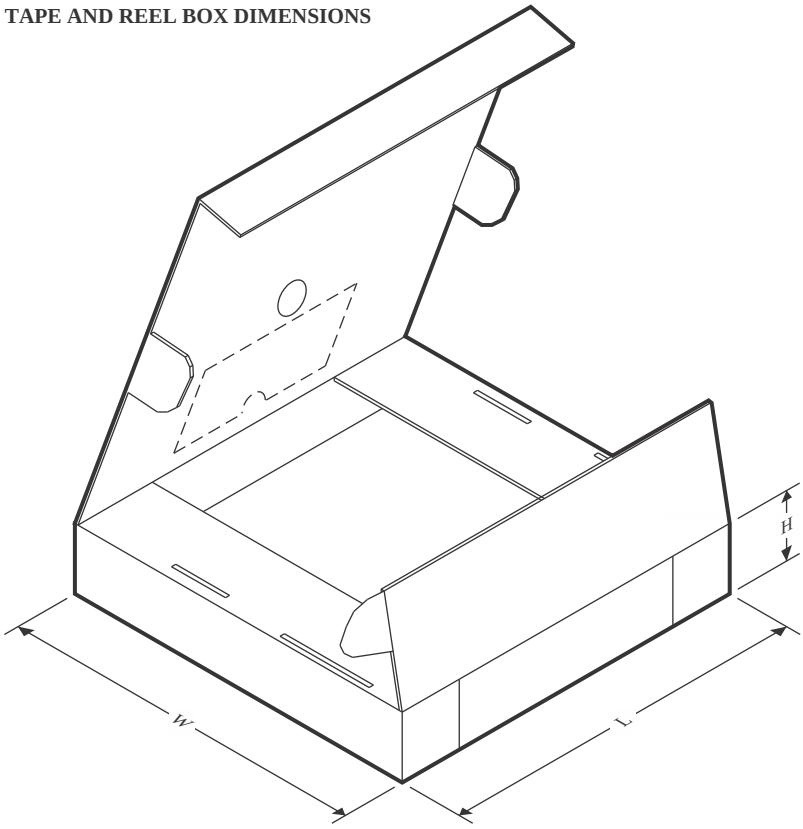
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV06ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV06ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV06ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV06ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV06APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV06APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

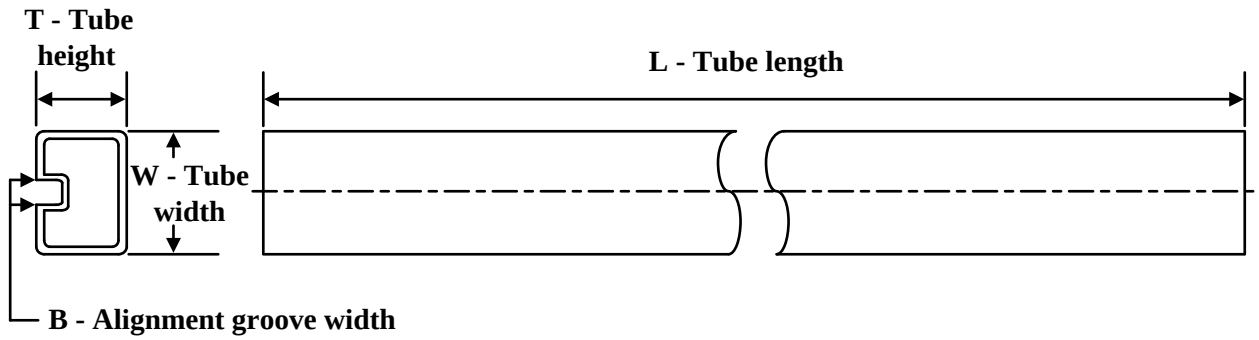
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV06ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV06ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV06ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV06ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV06APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV06APWT	TSSOP	PW	14	250	356.0	356.0	35.0

TUBE



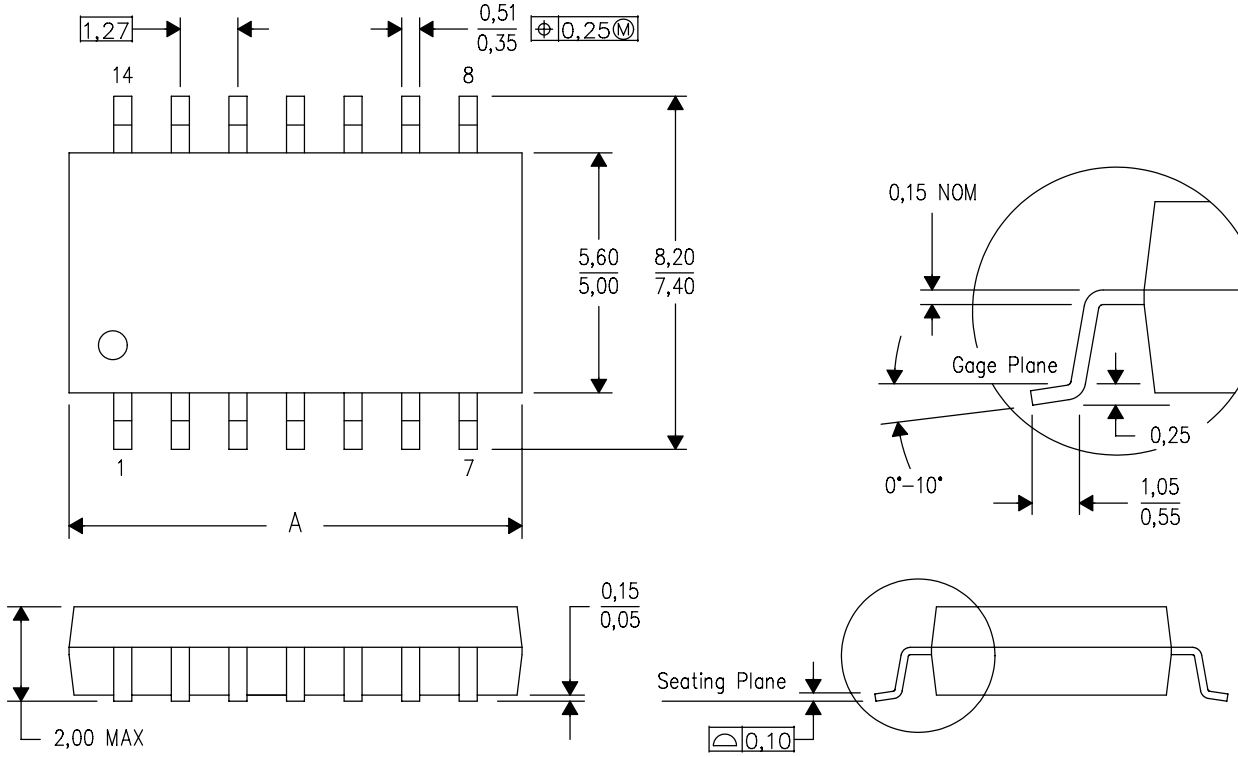
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LV06AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LV06APW	PW	TSSOP	14	90	530	10.2	3600	3.5

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



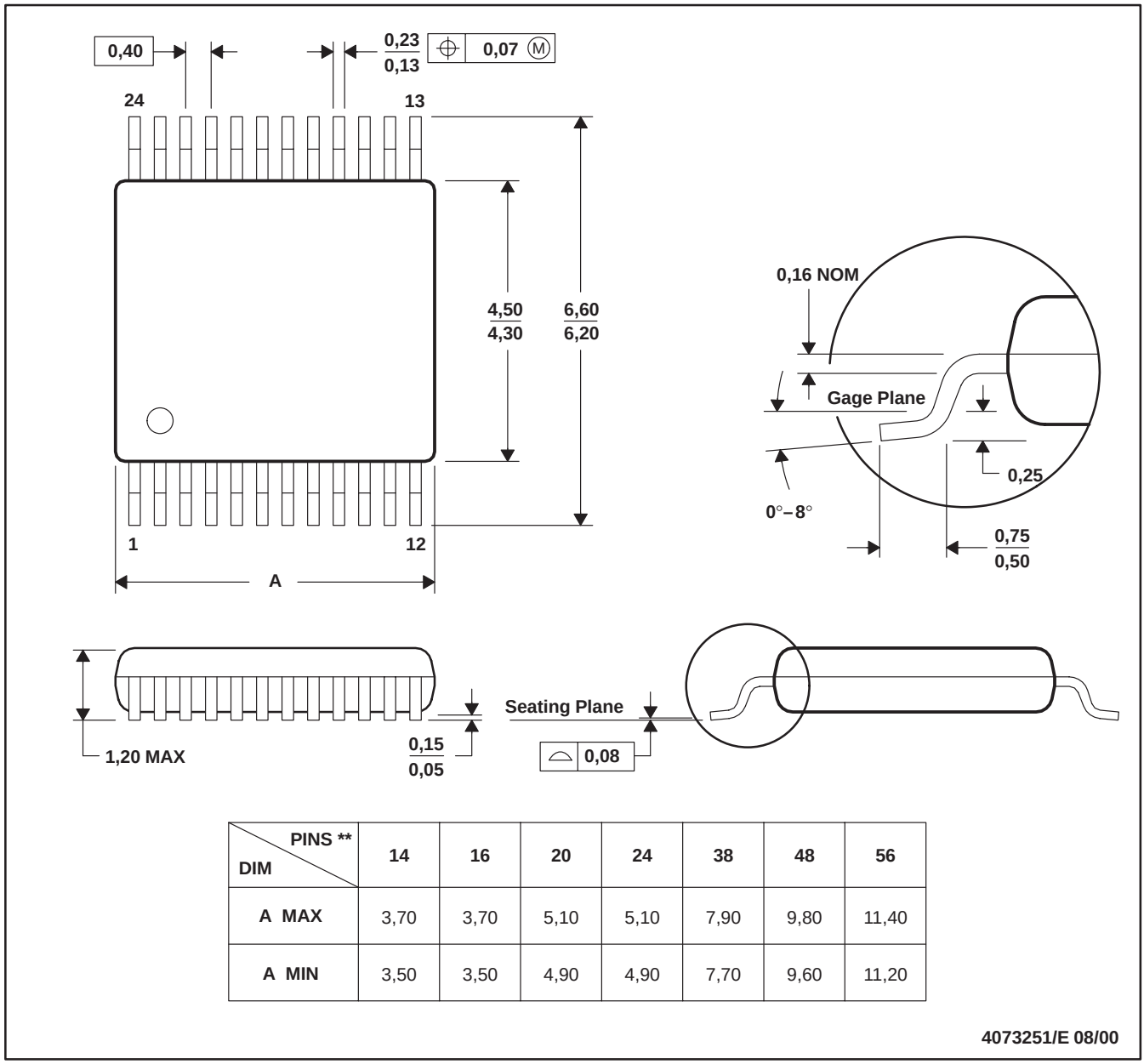
DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

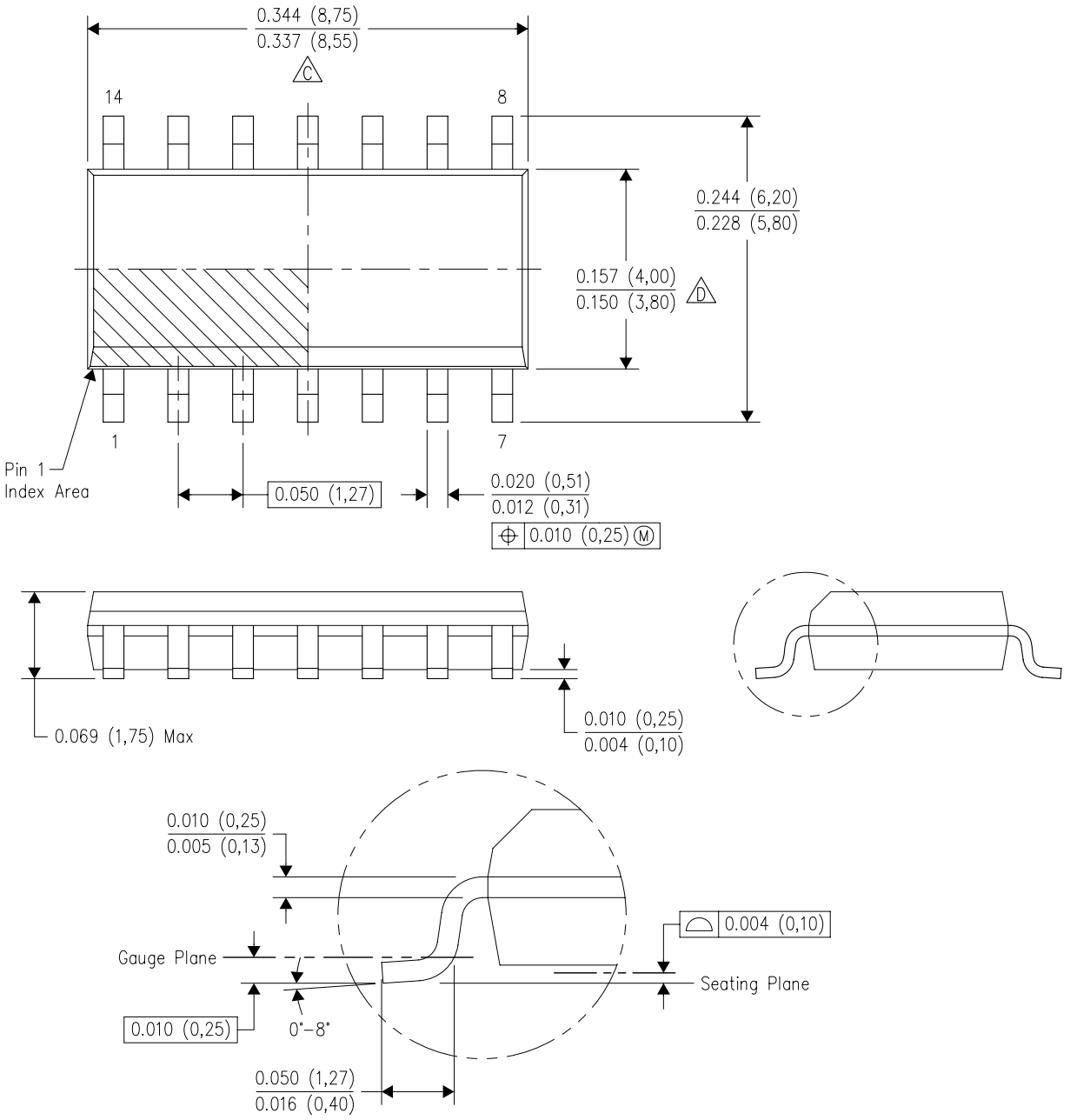


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

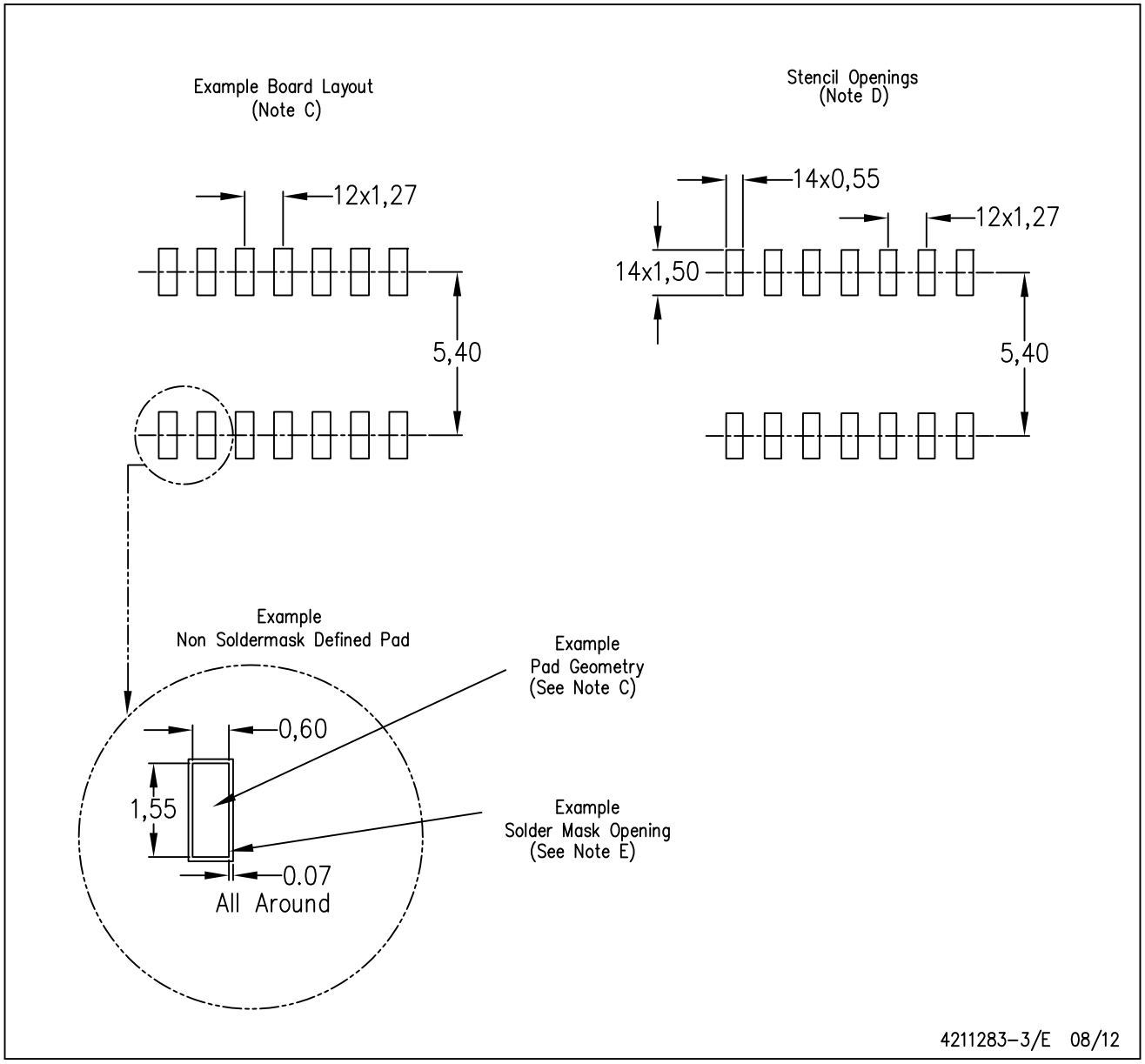
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

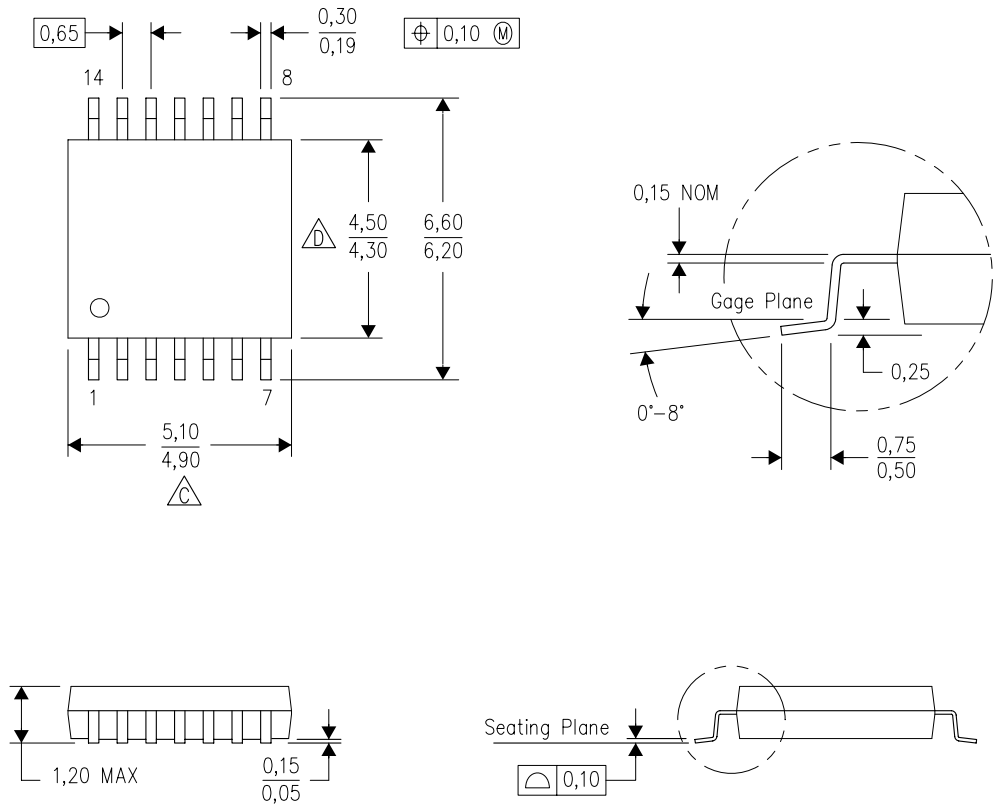
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

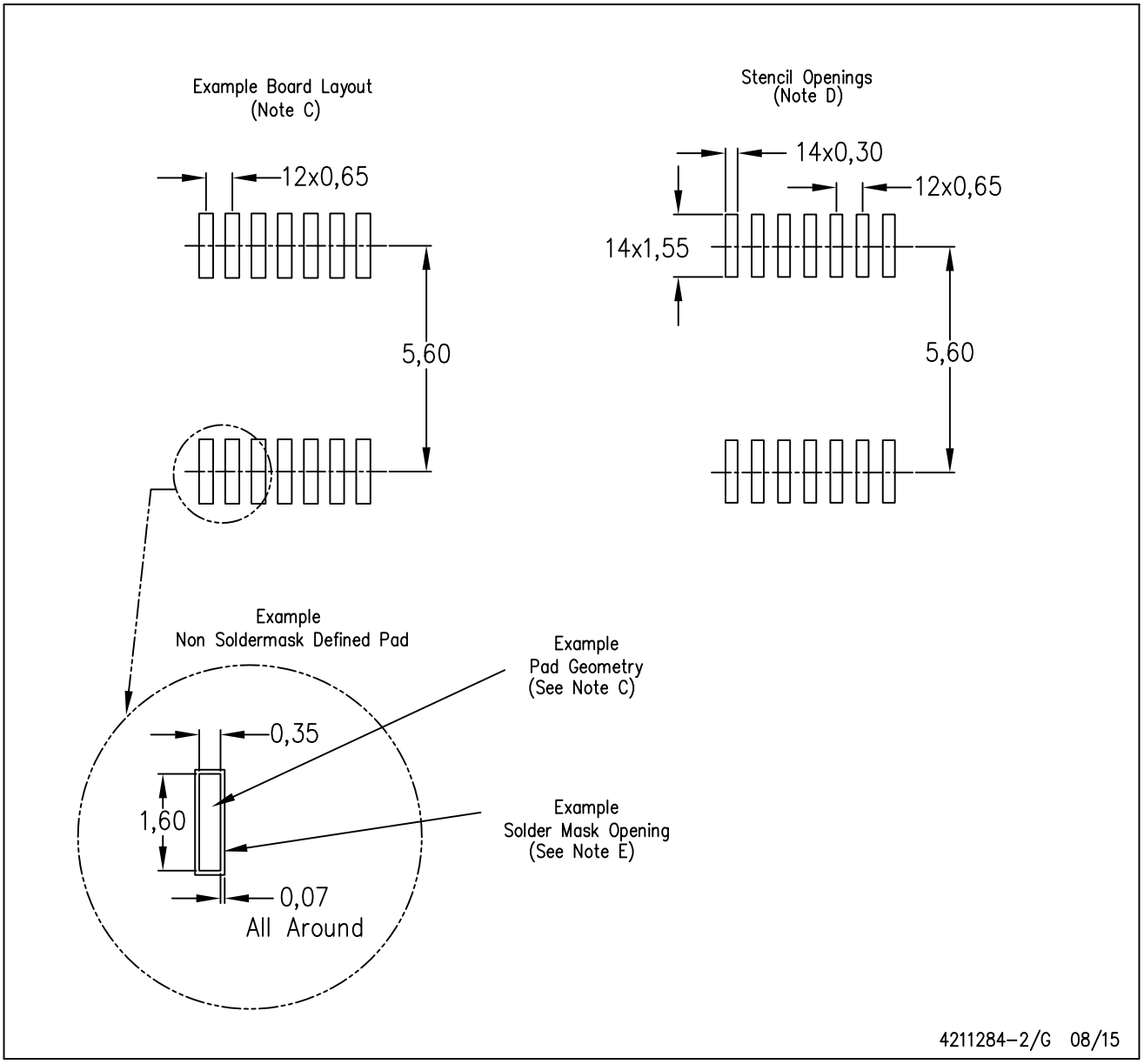
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE

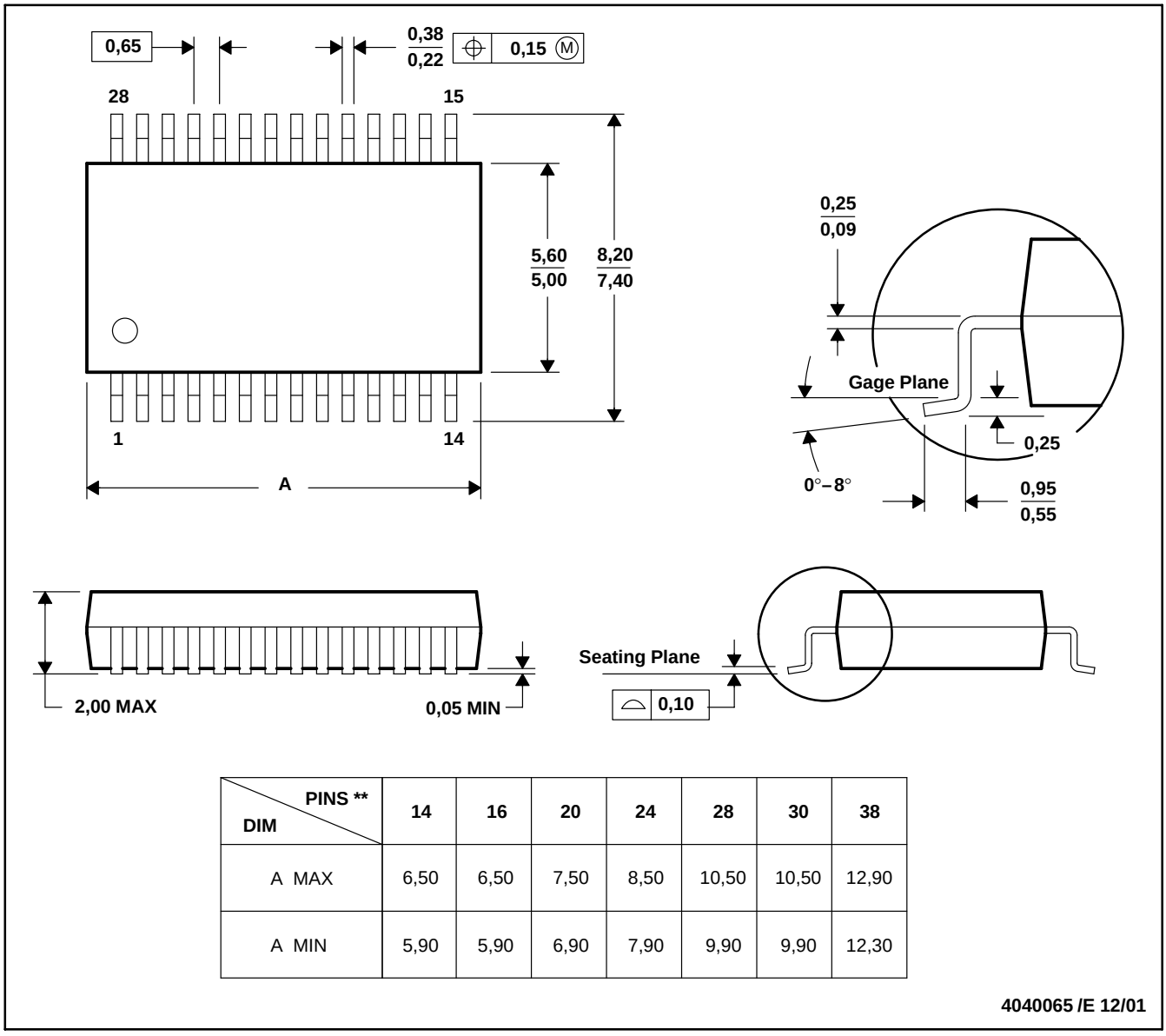


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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