LP3990-Q1 用于数字应用的 150mA 线性电压稳压器

1 特性

- 输入电压范围：2V 至 6V
- 符合 AEC-Q100 1 级标准
- 室温下电压精度为 1%
- 与陶瓷电容器搭配使用时可保持稳定
- 逻辑控制使能
- 无需噪声旁路电容
- 热过载保护和短路保护
- 输出电压范围：0.8V 至 3.3V
- 输出电流：150mA
- 输出稳定 - 1μF 电容
- 几乎零 I_Q（禁用时）：< 10nA
- 极低 I_Q（使能时）：43μA
- 低输出噪声：150μV_{RMS}
- 电源抑制比 (PSRR)：1kHz 频率时为 55dB
- 快速启动：105μs

2 应用

- 信息娱乐
- 仪表
- 车身电子装置

3 说明

LP3990-Q1 稳压器具有精确的输出电压、低噪声和低静态电流，其设计满足便携式电池供电系统的要求。LP3990-Q1 将在最高达 150mA 的负载电流条件下通过 2V 低输入电压提供 0.8V 输出。 当通过使能引脚 (EN) 上的逻辑信号切换到关断模式时，器件功耗几乎降为零。

LP3990-Q1 与节省空间的陶瓷电容器搭配使用时可保持稳定，其电容值低至 1μF。

此器件的额定运行结温范围为 –40°C 至 125°C

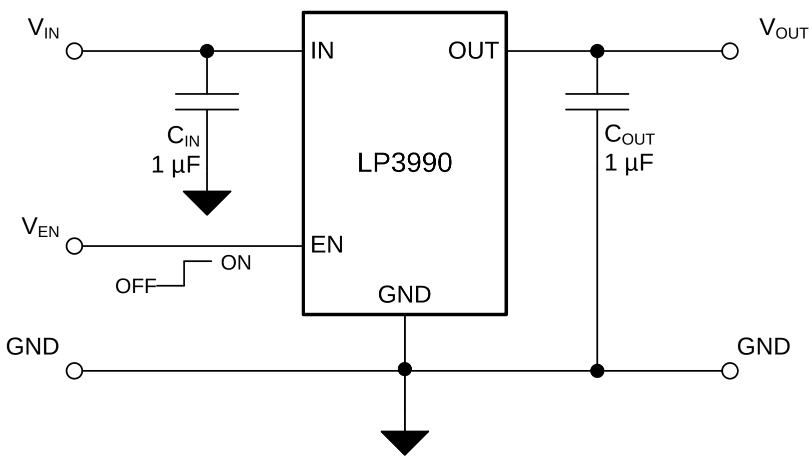
如需 0.8V、1.2V、1.35V、1.5V、1.8V、2.5V、2.8V 或 3.3V 以外的输出电压，请联系德州仪器 (TI) 销售办事处。

器件信息(1)

器件型号	封装	封装尺寸
LP3990-Q1	DSBGA (4)	1.324mm x 1.045mm（最大值）

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



目录

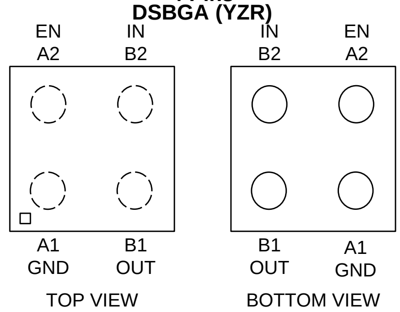
1 特性 ... 1
2 应用 ... 1
3 说明 ... 1
4 修订历史记录 ... 2
5 **Pin Configuration and Functions** ... 3
6 **Specifications** ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 Handling Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Output Capacitor, Recommended Specifications ... 5
6.7 Timing Requirements ... 6
6.8 Typical Performance Characteristics ... 6
7 **Detailed Description** ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 9
7.3 Feature Description ... 9
7.4 Device Functional Modes ... 10
8 **Application and Implementation** ... 11
8.1 Application Information ... 11
8.2 Typical Application ... 11
9 **Power Supply Recommendations** ... 14
10 **Layout** ... 14
10.1 Layout Guidelines ... 14
10.2 Layout Example ... 15
10.3 DSBGA Mounting ... 15
10.4 DSBGA Light Sensitivity ... 15
11 器件和文档支持 ... 16
11.1 文档支持 ... 16
11.2 商标 ... 16
11.3 静电放电警告 ... 16
11.4 术语表 ... 16
12 机械封装和可订购信息 ... 16

4 修订历史记录

日期	修订版本	注释
2014 年 10 月	*	最初发布。

5 Pin Configuration and Functions

4 Pins
DSBGA (YZR)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	DSBGA YZR		
GND	A1	—	Common Ground.
EN	A2	I	Enable Input; Enables the Regulator when ≥ 0.95 V. Disables the Regulator when ≤ 0.4 V. Enable Input has 1-MΩ (typical) pull-down resistor to GND.
OUT	B1	O	Voltage output. A 1-µF Low ESR Capacitor should be connected to this Pin. Connect this output to the load circuit.
IN	B2	I	Voltage supply Input. A 1-µF capacitor should be connected at this input.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Input voltage	–0.3	6.5	V
Output voltage	–0.3	See(4)	
ENABLE input voltage	–0.3	6.5	
Continuous power dissipation internally limited	See(5)		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) All voltages are with respect to the potential at the GND pin.
(4) The lower of V_{IN} + 0.3 V or 6.5 V.
(5) Internal thermal shutdown circuitry protects the device from permanent damage.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	–1500	1500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage, V_{IN}	2		6	V
Enable input voltage, V_{EN}	0.0		V_{IN}	
Junction temperature, T_J (1)	–40		125	°C

(1) $T_{J(max)} = (T_{A(max)} + (R_{\theta JA} \times P_{D(max)}))$

6.4 Thermal Information

THERMAL METRIC(1)		LP3990 YZR (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	188.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	105.3	
ψ_{JT}	Junction-to-top characterization parameter	0.7	
ψ_{JB}	Junction-to-board characterization parameter	105.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, V_{EN} = 950 mV, V_{IN} = V_{OUT} + 1 V or V_{IN} = 2 V, whichever is higher. C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT} = 0.47 µF. [1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	See[2]		2		6	V
ΔV_{OUT}	Output voltage tolerance	I_{LOAD} = 1 mA, T_J = 25°C		–1%		1%	
		Over full line and load regulation		–2.5%		2.5%	
	Line regulation error	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to 6 V		0.1	0.02	0.1	%/V
	Load regulation error	I_{OUT} = 1 mA to 150 mA	V_{OUT} = 0.8 V to 1.95 V	–0.005	0.002	0.005	%/mA
			V_{OUT} = 2 V to 3.3 V	–0.002	0.0005	0.002	
V_{DO}	Dropout voltage	I_{OUT} = 150 mA, see[3][4]			120	200	mV
I_{LOAD}	Load current	T_J = 25°, see[4][5]		0			µA
I_Q	Quiescent current	V_{EN} = 950 mV, I_{OUT} = 0 mA			43	80	µA
		V_{EN} = 950 mV, I_{OUT} = 150 mA			65	120	
		V_{EN} = 0.4 V (output disabled), T_J = 25°C			0.002	0.2	
I_{SC}	Short circuit current limit	See[6]			550	1000	mA
I_{OUT}	Maximum output current			150			
PSRR	Power Supply Rejection Ratio	f = 1 kHz, I_{OUT} = 1 mA to 150 mA			55		dB
		f = 10 kHz, I_{OUT} = 150 mA			35		
e_η	Output noise voltage[4]	BW = 10 Hz to 100 kHz	V_{OUT} = 0.8 V		60		μV_{RMS}
			V_{OUT} = 1.5 V		125		
			V_{OUT} = 3.3 V		180		
$T_{SHUTDOWN}$	Thermal shutdown junction temperature	Junction temperature (T_J) rising until the output is disabled			155		°C
		Hysteresis			15		
ENABLE CONTROL CHARACTERISTICS							
I_{EN}[7]	Maximum input current at EN pin	V_{EN} = 0 V (Output is disabled) T_J = 25°C			0.001	0.1	µA
		V_{EN} = 6 V		2.5	6	10	
V_{IL}	Low input threshold	V_{IN} = 2 V to 6 V V_{EN} falling from ≥ V_{IH} until the output is disabled				0.4	V
V_{IH}	High input threshold	V_{IN} = 2 V to 6 V V_{EN} rising from ≤ V_{IL} until the output is enabled		0.95			

(1) Minimum and Maximum limits are ensured through test, design, or statistical correlation over the operating junction temperature range (T_J) of –40°C to 125°C, unless otherwise stated. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.
(2) $V_{IN(MIN)}$ = $V_{OUT(NOM)}$ + 0.5 V, or 2 V, whichever is higher.
(3) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100 mV below its nominal value. This parameter applies only for output voltages above 2 V.
(4) This electrical specification is verified by design.
(5) The device maintains the regulated output voltage without the load.
(6) Short-circuit current is measured with V_{OUT} pulled to 0 V and V_{IN} worst case = 6 V.
(7) ENABLE Pin has 1-MΩ (typical) resistor connected to GND.

6.6 Output Capacitor, Recommended Specifications[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	Output capacitance	Capacitance[2]	0.7[3]	1	500	µF
		ESR	5			mΩ

(1) Unless otherwise specified, values and limits apply for T_J = 25°C.
(2) The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. (See *Detailed Design Procedure*.)
(3) Limit applies over the full operating junction temperature range (T_J) of −40°C to 125°C.

6.7 Timing Requirements

				MIN	NOM(1)	MAX(2)	UNIT
T_{ON}	Turnon time (3)	From V_{EN} ↑ V_{IH} to V_{OUT} 95% level ($V_{IN(MIN)}$) to 6 V)	V_{OUT} = 0.8 V		80	150	µs
			V_{OUT} = 1.5 V		105	200	
			V_{OUT} = 3.3 V		175	250	
Transient response	Line transient response (ΔV_{OUT})	T_{rise} = T_{fall} = 30 µs(3), ΔV_{IN} = 600 mV			8	16	mV (pk-pk)
	Load transient response (ΔV_{OUT})	T_{rise} = T_{fall} = 1 µs(3), I_{OUT} = 1 mA to 150 mA C_{OUT} = 1 µF			55	100	mV

(1) Nom values apply for T_J = 25°C.
(2) Maximum limits apply over the full operating junction temperature (T_J) range of −40°C to 125°C.
(3) This electrical specification is verified by design.

6.8 Typical Performance Characteristics

Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{OUT} = 0.47 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5 V; V_{EN} = V_{IN}.

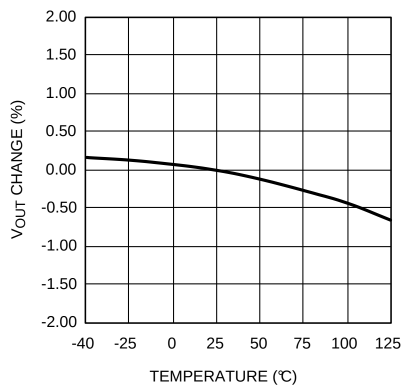


Figure 1. Output Voltage Change vs Temperature

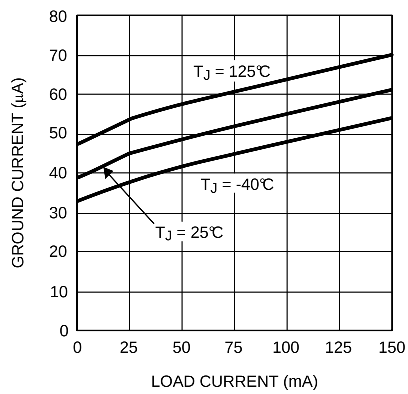
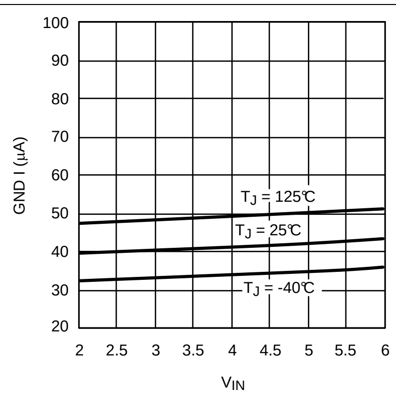
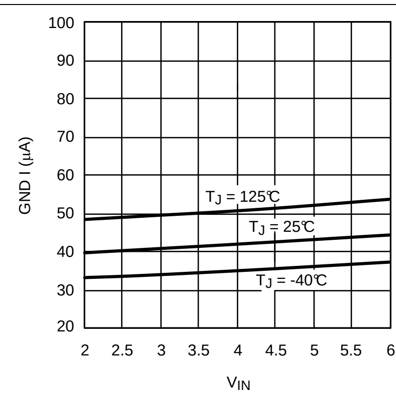


Figure 2. Ground Current vs Load Current



I_{LOAD} = 0 mA

Figure 3. Ground Current vs V_{IN}

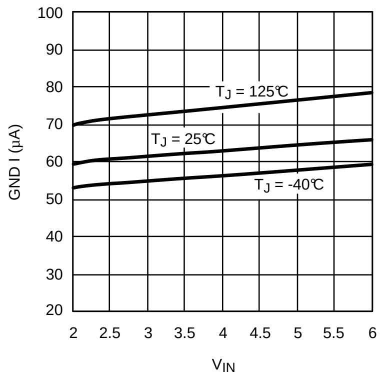


I_{LOAD} = 1 mA

Figure 4. Ground Current vs V_{IN}

Typical Performance Characteristics (continued)

Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{OUT} = 0.47 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5 V; V_{EN} = V_{IN}.



I_{LOAD} = 150 mA

Figure 5. Ground Current vs V_{IN}

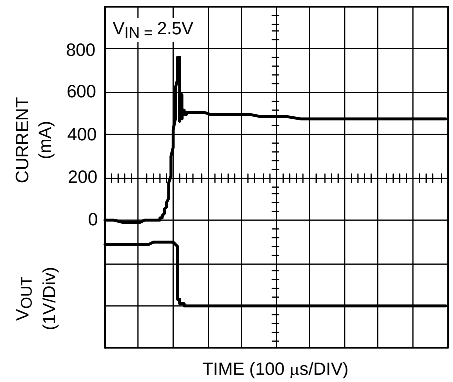


Figure 6. Short Circuit Current

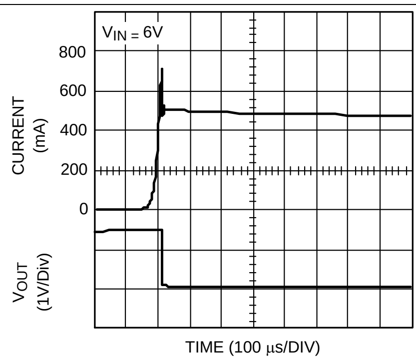


Figure 7. Short Circuit Current

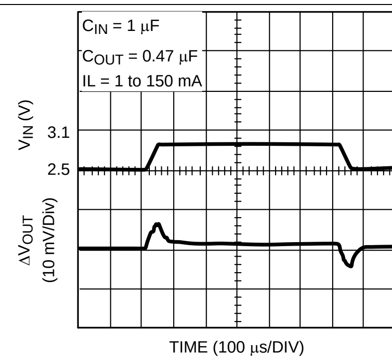


Figure 8. Line Transient

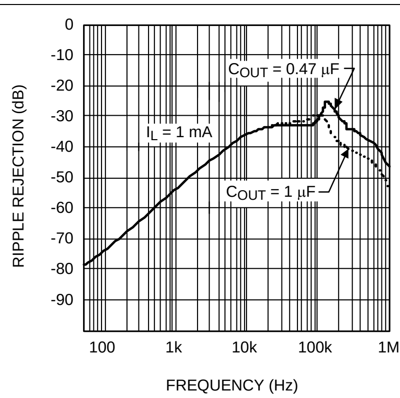


Figure 9. Power Supply Rejection Ratio

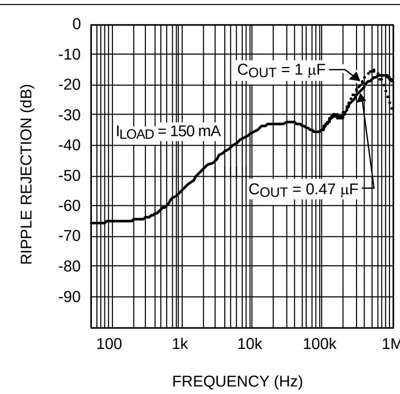


Figure 10. Power Supply Rejection Ratio

Typical Performance Characteristics (continued)

Unless otherwise specified, C_{IN} = 1 µF ceramic, C_{OUT} = 0.47 µF ceramic, V_{IN} = $V_{OUT(NOM)}$ + 1 V, T_A = 25°C, $V_{OUT(NOM)}$ = 1.5 V; V_{EN} = V_{IN}.

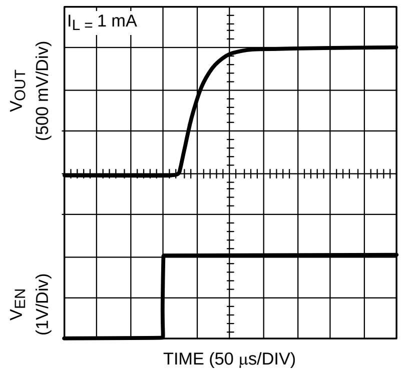


Figure 11. Enable Start-Up Time

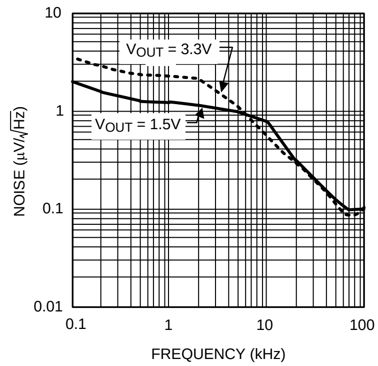


Figure 12. Noise Density

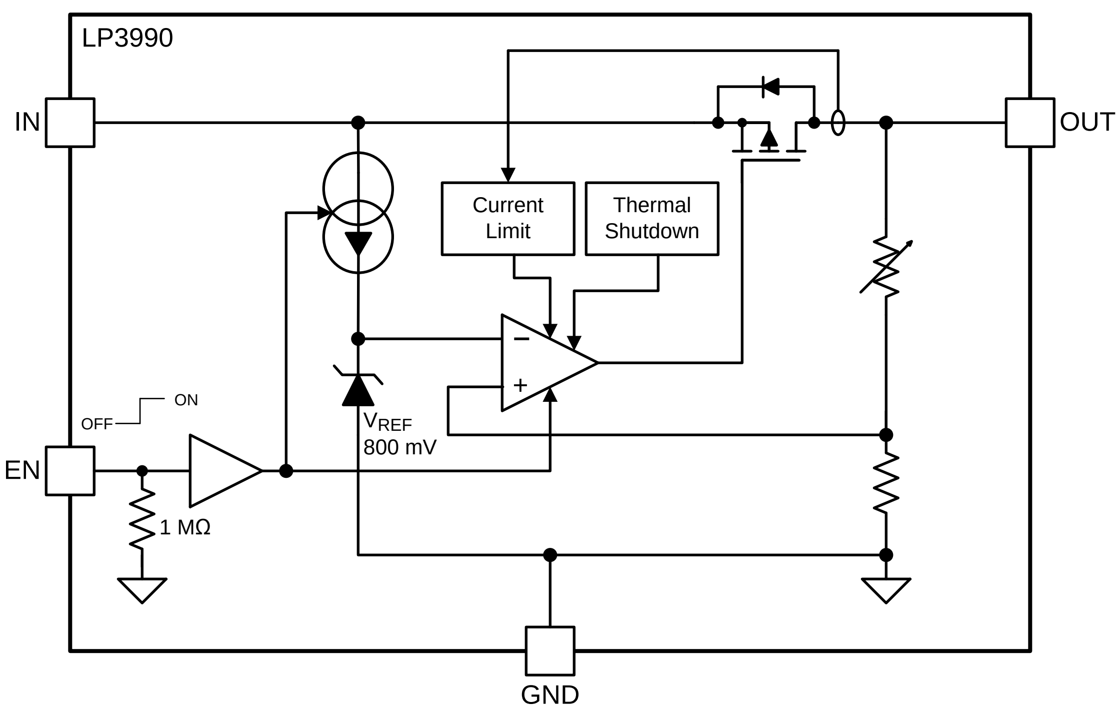
7 Detailed Description

7.1 Overview

The LP3990-Q1 is designed to meet the requirements of portable, battery-powered digital systems providing an accurate output voltage with fast start-up. When disabled via a low logic signal at the enable pin (EN), the power consumption is reduced to virtually zero.

The device is designed to perform with a single 1-μF input capacitor and a single 1-μF ceramic output capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The LP3990-Q1 Enable (EN) pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions. The EN pin voltage must be lower than the V_{IL} threshold to ensure that the device is fully disabled. If the EN pin is left open the LP3990-Q1 output will be disabled.

7.3.2 Thermal Overload Protection (T_{SD})

Thermal Shutdown disables the output when the junction temperature rises to approximately 155°C which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This thermal cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The Thermal Shutdown circuitry of the LP3990-Q1 has been designed to protect against temporary thermal overload conditions. The Thermal Shutdown circuitry was not intended to replace proper heat-sinking. Continuously running the LP3990-Q1 device into thermal shutdown may degrade device reliability.

7.4 Device Functional Modes

7.4.1 Enable (EN)

The LP3990-Q1 EN pin is internally held low by a 1-MΩ resistor to GND. The EN pin voltage must be higher than the V_{IH} threshold to ensure that the device is fully enabled under all operating conditions.

7.4.2 Minimum Operating Input Voltage (V_{IN})

The LP3990-Q1 does not include any dedicated UVLO circuitry. The LP3990-Q1 internal circuitry is not fully functional until V_{IN} is at least 2 V. The output voltage is not regulated until $V_{IN} \geq (V_{OUT} + V_{DO})$, or 2 V, whichever is higher.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP3990-Q1 is a linear voltage regulator for digital applications designed to be stable with space-saving ceramic capacitors as small as 1 µF.

8.2 Typical Application

Figure 13 shows the typical application circuit for the LP3990-Q1. The input and output capacitances may need to be increased above the 1 µF shown for some applications.

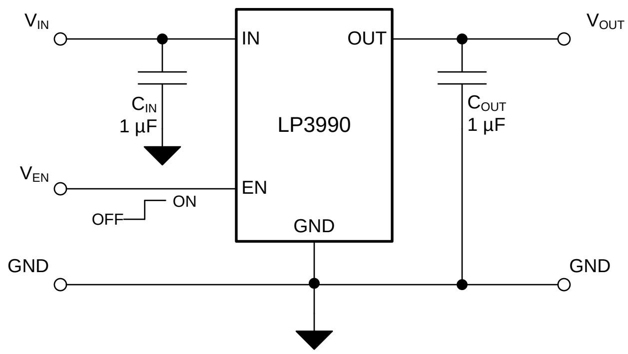


Figure 13. LP3990-Q1 Typical Application

8.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2 V to 6 V
Output voltage	1.8 V
Output current	100 mA
Output capacitor range	1 µF
Input/output capacitor ESR range	5 mΩ to 500 mΩ

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Available input voltage range
- Output voltage needed
- Output current needed
- Input and output capacitors

8.2.2.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum allowable power dissipation for the device in a given package can be calculated using Equation 1:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} - T_A) / R_{\theta JA}) \quad (1)$$

The actual power being dissipated in the device can be represented by Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

These two equations establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be derated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by Equation 3:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} - (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (3)$$

Alternately, if $T_{A\text{-}MAX}$ can not be derated, the P_D value must be reduced. This can be accomplished by reducing V_{IN} in the 'V_{IN}–V_{OUT}' term as long as the minimum V_{IN} is met, or by reducing the I_{OUT} term, or by some combination of the two.

8.2.2.2 External Capacitors

In common with most regulators, the LP3990-Q1 requires external capacitors for regulator stability. The LP3990-Q1 is specifically designed for portable applications requiring minimum board space and smallest components. These capacitors must be correctly selected for good performance.

8.2.2.3 Input Capacitor

An input capacitor is required for stability. It is recommended that a 1-µF capacitor be connected between the LP3990-Q1 IN pin and GND pin (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the IN pin and returned to a clean analogue ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB design practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long leads are used to connect the battery or other power source to the LP3990-Q1, then it is recommended that the input capacitor is increased. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1 µF over the entire operating temperature range.

8.2.2.4 Output Capacitor

The LP3990-Q1 is designed specifically to work with very small ceramic output capacitors. A 1-µF ceramic capacitor (temperature types Z5U, Y5V or X7R/X5R) with ESR between 5 mΩ to 500 mΩ, is suitable in the LP3990-Q1 application circuit.

For this device the output capacitor should be connected between the OUT pin and GND pin.

It is also possible to use tantalum or film capacitors at the device output, but these are not as attractive for reasons of size and cost (see *Capacitor Characteristics*).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

8.2.2.5 No-Load Stability

The LP3990-Q1 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

8.2.2.6 Capacitor Characteristics

The LP3990-Q1 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP3990-Q1.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 14 shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7 µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (for example, 0402) may not be suitable in the actual application.

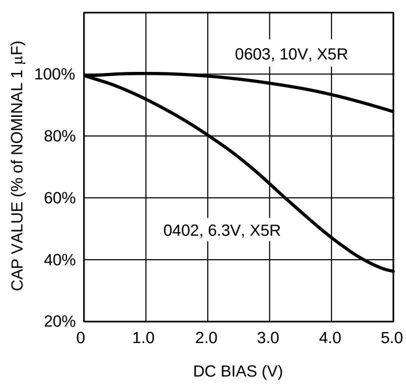


Figure 14. Typical Variation In Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of –55°C to 125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of –55°C to 85°C. Many large value ceramic capacitors, larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X7R and X5R types are recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47-µF to 4.7-µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C, so some guard band must be allowed.

8.2.2.7 Enable Control

The LP3990-Q1 features an active high Enable pin, EN, which turns the device on when pulled high. When not enabled the regulator output is off and the device typically consumes 2 nA.

If the application does not require the Enable switching feature, the EN pin should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the EN input must be able to swing above and below the specified turn-on/off voltage thresholds listed in the *Electrical Characteristics* section under V_{IL} and V_{IH}.

An internal 1-MΩ pull-down resistor ties the EN input to ground, ensuring that the device remains off if the EN pin is left open circuit.

8.2.3 Application Curves

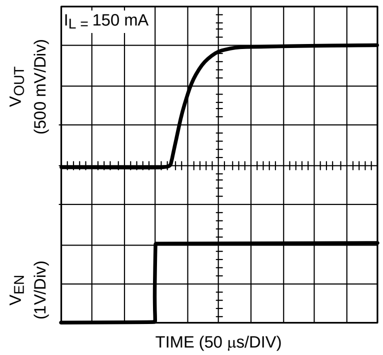


Figure 15. Enable Start-Up Time

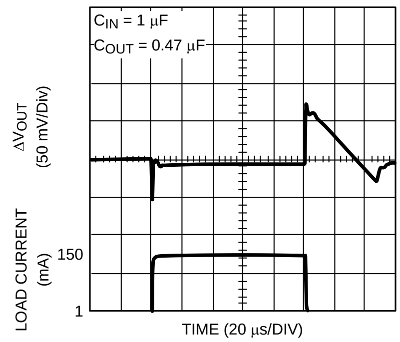


Figure 16. Load Transient

9 Power Supply Recommendations

This device is designed to operate from an input supply voltage range of 2 V to 6 V. The input supply should be well regulated and free of spurious noise. To ensure that the LP3990-Q1 output voltage is well regulated, the input supply should be at least V_{OUT} + 0.5 V, or 2 V, whichever is higher. A minimum capacitor value of 1-μF is required to be within 1 cm of the IN pin.

10 Layout

10.1 Layout Guidelines

The dynamic performance of the LP3990-Q1 is dependant on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the load regulation, PSRR, noise, or transient performance of the LP3990-Q1.

Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the LP3990-Q1, and as close as is practical to the package. The ground connections for C_{IN} and C_{OUT} should be back to the LP3990-Q1 ground pin using as wide, and as short, of a copper trace as is practical.

Connections using long trace lengths, narrow trace widths, and/or connections through vias should be avoided. These will add parasitic inductances and resistance that results in inferior performance especially during transient conditions.

A Ground Plane, either on the opposite side of a two-layer PCB, or embedded in a multi-layer PCB, is strongly recommended. This Ground Plane will provide a circuit reference plane to assure accuracy.

10.2 Layout Example

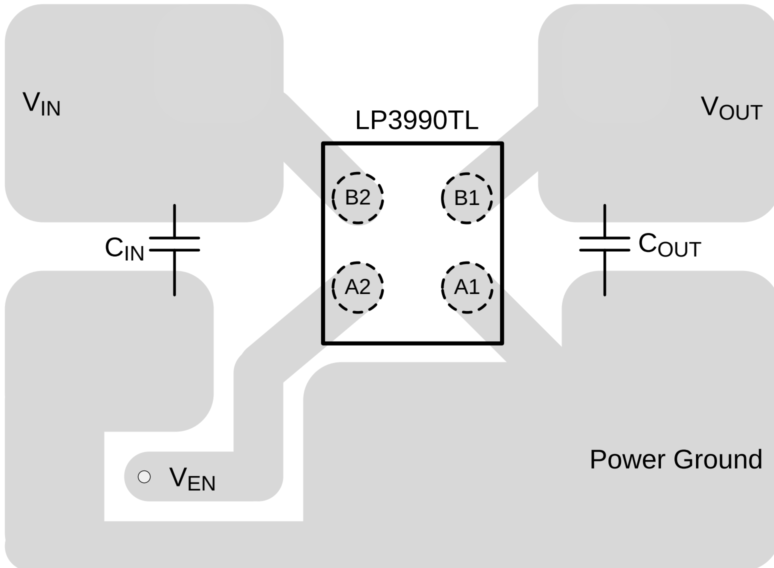


Figure 17. LP3990-Q1 DSBGA Layout

10.3 DSBGA Mounting

The DSBGA package requires specific mounting techniques, which are detailed in TI Application Note *DSBGA Wafer Level Chip Scale Package* (SNVA009).

For best results during assembly, alignment ordinals on the PC board may be used to facilitate placement of the DSBGA device.

10.4 DSBGA Light Sensitivity

Exposing the DSBGA device to direct light may affect the operation of the device. Light sources, such as halogen lamps, can affect electrical performance, if placed in close proximity to the device.

Light with wavelengths in the infra-red portion of the spectrum is the most detrimental, and so, fluorescent lighting used inside most buildings, has little or no effect on performance.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

相关文档如下：

- TI 应用手册《*DSBGA 晶圆级芯片规模封装*》（文献编号：SNVA009）。

11.2 商标

All trademarks are the property of their respective owners.

11.3 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

重要声明

德州仪器(TI) 及其下属子公司有权根据 JESD46 最新标准, 对所提供的产品和服务进行更正、修改、增强、改进或其它更改， 并有权根据 JESD48 最新标准中止提供任何产品和服务。客户在下订单前应获取最新的相关信息, 并验证这些信息是否完整且是最新的。所有产品的销售都遵循在订单确认时所提供的TI 销售条款与条件。

TI 保证其所销售的组件的性能符合产品销售时 TI 半导体产品销售条件与条款的适用规范。仅在 TI 保证的范围内，且 TI 认为 有必要时才会使用测试或其它质量控制技术。除非适用法律做出了硬性规定，否则没有必要对每种组件的所有参数进行测试。

TI 对应用帮助或客户产品设计不承担任何义务。客户应对其使用 TI 组件的产品和应用自行负责。为尽量减小与客户产品和应 用相关的风险，客户应提供充分的设计与操作安全措施。

TI 不对任何 TI 专利权、版权、屏蔽作品权或其它与使用了 TI 组件或服务的组合设备、机器或流程相关的 TI 知识产权中授予 的直接或隐含权限作出任何保证或解释。TI 所发布的与第三方产品或服务有关的信息，不能构成从 TI 获得使用这些产品或服 务的许可、授权、或认可。使用此类信息可能需要获得第三方的专利权或其它知识产权方面的许可，或是 TI 的专利权或其它 知识产权方面的许可。

对于 TI 的产品手册或数据表中 TI 信息的重要部分，仅在没有对内容进行任何篡改且带有相关授权、条件、限制和声明的情况 下才允许进行复制。TI 对此类篡改过的文件不承担任何责任或义务。复制第三方的信息可能需要服从额外的限制条件。

在转售 TI 组件或服务时，如果对该组件或服务参数的陈述与 TI 标明的参数相比存在差异或虚假成分，则会失去相关 TI 组件 或服务的所有明示或暗示授权，且这是不正当的、欺诈性商业行为。TI 对任何此类虚假陈述均不承担任何责任或义务。

客户认可并同意，尽管任何应用相关信息或支持仍可能由 TI 提供，但他们将独力负责满足与其产品及在其应用中使用 TI 产品 相关的所有法律、法规和安全相关要求。客户声明并同意，他们具备制定与实施安全措施所需的全部专业技术和知识，可预见 故障的危险后果、监测故障及其后果、降低有可能造成人身伤害的故障的发生机率并采取适当的补救措施。客户将全额赔偿因 在此类安全关键应用中使用任何 TI 组件而对 TI 及其代理造成的任何损失。

在某些场合中，为了推进安全相关应用有可能对 TI 组件进行特别的促销。TI 的目标是利用此类组件帮助客户设计和创立其特 有的可满足适用的功能安全性标准和要求的终端产品解决方案。尽管如此，此类组件仍然服从这些条款。

TI 组件未获得用于 FDA Class III（或类似的生命攸关医疗设备）的授权许可，除非各方授权官员已经达成了专门管控此类使 用的特别协议。

只有那些 TI 特别注明属于军用等级或“增强型塑料”的 TI 组件才是设计或专门用于军事/航空应用或环境的。购买者认可并同 意，对并非指定面向军事或航空航天用途的 TI 组件进行军事或航空航天方面的应用，其风险由客户单独承担，并且由客户独 力负责满足与此类使用相关的所有法律和法规要求。

TI 已明确指定符合 ISO/TS16949 要求的产品，这些产品主要用于汽车。在任何情况下，因使用非指定产品而无法达到 ISO/TS16949 要求，TI不承担任何责任。

	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
放大器和线性器件	www.ti.com.cn/amplifiers	计算机及周边	www.ti.com.cn/computer
数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
时钟和计时器	www.ti.com.cn/clockandtimers	医疗电子	www.ti.com.cn/medical
接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
逻辑	www.ti.com.cn/logic	汽车电子	www.ti.com.cn/automotive
电源管理	www.ti.com.cn/power	视频和影像	www.ti.com.cn/video
微控制器 (MCU)	www.ti.com.cn/microcontrollers		
RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
无线连通性	www.ti.com.cn/wirelessconnectivity	德州仪器在线技术支持社区	www.deyisupport.com

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3990QTLX-1.2Q1	ACTIVE	DSBGA	YZR	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990QTLX-1.8Q1	ACTIVE	DSBGA	YZR	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples
LP3990QTLX-2.8Q1	ACTIVE	DSBGA	YZR	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

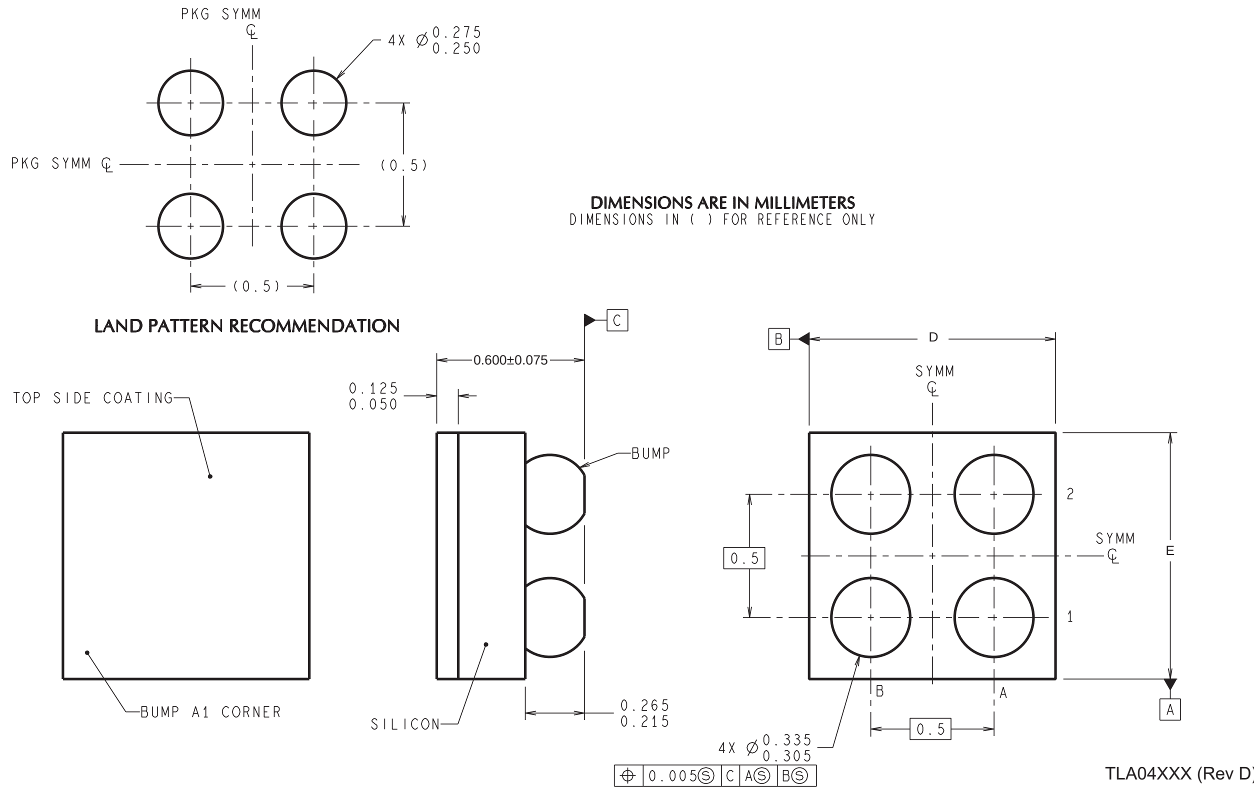
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



D: Max = 1.324 mm, Min =1.263 mm

E: Max = 1.045 mm, Min =0.984 mm

4215042/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

重要声明和免责声明

TI 均以"原样"提供技术性及可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (http://www.ti.com.cn/zh-cn/legal/termsofsale.html) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122