

CSD19531KCS 100V N 通道 NexFET™ 功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

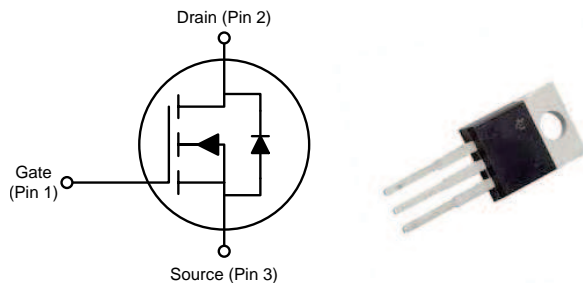
- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩额定值
- 无铅引脚镀层
- 符合 RoHS 环保标准
- 无卤素
- 晶体管 (TO)-220 塑料封装

2 应用范围

- 次级侧同步整流器
- 热插拔电信应用
- 电机控制

3 说明

此 100V、6.4mΩ、TO-220 NexFET™ 功率 MOSFET 被设计成在功率转换应用中大大降低 损耗。



产品概要

$T_A=25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	100		V
Q_g	栅极电荷总量 (10V)	37		nC
Q_{gd}	栅极电荷 (栅极到漏极)	7.5		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 6\text{V}$	7.3	mΩ
		$V_{GS} = 10\text{V}$	6.4	
$V_{GS(th)}$	阈值电压	2.7		V

器件信息(1)

器件	封装	包装介质	数量	运输
CSD19531KCS	TO-220 塑料封装	管	50	管

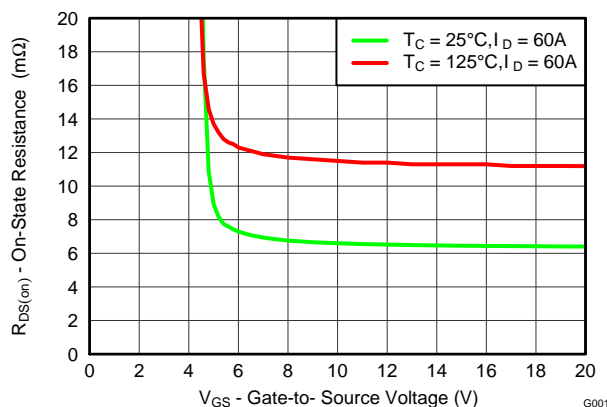
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

绝对最大额定值

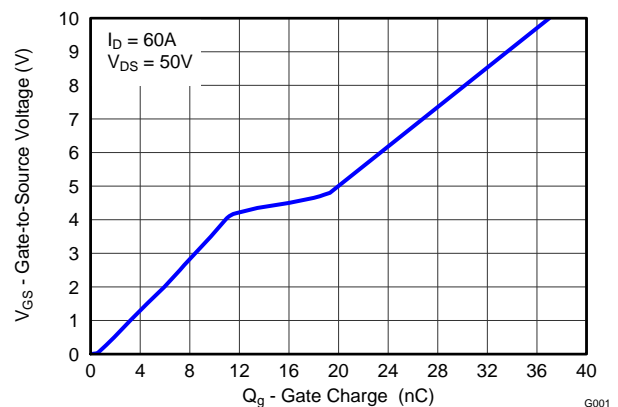
$T_A=25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	100	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	100	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	110	
	持续漏极电流 (受芯片限制), $T_C = 100^\circ\text{C}$ 时测得	78	
I_{DM}	脉冲漏极电流(1)	285	A
P_D	功率耗散	214	W
T_J, T_{stg}	工作结温, 储存温度	-55 至 175	$^\circ\text{C}$
E_{AS}	雪崩能量, 单一脉冲 $I_D = 60\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	180	mJ

(1) 最大 $R_{\theta JC} = 0.7^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$ 。

$R_{DS(on)}$ 与 V_{GS} 间的关系



栅极电荷



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4 修订历史记录

Changes from Revision B (June 2014) to Revision C	Page
• 已添加 接收文档更新通知部分和社区资源部分至器件和文档支持部分	7
• 已更改 KCS 封装尺寸部分中的封装图	8

Changes from Revision A (May 2014) to Revision B	Page
• Added value for max Q_g	3

Changes from Original (September 2013) to Revision A	Page
• 已将芯片限制电流更新为反映器件运行温度范围内的增加量	1
• 已增加脉冲电流来反映全新条件	1
• 已增加最大功率耗散来反映全新条件	1
• 已将运行温度范围和结温范围增加至 175°C	1
• 更新了脉冲漏极电流条件	1
• Changed Figure 1 from a normalized $R_{\theta JA}$ curve to a normalized $R_{\theta JC}$ curve	4
• Updated Figure 6 to reflect increase in device operating temperature range	5
• Updated Figure 8 to reflect increase in device operating temperature range	5
• Updated Figure 10 to reflect measured SOA data	6
• Updated Figure 12 to reflect increase in device operating temperature range	6

5 Specifications

5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$			1	μA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.2	2.7	3.3	V
$R_{DS(on)}$	Drain-to-source on resistance	$V_{GS} = 6\text{ V}, I_D = 60\text{ A}$		7.3	8.8	m Ω
		$V_{GS} = 10\text{ V}, I_D = 60\text{ A}$		6.4	7.7	
g_{fs}	Transconductance	$V_{DS} = 10\text{ V}, I_D = 60\text{ A}$		137		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}, f = 1\text{ MHz}$		2980	3870	pF
C_{oss}	Output capacitance			560	728	pF
C_{rss}	Reverse transfer capacitance			13	17	pF
R_G	Series gate resistance			1.3	2.6	Ω
Q_g	Gate charge total (10 V)	$V_{DS} = 50\text{ V}, I_D = 60\text{ A}$		38	49	nC
Q_{gd}	Gate charge gate-to-drain			7.5		nC
Q_{gs}	Gate charge gate-to-source			11.9		nC
$Q_{g(th)}$	Gate charge at V_{th}			7.3		nC
Q_{oss}	Output charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		98		nC
$t_{d(on)}$	Turnon delay time	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V},$ $I_{DS} = 60\text{ A}, R_G = 0\ \Omega$		8.4		ns
t_r	Rise Time			7.2		ns
$t_{d(off)}$	Turnoff delay time			16		ns
t_f	Fall time			4.1		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 60\text{ A}, V_{GS} = 0\text{ V}$		0.9	1	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 50\text{ V}, I_F = 60\text{ A},$ $di/dt = 300\text{ A}/\mu\text{s}$		270		nC
t_{rr}	Reverse recovery time			83		ns

5.2 Thermal Information

 $T_A = 25^\circ\text{C}$ (unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance			0.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C}/\text{W}$

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

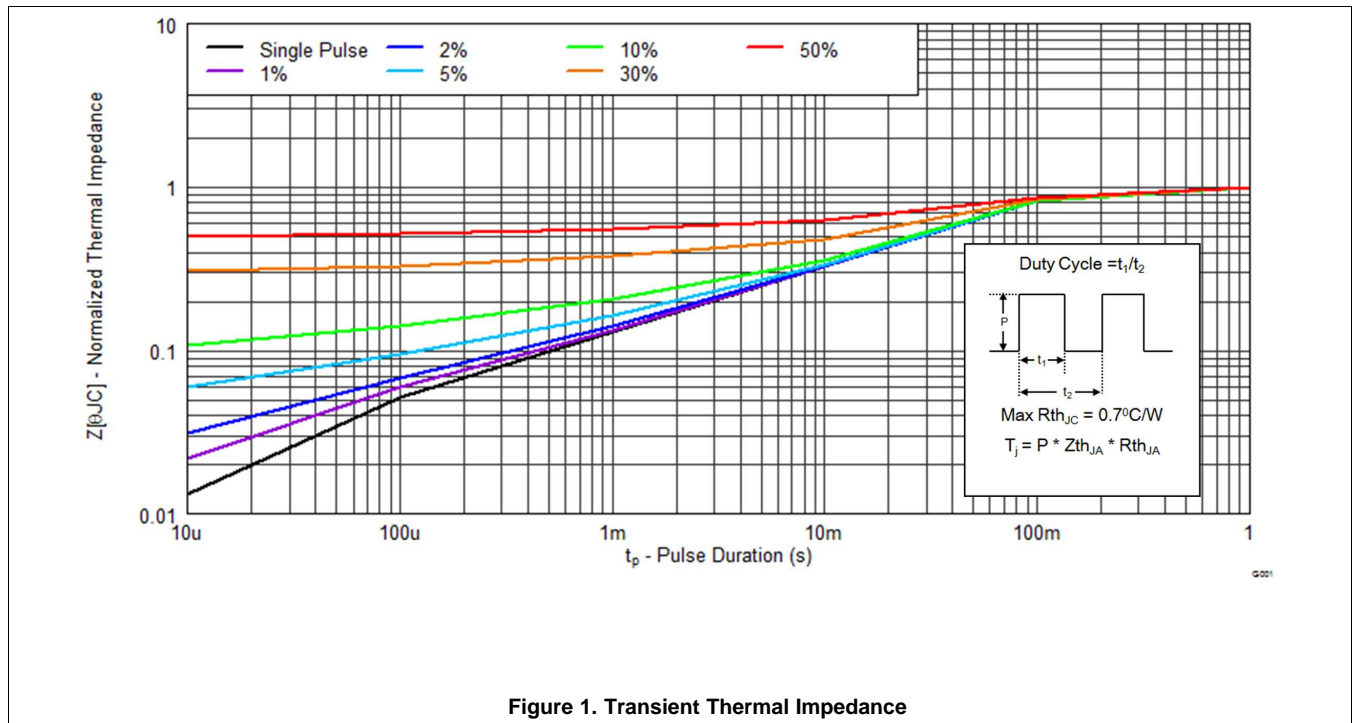


Figure 1. Transient Thermal Impedance

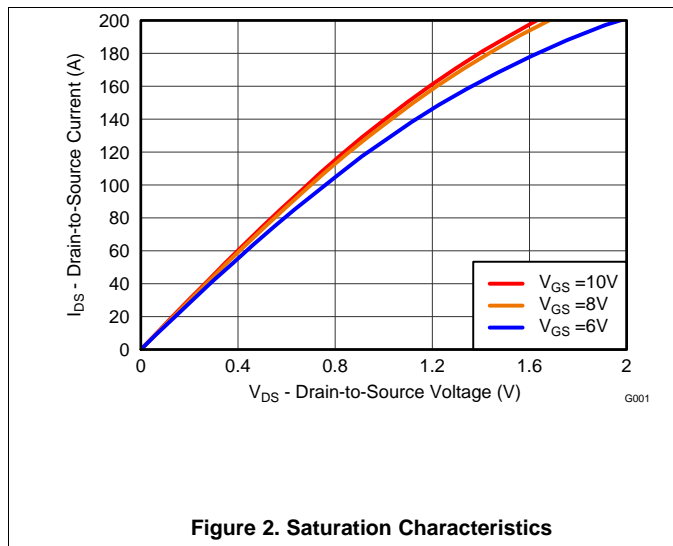


Figure 2. Saturation Characteristics

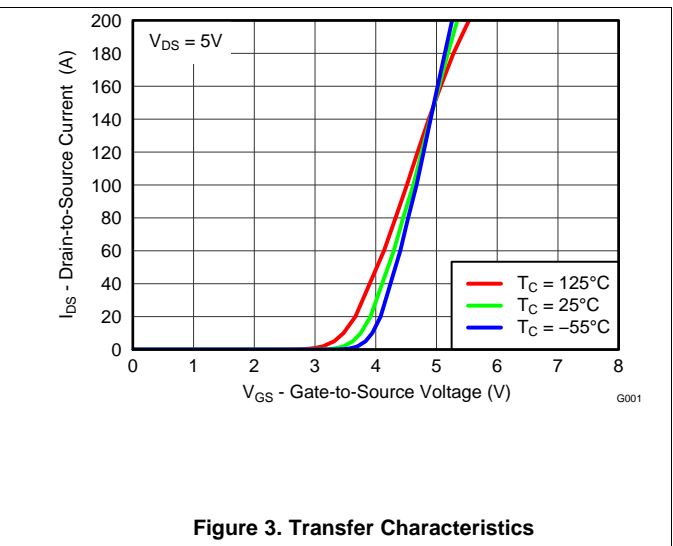


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)

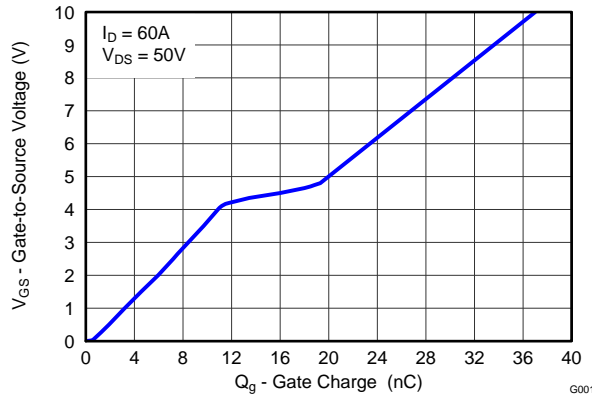


Figure 4. Gate Charge

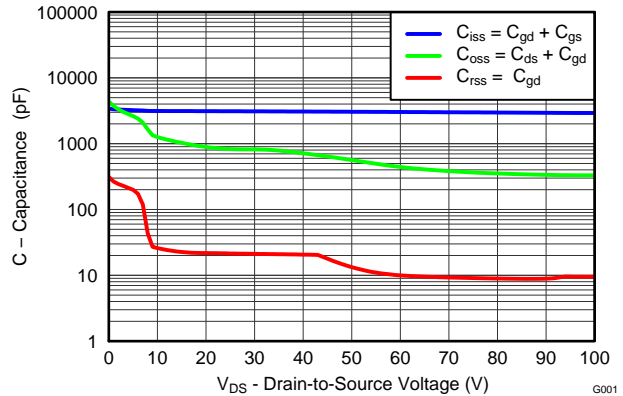


Figure 5. Capacitance

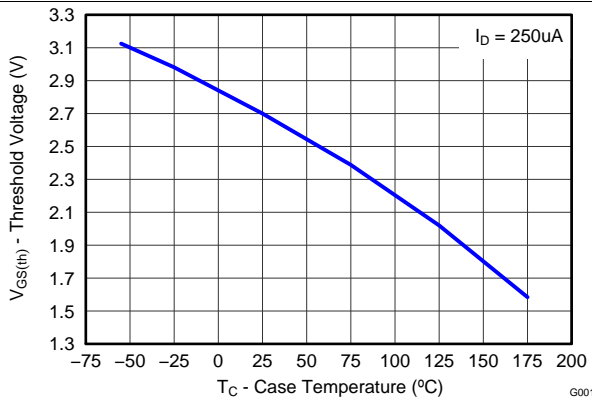


Figure 6. Threshold Voltage vs Temperature

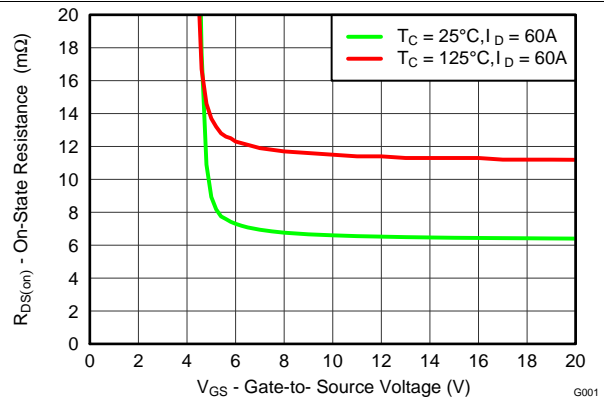


Figure 7. On-State Resistance vs Gate-to-Source Voltage

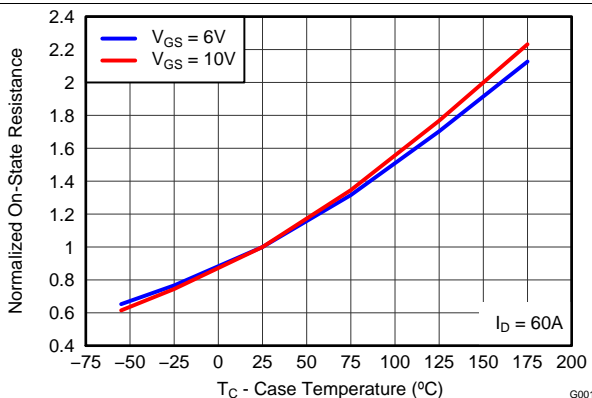


Figure 8. Normalized On-State Resistance vs Temperature

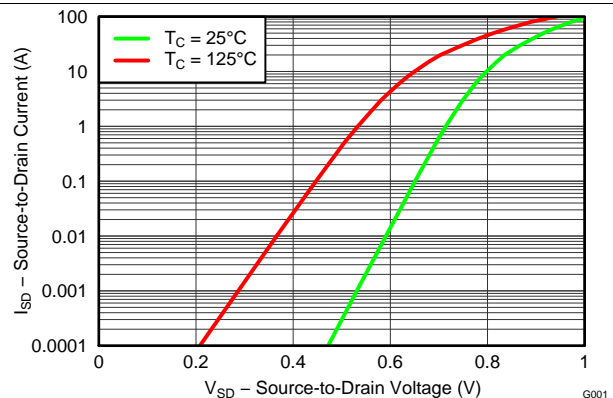
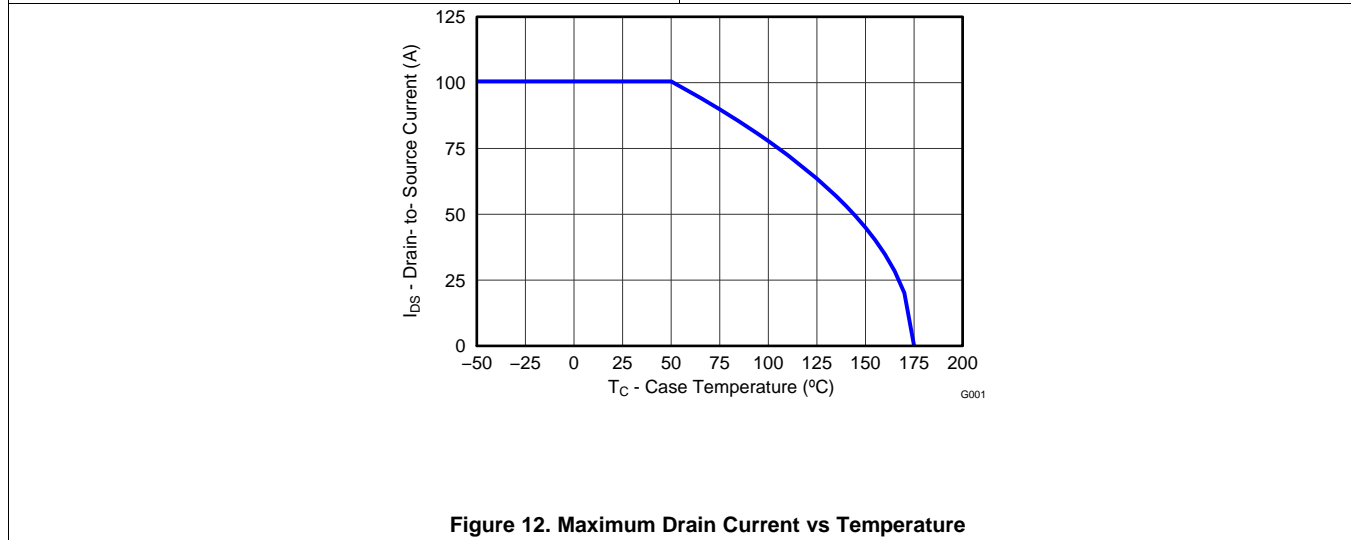
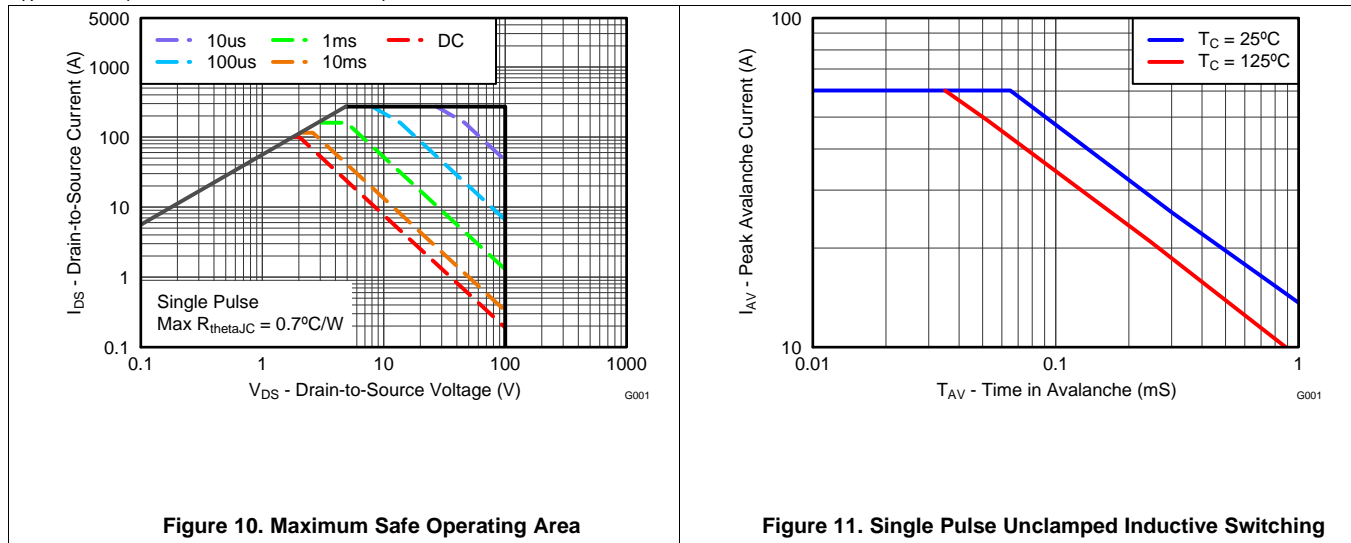


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



6 器件和文档支持

6.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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6.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

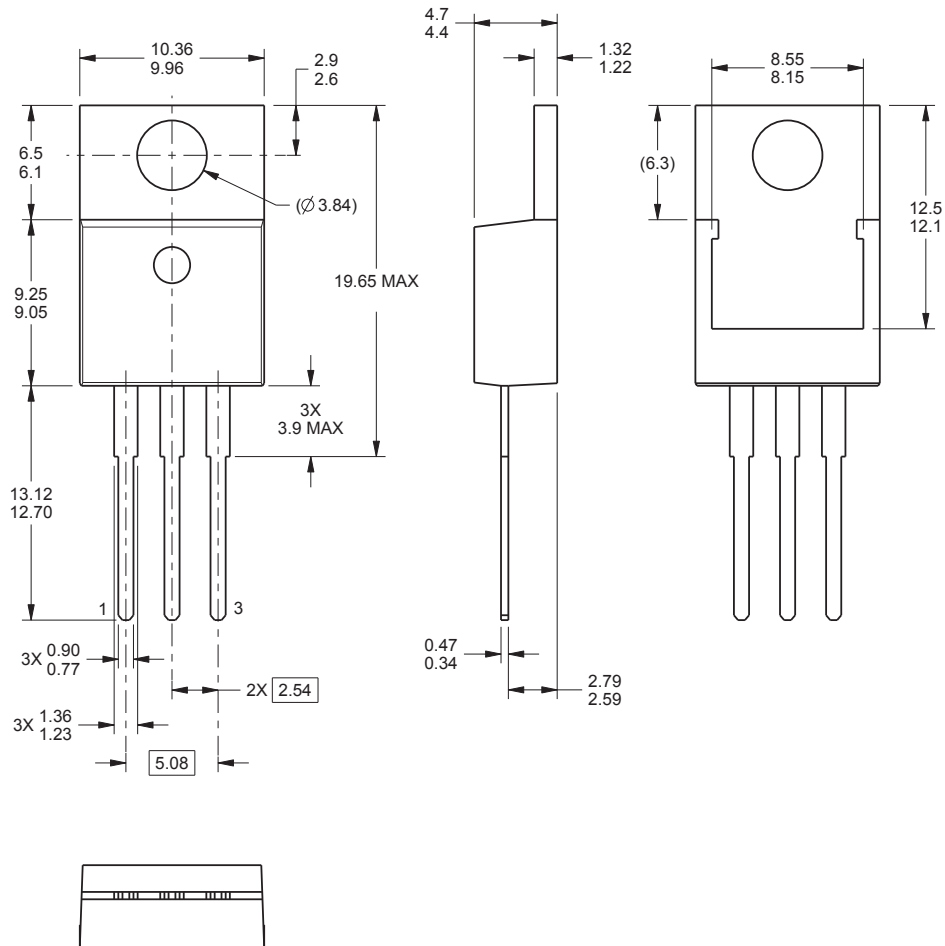
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧的导航栏。

7.1 KCS 封装尺寸



4222214/A 10/2015

注释:

1. 所有控制线性尺寸的单位均为英寸。括号中的尺寸单位均为毫米。括号或括弧中的尺寸均仅供参考。尺寸和容限值遵循 ASME Y14.5M。
2. 本图纸如有变更，恕不通知。
3. 参考 JEDEC 注册 TO-220。

表 1. 引脚配置

位置	名称
引脚 1	栅极
引脚 2 / 标签	漏极
引脚 3	源极

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19531KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Green	SN	N / A for Pkg Type	-55 to 175	CSD19531KCS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=100ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CSD19531KCS	KCS	TO-220	3	50	532	34.1	700	9.6
CSD19531KCS	KCS	TO-220	3	50	532	34.1	700	9.6

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