

# 具有 20V/24V 过压保护功能的 TS5USBC41 双路 2:1 USB 2.0 多路复用器 / 多路信号分离器或单端交叉开关

## 1 特性

- 电源电压范围为 2.3V 至 5.5V
- 差动 2:1 或 1:2 开关/多路复用器或灵活的双路单端交叉开关
- 在公共引脚上提供 0V 至 20V (TS5USBC410) 和 24V (TS5USBC412) 过压保护 (OVP) 功能
- $V_{CC} = 0V$  时具有断电保护
- 较低的  $R_{ON}$  (最大值为 9 $\Omega$ )
- 典型带宽为 1.1GHz (TS5USBC410) 和 1.2GHz (TS5USBC412)
- $C_{ON}$  典型值为 2.7pF (TS5USBC410) 和 2.5pF (TS5USBC412)
- 低功耗禁用模式
- 1.8V 兼容型逻辑输入
- ESD 保护性能超出 JESD 22 标准
  - 2000V 人体放电模型 (HBM)
- TS5USBC410 和 TS5USBC412: 0°C 至 70°C 的标准温度范围
- TS5USBC410I 和 TS5USBC412I: -40°C 至 85°C 的工业温度范围
- 小型 DSBGA 封装

## 2 应用

- 移动设备
- 台式机/笔记本电脑
- 平板电脑
- 使用 USB Type-C™ 或 Micro-B 连接器的任何场合

## 3 说明

TS5USBC41 是一款双向低功耗双端口高速 USB 2.0 模拟开关，具有针对 USB Type-C™ 系统的集成保护功能。该器件可配置为一个 2:1 或 1:2 开关。该器件经过优化，可用于 USB Type-C™ 系统中的 USB 2.0 D+/- 线路。

I/O 引脚上的 TS5USBC41 保护功能可承受最高 20V (TS5USBC410) 或 24V (TS5USBC412) 的电压，且会通过自动关闭电路来保护该开关后面的系统组件。

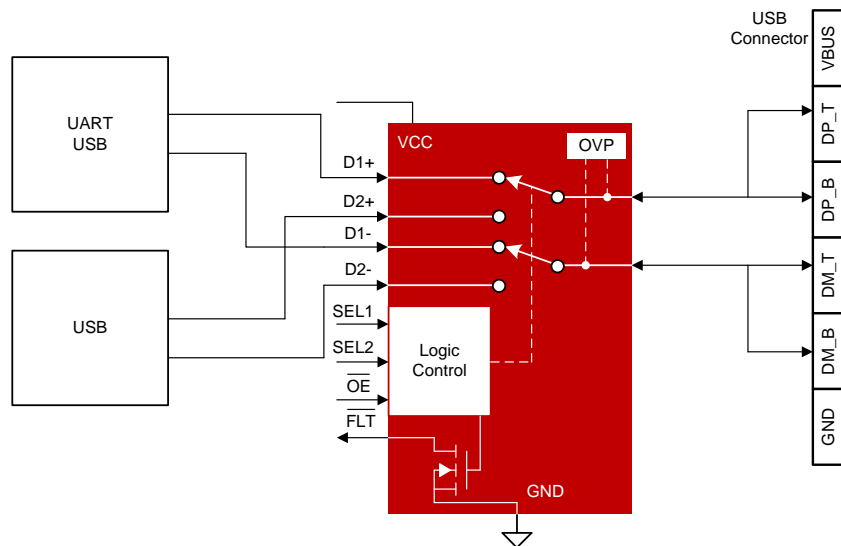
TS5USBC41 采用小型 12 引脚 DSBGA 封装，使其成为移动应用和空间受限型应用。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TS5USBC410 TS5USBC410I TS5USBC412 TS5USBC412I	DSBGA (12)	1.638mm × 1.238mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



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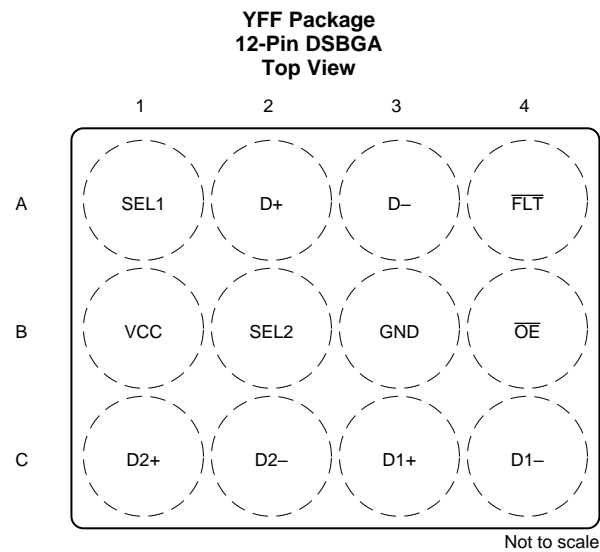
## 4 修订历史记录

### Changes from Revision A (May 2018) to Revision B

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| • 更改了器件状态：将预告信息 更改成了生产数据 ..... | <b>1</b> |
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## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	SEL1	I	Switch select1. Refer to <a href="#">表 1</a> .
A2	D+	I/O	Data switch input (Differential +).
A3	D-	I/O	Data switch input (Differential -)
A4	$\overline{\text{FLT}}$	O	Fault indicator output pin (Active low) - open drain
B1	VCC	PWR	Supply Voltage
B2	SEL2	I	Switch select2. Refer to <a href="#">表 1</a> .
B3	GND	GND	Ground
B4	$\overline{\text{OE}}$	I	Output enable (Active low). Refer to <a href="#">表 1</a> .
C1	D2+	I/O	Data switch output 2 (Differential +)
C2	D2-	I/O	Data switch output 2 (Differential -)
C3	D1+	I/O	Data switch output 1 (Differential +)
C4	D1-	I/O	Data switch output 1 (Differential -)

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage <sup>(3)</sup>	-0.5	6	V
$V_{I/O}$	Input/Output DC voltage (D+, D-) (TS5USBC412, TS5USBC412I) <sup>(3)</sup>	-0.5	28	V
$V_{I/O}$	Input/Output DC voltage (D+, D-) (TS5USBC410, TS5USBC410I) <sup>(3)</sup>	-0.5	24	V
$V_{I/O}$	Input/Output DC voltage (D1+/D1-, D2+/D2-) <sup>(3)</sup>	-0.5	6	V
$V_I$	Digital input voltage (SEL1, SEL2, $\overline{OE}$ )	-0.5	6	V
$V_O$	Digital output voltage ( $\overline{FLT}$ )	-0.5	6	V
$I_K$	Input-output port diode current (D+, D-, D1+, D1-, D2+, D2-) when $V_{IN} < 0$	-50		mA
$I_{IK}$	Digital logic input clamp current (SEL1, SEL2, $\overline{OE}$ ) when $V_I < 0$ <sup>(3)</sup>	-50		mA
$I_{CC}$	Continuous current through VCC		100	mA
$I_{GND}$	Continuous current through GND	-100		mA
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.3	5.5	V
$V_{I/O}$ (D+, D-)	Analog input/output voltage (TS5USBC412, TS5USBC412I)	0	24	V
$V_{I/O}$ (D+, D-)	Analog input/output voltage (TS5USBC410, TS5USBC410I)	0	20	V
$V_{I/O}$ (D1, D1-, D2+, D2-)	Analog input/output voltage	0	3.6	V
$V_I$	Digital input voltage (SEL1, SEL2, $\overline{OE}$ )	0	5.5	V
$V_O$	Digital output voltage ( $\overline{FLT}$ )	0	5.5	V
$I_{I/O}$ (D+, D-, D1+, D1-, D2+, D2-)	Analog input/output port continuous current	-50	50	mA
$I_{OL}$	Digital output current		3	mA
$T_A$	Operating free-air temperature (Standard) (TS5USBC410, TS5USBC412)	0	70	°C
$T_A$	Operating free-air temperature (Industrial) (TS5USBC410I, TS5USBC412I)	-40	85	°C
$T_J$	Junction temperature	-40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		Device	UNIT
		YFF	
		12 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	91.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	0.8	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	22.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	23.0	°C/W

(1) For more information about traditional and new thermalmetrics, see the [Semiconductor and ICPackage Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

T<sub>A</sub> = -40°C to +85°C (Industrial), T<sub>A</sub> = 0°C to 70°C (Standard), V<sub>CC</sub> = 2.3 V to 5.5 V, GND = 0 V, Typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>POWER</b>						
I <sub>CC-ACTIVE</sub>	Active supply current.	OE = 0 V SEL1, SEL2 = 0 V, 1.8 V or V <sub>CC</sub> 0 V < V <sub>I/O</sub> < 3.6 V		9	22	μA
I <sub>CC-OVP</sub>	Supply current during OVP condition.	OE = 0 V SEL1, SEL2 = 0 V, 1.8 V or V <sub>CC</sub> V <sub>I/O</sub> > V <sub>POS_THLD</sub>		10	35	μA
I <sub>CC-PD</sub>	Standby powered down supply current	OE = 1.8 V or V <sub>CC</sub> SEL1 = 0 V, 1.8 V, or V <sub>CC</sub> SEL2 = 0 V, 1.8 V, or V <sub>CC</sub>		2	6	μA
<b>DC Characteristics</b>						
R <sub>ON</sub>	ON-state resistance	V <sub>I/O</sub> = 0.4 V I <sub>SINK</sub> = 8 mA Refer to <a href="#">ON-State Resistance Figure</a>		5.6	9	Ω
ΔR <sub>ON</sub>	ON-state resistance match between channels	V <sub>I/O</sub> = 0.4 V I <sub>SINK</sub> = 8 mA Refer to <a href="#">ON-State Resistance Figure</a>		0.075	0.48	Ω
R <sub>ON (FLAT)</sub>	ON-state resistance flatness	V <sub>I/O</sub> = 0 V to 0.4 V I <sub>SINK</sub> = 8 mA Refer to <a href="#">ON-State Resistance Figure</a>		0.1	0.4	Ω
I <sub>OFF</sub>	I/O pin OFF leakage current	OE = H V <sub>D±</sub> = 0 V or 3.6 V V <sub>CC</sub> = 2.3 V to 5.5 V V <sub>D1±</sub> or V <sub>D2±</sub> = 3.6 V or 0 V Refer to <a href="#">Off Leakage Figure</a>	-4	0.1	4	μA
I <sub>OFF-20V</sub>	D1/D2+/- pin OFF leakage current during OVP scenario on D+/-	OE = H V <sub>D±</sub> = 20-V V <sub>CC</sub> = 2.3 V to 5.5 V V <sub>D1±</sub> or V <sub>D2±</sub> = 0 V Refer to <a href="#">Off Leakage Figure</a>	-0.5		0.5	μA
I <sub>OFF-20V-DP/N</sub>	D+/- pin OFF leakage current during OVP scenario	OE = H V <sub>D±</sub> = 20-V V <sub>CC</sub> = 2.3 V to 5.5 V V <sub>D1±</sub> or V <sub>D2±</sub> = 0 V Refer to <a href="#">Off Leakage Figure</a>	140	150	180	μA

**Electrical Characteristics (continued)**

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Industrial),  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Standard),  $V_{CC} = 2.3\text{ V}$  to  $5.5\text{ V}$ ,  $\text{GND} = 0\text{ V}$ , Typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{OFF-24V}}$	D1/D2 +/- pin OFF leakage current during OVP scenario on D+/-.	OE = H $V_{D\pm} = 24\text{-V}$ $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$ $V_{D1\pm}$ or $V_{D2\pm} = 0\text{ V}$ Refer to <a href="#">Off Leakage Figure</a>	-0.5		0.5	$\mu\text{A}$
$I_{\text{OFF-24V-DPN}}$	D+/- pin OFF leakage current during OVP scenario.	OE = H $V_{D\pm} = 0\text{ V}$ or $24\text{-V}$ $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$ $V_{D1\pm}$ or $V_{D2\pm} = 0\text{ V}$ Refer to <a href="#">Off Leakage Figure</a>	220	250	270	$\mu\text{A}$
$I_{\text{ON}}$	ON leakage current.	$V_{D\pm} = 0\text{ V}$ or $3.6\text{ V}$ $V_{D1\pm}$ and $V_{D2+/-} = \text{high-Z}$ Refer to <a href="#">On Leakage Figure</a>	-5.5	0.25	7.5	$\mu\text{A}$
<b>Digital Characteristics</b>						
$V_{\text{IH}}$	Input logic high	SEL1, SEL2, $\overline{\text{OE}}$	1.4			V
$V_{\text{IL}}$	Input logic low	SEL1, SEL2, $\overline{\text{OE}}$			0.5	V
$V_{\text{OL}}$	Output logic low	$\overline{\text{FLT}}$ $I_{\text{OL}} = 3\text{ mA}$			0.4	V
$I_{\text{IH}}$	Input high leakage current	SEL1, SEL2, $\overline{\text{OE}} = 1.8\text{ V}$ , $V_{CC}$	-1	1	5	$\mu\text{A}$
$I_{\text{IL}}$	Input low leakage current	SEL1, SEL2, $\overline{\text{OE}} = 0\text{ V}$	-1	$\pm 0.2$	5	$\mu\text{A}$
$R_{\text{PD}}$	Internal pull-down resistor on digital input pins			6		$\text{M}\Omega$
$C_{\text{I}}$	Digital input capacitance	SEL1, SEL2 = $0\text{ V}$ , $1.8\text{ V}$ or $V_{CC}$ $f = 1\text{ MHz}$		4		pF
<b>Protection</b>						
$V_{\text{OVP\_TH}}$	OVP positive threshold		4.4	4.8	5.2	V
$V_{\text{OVP\_HYST}}$	OVP threshold hysteresis		125	250	440	mV
$V_{\text{CLAMP\_V}}$	Maximum voltage to appear on D1± and D2± pins during OVP scenario (TS5USBC412, TS5USBC412I)	$V_{D\pm} = 0$ to $24\text{ V}$ $t_{\text{RISE}}$ and $t_{\text{FALL}}(10\% \text{ to } 90\%) = 100\text{ ns}$ $R_L = \text{Open}$ Switch on or off $\overline{\text{OE}} = 0\text{ V}$			11.2	V
$V_{\text{CLAMP\_V}}$	Maximum voltage to appear on D1± and D2± pins during OVP scenario (TS5USBC412, TS5USBC412I)	$V_{D\pm} = 0$ to $24\text{ V}$ $t_{\text{RISE}}$ and $t_{\text{FALL}}(10\% \text{ to } 90\%) = 100\text{ ns}$ $R_L = 50\Omega$ Switch on or off $\overline{\text{OE}} = 0\text{ V}$			10.8	V
$V_{\text{CLAMP\_V}}$	Maximum voltage to appear on D1± and D2± pins during OVP scenario (TS5USBC410, TS5USBC410I)	$V_{D\pm} = 0$ to $20\text{ V}$ $t_{\text{RISE}}$ and $t_{\text{FALL}}(10\% \text{ to } 90\%) = 100\text{ ns}$ $R_L = \text{Open}$ Switch on or off $\overline{\text{OE}} = 0\text{ V}$			10.8	V
$V_{\text{CLAMP\_V}}$	Maximum voltage to appear on D1± and D2± pins during OVP scenario (TS5USBC410, TS5USBC410I)	$V_{D\pm} = 0$ to $20\text{ V}$ $t_{\text{RISE}}$ and $t_{\text{FALL}}(10\% \text{ to } 90\%) = 100\text{ ns}$ $R_L = 50\Omega$ Switch on or off $\overline{\text{OE}} = 0\text{ V}$			9.8	V

**Electrical Characteristics (continued)**

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Industrial),  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Standard),  $V_{CC} = 2.3\text{ V}$  to  $5.5\text{ V}$ ,  $\text{GND} = 0\text{ V}$ , Typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{CLAMP\_T}}$	Maximum OVP transient duration above 5 V (TS5USBC412, TS5USBC412I).	$V_{D\pm} = 0$ to 24 V $t_{\text{RISE}}$ and $t_{\text{FALL}}$ (10% to 90 %) = 100 ns $R_L = \text{Open } C_L = 10\text{pF}$ Switch on or off $\overline{\text{OE}} = 0\text{ V}$		75	100	ns
$V_{\text{CLAMP\_T}}$	Maximum OVP transient duration above 5 V (TS5USBC412, TS5USBC412I)	$V_{D\pm} = 0$ to 24 V $t_{\text{RISE}}$ and $t_{\text{FALL}}$ (10% to 90 %) = 100 ns $R_L = 50\Omega C_L = 10\text{pF}$ Switch on or off $\overline{\text{OE}} = 0\text{ V}$		68	95	ns
$V_{\text{CLAMP\_T}}$	Maximum OVP transient duration above 5 V (TS5USBC410, TS5USBC410I)	$V_{D\pm} = 0$ to 20 V $t_{\text{RISE}}$ and $t_{\text{FALL}}$ (10% to 90 %) = 100 ns $R_L = \text{Open } C_L = 10\text{pF}$ Switch on or off $\overline{\text{OE}} = 0\text{ V}$		64	100	ns
$V_{\text{CLAMP\_T}}$	Maximum OVP transient duration above 5 V (TS5USBC410, TS5USBC410I)	$V_{D\pm} = 0$ to 20 V $t_{\text{RISE}}$ and $t_{\text{FALL}}$ (10% to 90 %) = 100 ns $R_L = 50\Omega C_L = 10\text{pF}$ Switch on or off $\overline{\text{OE}} = 0\text{ V}$		55	95	ns
$t_{\text{EN\_OVP}}$	OVP enable time	$R_{\text{PU}} = 10\text{ k}\Omega$ to $V_{CC} (\overline{\text{FLT}})$ $C_L = 35\text{ pF}$ Refer to <a href="#">OVP Timing Diagram Figure</a>			3	$\mu\text{s}$
$t_{\text{REC\_OVP}}$	OVP recovery time	$R_{\text{PU}} = 10\text{ k}\Omega$ to $V_{CC} (\overline{\text{FLT}})$ $C_L = 35\text{ pF}$ Refer to <a href="#">OVP Timing Diagram Figure</a>			5	$\mu\text{s}$

## 6.6 Dynamic Characteristics

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Industrial),  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Standard),  $V_{CC} = 2.3\text{ V}$  to  $5.5\text{ V}$ ,  $GND = 0\text{ V}$ , Typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$C_{OFF}$	D+, D- off capacitance	$V_{D+/-} = 0$ or $3.3\text{ V}$ , $\overline{OE} = V_{CC}$ $f = 240\text{ MHz}$	Switch OFF	1.2	1.6	3.2	pF
	D1+, D1-, D2+, D2- off capacitance	$V_{D+/-} = 0$ or $3.3\text{ V}$ , $\overline{OE} = V_{CC}$ or $\overline{OE} = 0\text{ V}$ with SEL1, SEL2 (switch not selected) $f = 240\text{ MHz}$	Switch OFF or not selected	1.2	1.5	3.0	pF
$C_{ON}$	IO pins ON capacitance (TS5USBC412, TS5USBC412I)	$V_{D+/-} = 0$ or $3.3\text{ V}$ , $f = 240\text{ MHz}$	Switch ON	2.0	2.5	3.9	pF
$C_{ON}$	IO pins ON capacitance (TS5USBC410, TS5USBC410I)	$V_{D+/-} = 0$ or $3.3\text{ V}$ , $f = 240\text{ MHz}$	Switch ON	2.0	2.7	4	pF
$O_{ISO}$	Differential off isolation	$R_L = 50\ \Omega$ $C_L = 5\text{ pF}$ $f = 100\text{ kHz}$ Refer to <a href="#">Off Isolation Figure</a>	Switch OFF		-95		dB
		$R_L = 50\ \Omega$ $C_L = 5\text{ pF}$ $f = 240\text{ MHz}$ Refer to <a href="#">Off Isolation Figure</a>	Switch OFF		-25		dB
$X_{TALK}$	Channel to Channel crosstalk	$R_L = 50\ \Omega$ $C_L = 5\text{ pF}$ $f = 100\text{ kHz}$ Refer to <a href="#">Crosstalk Figure</a>	Switch ON		-90		dB
BW	Bandwidth (TS5USBC412, TS5USBC412I)	$R_L = 50\ \Omega$ ; Refer to <a href="#">BW and Insertion Loss Figure</a>	Switch ON		1.2		GHz
BW	Bandwidth (TS5USBC410, TS5USBC410I)	$R_L = 50\ \Omega$ ; Refer to <a href="#">BW and Insertion Loss Figure</a>	Switch ON		1.1		GHz
$I_{LOSS}$	Insertion loss	$R_L = 50\ \Omega$ $f = 240\text{ MHz}$ ; Refer to <a href="#">BW and Insertion Loss Figure</a>	Switch ON		-0.8		dB

## 6.7 Timing Requirements

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$  (Industrial),  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$  (Standard),  $V_{CC} = 2.3\text{ V}$  to  $5.5\text{ V}$ ,  $GND = 0\text{ V}$ , Typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{SWITC H}$	Switching time between channels (SEL1, SEL2 to output)	$V_{D+/-} = 0.8\text{ V}$ Refer to <a href="#">Tswitch Timing Figure</a>		0.8	2.5	$\mu\text{s}$
$t_{ON}$	Device turn on time ( $\overline{OE}$ to output).	$V_{D+/-} = 0.8\text{ V}$ Refer to <a href="#">Ton and Toff Figure</a>	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$	84	250	$\mu\text{s}$
$t_{OFF}$	Device turn off time ( $\overline{OE}$ to output)	$V_{D+/-} = 0.8\text{ V}$ Refer to <a href="#">Ton and Toff Figure</a>		0.75	1	$\mu\text{s}$
$t_{SK(P)}$	Skew of opposite transitions of same output (between D+ and D-).	$V_{D+/-} = 0.4\text{ V}$ Refer to <a href="#">Tsk Figure</a>	$R_L = 50\ \Omega$ , $C_L = 1\text{ pF}$ , $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$	11	50	ps
$t_{PD}$	Propagation delay.	$f = 240\text{ MHz}$ $V_{D+/-} = 0.4\text{ V}$ Refer to <a href="#">Tpd Figure</a>	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $V_{CC} = 2.3\text{ V}$ to $5.5\text{ V}$	150	230	ps



### 6.8 Typical Characteristics

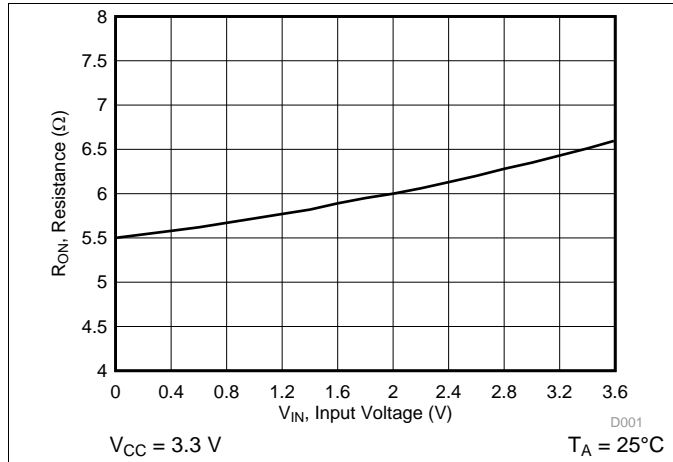


图 1. ON-Resistance vs Input Voltage

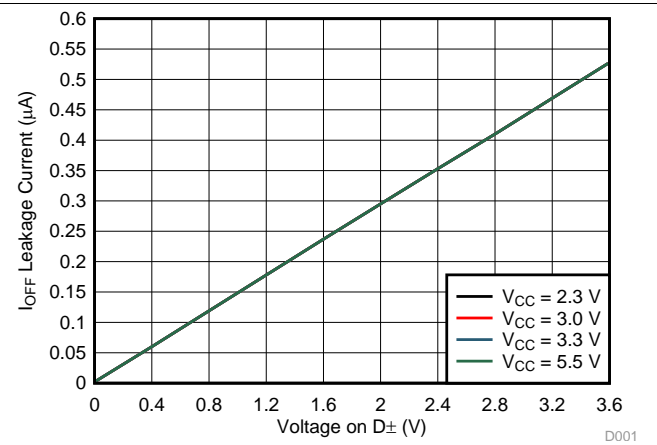


图 2.  $I_{OFF}$  Leakage Current vs Voltage on  $D_{\pm}$

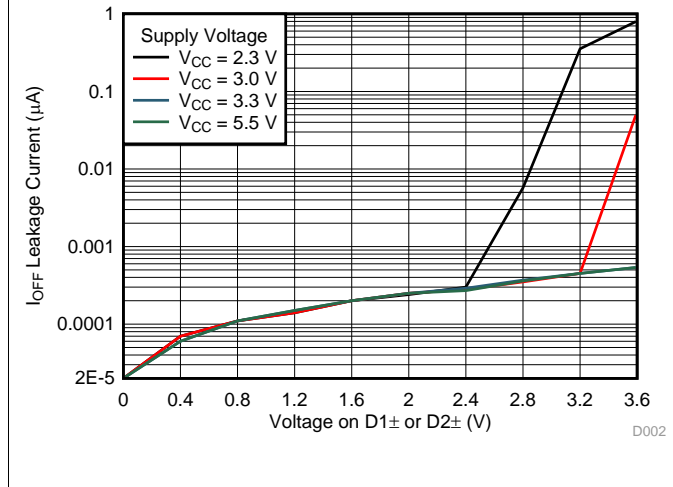


图 3.  $I_{OFF}$  Leakage Current vs Voltage on  $D1_{\pm}$  or  $D2_{\pm}$

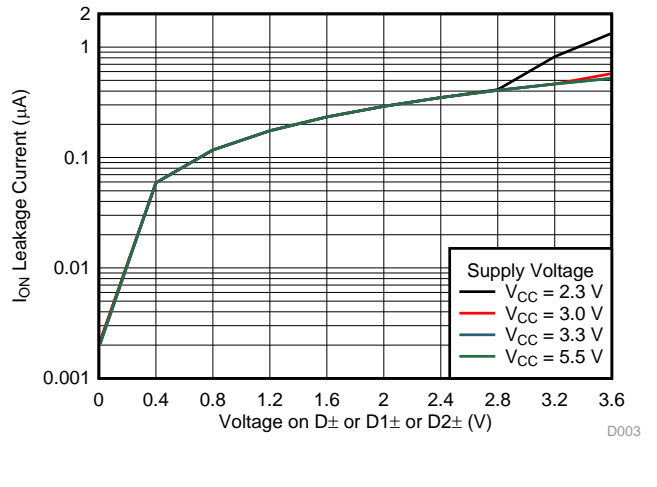
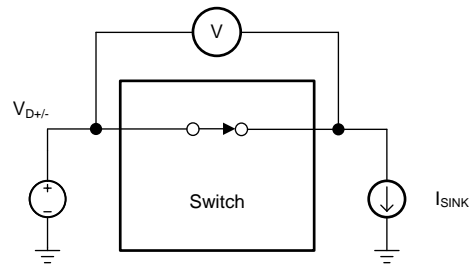


图 4.  $I_{ON}$  Leakage Current vs Voltage on  $D_{\pm}$  or  $D1_{\pm}$  or  $D2_{\pm}$

## 7 Parameter Measurement Information



Channel ON,  $R_{ON} = V/I_{SINK}$

图 5. ON-State Resistance ( $R_{ON}$ )

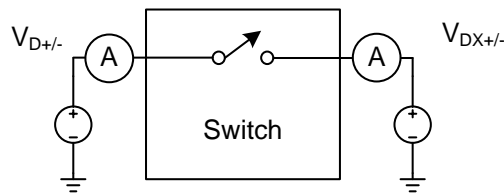


图 6. Off Leakage

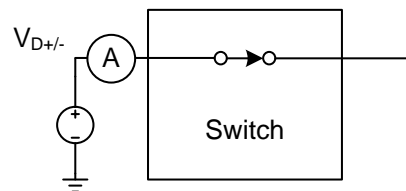
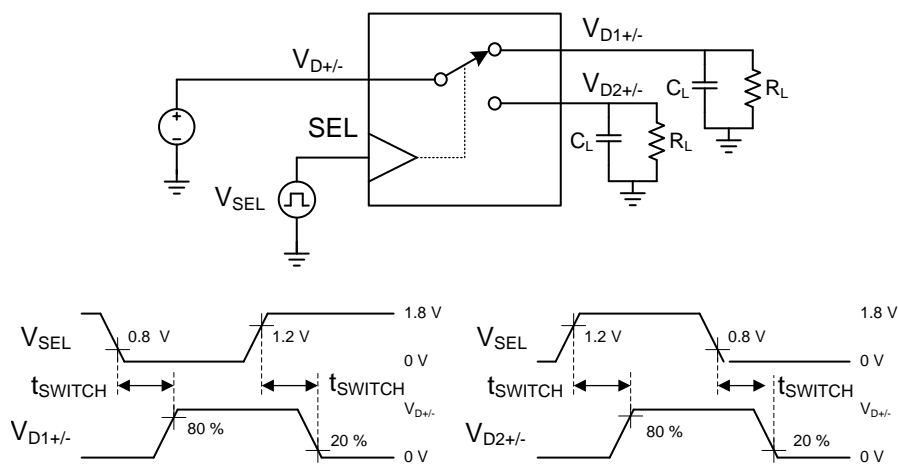


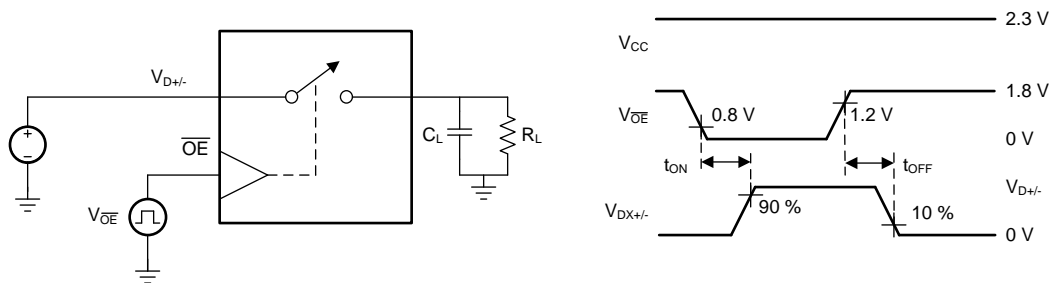
图 7. On Leakage



- (1) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r < 500 \text{ ps}$ .
- (2)  $C_L$  includes probe and jig capacitance.

图 8.  $t_{SWITCH}$  Timing

Parameter Measurement Information (接下页)



- (1) All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz,  $Z_0 = 50 \Omega$ ,  $t_r < 500$  ps,  $t_f < 500$  ps.
- (2)  $C_L$  includes probe and jig capacitance.

图 9.  $t_{ON}$ ,  $t_{OFF}$  for  $\overline{OE}$

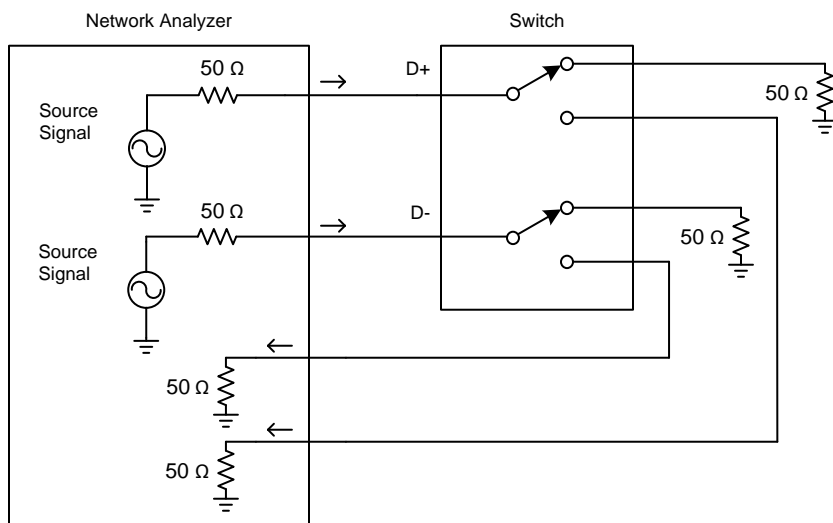


图 10. Off Isolation

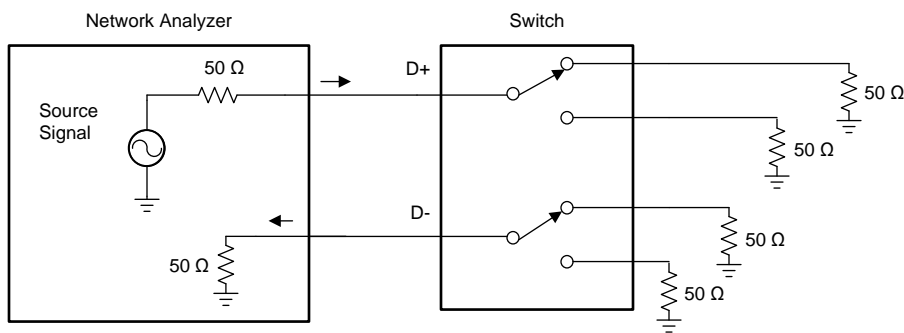
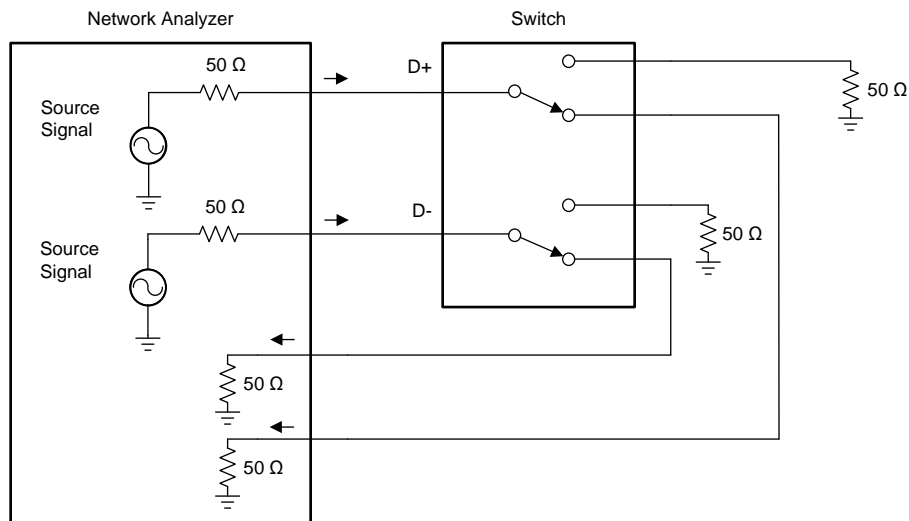
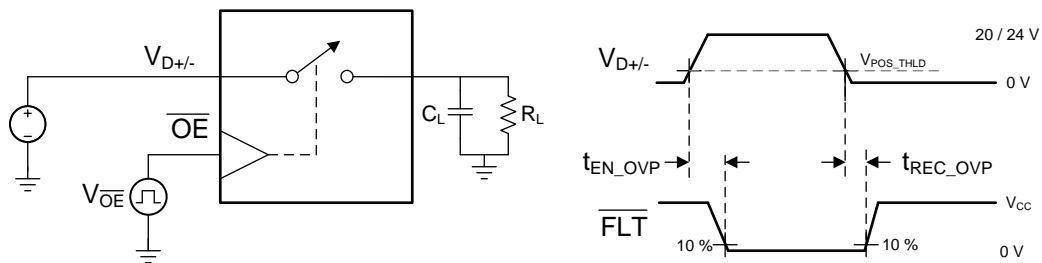
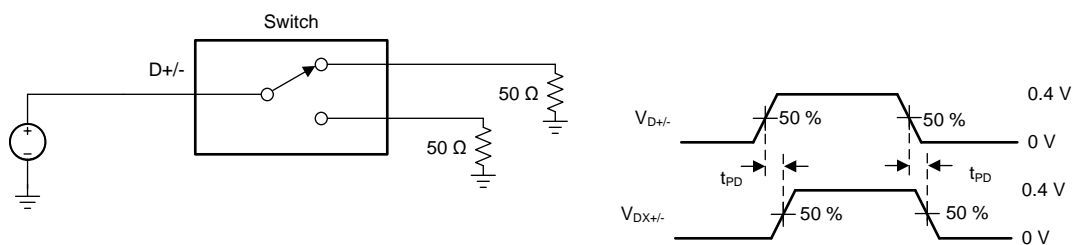


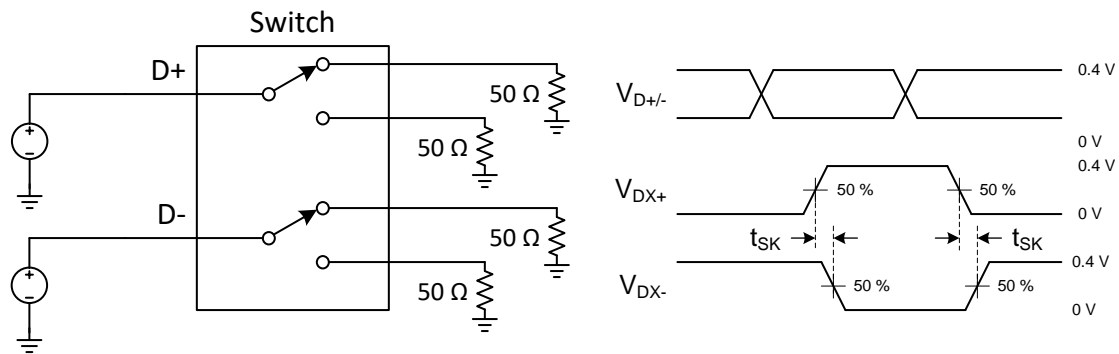
图 11. Cross Talk

**Parameter Measurement Information (接下页)**

**图 12. BW and Insertion Loss**

**图 13.  $t_{EN\_OVP}$  and  $t_{DIS\_OVP}$  Timing Diagram**


- (1) All input pulses are supplied by generators having the following characteristics: PRR = 240 MHz,  $Z_O = 50 \Omega$ ,  $t_r < 500$  ps,  $t_f < 500$  ps.
- (2)  $C_L$  includes probe and jig capacitance.

**图 14.  $t_{PD}$**

Parameter Measurement Information (接下页)



- (1) All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r < 500 \text{ ps}$ ,  $t_f < 500 \text{ ps}$ .
- (2)  $C_L$  includes probe and jig capacitance.

图 15.  $t_{SK}$

## 8 Detailed Description

### 8.1 Overview

The TS5USBC41 is a bidirectional low-power dual port, high-speed, USB 2.0 analog switch with integrated protection for USB Type-C systems. The device is configured as a dual 2:1 or 1:2 switch and is optimized for handling the USB 2.0 D+/- lines in a USB Type-C system as shown in [图 16](#).

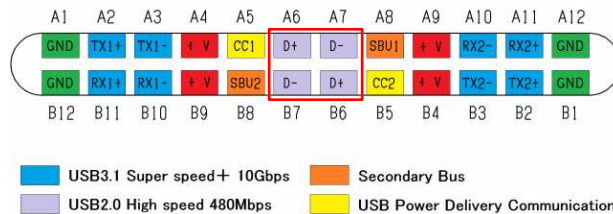
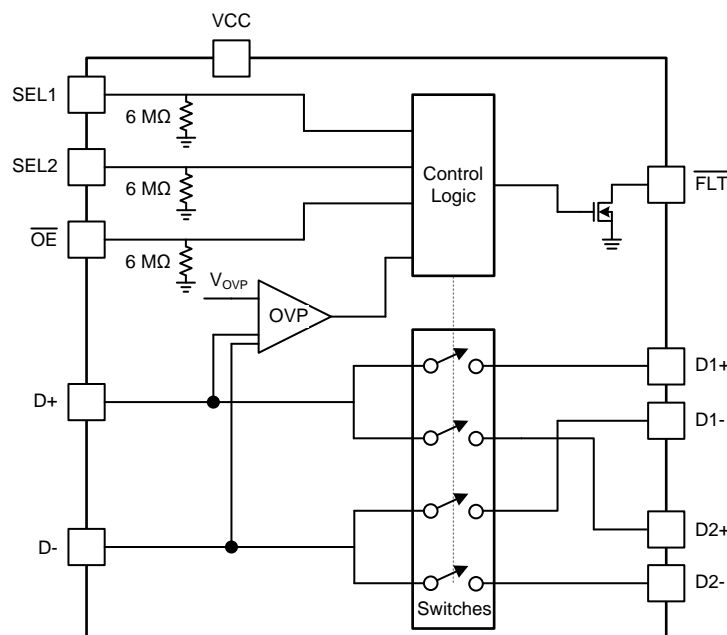


图 16. USB Type-C Connector Pinout

The TS5USBC41 also works in traditional USB systems that need protection from fault conditions such as automotive and applications that require higher voltage charging. The device maintains excellent signal integrity through the optimization of both  $R_{ON}$  and BW while protecting the system with 20 V (TS5USBC410) and 24 V (TS5USBC412) OVP protection. The OVP implementation is designed to protect sensitive system components behind the switch that cannot survive a fault condition where VBUS is shorted to the D+ and D- pins on the connector.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Powered-off Protection

When the TS5USBC41 is powered off the I/Os of the device remain in a high-Z state. The crosstalk, off-isolation, and leakage remain within the [Electrical Specifications](#).

This prevents errant voltages from reaching the rest of the system and maintains isolation when the system is powering up.

#### 8.3.2 Overvoltage Protection

The OVP of the TS5USBC41 is designed to protect the system from D+/- shorts to VBUS at the USB and USB Type-C connector. [图 17](#) depicts a moisture short that would cause high voltage (20 V for TS5USBC410 or 20 V for TS5USBC412) to appear on an existing USB solution that could pass through the device and damage components behind the device.

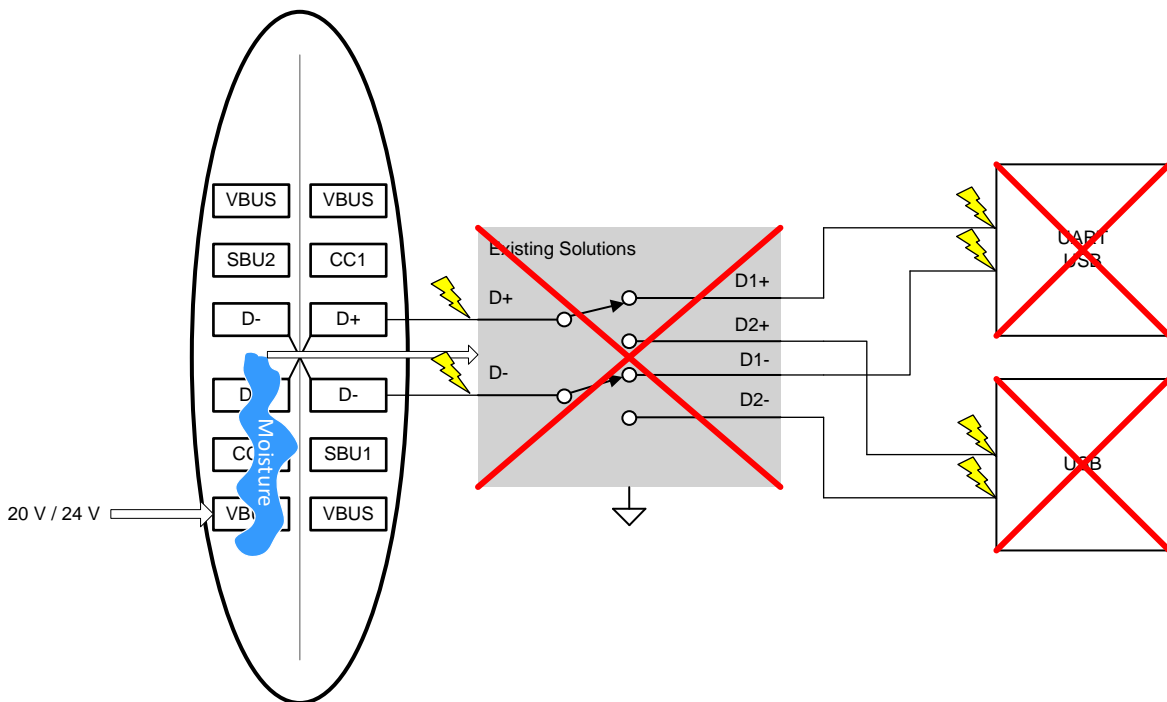


图 17. Existing Solution Being Damaged by a Short

TS5USBC41

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Feature Description (接下页)

The TS5USBC41 will open the switches and protect the rest of the system by blocking the 20 V / 24 V as depicted in 图 18.

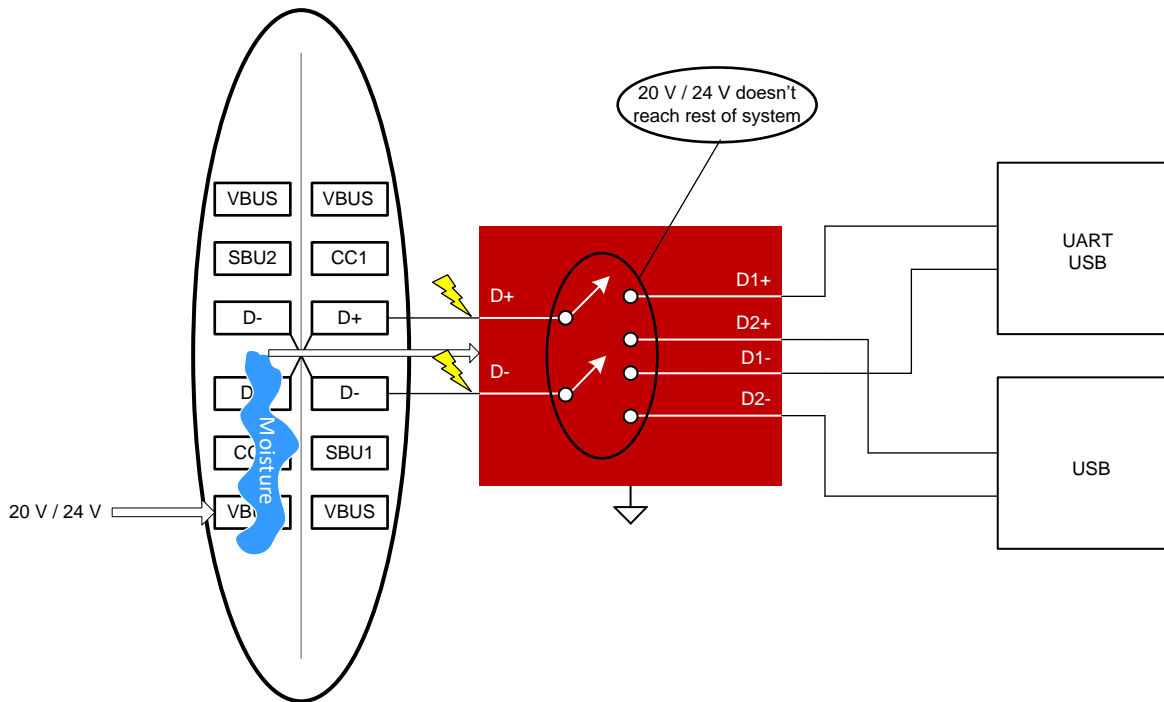


图 18. Protecting During a 20-V / 24-V Short

图 19 is a waveform showing the voltage on the pins during an over-voltage scenario.

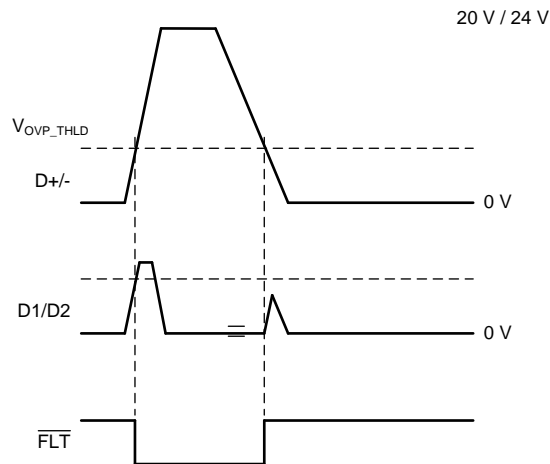


图 19. Overvoltage Protection Waveform



## 8.4 Device Functional Modes

### 8.4.1 Pin Functions

**表 1. Function Table**

$\overline{OE}$	SEL1	SEL2	D- Connection	D+ Connection
H	X	X	High-Z	High-Z
L	L	L	D- to D1-	D+ to D1+
L	L	H	D- to D1-	D+ to D2+
L	H	L	D- to D2-	D+ to D1+
L	H	H	D- to D2-	D+ to D2+

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

There are many USB applications in which the USB hubs or controllers have a limited number of USB I/Os or need to route signals from a single USB connector. The TS5USBC41 solution can effectively expand the limited USB I/Os by switching between multiple USB buses to interface them to a single USB hub or controller or route signals from one connector to two different locations. With independent control of the two switches using SEL1 and SEL2, TS5USBC41 can be used to cross switch single ended signals.

### 9.2 Typical Application

TS5USBC41 USB/UART switch. The TS5USBC41 is used to switch signals between the USB path, which goes to the baseband or application processor, or the UART path, which goes to debug port. The TS5USBC41 has internal 6-M $\Omega$  pull-down resistors on SEL1, SEL2, and OE. The pull-down on SEL1 and SEL2 pins ensure the D1+/D1- channel is selected by default. The pull-down on OE enables the switch when power is applied.

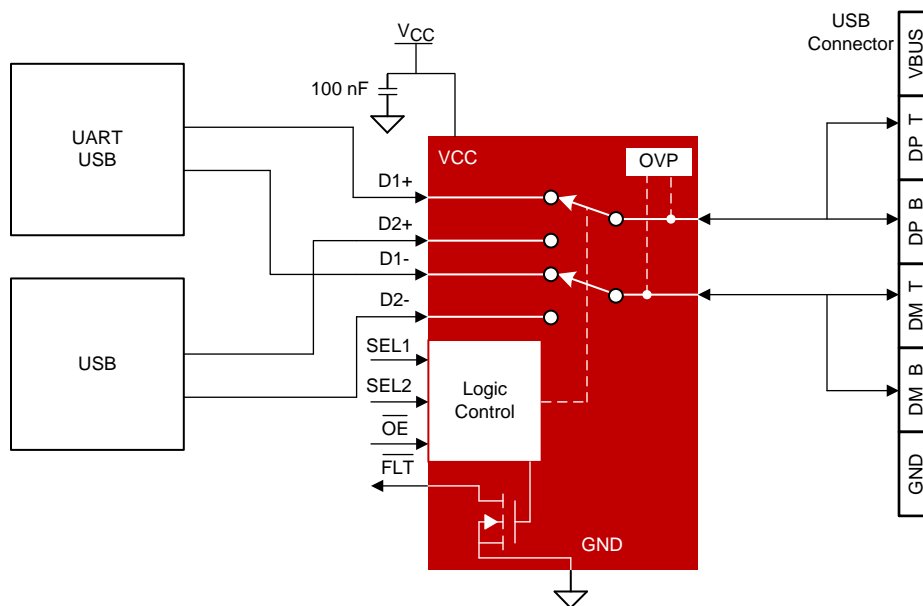


图 20. Typical Application

#### 9.2.1 Design Requirements

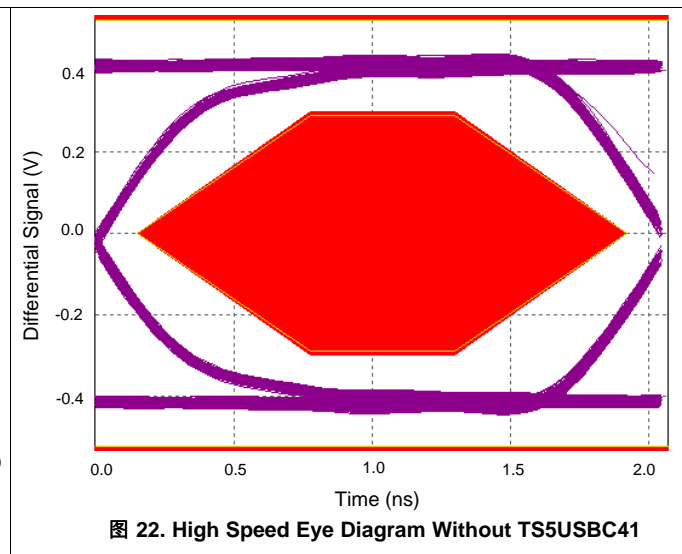
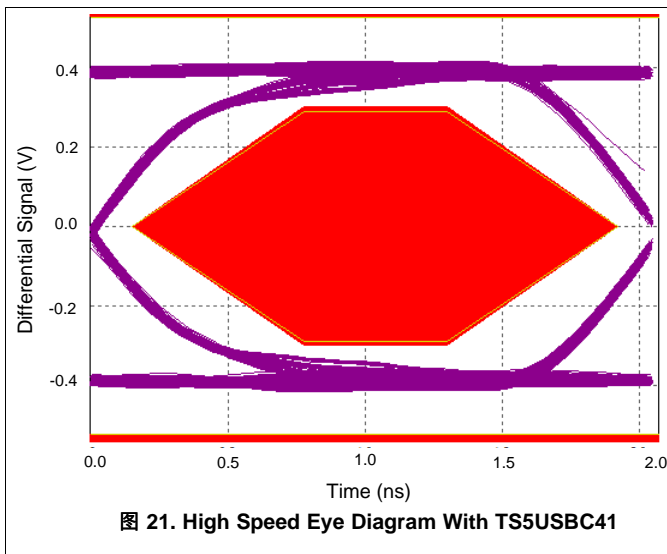
Design requirements of USB 1.0, 1.1, and 2.0 standards must be followed. The TS5USBC41 has internal 6-M $\Omega$  pull-down resistors on SEL1, SEL2, and OE, so no external resistors are required on the logic pins. The internal pull-down resistor on SEL1 and SEL2 pins ensures the D1+ and D1- channels are selected by default. The internal pull-down resistor on OE enables the switch when power is applied to VCC.

#### 9.2.2 Detailed Design Procedure

The TS5USBC41 can be properly operated without any external components. However, TI recommends that unused pins must be connected to ground through a 50- $\Omega$  resistor to prevent signal reflections back into the device. TI does recommend a 100-nF bypass capacitor placed close to TS5USBC41 VCC pin.

## Typical Application (接下页)

### 9.2.3 Application Curves



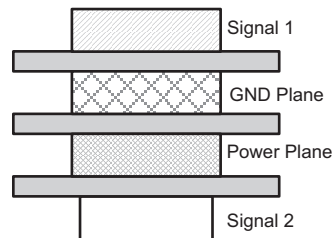
## 10 Power Supply Recommendations

Power to the device is supplied through the VCC pin and must follow the USB 1.0, 1.1, and 2.0 standards. TI recommends placing a 100 nF bypass capacitor as close to the supply pin VCC as possible to help smooth out lower frequency noise to provide better load regulation across the frequency spectrum.

## 11 Layout

### 11.1 Layout Guidelines

1. Place supply bypass capacitors as close to VCC pin as possible and avoid placing the bypass caps near the  $D_{\pm}$  traces.
2. The high-speed  $D_{\pm}$  must match and be no more than 4 inches long; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance. In layout, the impedance of  $D+$  and  $D-$  traces must match the cable characteristic differential impedance for optimal performance.
3. Route the high-speed USB signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.
4. When it becomes necessary to turn  $90^{\circ}$ , use two  $45^{\circ}$  turns or an arc instead of making a single  $90^{\circ}$  turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.
5. Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.
6. Avoid stubs on the high-speed USB signals due to signal reflections. If a stub is unavoidable, then the stub must be less than 200 mm.
7. Route all high-speed USB signal traces over continuous GND planes, with no interruptions.
8. Avoid crossing over anti-etch, commonly found with plane splits.
9. Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in [图 23](#).

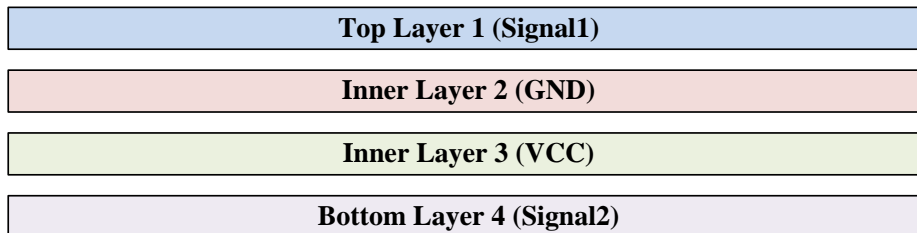


**图 23. Four-Layer Board Stack-Up**

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

## 11.2 Layout Example

Example 4 layer PCB Stackup



- Via to layer 2 (GND)
- Via to layer 3 (VCC)
- Via to layer 4 (Signal)

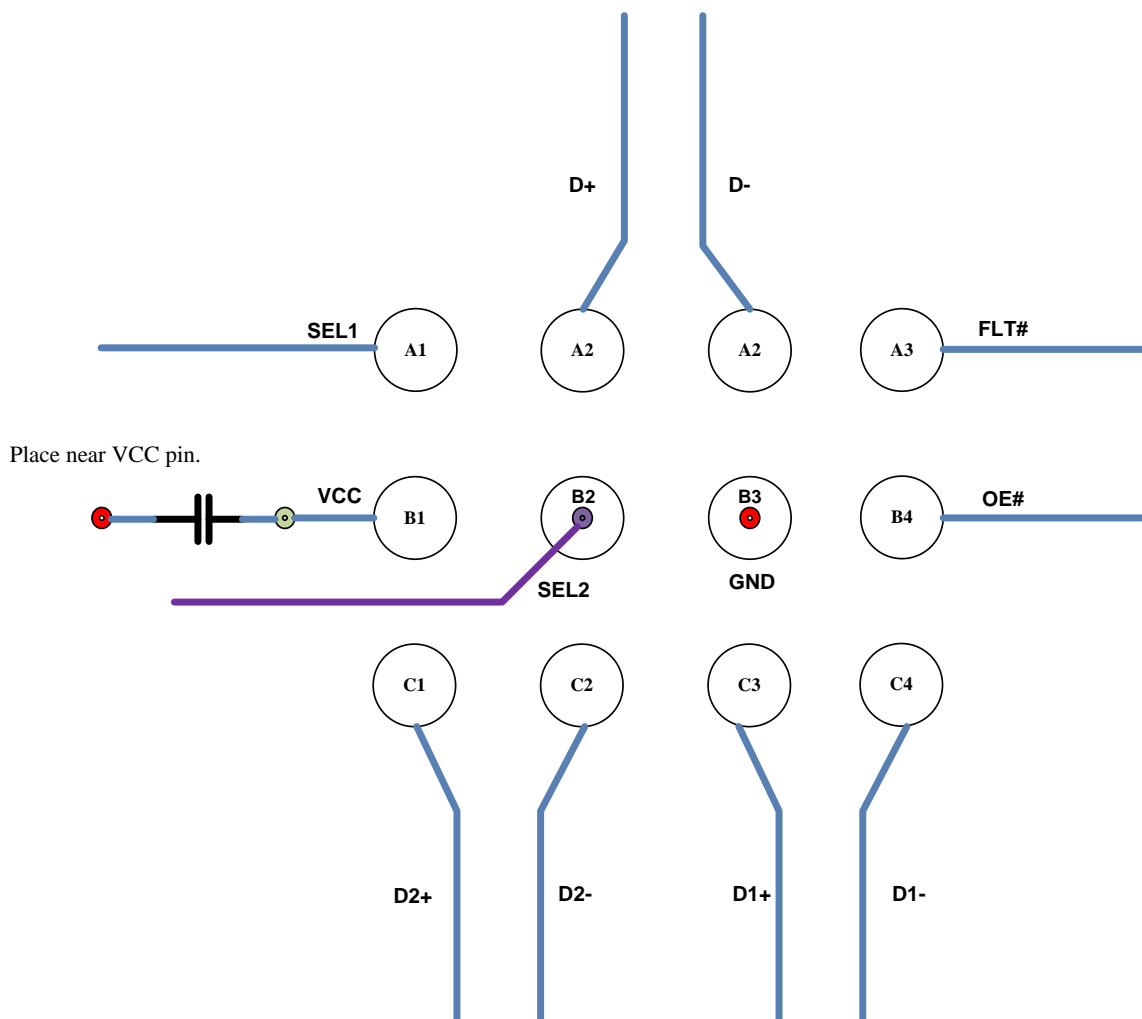


图 24. Layout Example

## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

请参阅如下相关文档：

- [《USB 2.0 电路板设计和布局指南》](#)
- [《高速布局指南》应用报告](#)
- [《高速接口布局指南》](#)

### 12.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

**TI E2E™ 在线社区** [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 12.4 商标

E2E is a trademark of Texas Instruments.

USB Type-C is a trademark of USB Implementers Forum.

All other trademarks are the property of their respective owners.

### 12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 术语表

[SLYZ022](#) — *TI* 术语表。

这份术语表列出并解释术语、缩写和定义。

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查看左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5USBC410IYFFR	ACTIVE	DSBGA	YFF	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TU41	<a href="#">Samples</a>
TS5USBC410IYFFT	ACTIVE	DSBGA	YFF	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TU41	<a href="#">Samples</a>
TS5USBC410YFFR	ACTIVE	DSBGA	YFF	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 70	TU41	<a href="#">Samples</a>
TS5USBC410YFFT	ACTIVE	DSBGA	YFF	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 70	TU41	<a href="#">Samples</a>
TS5USBC412IYFFR	ACTIVE	DSBGA	YFF	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TU41	<a href="#">Samples</a>
TS5USBC412IYFFT	ACTIVE	DSBGA	YFF	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TU41	<a href="#">Samples</a>
TS5USBC412YFFR	ACTIVE	DSBGA	YFF	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 70	TU41	<a href="#">Samples</a>
TS5USBC412YFFT	ACTIVE	DSBGA	YFF	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	0 to 70	TU41	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

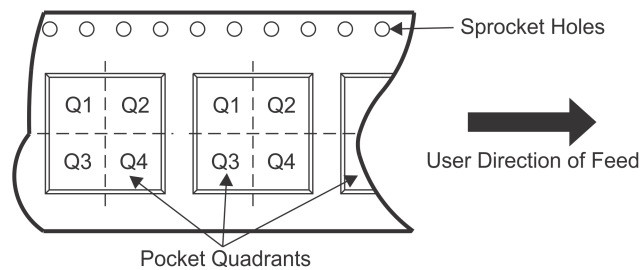
<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

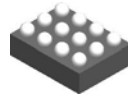
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5USBC410IYFFR	DSBGA	YFF	12	3000	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2
TS5USBC410IYFFR	DSBGA	YFF	12	3000	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2
TS5USBC410IYFFT	DSBGA	YFF	12	250	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2
TS5USBC410IYFFT	DSBGA	YFF	12	250	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2
TS5USBC410YFFR	DSBGA	YFF	12	3000	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2
TS5USBC410YFFT	DSBGA	YFF	12	250	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2
TS5USBC412IYFFR	DSBGA	YFF	12	3000	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2
TS5USBC412IYFFT	DSBGA	YFF	12	250	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2
TS5USBC412YFFR	DSBGA	YFF	12	3000	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2
TS5USBC412YFFT	DSBGA	YFF	12	250	180.0	8.4	1.38	1.76	0.77	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5USBC410IYFFR	DSBGA	YFF	12	3000	182.0	182.0	20.0
TS5USBC410IYFFR	DSBGA	YFF	12	3000	182.0	182.0	20.0
TS5USBC410IYFFT	DSBGA	YFF	12	250	182.0	182.0	20.0
TS5USBC410IYFFT	DSBGA	YFF	12	250	182.0	182.0	20.0
TS5USBC410YFFR	DSBGA	YFF	12	3000	182.0	182.0	20.0
TS5USBC410YFFT	DSBGA	YFF	12	250	182.0	182.0	20.0
TS5USBC412IYFFR	DSBGA	YFF	12	3000	182.0	182.0	20.0
TS5USBC412IYFFT	DSBGA	YFF	12	250	182.0	182.0	20.0
TS5USBC412YFFR	DSBGA	YFF	12	3000	182.0	182.0	20.0
TS5USBC412YFFT	DSBGA	YFF	12	250	182.0	182.0	20.0

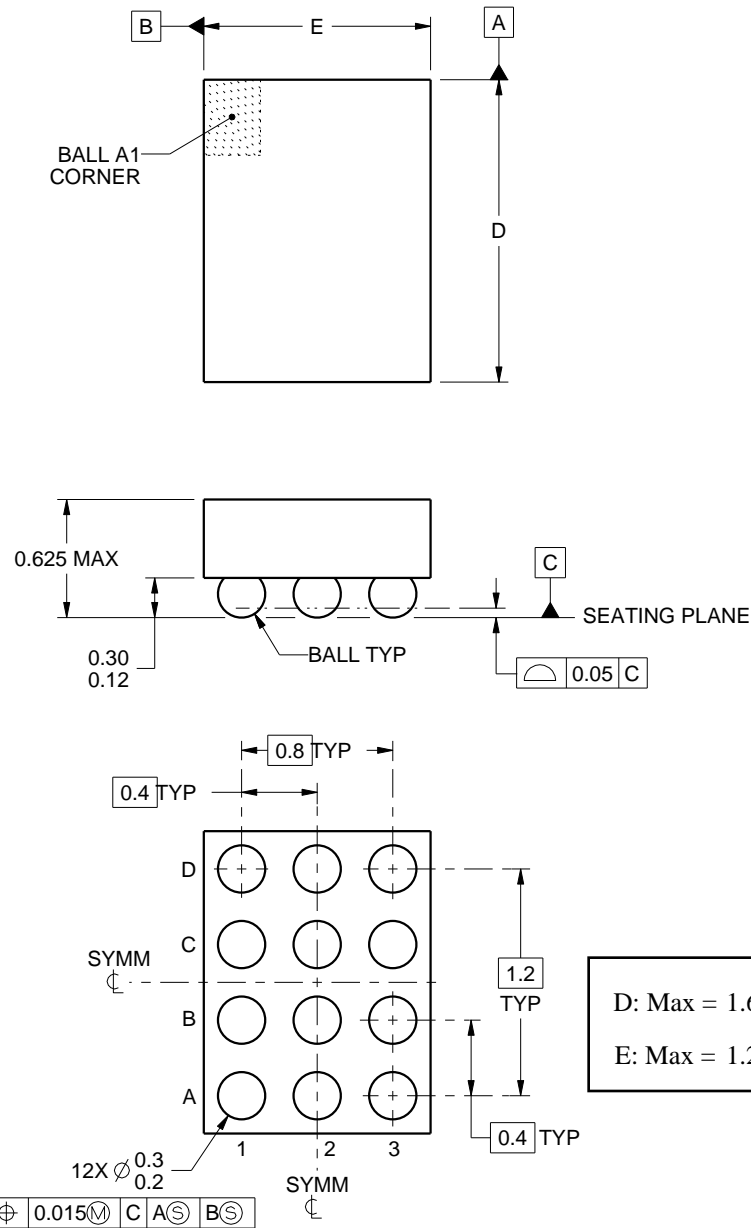
YFF0012



# PACKAGE OUTLINE

## DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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**NOTES:**

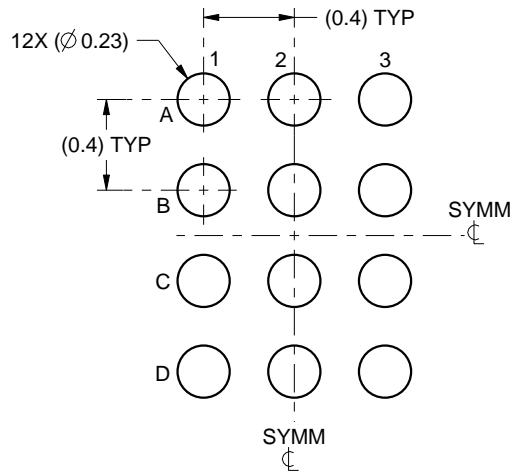
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

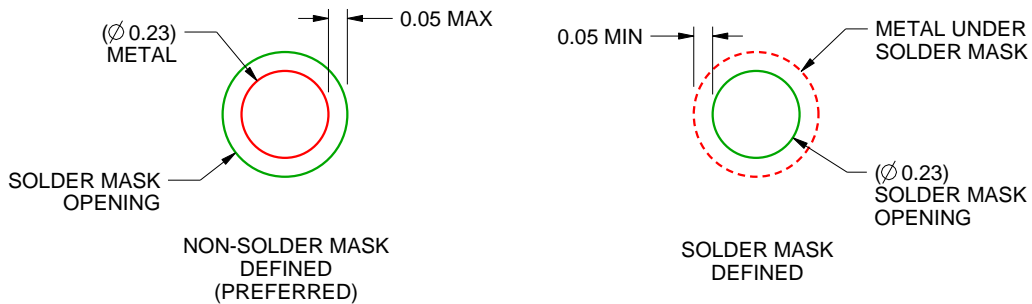
YFF0012

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

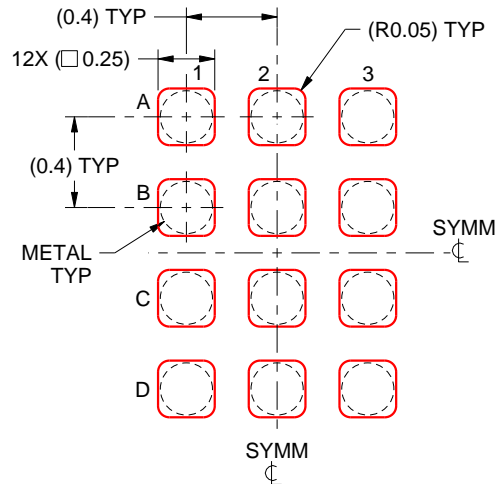
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFF0012

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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