

TPS22919-Q1 5.5V、1.5A、90mΩ 自保护负载开关

1 特性

- 符合汽车类应用要求
- 符合 AEC-Q100 标准：
 - 器件温度等级 1: -40°C 至 125°C 的环境工作温度范围
- 输入工作电压范围 (V_{IN}): 1.6V 至 5.5V
- 最大持续电流 (I_{MAX}): 1.5A
- 导通电阻 (R_{ON}):
 - 5V V_{IN} : 89mΩ (典型值)
 - 3.6V V_{IN} : 90mΩ (典型值)
 - 1.8V V_{IN} : 105mΩ (典型值)
- 输出短路保护 (I_{SC}): 3A (典型值)
- 低功耗:
 - 导通状态 (I_{Q}): 8μA (典型值)
 - 关断状态 (I_{SD}): 2nA (典型值)
- 智能 ON 引脚下拉电阻 (R_{PD}):
 - $\text{ON} \geq V_{\text{IH}}$ (I_{ON}): 100nA (最大值)
 - $\text{ON} \leq V_{\text{IL}}$ (R_{PD}): 530kΩ (典型值)
- 可限制浪涌电流的慢速导通时序 (t_{ON}):
 - 5.0V 导通时间 (t_{ON}): 3.2mV/μs 下为 1.95ms
 - 3.6V 导通时间 (t_{ON}): 2.7mV/μs 下为 1.75ms
 - 1.8V 导通时间 (t_{ON}): 1.8mV/μs 下为 1.5ms
- 可调节输出放电和下降时间:
 - 内部 QOD 电阻 = 24Ω (典型值)

2 应用

- 信息娱乐系统、仪表组和音响主机
- 汽车仪表组显示屏
- ADAS 环视系统 ECU
- 车身控制模块和网关

3 说明

TPS22919-Q1 器件是一款压摆率可控的小型单通道负载开关。此器件包含一个可在 1.6V 至 5.5V 输入电压范围内运行的 N 沟道 MOSFET，并且支持 1.5A 的最大持续电流。

开关导通状态由数字输入控制，此输入可与低压控制信号直接连接。首次加电时，此器件使用智能下拉电阻来保持 ON 引脚不悬空，直到系统定序完成。故意将该引脚驱动为高电平 ($>V_{\text{IH}}$) 之后，便会断开智能下拉电阻，以防止不必要的功率损耗。

TPS22919-Q1 负载开关也是自保护的，这意味着它可以保护自己免受器件输出上短路事件的影响。它还具有热关断功能，可防止因过热而造成任何损坏。

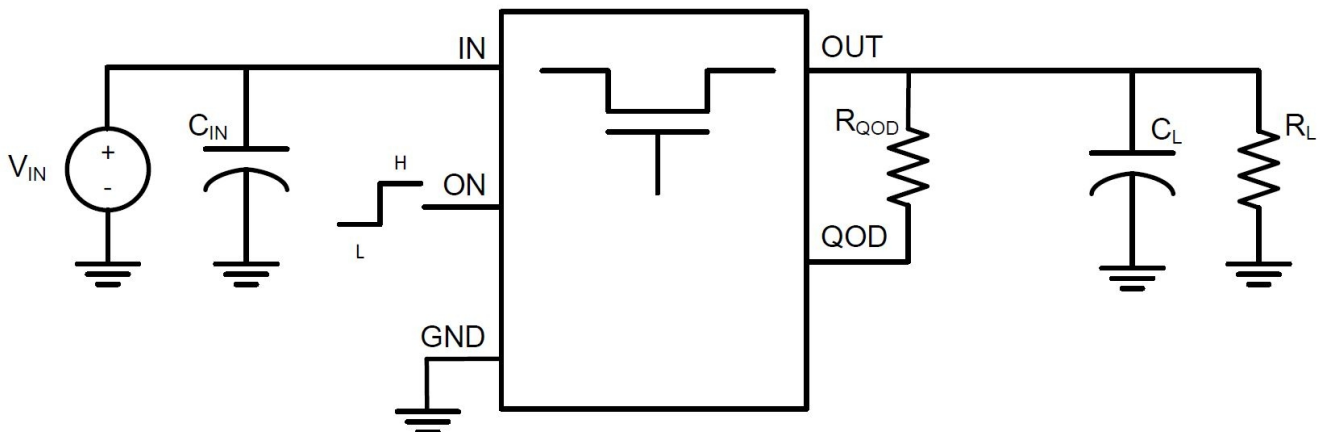
TPS22919-Q1 采用标准 SC-70 封装，工作结温范围为 -40°C 至 125°C 。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS22919-Q1	SC-70 (6)	2.1mm × 2.0mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



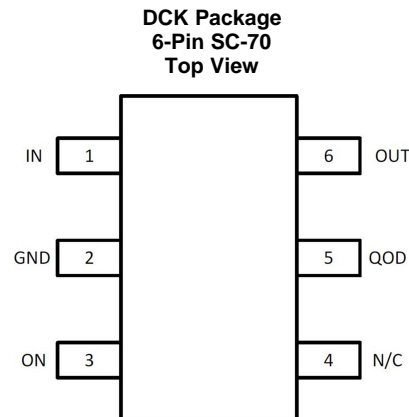
目录

1	特性	1	8.2	Functional Block Diagram	12
2	应用	1	8.3	Feature Description	13
3	说明	1	8.4	Device Functional Modes	14
4	修订历史记录	2	9	Application and Implementation	15
5	Pin Configuration and Functions	3	9.1	Application Information	15
6	Specifications	4	9.2	Typical Application	15
6.1	Absolute Maximum Ratings	4	10	Power Supply Recommendations	17
6.2	ESD Ratings	4	11	Layout	18
6.3	Recommended Operating Conditions	4	11.1	Layout Guidelines	18
6.4	Thermal Information	4	11.2	Layout Example	18
6.5	Electrical Characteristics	4	11.3	Thermal Considerations	18
6.6	Switching Characteristics	5	12	器件和文档支持	19
6.7	Typical Characteristics	7	12.1	商标	19
7	Parameter Measurement Information	11	12.2	静电放电警告	19
7.1	Test Circuit and Timing Waveforms Diagrams	11	12.3	Glossary	19
8	Detailed Description	12	13	机械、封装和可订购信息	19
8.1	Overview	12			

4 修订历史记录

日期	修订版本	说明
2020 年 1 月	*	初始发行版。

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input.
2	GND	—	Device ground.
3	ON	I	Active high switch control input. Do not leave floating.
4	NC	—	No connect pin, leave floating.
5	QOD	O	Quick Output Discharge pin. This functionality can be enabled in one of three ways. <ul style="list-style-type: none"> Placing an external resistor between VOUT and QOD Tying QOD directly to VOUT and using the internal resistor value (R_{PD}) Disabling QOD by leaving pin floating See the Fall Time (t_{FALL}) and Quick Output Discharge (QOD) section for more information.
6	VOUT	O	Switch output.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Maximum Input Voltage Range	-0.3	6	V
V _{OUT}	Maximum Output Voltage Range	-0.3	6	V
V _{ON}	Maximum ON Pin Voltage Range	-0.3	6	V
V _{QOD}	Maximum QOD Pin Voltage Range	-0.3	6	V
I _{MAX}	Maximum Continuous Current		1.5	A
I _{PLS}	Maximum Pulsed Current (2 ms, 2% Duty Cycle)		2.5	A
T _J	Junction temperature	Internally Limited		°C
T _{STG}	Storage temperature	-65	150	°C
T _{LEAD}	Maximum Lead Temperature (10 s soldering time)		300	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{IN}	Input Voltage Range	1.6		5.5	V
V _{OUT}	Output Voltage Range	0		5.5	V
V _{IH}	ON Pin High Voltage Range	1		5.5	V
V _{IL}	ON Pin Low Voltage Range	0		0.35	V
T _A	Ambient Temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS22919-Q1	UNIT
		DCK (SC-70)	
		PINS	
R _{θJA}	Junction-to-ambient thermal resistance	214.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	147.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	75.2	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	58.5	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	75.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Typical values at V_{IN} = 3.6V unless otherwise specified

PARAMETER	TEST CONDITIONS	T _J	MIN	TYP	MAX	UNIT
Input Supply (VIN)						

Electrical Characteristics (continued)

Typical values at $V_{IN} = 3.6V$ unless otherwise specified

PARAMETER		TEST CONDITIONS	T_J	MIN	TYP	MAX	UNIT	
$I_{Q, VIN}$	VIN Quiescent Current	$V_{ON} \geq V_{IH}$, $V_{OUT} = \text{Open}$	25°C	8	15		μA	
			-40°C to 125°C			20	μA	
$I_{SD, VIN}$	VIN Shutdown Current	$V_{ON} \leq V_{IL}$, $V_{OUT} = \text{GND}$	25°C	2	20		nA	
			-40°C to 125°C			800	nA	
ON-Resistance (RON)								
R_{ON}	ON-State Resistance	$I_{OUT} = -200 \text{ mA}$	$V_{IN} = 5 \text{ V}$	25°C	89	125	m Ω	
				-40°C to 85°C			150	m Ω
				-40°C to 105°C			175	m Ω
				-40°C to 125°C			200	m Ω
			$V_{IN} = 3.6 \text{ V}$	25°C	90	150	m Ω	
				-40°C to 85°C			200	m Ω
				-40°C to 105°C			225	m Ω
				-40°C to 125°C			250	m Ω
			$V_{IN} = 1.8 \text{ V}$	25°C	105	300	m Ω	
				-40°C to 85°C			330	m Ω
				-40°C to 105°C			340	m Ω
				-40°C to 125°C			350	m Ω
Output Short Protection (ISC)								
I_{SC}	Short Circuit Current Limit	$V_{OUT} \leq V_{IN} - 1.5 \text{ V}$	-40°C to 125°C	3			A	
		$V_{OUT} \leq V_{SC}$	-40°C to 125°C	30	500	900	mA	
V_{SC}	Output Short Detection Threshold	$V_{IN} - V_{OUT}$	-40°C to 125°C	0.3	0.36	0.46	V	
t_{SC}	Output Short Reponse Time	$V_{IN} = 1.6V \text{ to } 5.5V$, 10m Ω short applied	-40°C to 125°C	2			μs	
T_{SD}	Thermal Shutdown		Rising	180			°C	
			Falling	145			°C	
Enable Pin (ON)								
I_{ON}	ON Pin Leakage	$V_{ON} \geq V_{IH}$	-40°C to 125°C			100	nA	
$R_{PD, ON}$	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$	-40°C to 125°C			530	k Ω	
Quick-output Discharge (QOD)								
$R_{PD, QOD}$	QOD Pin Internal Discharge Resistance	$V_{ON} \leq V_{IL}$	-40°C to 125°C			24	Ω	

ADVANCE INFORMATION

6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of $C_L = 0.1 \mu F$, $R_L = 100 \Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	$V_{IN} = 5.0 \text{ V}$		1950	μs
		$V_{IN} = 3.6 \text{ V}$		1750	μs
		$V_{IN} = 1.8 \text{ V}$		1500	μs
t_R	Output Rise Time	$V_{IN} = 5.0 \text{ V}$		1280	μs
		$V_{IN} = 3.6 \text{ V}$		1100	μs
		$V_{IN} = 1.8 \text{ V}$		750	μs
SR_{ON}	Turn ON Slew Rate	$V_{IN} = 5.0 \text{ V}$		3.2	mV/ μs
		$V_{IN} = 3.6 \text{ V}$		2.7	mV/ μs
		$V_{IN} = 1.8 \text{ V}$		1.8	mV/ μs
t_{OFF}	Turn OFF Time	$V_{IN} = 1.8 \text{ V to } 5.0V$	$R_L = 100\Omega$, $C_L = 0.1\mu F$	6	μs

Switching Characteristics (continued)

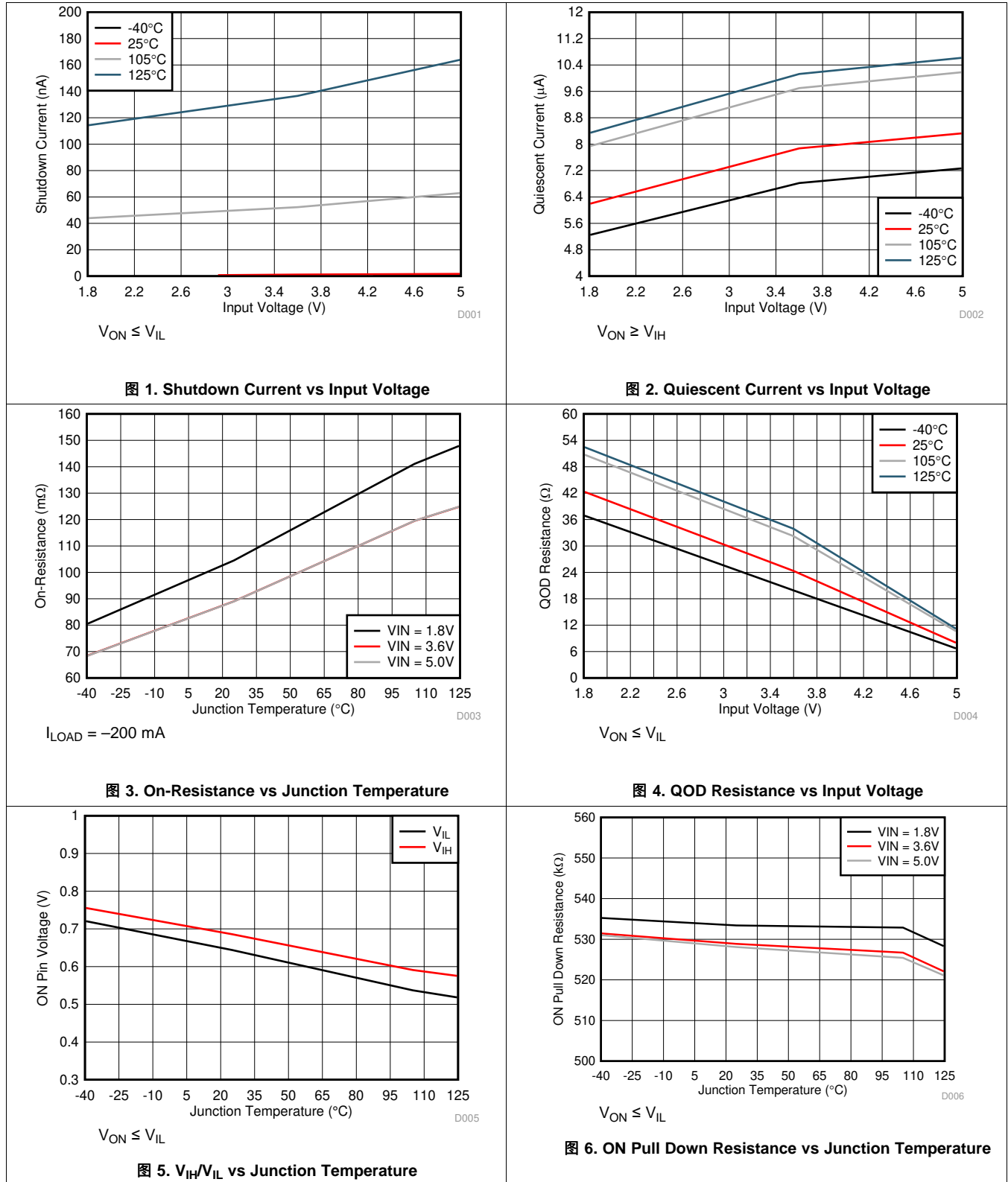
Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.6V, an ambient temperature of 25°C, and a load of $C_L = 0.1 \mu\text{F}$, $R_L = 100 \Omega$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{FALL}	Output Fall Time (1)	$R_L = 100\Omega$	$C_L = 0.1\mu\text{F}$, $R_{\text{QOD}} = \text{Short}$		10		μs
		$R_L = \text{Open}^{(2)}$	$C_L = 10\mu\text{F}$, $R_{\text{QOD}} = \text{Short}$		0.4		ms
			$C_L = 10\mu\text{F}$, $R_{\text{QOD}} = 100 \Omega$		3.5		ms
			$C_L = 100\mu\text{F}$, $R_{\text{QOD}} = \text{Short}$		4		ms

(1) Output may not discharge completely if QOD is not connected to VOUT

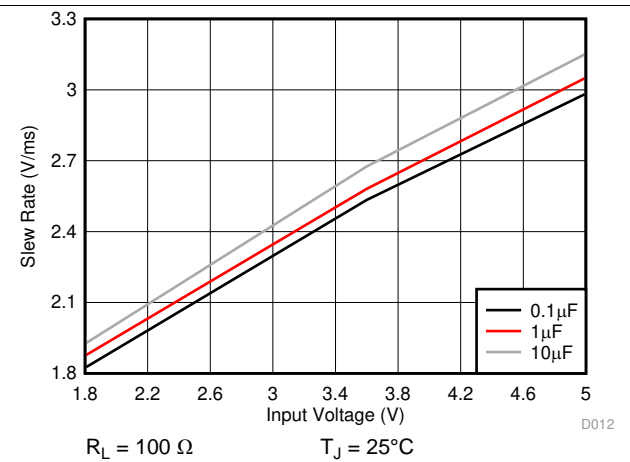
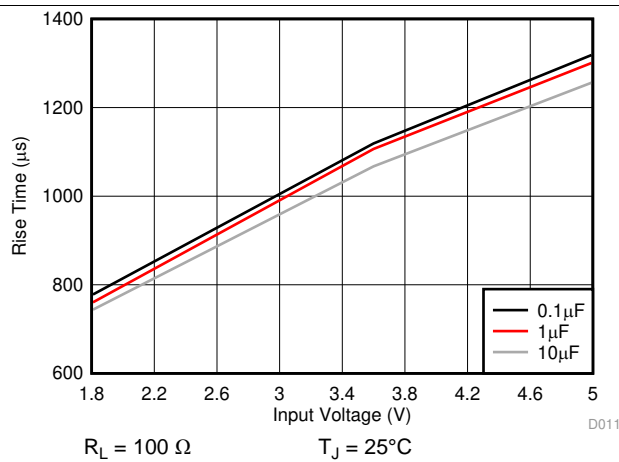
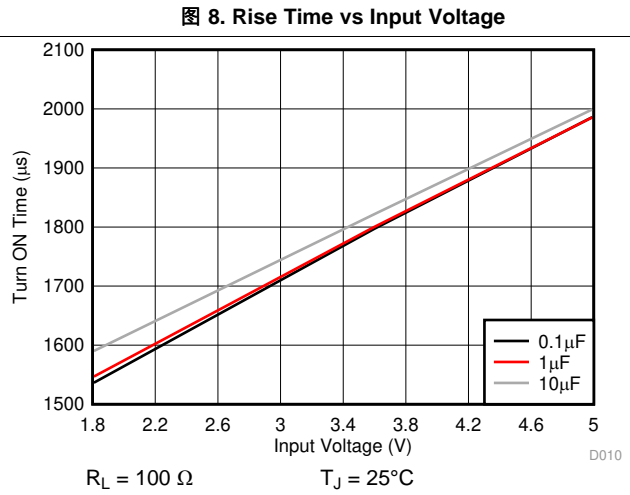
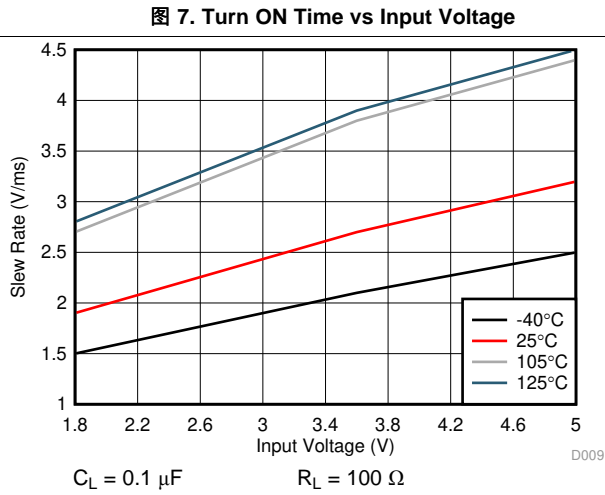
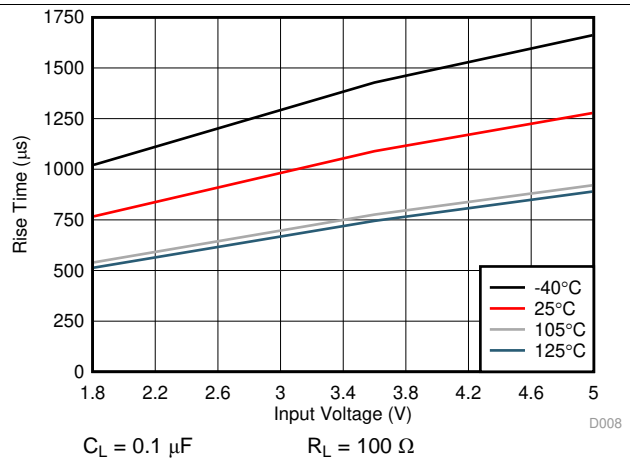
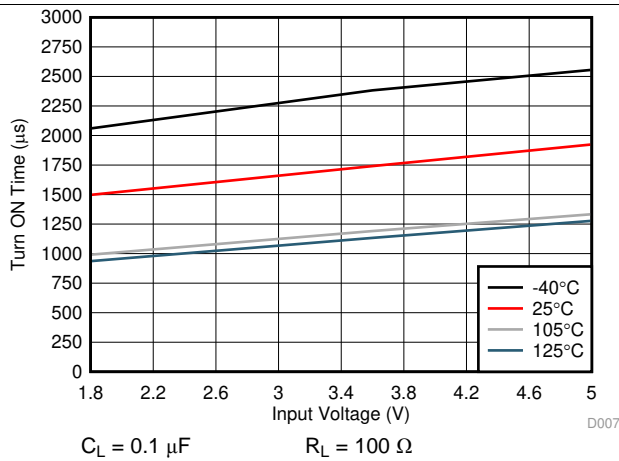
(2) See the *Timing Application* section for information on how R_L and C_L affect Fall Time.

6.7 Typical Characteristics



ADVANCE INFORMATION

Typical Characteristics (接下页)



ADVANCE INFORMATION

Typical Characteristics (接下页)

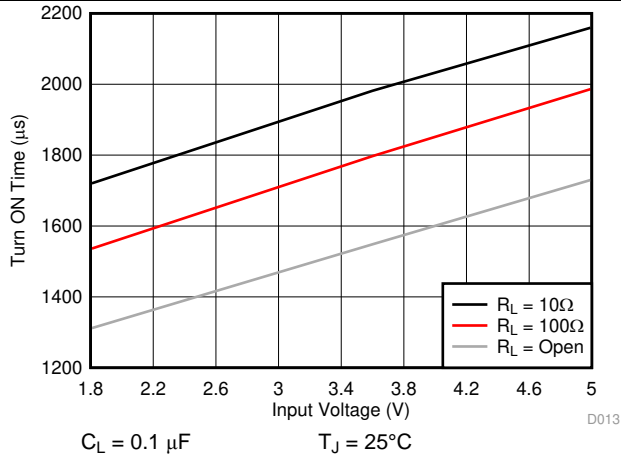


图 13. Turn ON Time vs Input Voltage Across Load Resistance

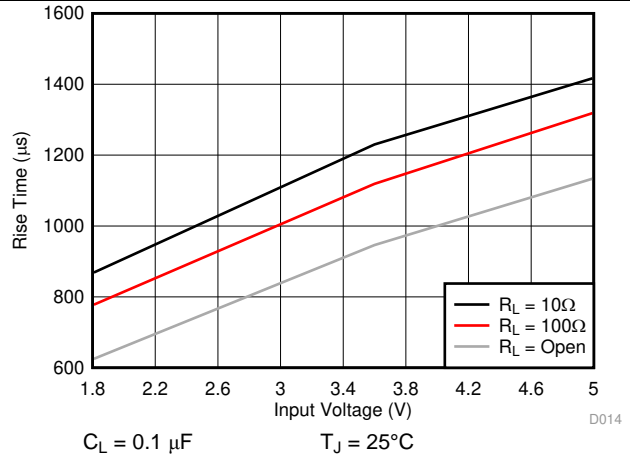


图 14. Rise Time vs Input Voltage Across Load Resistance

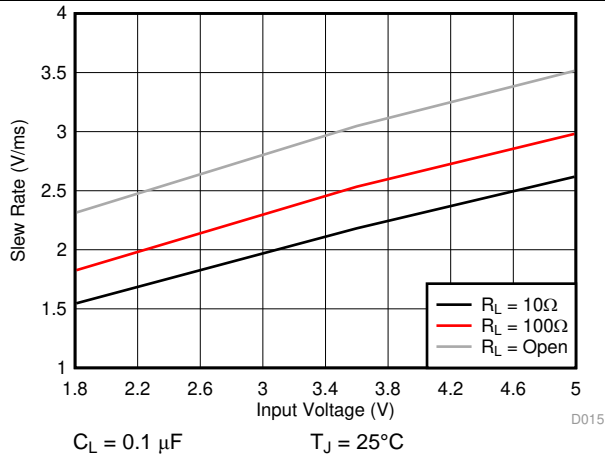


图 15. Output Slew Rate vs Input Voltage Across Load Resistance

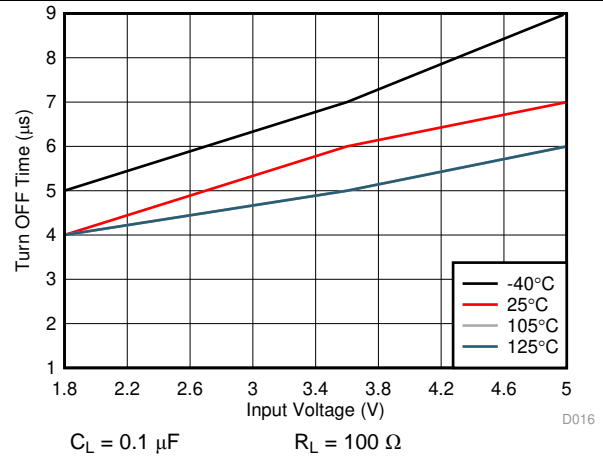


图 16. Turn OFF Time vs Input Voltage

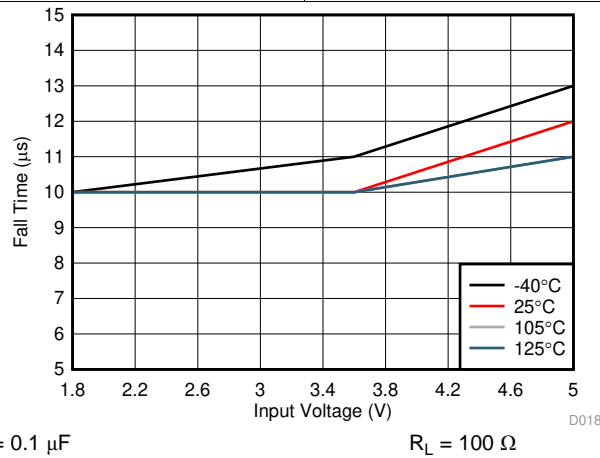


图 17. Fall Time vs Input Voltage

ADVANCE INFORMATION

Typical Characteristics (接下页)

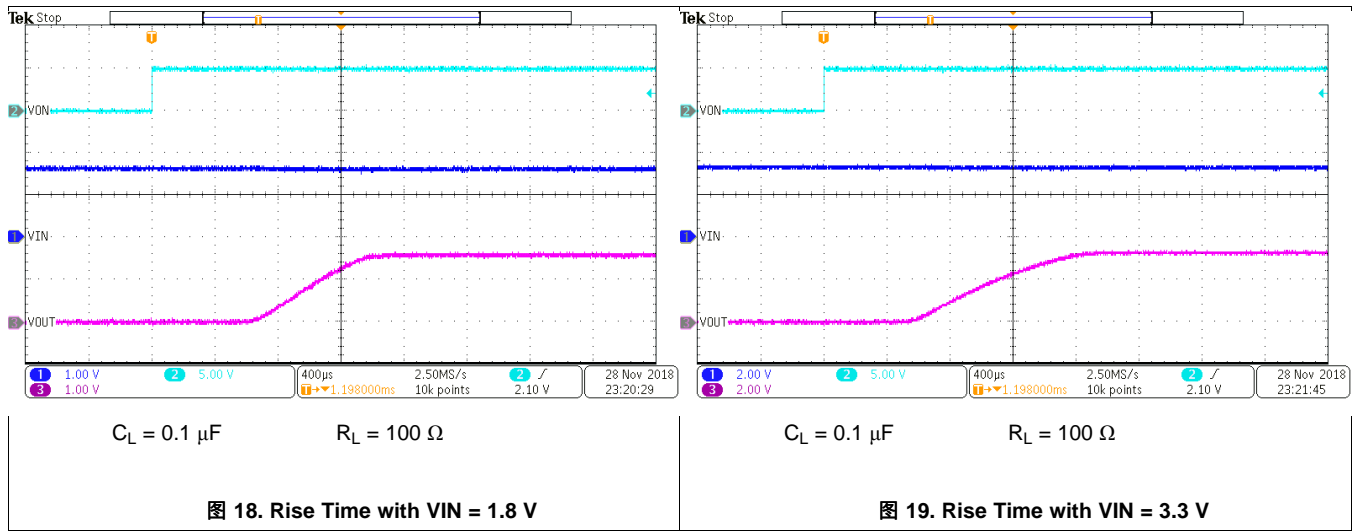


图 18. Rise Time with VIN = 1.8 V

图 19. Rise Time with VIN = 3.3 V

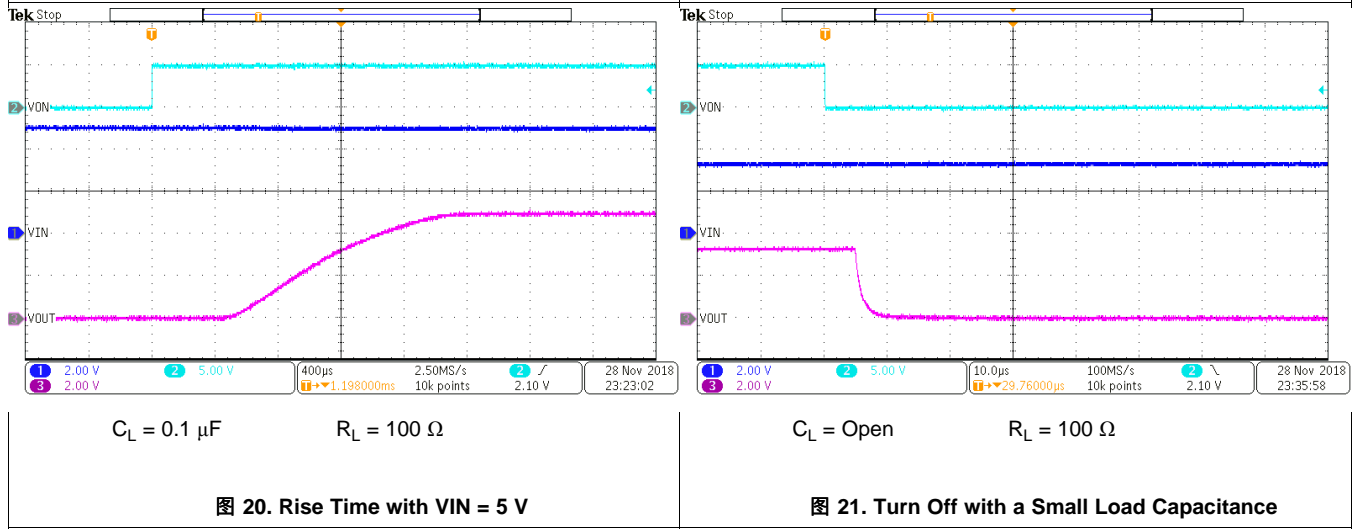


图 20. Rise Time with VIN = 5 V

图 21. Turn Off with a Small Load Capacitance

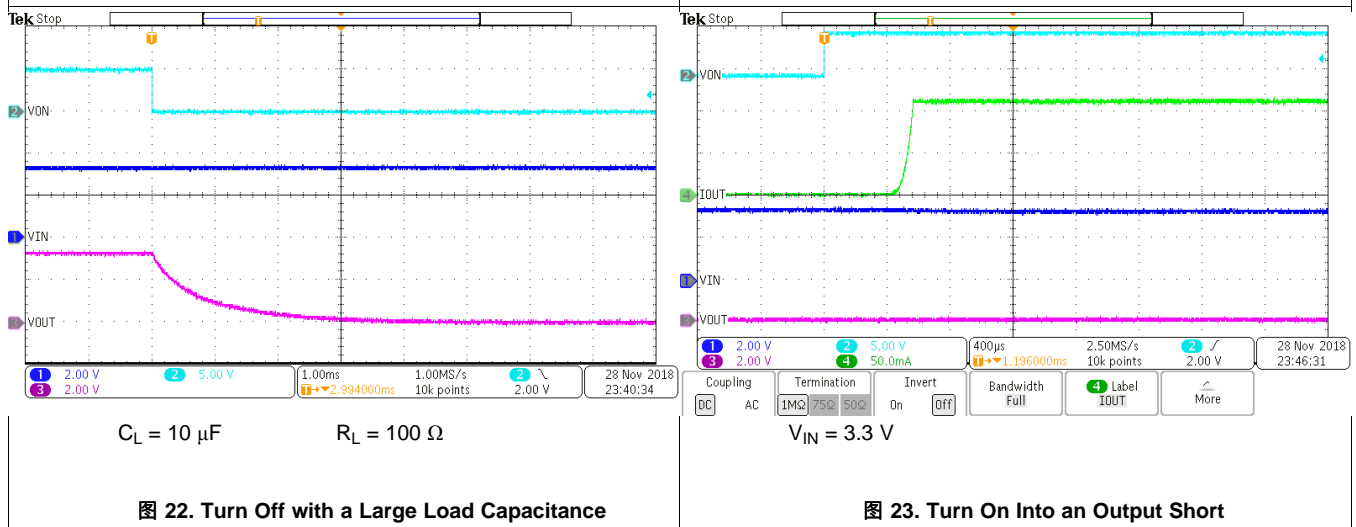
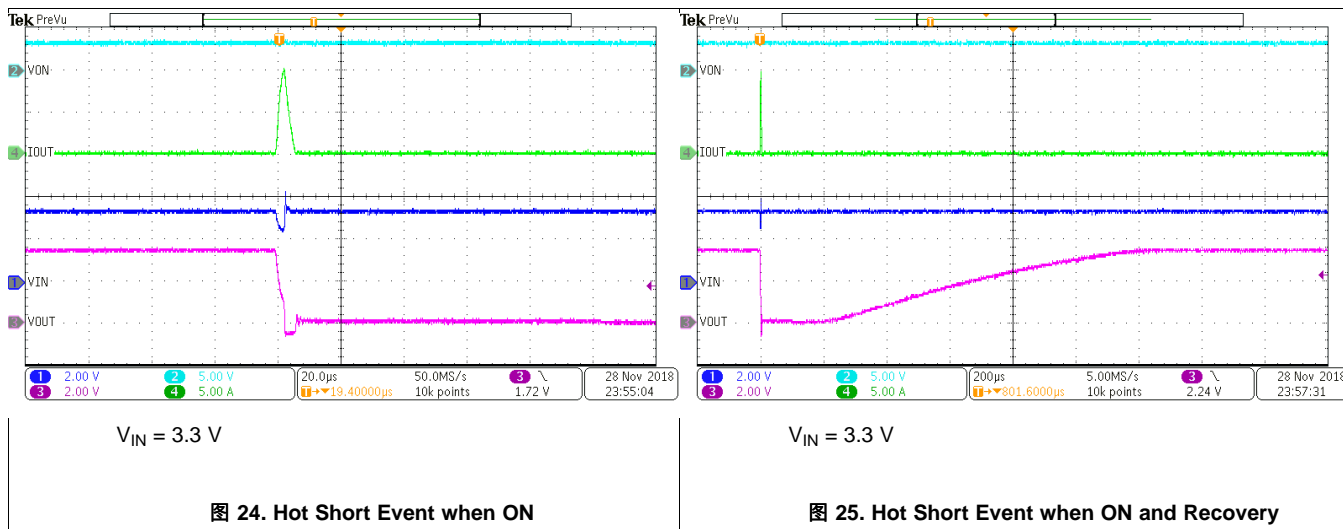


图 22. Turn Off with a Large Load Capacitance

图 23. Turn On Into an Output Short

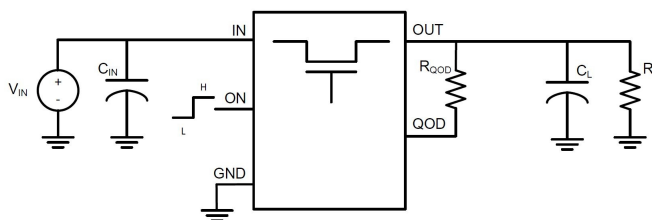
ADVANCE INFORMATION

Typical Characteristics (接下页)



7 Parameter Measurement Information

7.1 Test Circuit and Timing Waveforms Diagrams



- (1) Rise and fall times of the control signal are 100 ns
- (2) Turn-off times and fall times are dependent on the time constant at the load. For the TPS22919-Q1 devices, the internal pull-down resistance QOD is enabled when the switch is disabled. The time constant is $(R_{QOD} + R_{PD,QOD} \parallel R_L) \times C_L$.

图 26. Test Circuit

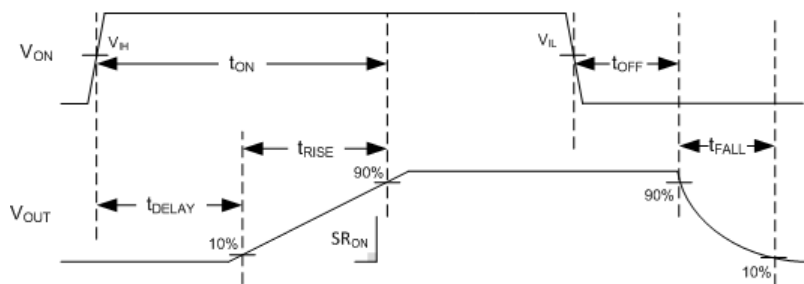


图 27. Timing Waveforms

ADVANCE INFORMATION

8 Detailed Description

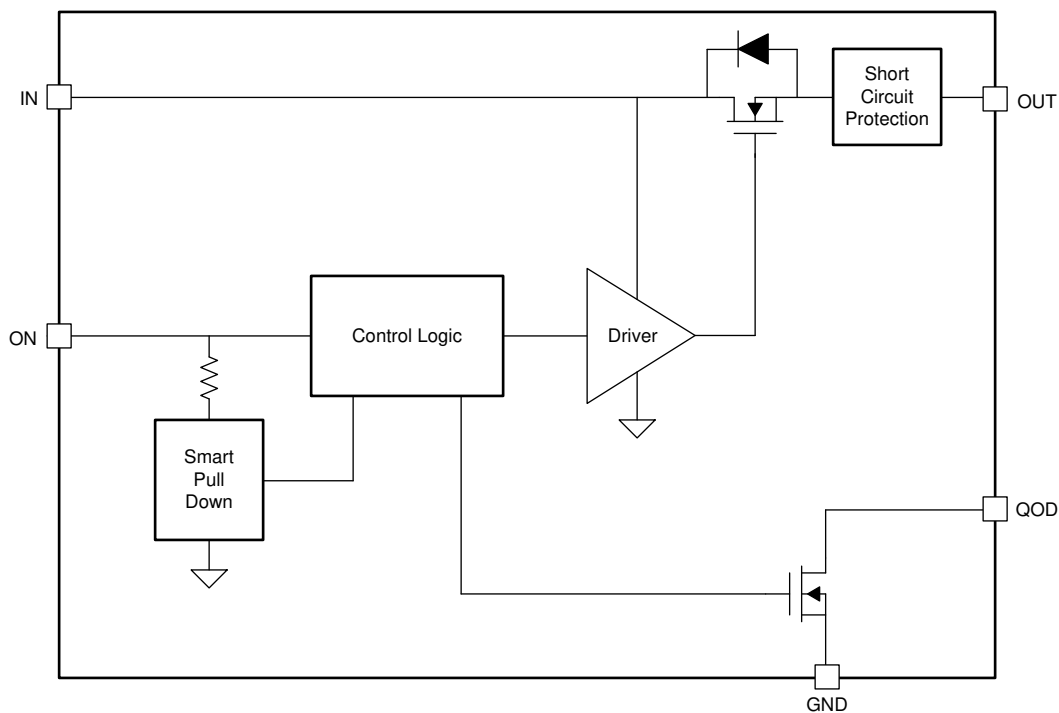
8.1 Overview

The TPS22919-Q1 device is a 5.5-V, 1.5-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET which reduces the drop out voltage across the device.

The TPS22919-Q1 device has a slow slew rate which helps reduce or eliminate power supply droop because of large inrush currents. Furthermore, the device features a QOD pin, which allows the configuration of the discharge rate of VOUT once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components which reduces solution size and bill of materials (BOM) count.

The TPS22919-Q1 load switch is also self-protected, meaning that it will protect itself from short circuit events on the output of the device. It also has thermal shutdown to prevent any damage from overheating.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard GPIO logic threshold so it can be used in a wide variety of applications. When power is first applied to VIN, a Smart Pull Down is used to keep the ON pin from floating until the system sequencing is complete. Once the ON pin is deliberately driven high ($\geq V_{IH}$), the Smart Pull Down is disconnected to prevent unnecessary power loss. See 表 1 when the ON Pin Smart Pull Down is active.

表 1. Smart-ON Pull Down

VON	Pull Down
$\leq V_{IL}$	Connected
$\geq V_{IH}$	Disconnected

8.3.2 Output Short Circuit Protection (I_{SC})

The device will limit current to the output in case of output shorts. When a short occurs, the large VIN to VOUT voltage drop causes the switch to limit the output current (I_{SC}) within (t_{SC}). When the output is below the hard short threshold (V_{SC}), a lower limit is used to minimize the power dissipation while the fault is present. The device will continue to limit the current until it reaches its thermal shutdown temperature. At this time, the device will turn off until its temperature has lowered by the thermal hysteresis (35°C typical) before turning on again.

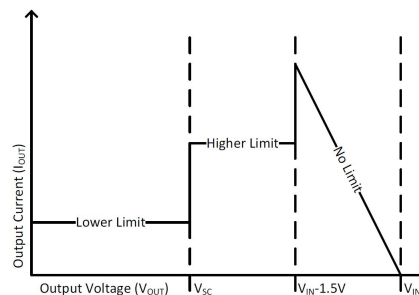


图 28. Output Short Circuit Current Limit

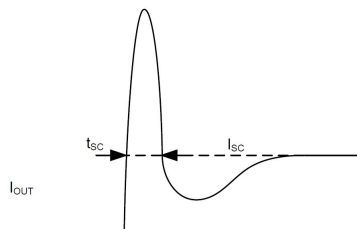


图 29. Output Short Circuit Response

8.3.3 Fall Time (t_{FALL}) and Quick Output Discharge (QOD)

The TPS22919-Q1 device includes a QOD pin that can be configured in one of three ways:

- QOD pin shorted to VOUT pin. Using this method, the discharge rate after the switch becomes disabled is controlled with the value of the internal resistance QOD ($R_{PD,QOD}$).
- QOD pin connected to VOUT pin using an external resistor R_{QOD} . After the switch becomes disabled, the discharge rate is controlled by the value of the total discharge resistance. To adjust the total discharge resistance, 公式 1 can be used:

$$R_{DIS} = R_{PD,QOD} + R_{QOD}$$

Where:

- R_{DIS} = Total output discharge resistance (Ω)

- $R_{PD,QOD}$ = Internal pulldown resistance (Ω)
- R_{QOD} = External resistance placed between the VOUT and QOD pins (Ω) (1)
- QOD pin is unused and left floating. Using this method, there will be no quick output discharge functionality, and the output will remain floating after the switch is disabled.

The fall times of the device depend on many factors including the total discharge resistance (R_{DIS}) and the output capacitance (C_L). To calculate the approximate fall time of V_{OUT} use [公式 2](#).

$$t_{FALL} = 2.2 \times (R_{DIS} \parallel R_L) \times C_L$$

Where:

- t_{FALL} = Output Fall Time from 90% to 10% (μs)
- R_{DIS} = Total QOD + R_{QOD} Resistance (Ω)
- R_L = Output Load Resistance (Ω)
- C_L = Output Load Capacitance (μF) (2)

8.3.3.1 QOD When System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V_{IN} . Past a certain V_{IN} level, the strength of the R_{PD} will be reduced. If there is still remaining charge on the output capacitor, this will result in longer fall times. For further information regarding this condition, see the [Setting Fall Time for Shutdown Power Sequencing](#) section.

8.4 Device Functional Modes

[表 2](#) describes the connection of the VOUT pin depending on the state of the ON pin as well as the various QOD pin configurations.

表 2. VOUT Connection

ON	QOD CONFIGURATION	TPS22919-Q1 VOUT
L	QOD pin connected to VOUT with R_{QOD}	GND ($R_{PD, QOD} + R_{QOD}$)
L	QOD pin tied to VOUT directly	GND ($R_{PD, QOD}$)
L	QOD pin left open	Floating
H	N/A	VIN

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS22919-Q1 devices can be used to power downstream modules.

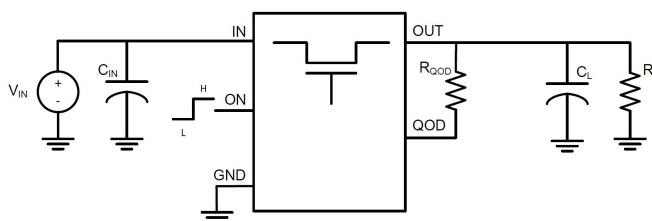


图 30. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in 表 3 as the design parameters:

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	3.6 V
Load Current / Resistance (R_L)	1 k Ω
Load Capacitance (C_L)	47 μ F
Minimum Fall Time (t_F)	40 ms
Maximum Inrush Current (I_{RUSH})	150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use 公式 3 to find the maximum slew rate value to limit inrush current for a given capacitance:

$$(\text{Slew Rate}) = I_{\text{RUSH}} \div C_L$$

where

- I_{INRUSH} = maximum acceptable inrush current (mA)
- C_L = capacitance on VOUT (μF)
- Slew Rate = Output Slew Rate during turn on ($\text{mV}/\mu\text{s}$) (3)

Based on 公式 3, the required slew rate to limit the inrush current to 150 mA is 3.2 $\text{mV}/\mu\text{s}$. The TPS22919-Q1 has a slew rate of 2.3 $\text{mV}/\mu\text{s}$, so the inrush current will be below 150 mA.

9.2.2.2 Setting Fall Time for Shutdown Power Sequencing

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS22919-Q1 device, adding a load switch to each power rail can be used to manage the power down sequencing. To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down.

Once the required fall time is determined, the maximum external discharge resistance (R_{DIS}) value can be found using 公式 2:

$$t_{\text{FALL}} = 2.2 \times (R_{\text{DIS}} \parallel R_L) \times C_L \tag{4}$$

$$R_{\text{DIS}} = 630 \Omega \tag{5}$$

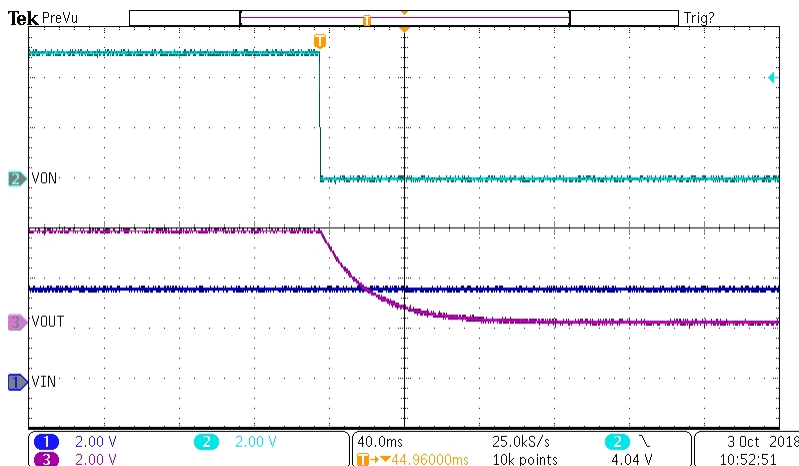
公式 1 can then be used to calculate the R_{QOD} resistance needed to achieve a particular discharge value:

$$R_{\text{DIS}} = \text{QOD} + R_{\text{QOD}} \tag{6}$$

$$R_{\text{QOD}} = 600 \Omega \tag{7}$$

To ensure a fall time greater than, choose an R_{QOD} value greater than 600 Ω .

9.2.2.3 Application Curves



A.

$$C_L = 47\mu\text{F}$$

图 31. Fall Time ($R_{\text{QOD}} = 1 \text{ k}\Omega$)

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.6 V to 5.5 V. The VIN power supply must be well regulated and placed as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 μ F is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

11 Layout

11.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

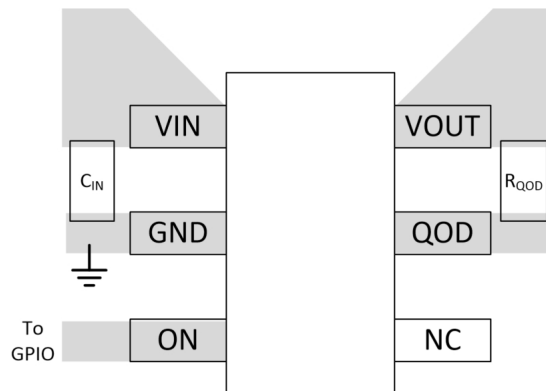


图 32. Recommended Board Layout

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use [公式 8](#):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where

- $P_{D(MAX)}$ = maximum allowable power dissipation
- $T_{J(MAX)}$ = maximum allowable junction temperature (125°C for the TPS22919-Q1 devices)
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. Refer to the Thermal Parameters table. This parameter is highly dependent upon board layout.

(8)

12 器件和文档支持

12.1 商标

All trademarks are the property of their respective owners.

12.2 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

重要声明和免责声明

TI 均以“原样”提供技术性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2020 德州仪器半导体技术（上海）有限公司

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22919QDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1H2	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22919QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22919QDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

重要声明和免责声明

TI 均以“原样”提供技术性及其可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对TI 及其代表造成的损害。

TI 所提供产品均受TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及ti.com.cn上或随附TI产品提供的其他可适用条款的约束。TI提供所述资源并不扩展或以其他方式更改TI 针对TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

Copyright © 2020 德州仪器半导体技术（上海）有限公司