

# SN65DSI84 MIPI® DSI 桥转 FLATLINK™ LVDS

## 单通道 DSI 转双链路 LVDS 桥接器

### 1 特性

- 实现 MIPI® D-PHY 1.00.00 版本的物理层前端和 1.02.00 版本的显示串行接口 (DSI)
- 单通道 DSI 接收器在每个通道上可针对 1 条、2 条、3 条或 4 条 D-PHY 数据信道进行配置，每信道的运行速率高达 1Gbps
- 支持格式为 RGB666 和 RGB888 的 18bpp 和 24bpp DSI 视频数据包
- 适用于 60fps WUXGA 1920 × 1200 分辨率 (18bpp 和 24bpp 彩色) 和 60fps 1366 × 768 (18bpp 和 24bpp)
- Flatlink™ 针对单链路或双链路 LVDS 的输出配置
- 支持单通道 DSI 至双链路 LVDS 运行模式
- 在双链路或单链路模式下，LVDS 输出时钟范围为 25MHz 至 154MHz
- LVDS 像素时钟可采用自由运行持续 D-PHY 时钟或外部基准时钟 (REFCLK)
- 1.8V 主 V<sub>CC</sub> 电源
- 低功耗特性包括关断模式、低 LVDS 输出电压摆幅、共模以及 MIPI 超低功耗状态 (ULPS) 支持
- 针对简化印刷电路板 (PCB) 走线的 LVDS 通道交换 (SWAP)，LVDS 引脚顺序反向特性
- 静电放电 (ESD) 额定值 ±2kV (人体放电模式 (HBM))
- 采用 64 引脚 5mm × 5mm BGA (ZQE) 封装
- 温度范围: -40°C 至 85°C

### 2 应用

- 平板电脑、笔记本电脑、上网本
- 移动因特网设备

### 3 说明

SN65DSI84 DSI 至 FlatLink™ 桥采用了单通道 MIPI® D-PHY 接收器前端配置，此配置在每个通道上具有 4 条信道，每条信道的运行速率为 1Gbps；最大输入带宽为 4Gbps。此桥解码 MIPI® DSI 18bpp RGB666 和 24bpp RGB888 数据包并将已格式化的视频数据流转换为一个运行在频率范围介于 25MHz 至 154MHz 之间的像素时钟上的 FlatLink™ 兼容 LVDS 输出，从而提供一个单链路 LVDS，每条链路具有 4 条数据信道。

SN65DSI84 非常适合于每秒 60 帧的 WUXGA 1920 × 1200 应用，每像素比特位高达 24。该器件实现了部分线路缓冲以适应 DSI 与 LVDS 接口间的数据流不匹配的情况。

SN65DSI84 采用符合工业标准的接口技术设计，能够与多种微处理器兼容，并具有多种电源管理特性，包括低摆幅 LVDS 输出和 MIPI® 定义的超低功耗状态 (ULPS) 支持。

SN65DSI84 采用小外形尺寸的 5x5mm BGA 封装（焊球间距为 0.5mm），工作温度范围为 -40°C 至 85°C。

#### 器件信息<sup>(1)</sup>

器件编号	封装	封装尺寸 (标称值)
SN65DSI84	BGA MICROSTAR JUNIOR (64)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

#### 典型应用



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision F (August 2015) to Revision G	Page
• Deleted figure <i>Shutdown and Reset Timing Definition While V<sub>CC</sub> Is High</i> .....	12
• Changed the paragraph following <a href="#">Figure 8</a> .....	15
• Changed <i>Recommended Initialization Sequence To: Initialization Sequence</i> .....	15
• Changed <a href="#">Table 2</a> .....	15
• Changed item 3 in <i>Video Stop and Restart Sequence</i> From: Drive all DSI input lanes including DSI CLK lane to LP11. To: Drive all DSI data lanes to LP11, but keep the DSI CLK lanes in HS. ....	33

Changes from Revision E (October 2013) to Revision F	Page
• 已添加 添加了引脚配置和功能 部分、ESD 额定值表、特性 说明 部分， 器件功能模式， 应用和实施部分， 电源相关建议部分， 布局部分， 器件和文档支持部分以及机械、封装和可订购信息部分 .....	1
• Changed ULPS Itemized List, item 3 from "Wait for the PLL_LOCK bit (CSR 0x0A.7) to be set" to "Wait for a minimum of 3 ms." .....	14
• Changed Initialization Sequence Description for Init seq7 from "Wait for the PLL_LOCK bit to be set (CSR 0x0A.7)" to "Wait for a minimum of 3 ms." .....	15
• Changed <a href="#">Table 6</a> Address 0x0A, Bit 7 description from "PLL_LOCK" to "PLL_EN_STAT" .....	24
• Changed Address 0x18, Bits 3, 2, 1, and 0 Descriptions in <a href="#">Table 8</a> for clarification. ....	26
• Changed Item 1 of the Video STOP and Restart sequence from "Clear the PLL_EN bit to 0(CSR 0x0A.7)" to "Clear the PLL_EN bit to 0 (CSR 0x0D.0)" .....	33

Changes from Revision D (August 2013) to Revision E	Page
• Added rows for Bits 7, and 6:5 to CSR Bit Field Definition – DSI Registers .....	25

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- 对齐了 整篇产品说明书的 封装说明。 ..... 1
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**Changes from Revision A (December 2012) to Revision B** **Page**


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- 将 PGBA 更改为 PBGA ..... 1
- 

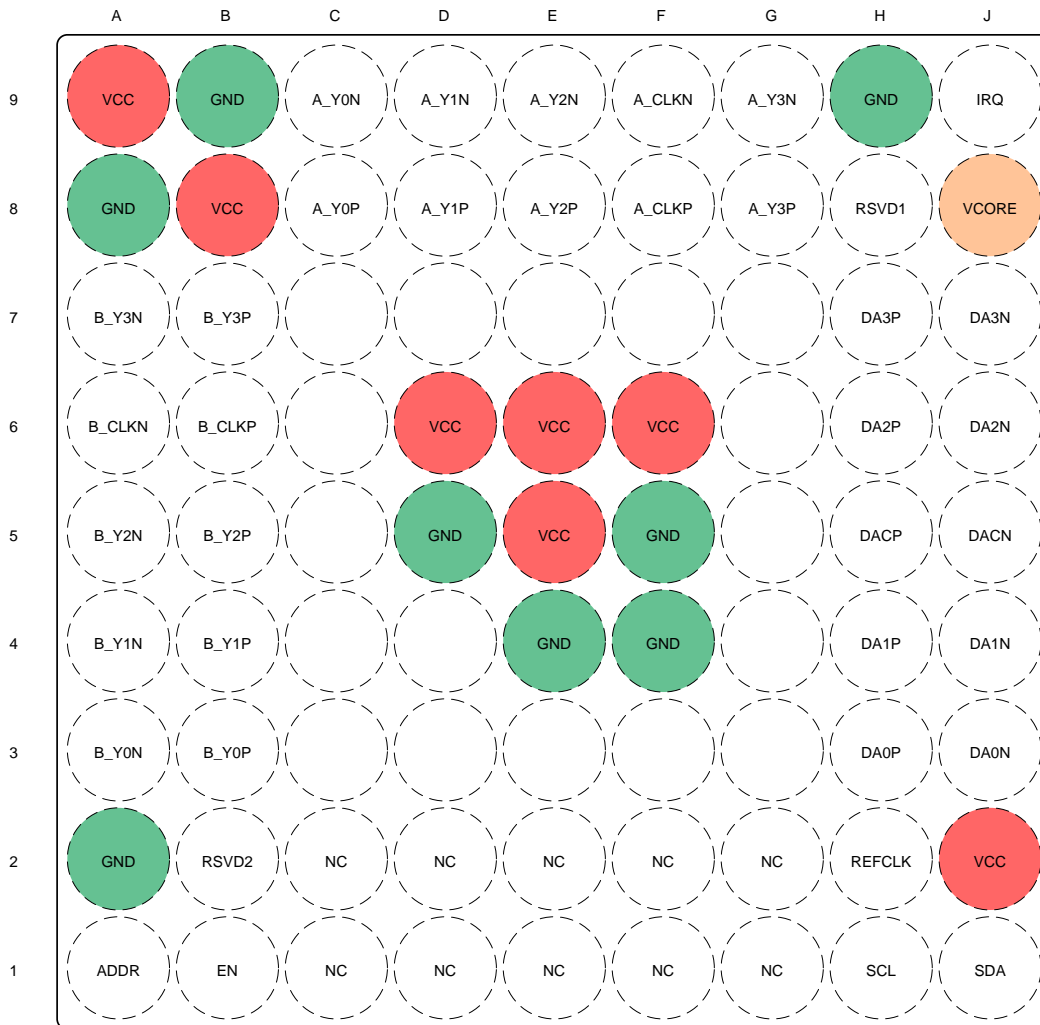
**Changes from Original (August 2012) to Revision A** **Page**


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- Changed the value of  $V_{OH}$  From: 1.3 MIN To: 1.25 MIN ..... 8
  - Changed the  $I_{CC}$  TYP value From: 125 To: 106 and MAX value From: 200 To: 150 ..... 8
  - Added a TYP value of 7.7 to  $I_{ULPS}$  ..... 8
  - Changed the  $I_{RST}$  TYP value From: 0.05 To: 0.04 and MAX value From: 0.2 To: 0.06 ..... 8
  - Changed table note 2 ..... 8
  - changed the values of  $|VOD|$  ..... 9
  - Changed the values of  $V_{OC(SS)}$  for test conditions CSR 0x19.6 = 0 and, or CSR 0x19.4 = 0 ..... 9
  - Added table note 3 ..... 9
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  - Changed the description of CHA\_LVDS\_VOD\_SWING ..... 27
  - Changed the description of CHB\_LVDS\_VOD\_SWING ..... 27
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## 5 Pin Configuration and Functions

**ZQE Package  
64-Pin (Bump) BGA MICROSTAR JUNIOR  
Top View**



Not to scale

To minimize the power supply noise floor, provide good decoupling near the SN65DSI84 power pins. The use of four ceramic capacitors (2x 0.1  $\mu$ F and 2x 0.01  $\mu$ F) provides good performance. At the least, it is recommended to install one 0.1  $\mu$ F and one 0.01  $\mu$ F capacitor near the SN65DSI84. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized. Placing the capacitor underneath the SN65DSI84 on the bottom of the PCB is often a good choice.

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DA0P	H3	LVDS Input (HS) CMOS Input (LS) (Failsafe)	MIPI® D-PHY Channel A Data Lane 0; data rate up to 1 Gbps.
DA0N	J3		
DA1P	H4		MIPI® D-PHY Channel A Data Lane 1; data rate up to 1 Gbps.
DA1N	J4		
DA2P	H6		MIPI® D-PHY Channel A Data Lane 2; data rate up to 1 Gbps.
DA2N	J6		
DA3P	H7		MIPI® D-PHY Channel A Data Lane 3; data rate up to 1 Gbps.
DA3N	J7		
DACP	H5		MIPI® D-PHY Channel A Clock Lane; operates up to 500 MHz.
DACN	J5		
NC	C2, C1, D2, D1, F2, F1, G2, G1, E2, E1	No connects.	These pins should not be connected to any signal, power or ground.
A_Y0P	C8	LVDS Output	FlatLink™ Channel A LVDS Data Output 0.
A_Y0N	C9		
A_Y1P	D8		FlatLink™ Channel A LVDS Data Output 1.
A_Y1N	D9		
A_Y2P	E8		FlatLink™ Channel A LVDS Data Output 2.
A_Y2N	E9		
A_Y3P	G8		FlatLink™ Channel A LVDS Data Output 3. A_Y3P and A_Y3N shall be left NC for 18 bpp panels.
A_Y3N	G9		
A_CLKP	F8		FlatLink™ Channel A LVDS Clock
A_CLKN	F9		
B_Y0P	B3		FlatLink™ Channel B LVDS Data Output 0.
B_Y0N	A3		
B_Y1P	B4		FlatLink™ Channel B LVDS Data Output 1.
B_Y1N	A4		
B_Y2P	B5		FlatLink™ Channel B LVDS Data Output 2.
B_Y2N	A5		
B_Y3P	B7		FlatLink™ Channel B LVDS Data Output 3. B_Y3P and B_Y3N shall be left NC for 18 bpp panels.
B_Y3N	A7		
B_CLKP	B6		FlatLink™ Channel B LVDS Clock.
B_CLKN	A6		
RSVD1	H8	CMOS Input/Output with pulldown	Reserved. This pin should be left unconnected for normal operation.
RSVD2	B2	CMOS Input with pulldown	Reserved. This pin should be left unconnected for normal operation.
ADDR	A1	CMOS Input/Output	Local I <sup>2</sup> C Interface Target Address Select. See Table 4. In normal operation this pin is an input. When the ADDR pin is programmed high, it should be tied to the same 1.8 V power rails where the SN65DSI84 VCC 1.8 V power rail is connected.
EN	B1	CMOS Input with pullup (Failsafe)	Chip Enable and Reset. Device is reset (shutdown) when EN is low.
REFCLK	H2	CMOS Input (Failsafe)	Optional External Reference Clock for LVDS Pixel Clock. If an External Reference Clock is not used, this pin should be pulled to GND with an external resistor. The source of the reference clock should be placed as close as possible with a series resistor near the source to reduce EMI.
SCL	H1		Local I <sup>2</sup> C Interface Clock.
SDA	J1	Open Drain Input/Output (Failsafe)	Local I <sup>2</sup> C Interface Bi-directional Data Signal.
IRQ	J9	CMOS Output	Interrupt Signal.

**Pin Functions (continued)**

PIN			DESCRIPTION
NAME	NO.	I/O	
GND	A2, A8, B9, D5, E4, F4, F5, H9	Power Supply	Reference Ground.
VCC	A9, B8, D6, E5, E6, F6, J2		1.8 V Power Supply.
VCORE	J8		1.1 V Output from Voltage Regulator. This pin must have a 1 $\mu$ F external capacitor to GND.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Supply Voltage	V <sub>CC</sub>	-0.3	2.175	V
Input Voltage	CMOS Input Terminals	-0.5	2.175	V
	DSI Input Terminals (DA x P/N, DB x P/N)	-0.4	1.4	V
Storage Temperature T <sub>stg</sub>		-65	105	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 EDS Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±200	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	VCC Power supply	165	18	195	V
V <sub>PSN</sub>	Supply noise on any V <sub>CC</sub> pin	f <sub>(noise)</sub> > 1MHz		0.05	V
T <sub>A</sub>	Operating free-air temperature	-40		85	°C
T <sub>CASE</sub>	Case temperature			92.2	°C
V <sub>DSI_PIN</sub>	DSI input pin voltage range	-50		1350	mV
f <sub>(I2C)</sub>	Local I <sup>2</sup> C input frequency			400	kHz
f <sub>HS_CLK</sub>	DSI HS clock input frequency	40		500	MHz
t <sub>setup</sub>	DSI HS data to clock setup time		0.15		UI <sup>(1)</sup>
t <sub>hold</sub>	DSI HS data to clock hold time; see <a href="#">Figure 4</a>	0.15			
Z <sub>L</sub>	LVDS output differential impedance	90		132	Ω

(1) The unit interval (UI) is one half of the period of the HS clock; at 500 MHz the minimum setup and hold time is 150 ps.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN65DSI84	UNIT
		ZQE (BGA MICROSTAR JUNIOR)	
		64 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	72.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	35.7	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	35.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	36.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IL</sub>	Low-level control signal input voltage				0.3 x V <sub>CC</sub>	V
V <sub>IH</sub>	High-level control signal input voltage		0.7 x V <sub>CC</sub>			V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -4 mA	1.25			V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 4 mA			0.4	V
I <sub>LKG</sub>	Input failsafe leakage current	V <sub>CC</sub> = 0; V <sub>CC(PIN)</sub> = 1.8 V			±30	μA
I <sub>IH</sub>	High level input current	Any input terminal			±30	μA
I <sub>IL</sub>	Low level input current	Any input terminal			±30	μA
I <sub>OZ</sub>	High-impedance output current	Any output terminal			±10	μA
I <sub>OS</sub>	Short-circuit output current	Any output driving GND short			±20	mA
I <sub>CC</sub>	Device active current	see <sup>(2)</sup>		106	150	mA
I <sub>ULPS</sub>	Device standby current	All data and clock lanes are in ultra-low power state (ULPS)		7.7	10	mA
I <sub>RST</sub>	Shutdown current	EN = 0		0.04	0.06	mA
R <sub>EN</sub>	EN control input resistor			200		kΩ
<b>MIPI DSI INTERFACE</b>						
V <sub>IH-LP</sub>	LP receiver input high threshold	See Figure 1	880			mV
V <sub>IL-LP</sub>	LP receiver input low threshold	See Figure 1			550	mV
V <sub>ID</sub>	HS differential input voltage		70		270	mV
V <sub>IDT</sub>	HS differential input voltage threshold				50	mV
V <sub>IL-ULPS</sub>	LP receiver input low threshold; ultra-low power state (ULPS)				300	mV
V <sub>CM-HS</sub>	HS common mode voltage; steady-state		70		330	mV
ΔV <sub>CM-HS</sub>	HS common mode peak-to-peak variation including symbol delta and interference				100	mV
V <sub>IH-HS</sub>	HS single-ended input high voltage	See Figure 1			460	mV
V <sub>IL-HS</sub>	HS single-ended input low voltage	See Figure 1	-40			mV
V <sub>TERM-EN</sub>	HS termination enable; single-ended input voltage (both Dp AND Dn apply to enable)	Termination is switched simultaneous for Dn and Dp			450	mV
R <sub>DIFF-HS</sub>	HS mode differential input impedance		80		125	Ω

- (1) All typical values are at V<sub>CC</sub> = 1.8 V and T<sub>A</sub> = 25°C
- (2) SN65DSI84: SINGLE Channel DSI to DUAL Channel LVDS, 1440 x 900
- (a) number of LVDS lanes = 2 x (3 data lanes + 1 CLK lane)
  - (b) number of DSI lanes = 2 data lanes + 1 CLK lane
  - (c) LVDS CLK OUT = 53.25 M
  - (d) DSI CLK = 500 M
  - (e) RGB888, LVDS18bpp
- Maximum values are at V<sub>CC</sub> = 1.95 V and T<sub>A</sub> = 85°C



## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
<b>FLATLINK LVDS OUTPUT</b>						
V <sub>od</sub>	Steady-state differential output voltage for A_Y x P/N and B_Y x P/N	CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00; 100 Ω near end termination	180	245	313	mV
		CSR 0x19.3:2=01 and/or CSR 0x19.1:0=01; 100 Ω near end termination	215	293	372	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10; 100 Ω near end termination	250	341	430	
		CSR 0x19.3:2=11 and/or CSR 0x19.1:0=11; 100 Ω near end termination	290	389	488	
		CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00; 200 Ω near end termination	150	204	261	
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01; 200 Ω near end termination	200	271	346	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10; 200 Ω near end termination	250	337	428	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11; 200 Ω near end termination	300	402	511	
	Steady-state differential output voltage for A_CLKP/N and B_CLKP/N	CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 100 Ω near end termination	140	191	244	mV
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 100 Ω near end termination	168	229	290	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 100 Ω near end termination	195	266	335	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 100 Ω near end termination	226	303	381	
		CSR 0x19.3:2=00 and, or CSR 0x19.1:0=00 200 Ω near end termination	117	159	204	
		CSR 0x19.3:2=01 and, or CSR 0x19.1:0=01 200 Ω near end termination	156	211	270	
		CSR 0x19.3:2=10 and, or CSR 0x19.1:0=10 200 Ω near end termination	195	263	334	
		CSR 0x19.3:2=11 and, or CSR 0x19.1:0=11 200 Ω near end termination	234	314	399	
Δ V <sub>od</sub>	Change in steady-state differential output voltage between opposite binary states	RL = 100 Ω		35	mV	
V <sub>OC(SS)</sub>	Steady state common-mode output voltage <sup>(3)</sup>	CSR 0x19.6 = 1 and CSR 0x1B.6 = 1; and, or CSR 0x19.4 = 1 and CSR 0x1B.4 = 1; see <a href="#">Figure 2</a>	0.8	0.9	1	V
		CSR 0x19.6 = 0 and, or CSR 0x19.4 = 0; see <a href="#">Figure 2</a>	1.15	1.25	1.35	
V <sub>OC(PP)</sub>	Peak-to-peak common-mode output voltage	see <a href="#">Figure 2</a>		35	mV	
R <sub>LVDS_DIS</sub>	Pull-down resistance for disabled LVDS outputs		1		kΩ	

(3) Tested at V<sub>CC</sub> = 1.8 V, T<sub>A</sub> = -40°C for MIN, T<sub>A</sub> = 25°C for TYP, T<sub>A</sub> = 85°C for MAX.

## 6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>DSI</b>						
$t_{GS}$	DSI LP glitch suppression pulse width				300	ps
<b>LVDS</b>						
$t_c$	Output clock period		6.49		40	ns
$t_w$	High-level output clock (CLK) pulse duration		4/7 $t_c$			ns
$t_0$	Delay time, CLK $\uparrow$ to 1st serial bit position	$t_c = 6.49\text{ns}$ ; Input clock jitter < 25ps (REFCLK)	-0.15		0.15	ns
$t_1$	Delay time, CLK $\uparrow$ to 2nd serial bit position		1/7 $t_c - 0.15$		1/7 $t_c + 0.15$	ns
$t_2$	Delay time, CLK $\uparrow$ to 3rd serial bit position		2/7 $t_c - 0.15$		2/7 $t_c + 0.15$	ns
$t_3$	Delay time, CLK $\uparrow$ to 4th serial bit position		3/7 $t_c - 0.15$		3/7 $t_c + 0.15$	ns
$t_4$	Delay time, CLK $\uparrow$ to 5th serial bit position		4/7 $t_c - 0.15$		4/7 $t_c + 0.15$	ns
$t_5$	Delay time, CLK $\uparrow$ to 6th serial bit position		5/7 $t_c - 0.15$		5/7 $t_c + 0.15$	ns
$t_6$	Delay time, CLK $\uparrow$ to 7th serial bit position		6/7 $t_c - 0.15$		6/7 $t_c + 0.15$	ns
$t_r$	Differential output rise-time	See <a href="#">Figure 5</a>	180		500	ps
$t_f$	Differential output fall-time					
<b>EN, ULPS, RESET</b>						
$t_{en}$	Enable time from EN or ULPS	$t_{c(o)} = 12.9\text{ ns}$			1	ms
$t_{dis}$	Disable time to standby				0.1	
$t_{reset}$	Reset time		10			ms
<b>REFCLK</b>						
$F_{REFCLK}$	REFCLK Frequency. Supported frequencies: 25 MHz-154 MHz		25		154	MHz
$t_r, t_f$	REFCLK rise and fall time		100 ps		1ns	s
$t_{pj}$	REFCLK Peak-to-Peak Phase Jitter				50	ps
Duty	REFCLK Duty Cycle		40%	50%	60%	
<b>REFCLK or DSI CLK (DACP/N, DBCP/N)</b>						
SSC_CLKIN	SSC enabled Input CLK center spread depth <sup>(2)</sup>		0.5%	1%	2%	
	Modulation Frequency Range		30		60	KHz

 (1) All typical values are at  $V_{CC} = 1.8\text{ V}$  and  $T_A = 25^\circ\text{C}$ 

(2) For EMI reduction purpose, SN65DSI84 supports the center spreading of the LVDS CLK output through the REFCLK or DSI CLK input. The center spread CLK input to the REFCLK or DSI CLK is passed through to the LVDS CLK output A\_CLKP/N and/or B\_CLKP/N.

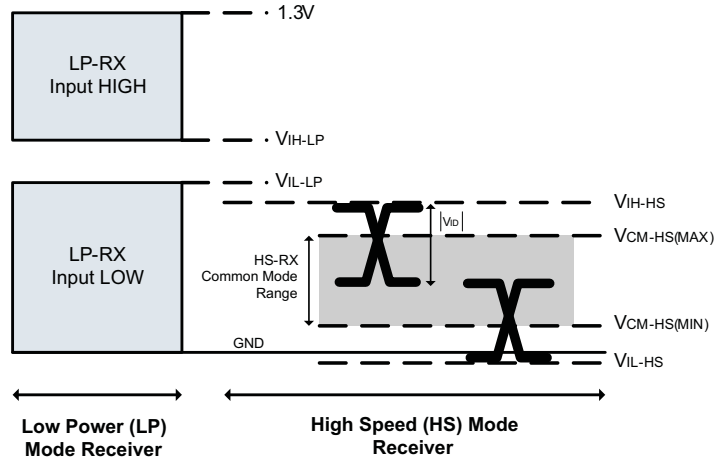


Figure 1. DSI Receiver Voltage Definitions

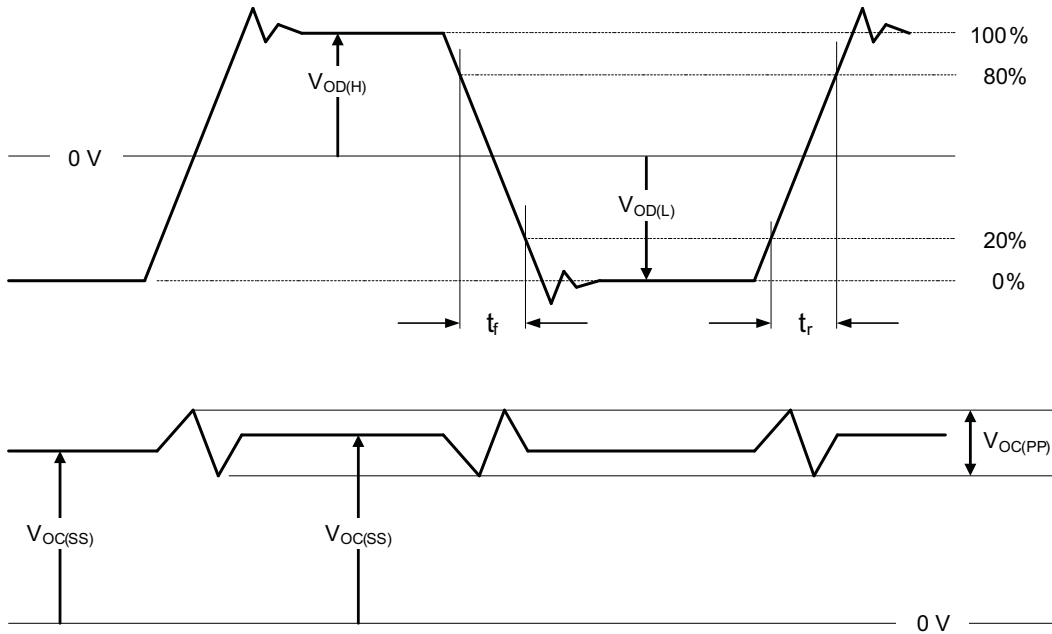
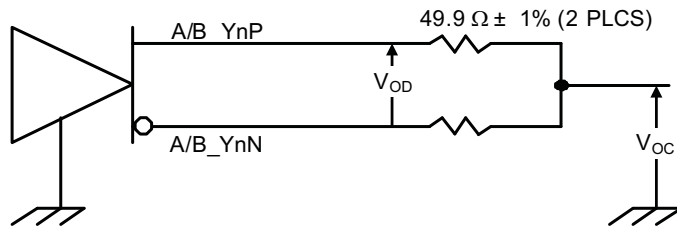
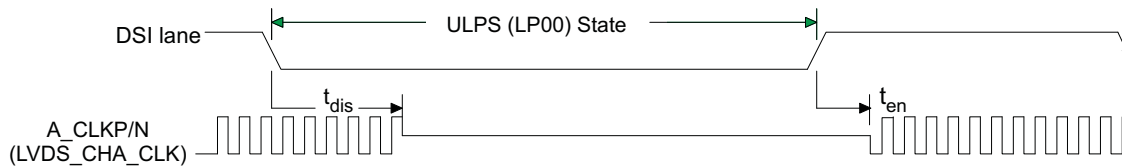
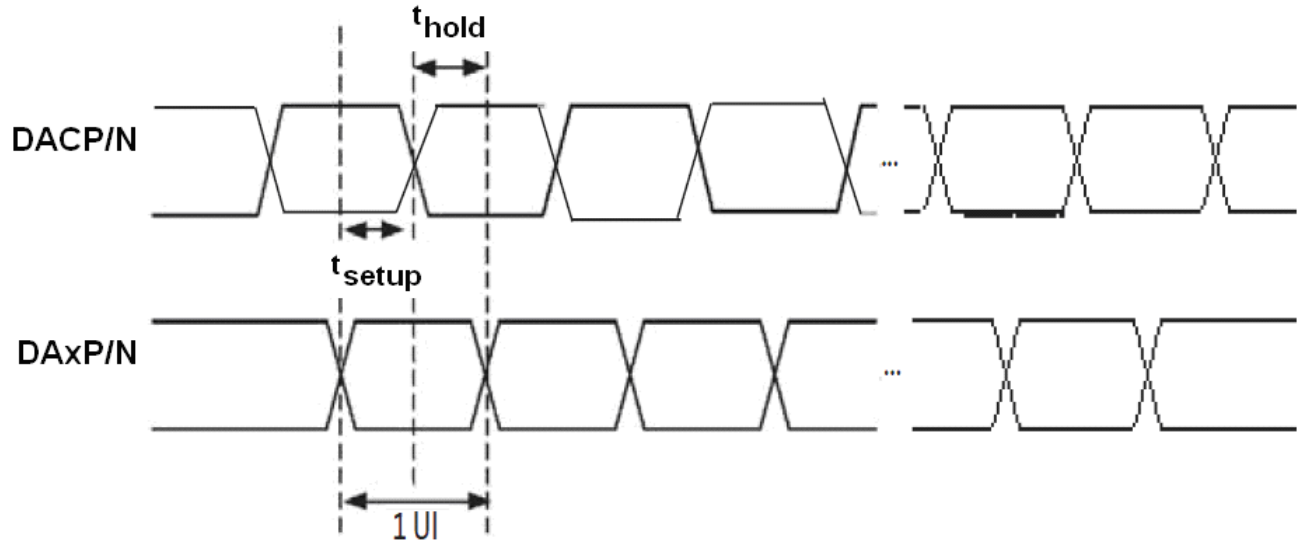


Figure 2. Test Load and Voltage Definitions for Flatlink Outputs

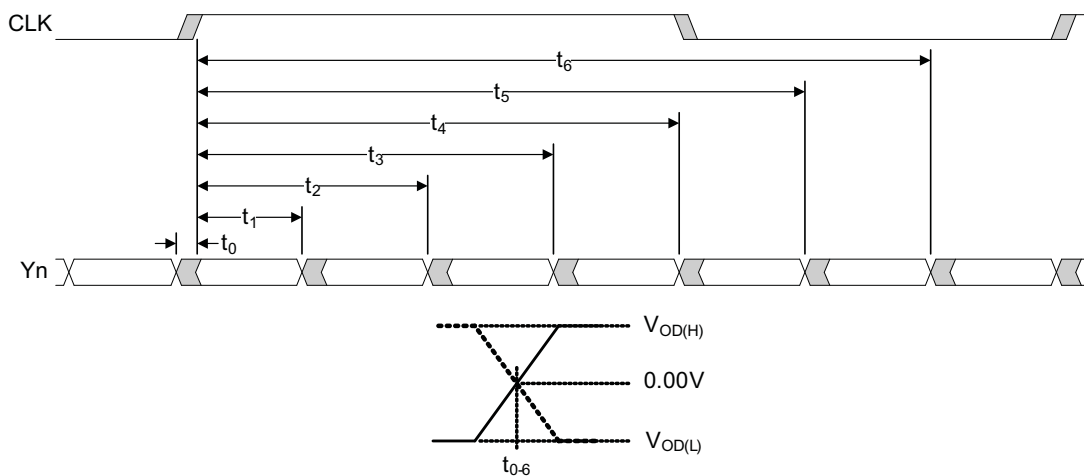


- (1) See the **ULPS** section of the data sheet for the ULPS entry and exit sequence.
- (2) ULPS entry and exit protocol and timing requirements must be met per MIPI® DPHY specification.

**Figure 3. ULPS Timing Definition**



**Figure 4. DSI HS Mode Receiver Timing Definitions**



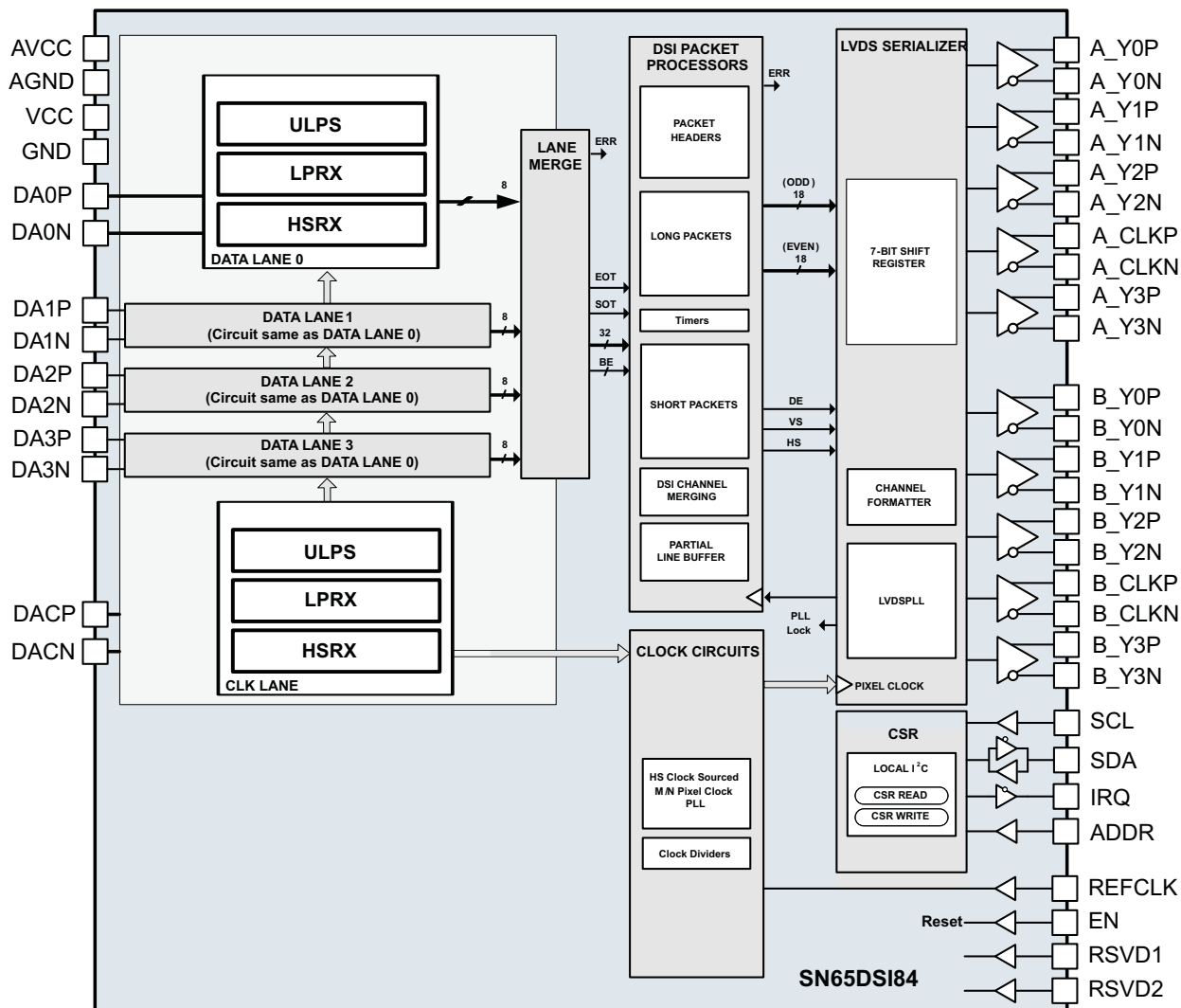
**Figure 5. SN65DSI84 Flatlink Timing Definitions**

## 7 Detailed Description

### 7.1 Overview

The SN65DSI84 DSI to FlatLink bridge features a single channel MIPI D-PHY receiver front-end configuration with 4 lanes per channel operating at 1 Gbps per lane; a maximum input bandwidth of 4 Gbps. The bridge decodes MIPI DSI 18bpp RGB666 and 240bpp RG888 packets and converts the formatted video data stream to a FlatLink compatible LVDS output operating at pixel clocks operating from 25 MHz to 154 MHz, offering a Dual-Link LVDS, Single-Link LVDS interface with four data lanes per link.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Clock Configurations and Multipliers

The FlatLink™ LVDS clock may be derived from the DSI channel A clock, or from an external reference clock source. When the MIPI® D-PHY channel A HS clock is used as the LVDS clock source, the D-PHY clock lane must operate in HS free-running (continuous) mode; this feature eliminates the need for an external reference clock reducing system costs

The reference clock source is selected by HS\_CLK\_SRC (CSR 0x0A.0) programmed through the local I<sup>2</sup>C interface. If an external reference clock is selected, it is multiplied by the factor in REFCLK\_MULTIPLIER (CSR 0x0B.1:0) to generate the FlatLink™ LVDS output clock. When an external reference clock is selected, it must be between 25 MHz and 154 MHz. If the DSI channel A clock is selected, it is divided by the factor in DSI\_CLK\_DIVIDER (CSR 0x0B.7:3) to generate the FlatLink™ LVDS output clock. Additionally, LVDS\_CLK\_RANGE (CSR 0x0A.3:1) and CH\_DSI\_CLK\_RANGE(CSR 0x12) must be set to the frequency range of the FlatLink™ LVDS output clock for and DSI Channel A input clock respectively the internal PLL to operate correctly. After these settings are programmed, PLL\_EN (CSR 0x0D.0) must be set to enable the internal PLL.

### 7.3.2 ULPS

The SN65DSI84 supports the MIPI defined ultra-low power state (ULPS). While the device is in the ULPS, the CSR registers are accessible via I2C interface. ULPS sequence should be issued to all active DSI CLK and/or DSI data lanes of the enabled DSI Channels for the SN65DSI84 enter the ULPS. The Following sequence should be followed to enter and exit the ULPS.

1. Host issues a ULPS entry sequence to all DSI CLK and data lanes enabled.
2. When host is ready to exit the ULPS mode, host issues a ULPS exit sequence to all DSI CLK and data lanes that need to be active in normal operation.
3. Wait for a minimum of 3 ms.
4. Set the SOFT\_RESET bit (CSR 0x09.0).
5. Device resumes normal operation.(i.e video streaming resumes on the panel).

### 7.3.3 LVDS Pattern Generation

The SN65DSI84 supports a pattern generation feature on LVDS Channels. This feature can be used to test the LVDS output path and LVDS panels in a system platform. The pattern generation feature can be enabled by setting the CHA\_TEST\_PATTERN bit at address 0x3C. No DSI data is received while the pattern generation feature is enabled.

There are three modes available for LVDS test pattern generation. The mode of test pattern generation is determined by register configuration as shown in [Table 1](#).

**Table 1. Video Registers**

Addr. bit	Register Name
0x20.7:0	CHA_ACTIVE_LINE_LENGTH_LOW
0x21.3:0	CHA_ACTIVE_LINE_LENGTH_HIGH
0x24.7:0	CHA_VERTICAL_DISPLAY_SIZE_LOW
0x25.3:0	CHA_VERTICAL_DISPLAY_SIZE_HIGH
0x2C.7:0	CHA_HSYNC_PULSE_WIDTH_LOW
0x2D.1:0	CHA_HSYNC_PULSE_WIDTH_HIGH
0x30.7:0	CHA_VSYNC_PULSE_WIDTH_LOW
0x31.1:0	CHA_VSYNC_PULSE_WIDTH_HIGH
0x34.7:0	CHA_HORIZONTAL_BACK_PORCH
0x36.7:0	CHA_VERTICAL_BACK_PORCH
0x38.7:0	CHA_HORIZONTAL_FRONT_PORCH
0x3A.7:0	CHA_VERTICAL_FRONT_PORCH

## 7.4 Device Functional Modes

### 7.4.1 Reset Implementation

When EN is de-asserted (low), the SN65DSI84 is in SHUTDOWN or RESET state. In this state, CMOS inputs are ignored, the MIPI® D-PHY inputs are disabled and outputs are high impedance. It is critical to transition the EN input from a low to a high level after the  $V_{CC}$  supply has reached the minimum operating voltage as shown in Figure 6. This is achieved by a control signal to the EN input, or by an external capacitor connected between EN and GND.

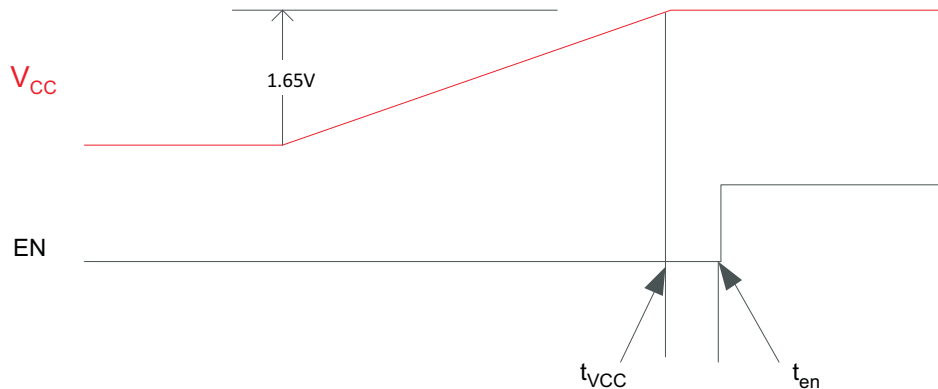


Figure 6. Cold Start  $V_{CC}$  Ramp up to EN

When implementing the external capacitor, the size of the external capacitor depends on the power up ramp of the  $V_{CC}$  supply, where a slower ramp-up results in a larger value external capacitor. See the latest reference schematic for the SN65DSI84 device and, or consider approximately 200 nF capacitor as a reasonable first estimate for the size of the external capacitor.

Both EN implementations are shown in Figure 7 and Figure 8.

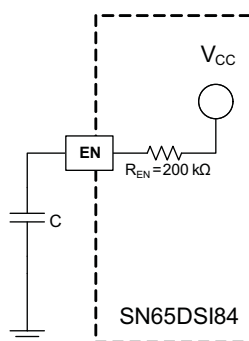


Figure 7. External Capacitor Controlled EN

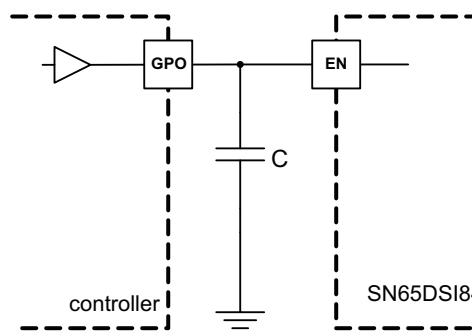


Figure 8. EN Input From Active Controller

When the SN65DSI84 is reset while  $V_{CC}$  is high, the EN pin must be held low for at least 10 ms before being asserted high as described in Table 2 to be sure that the device is properly reset. The DSI CLK lane MUST be in HS and the DSI data lanes MUST be driven to LP11 while the device is in reset before the EN pin is asserted per the timing described in Table 2.

### 7.4.2 Initialization Sequence

Use the following initialization sequence to setup the SN65DSI84. This sequence is required for proper operation of the device. Steps 9 through 11 in the sequence are optional.

Also see to Figure 6.

**Device Functional Modes (continued)**
**Table 2. Initialization Sequence**

INITIALIZATION SEQUENCE NUMBER	INITIALIZATION SEQUENCE DESCRIPTION
Init seq 1	Power on
Init seq 2	After power is applied and stable, the DSI CLK lanes MUST be in HS state and the DSI data lanes MUST be driven to LP11 state
Init seq 3	Set EN pin to Low
Wait 10 ms <sup>(1)</sup>	
Init seq 4	Tie EN pin to High
Wait 10 ms <sup>(1)</sup>	
Init seq 5	Initialize all CSR registers to their appropriate values based on the implementation (The SN65DSI8x is not functional until the CSR registers are initialized)
Init seq 6	Set the PLL_EN bit (CSR 0x0D.0)
Wait 10 ms <sup>(1)</sup>	
Init seq 7	Set the SOFT_RESET bit (CSR 0x09.0)
Wait 10 ms <sup>(1)</sup>	
Init seq 8	Change DSI data lanes to HS state and start DSI video stream
Wait 5 ms <sup>(1)</sup>	
Init seq 9	Read back all registers and confirm they were correctly written
Init seq 10	Write 0xFF to CSR 0xE5 to clear the error registers
Wait 1 ms <sup>(1)</sup>	
Init seq 11	Read CSR 0xE5. If CSR 0xE5 != 0x00, then go back to step #2 and re-initialize

(1) Minimum recommended delay. It is fine to exceed these.

**7.4.3 LVDS Output Formats**

The SN65DSI84 processes DSI packets and produces video data driven to the FlatLink™ LVDS interface in an industry standard format. Single-Link LVDS and Dual-Link LVDS are supported by the SN65DSI84; when the FlatLink™ output is implemented in a Dual-Link configuration, channel A carries the odd pixel data, and channel B carries the even pixel data. During conditions such as the default condition, and some video synchronization periods, where no video stream data is passing from the DSI input to the LVDS output, the SN65DSI84 transmits zero value pixel data on the LVDS outputs while maintaining transmission of the vertical sync and horizontal sync status.

Figure 9 illustrates a Single-Link LVDS 18bpp application.

Figure 10 illustrates a Dual-Link 24 bpp application using Format 2, controlled by CHA\_24BPP\_FORMAT1 (CSR 0x18.1) and CHB\_24BPP\_FORMAT1 (CSR 0x18.0). In data Format 2, the two MSB per color are transferred on the Y3P/N LVDS lane.

Figure 11 illustrates a 24 bpp Single-Link application using Format 1. In data Format 1, the two LSB per color are transferred on the Y3P/N LVDS lane.

Figure 12 illustrates a Single-Link LVDS application where 24 bpp data is received from DSI and converted to 18 bpp data for transmission to an 18 bpp panel. This application is configured by setting CHA\_24BPP\_FORMAT1 (CSR 0x18.1) to '1' and CHA\_24BPP\_MODE (CSR 0x18.3) to '0'. In this configuration, the SN65DSI84 will not transmit the 2 LSB per color since the Y3P/N LVDS lane is disabled.

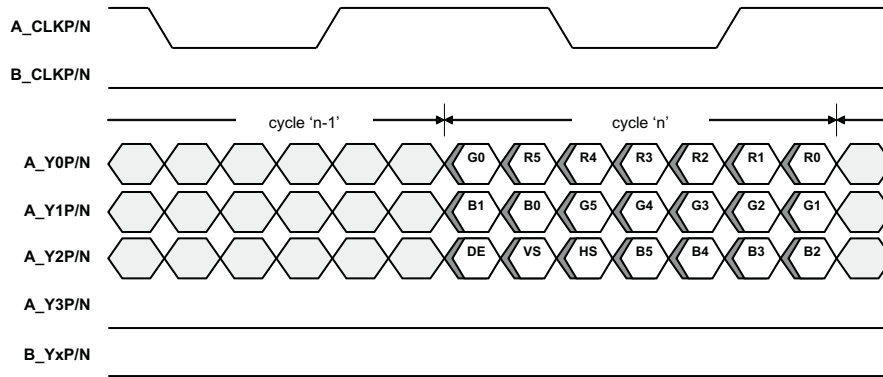
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**NOTE**

Note: Figure 9, Figure 10, Figure 11, and Figure 12 only illustrate a few example applications for the SN65DSI84. Other applications are also supported.

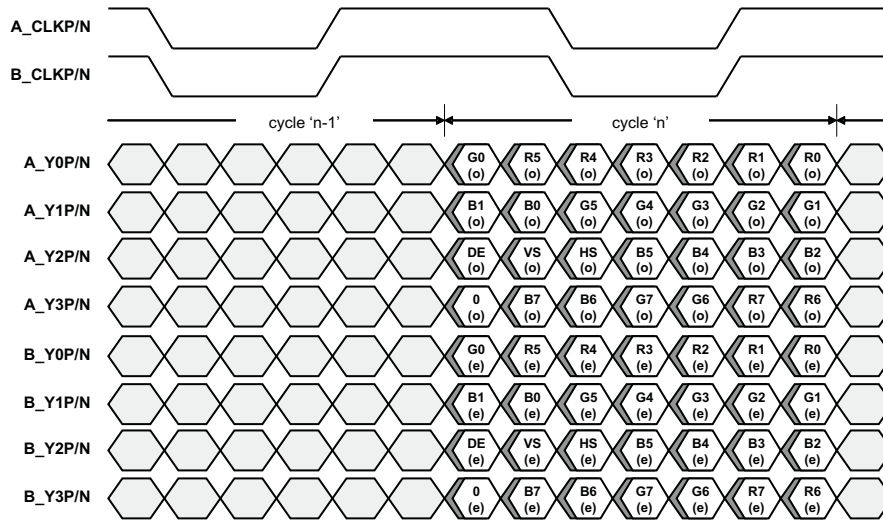
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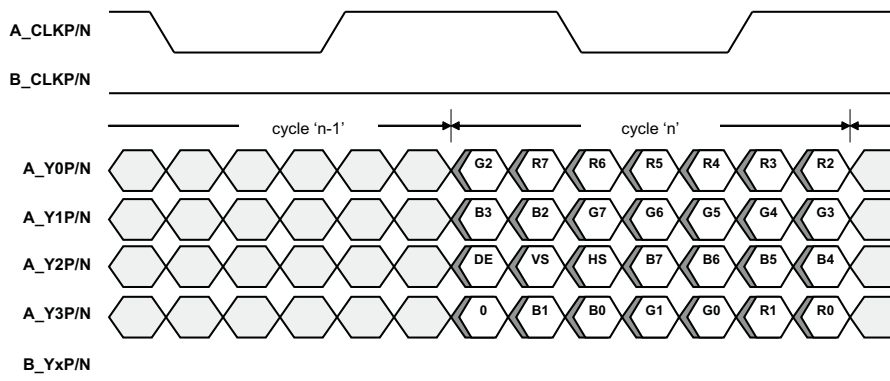
DE = Data Enable; Channel B Clock, Channel B Data, and A\_Y3P/N are Output Low

**Figure 9. Flatlink Output Data; Single-Link 18 Bpp**



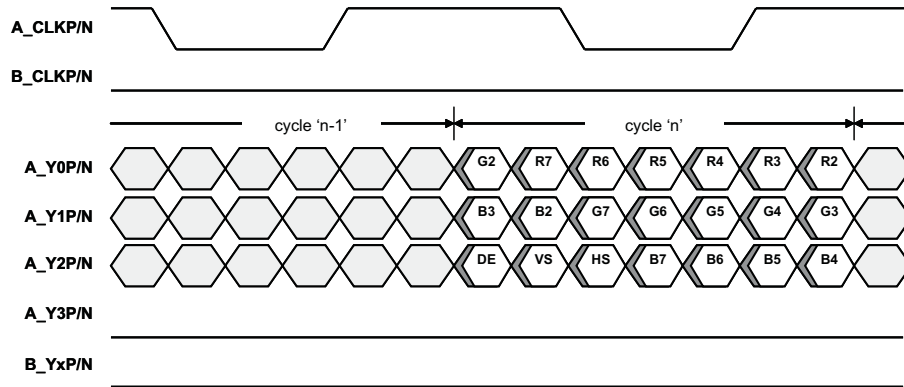
DE = Data Enable; (o) = Odd Pixels; (e) = Even Pixels

**Figure 10. Flatlink Output Data (Format 2); Dual-Link 24 Bpp**



DE = Data Enable; Channel B Clock and Data are Output Low

**Figure 11. Flatlink Output Data (Format 1); Single-Link 24 Bpp**



DE = Data Enable; Channel B Clock, Channel B Data, and A\_Y3P/N are Output Low; Channel B Clock, Channel B Data, and A\_Y3P/N are Output Low

**Figure 12. Flatlink Output Data (Format 1); 24-Bpp to Single-Link 18-Bpp Conversion**

### 7.4.4 DSI Lane Merging

The SN65DSI84 supports four DSI data lanes per input channel, and may be configured to support one, two, or three DSI data lanes per channel. Unused DSI input pins on the SN65DSI84 should be left unconnected or driven to LP11 state. The bytes received from the data lanes are merged in HS mode to form packets that carry the video stream. DSI data lanes are bit and byte aligned.

Figure 13 illustrates the lane merging function for each channel; 4-Lane, 3-Lane, and 2-Lane modes are illustrated

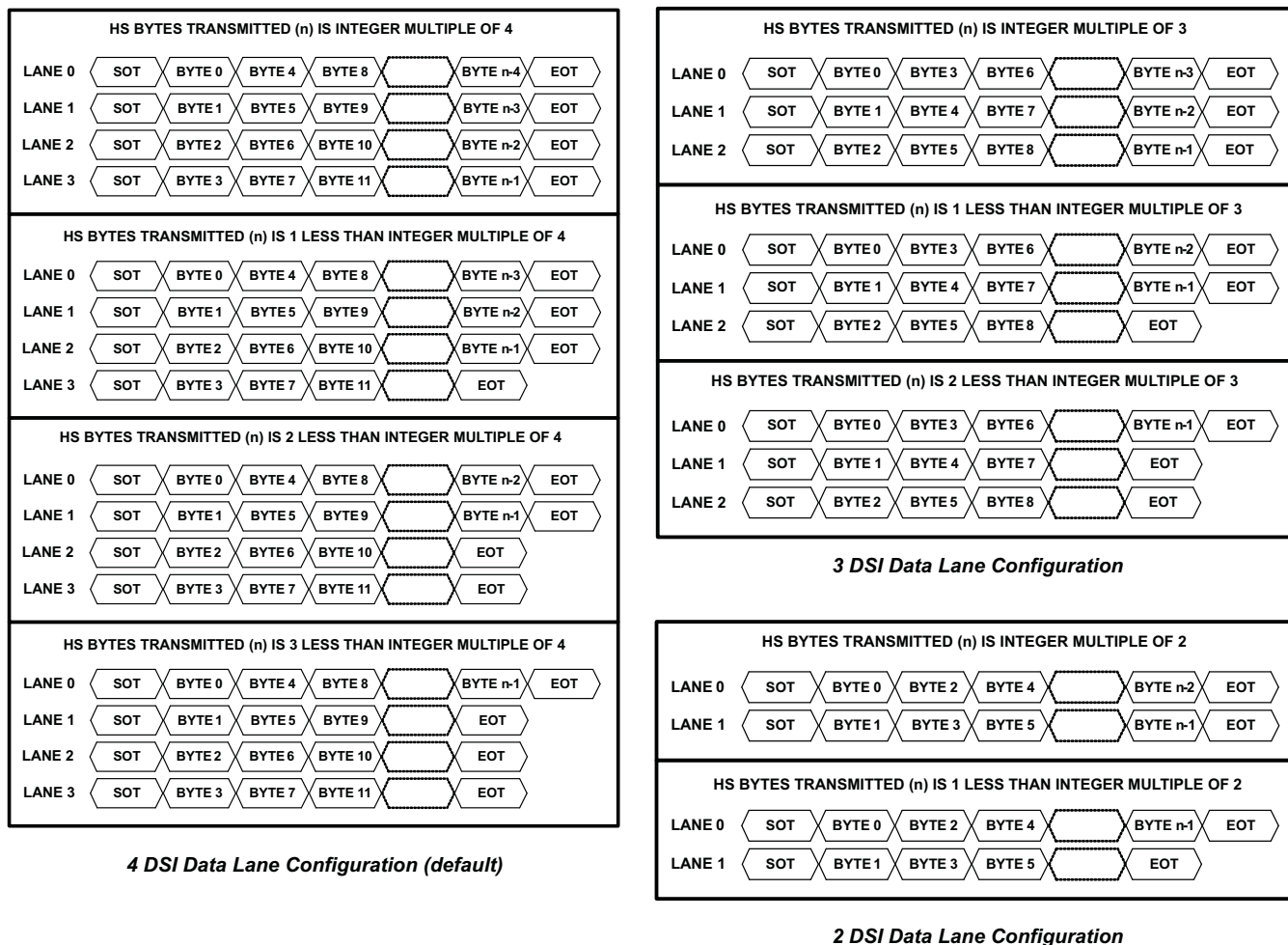


Figure 13. SN65DSI84 DSI Lane Merging Illustration

### 7.4.5 DSI Pixel Stream Packets

The SN65DSI84 processes 18bpp (RGB666) and 24 bpp (RGB888) DSI packets on each channel as shown in Figure 14, Figure 15, and Figure 16.

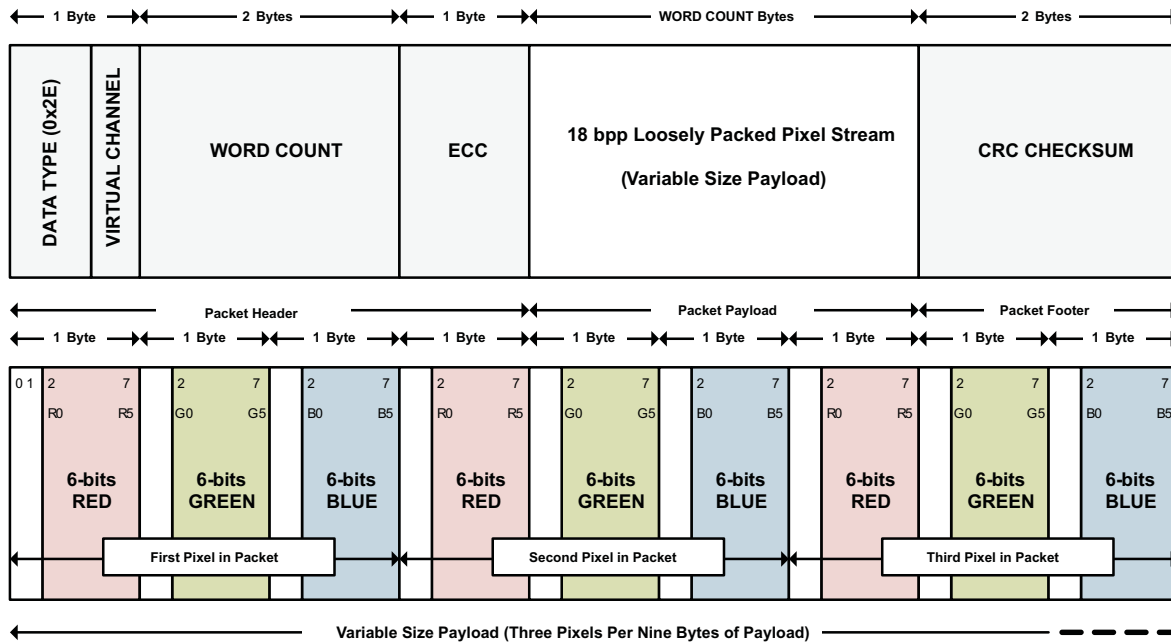


Figure 14. 18 Bpp (Loosely Packed) DSI Packet Structure

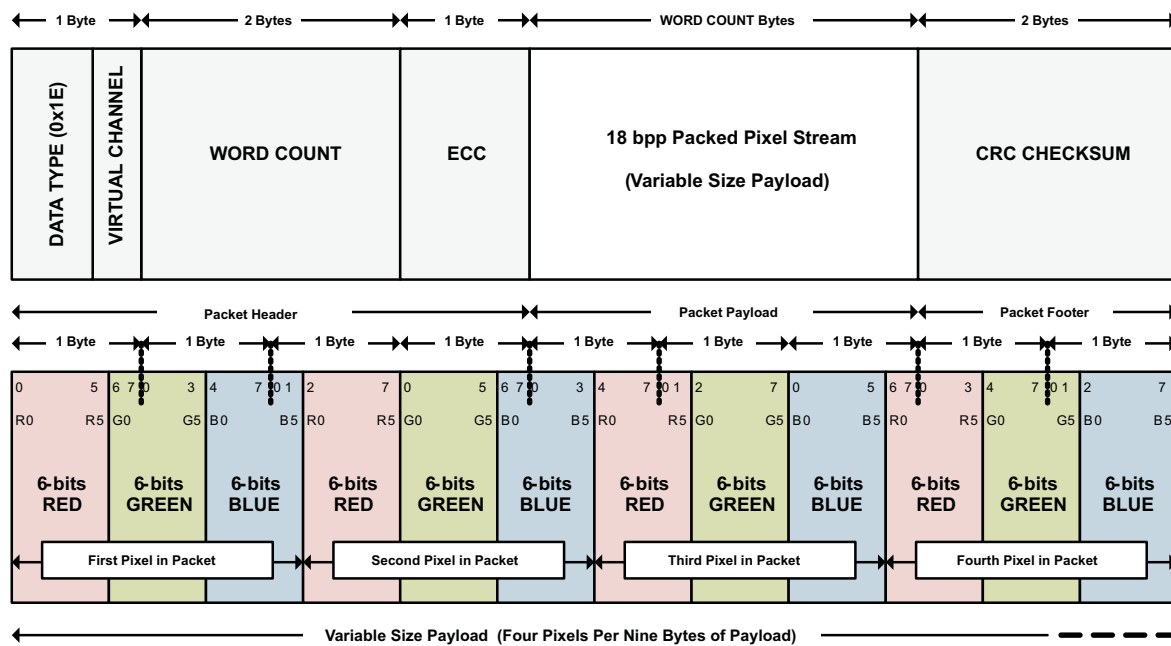


Figure 15. 18-Bpp (Tightly Packed) DSI Packet Structure

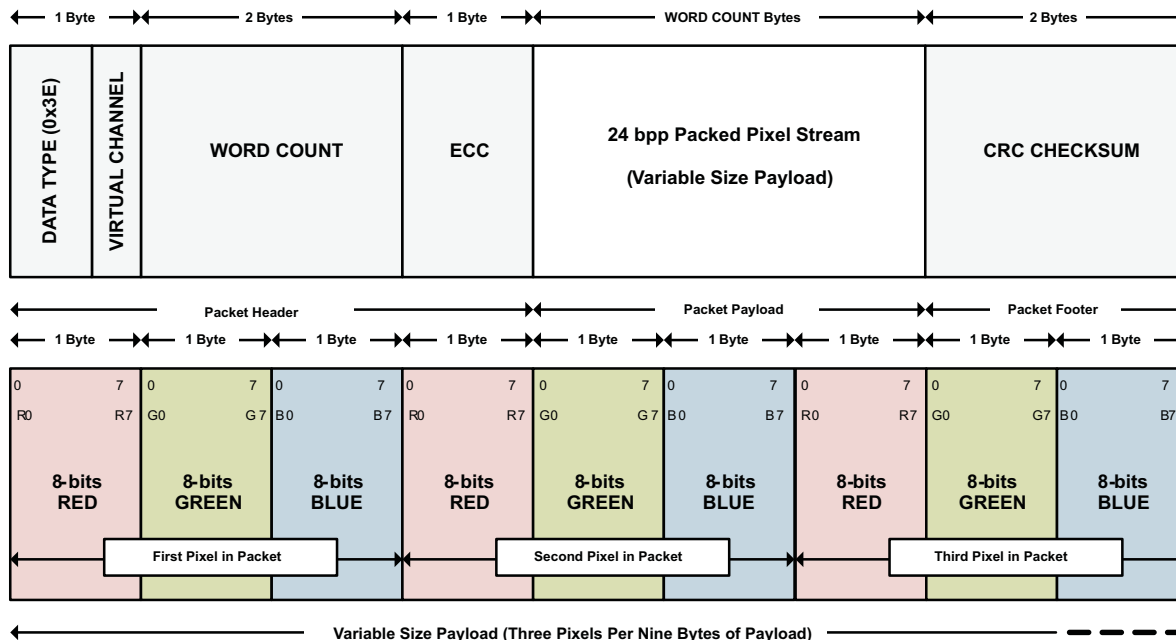


Figure 16. 24-Bpp DSI Packet Structure

#### 7.4.6 DSI Video Transmission Specifications

The SN65DSI84 supports burst video mode and non-burst video mode with sync events or with sync pulses packet transmission as described in the DSI specification. The burst mode supports time-compressed pixel stream packets that leave added time per scan line for power savings LP mode. The SN65DSI84 requires a transition to LP mode once per frame to enable PHY synchronization with the DSI host processor; however, for a robust and low-power implementation, the transition to LP mode is recommended on every video line.

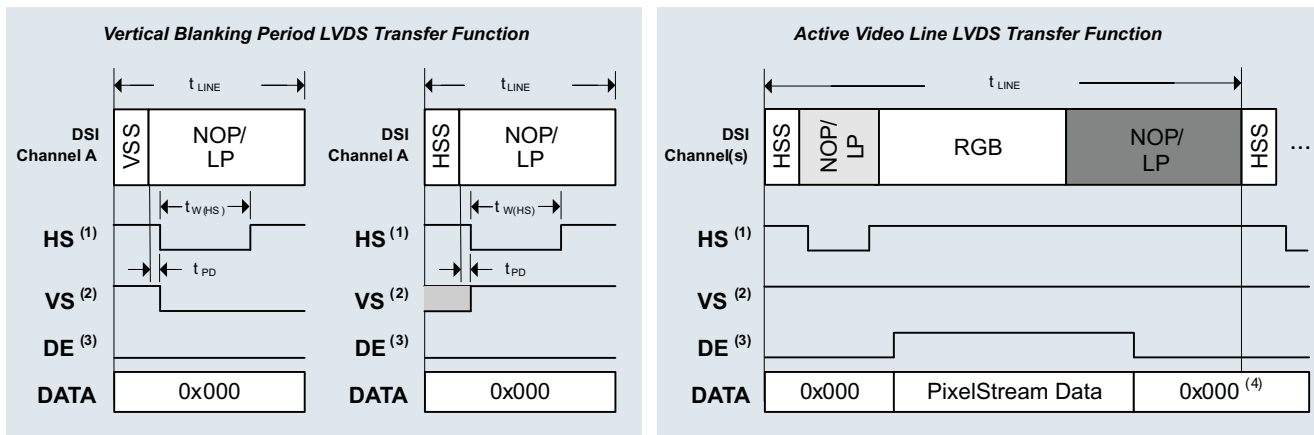
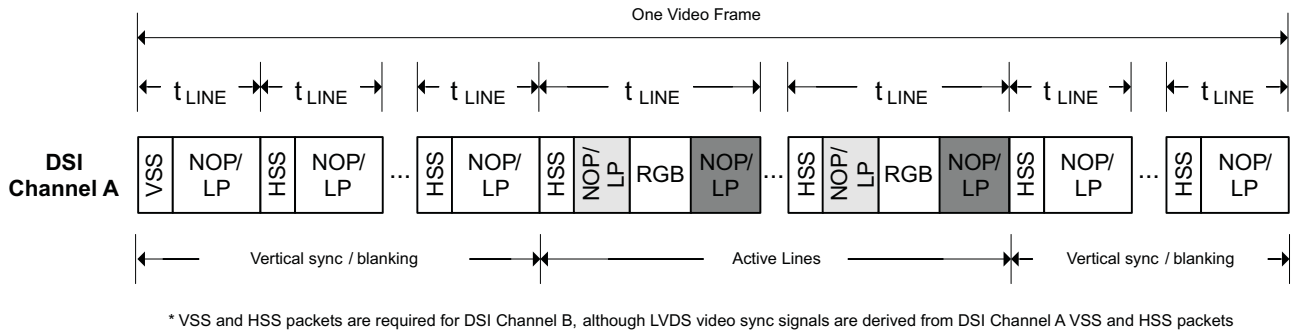
Figure 17 illustrates the DSI video transmission applied to SN65DSI84 applications. In all applications, the LVDS output rate must be less than or equal to the DSI input rate. The first line of a video frame shall start with a VSS packet, and all other lines start with VSE or HSS. The position of the synchronization packets in time is of utmost importance since this has a direct impact on the visual performance of the display panel; that is, these packets generate the HS and VS (horizontal and vertical sync) signals on the LVDS interface after the delay programmed into CHA\_SYNC\_DELAY\_LOW/HIGH (CSR 0x28.7:0 and 0x29.3:0).

As required in the DSI specification, the SN65DSI84 requires that pixel stream packets contain an integer number of pixels (i.e. end on a pixel boundary); it is recommended to transmit an entire scan line on one pixel stream packet. When a scan line is broken in to multiple packets, inter-packet latency shall be considered such that the video pipeline (ie. pixel queue or partial line buffer) does not run empty (i.e. under-run); during scan line processing, if the pixel queue runs empty, the SN65DSI84 transmits zero data (18'b0 or 24'b0) on the LVDS interface.

#### NOTE

When the HS clock is used as a source for the LVDS pixel clock, the LP mode transitions apply only to the data lanes, and the DSI clock lane remains in the HS mode during the entire video transmission.

The DSI84 does not support the DSI Virtual Channel capability or reverse direction (peripheral to processor) transmissions.



- (1) The assertion of HS is delayed ( $t_{PD}$ ) by a programmable number of pixel clocks from the last bit of VSS/HSS packet received on DSI. The HS pulse width ( $t_{W(HS)}$ ) is also programmable. The illustration shows HS active low.
- (2) VS is signaled for a programmable number of lines ( $t_{LINE}$ ) and is asserted when HS is asserted for the first line of the frame. VS is de-asserted when HS is asserted after the number of lines programmed has been reached. The illustration shows VS active low
- (3) DE is asserted when active pixel data is transmitted on LVDS, and polarity is set independent to HS/VS. The illustration shows DE active high
- (4) After the last pixel in an active line is output to LVDS, the LVDS data is output zero

**LEGEND**

**VSS**      **DSI Sync Event Packet: V Sync Start**

**HSS**      **DSI Sync Event Packet: H Sync Start**

**RGB**      **A sequence of DSI Pixel Stream Packets and Null Packets**

**NOP/LP**    **DSI Null Packet, Blanking Packet, or a transition to LP Mode**

**Figure 17. DSI Channel Transmission and Transfer Function**

**7.4.7 Operating Modes**

The SN65DSI84 can be configured for several different operating modes via LVDS\_LINK\_CFG (CSR 0x18.4), LEFT\_RIGHT\_PIXELS (CSR 0x10.7), and DSI\_CHANNEL\_MODE (CSR 0x10.6:5). These modes are summarized in Table 3. In each of the modes, video data can be 18 bpp or 24 bpp.

**Table 3. SN65DSI84 Operating Modes**

MODE	CSR 0x18.4	DESCRIPTION
	LVDS_LINK_CFG	
Single DSI Input to Single-Link LVDS	1	Single DSI Input on Channel A to Single-Link LVDS output on Channel A.
Single DSI Input to Dual-Link LVDS	0	Single DSI Input on Channel A to Dual-Link LVDS output with Odd pixels on Channel A and Even pixels on Channel B.

## 7.5 Programming

### 7.5.1 Local I<sup>2</sup>C Interface Overview

The SN65DSI84 local I<sup>2</sup>C interface is enabled when EN is input high, access to the CSR registers is supported during ultra-low power state (ULPS). The SCL and SDA terminals are used for I<sup>2</sup>C clock and I<sup>2</sup>C data respectively. The SN65DSI84 I<sup>2</sup>C interface conforms to the two-wire serial interface defined by the I<sup>2</sup>C Bus Specification, Version 2.1 (January 2000), and supports fast mode transfers up to 400 kbps.

The device address byte is the first byte received following the START condition from the master device. The 7 bit device address for SN65DSI84 is factory preset to 010110X with the least significant bit being determined by the ADDR control input. Table 4 clarifies the SN65DSI84 target address.

**Table 4. SN65DSI84 I<sup>2</sup>C Target Address Description** <sup>(1)(2)</sup>

SN65DSI84 I <sup>2</sup> C TARGET ADDRESS							
BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (W/R)
0	1	0	1	1	0	ADDR	0/1

(1) When ADDR=1, Address Cycle is 0x5A (Write) and 0x5B (Read)

(2) When ADDR=0, Address Cycle is 0x58 (Write) and 0x59 (Read)

The following procedure is followed to write to the SN65DSI84 I<sup>2</sup>C registers.

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI84 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The SN65DSI84 acknowledges the address cycle.
3. The master presents the sub-address (I<sup>2</sup>C register within SN65DSI84) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSI84 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I<sup>2</sup>C register.
6. The SN65DSI84 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SN65DSI84.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure is followed to read the SN65DSI84 I<sup>2</sup>C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SN65DSI84 7-bit address and a one-value “W/R” bit to indicate a read cycle.
2. The SN65DSI84 acknowledges the address cycle.
3. The SN65DSI84 transmit the contents of the memory registers MSB-first starting at register 00h. If a write to the SN65DSI84 I<sup>2</sup>C register occurred prior to the read, then the SN65DSI84 will start at the sub-address specified in the write.
4. The SN65DSI84 will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I<sup>2</sup>C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the SN65DSI84 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure is followed for setting a starting sub-address for I<sup>2</sup>C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the SN65DSI84 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The SN65DSI84 acknowledges the address cycle.
3. The master presents the sub-address (I<sup>2</sup>C register within SN65DSI84) to be written, consisting of one byte of data, MSB-first.
4. The SN65DSI84 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

## 7.6 Register Maps

### 7.6.1 Control and Status Registers Overview

Many of the SN65DSI84 functions are controlled by the Control and Status Registers (CSR). All CSR registers are accessible through the local I<sup>2</sup>C interface.

See the following tables for the SN65DSI84 CSR descriptions. Reserved or undefined bit fields should not be modified. Otherwise, the device may operate incorrectly.

**Table 5. CSR Bit Field Definitions – ID Registers**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x00 – 0x08	7:0	Reserved Addresses 0x08 - 0x00 = {0x01, 0x20, 0x20, 0x20, 0x44, 0x53, 0x49, 0x38, 0x35}	Reserved	RO

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)

**Table 6. CSR Bit Field Definitions – Reset and Clock Registers**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x09	0	SOFT_RESET This bit automatically clears when set to '1' and returns zeros when read. This bit must be set after the CSR's are updated. This bit must also be set after making any changes to the DIS clock rate or after changing between DSI burst and non-burst modes. 0 – No action (default) 1 – Reset device to default condition excluding the CSR bits.	0	WO
0x0A	7	PLL_EN_STAT 0 – PLL not enabled (default) 1 – PLL enabled Note: After PLL_EN_STAT = 1, wait at least 3ms for PLL to lock.	0	RO
	3:1	LVDS_CLK_RANGE This field selects the frequency range of the LVDS output clock. 000 – 25 MHz ≤ LVDS_CLK < 37.5 MHz 001 – 37.5 MHz ≤ LVDS_CLK < 62.5 MHz 010 – 62.5 MHz ≤ LVDS_CLK < 87.5 MHz 011 – 87.5 MHz ≤ LVDS_CLK < 112.5 MHz 100 – 112.5 MHz ≤ LVDS_CLK < 137.5 MHz 101 – 137.5 MHz ≤ LVDS_CLK ≤ 154 MHz (default) 110 – Reserved 111 – Reserved	101	RW
	0	HS_CLK_SRC 0 – LVDS pixel clock derived from input REFCLK (default) 1 – LVDS pixel clock derived from MIPI D-PHY channel A HS continuous clock	0	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)



**Table 6. CSR Bit Field Definitions – Reset and Clock Registers (continued)**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x0B	7:3	<b>DSI_CLK_DIVIDER</b> When CSR 0x0A.0 = '1', this field controls the divider used to generate the LVDS output clock from the MIPI D-PHY Channel A HS continuous clock. When CSR 0x0A.0 = '0', this field must be programmed to 00000. 00000 – LVDS clock = source clock (default) 00001 – Divide by 2 00010 – Divide by 3 00011 – Divide by 4 • • • 10111 – Divide by 24 11000 – Divide by 25 11001 through 11111 – Reserved	00000	RW
	1:0	<b>REFCLK_MULTIPLIER</b> When CSR 0x0A.0 = '0', this field controls the multiplier used to generate the LVDS output clock from the input REFCLK. When CSR 0x0A.0 = '1', this field must be programmed to 00. 00 – LVDS clock = source clock (default) 01 – Multiply by 2 10 – Multiply by 3 11 – Multiply by 4	00	RW
0x0D	0	<b>PLL_EN</b> When this bit is set, the PLL is enabled with the settings programmed into CSR 0x0A and CSR 0x0B. The PLL should be disabled before changing any of the settings in CSR 0x0A and CSR 0x0B. The input clock source must be active and stable before the PLL is enabled. 0 – PLL disabled (default) 1 – PLL enabled	0	RW

**Table 7. CSR Bit Field Definitions – DSI Registers**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x10	7	Reserved - Do not write to this field. Must remain at default.	0	RW
	6:5	Reserved - Do not write to this field. Must remain at default.	01	RW
	4:3	<b>CHA_DSI_LANES</b> This field controls the number of lanes that are enabled for DSI Channel A. 00 – Four lanes are enabled 01 – Three lanes are enabled 10 – Two lanes are enabled 11 – One lane is enabled (default) Note: Unused DSI input pins on the SN65DSI84 should be left unconnected.	11	RW
	0	<b>SOT_ERR_TOL_DIS</b> 0 – Single bit errors are tolerated for the start of transaction SoT leader sequence (default) 1 – No SoT bit errors are tolerated	0	RW
0x11	7:6	<b>CHA_DSI_DATA_EQ</b> This field controls the equalization for the DSI Channel A Data Lanes 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization	00	RW
	3:2	<b>CHA_DSI_CLK_EQ</b> This field controls the equalization for the DSI Channel A Clock 00 – No equalization (default) 01 – 1 dB equalization 10 – Reserved 11 – 2 dB equalization	00	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)

**Table 7. CSR Bit Field Definitions – DSI Registers (continued)**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x12	7:0	CHA_DSI_CLK_RANGE This field specifies the DSI Clock frequency range in 5 MHz increments for the DSI Channel A Clock 0x00 through 0x07 – Reserved 0x08 – 40 ≤ frequency < 45 MHz 0x09 – 45 ≤ frequency < 50 MHz • • • 0x63 – 495 ≤ frequency < 500 MHz 0x64 – 500 MHz 0x65 through 0xFF – Reserved	0	RW

**Table 8. CSR Bit Field Definitions – LVDS Registers**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x18	7	DE_NEG_POLARITY 0 – DE is positive polarity driven '1' during active pixel transmission on LVDS (default) 1 – DE is negative polarity driven '0' during active pixel transmission on LVDS	0	RW
	6	HS_NEG_POLARITY 0 – HS is positive polarity driven '1' during corresponding sync conditions 1 – HS is negative polarity driven '0' during corresponding sync (default)	1	RW
	5	VS_NEG_POLARITY 0 – VS is positive polarity driven '1' during corresponding sync conditions 1 – VS is negative polarity driven '0' during corresponding sync (default)	1	RW
	4	LVDS_LINK_CFG 0 – LVDS Channel A and Channel B outputs enabled When CSR 0x10.6:5 = '00' or '01', the LVDS is in Dual-Link configuration 1 – LVDS Single-Link configuration; Channel A output enabled and Channel B output disabled (default)	1	RW
	3	CHA_24BPP_MODE 0 – Force 18bpp; LVDS channel A lane 4 (A_Y3P/N) is disabled (default) 1 – Force 24bpp; LVDS channel A lane 4 (B_Y3P/N) is enabled	0	RW
	2	CHB_24BPP_MODE 0 – Force 18bpp; LVDS channel B lane 4 (A_Y3P/N) is disabled (default) 1 – Force 24bpp; LVDS channel B lane 4 (B_Y3P/N) is enabled	0	RW
	1	CHA_24BPP_FORMAT1 This field selects the 24bpp data format 0 – LVDS channel A lane A_Y3P/N transmits the 2 most significant bits (MSB) per color; Format 2 (default) 1 – LVDS channel B lane A_Y3P/N transmits the 2 least significant bits (LSB) per color; Format 1 Note1: This field must be '0' when 18bpp data is received from DSI. Note2: If this field is set to '1' and CHA_24BPP_MODE is '0', the SN65DSI84 will convert 24bpp data to 18bpp data for transmission to an 18bpp panel. In this configuration, the SN65DSI84 will not transmit the 2 LSB per color on LVDS channel A, since LVDS channel A lane A_Y3P/N is disabled.	0	RW
	0	CHB_24BPP_FORMAT1 This field selects the 24bpp data format 0 – LVDS channel B lane B_Y3P/N transmits the 2 most significant bits (MSB) per color; Format 2 (default) 1 – LVDS channel B lane B_Y3P/N transmits the 2 least significant bits (LSB) per color; Format 1 Note1: This field must be '0' when 18bpp data is received from DSI. Note2: If this field is set to '1' and CHB_24BPP_MODE is '0', the SN65DSI84 will convert 24bpp data to 18bpp data for transmission to an 18bpp panel. In this configuration, the SN65DSI84 will not transmit the 2 LSB per color on LVDS channel B, since LVDS channel B lane B_Y3P/N is disabled.	0	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)

**Table 8. CSR Bit Field Definitions – LVDS Registers (continued)**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x19	6	CHA_LVDS_VOCM This field controls the common mode output voltage for LVDS Channel A 0 – 1.2V (default) 1 – 0.9V (CSR 0x1B.5:4 CHA_LVDS_CM_ADJUST must be set to '01b')	0	RW
	4	CHB_LVDS_VOCM This field controls the common mode output voltage for LVDS Channel B 0 – 1.2V (default) 1 – 0.9V (CSR 0x1B.1:0 CHB_LVDS_CM_ADJUST must be set to '01b')	0	RW
	3:2	CHA_LVDS_VOD_SWING This field controls the differential output voltage for LVDS Channel A. See the <a href="#">Electrical Characteristics table</a> for  V <sub>OD</sub>   for each setting: 00, 01 (default), 10, 11.	01	RW
	1:0	CHB_LVDS_VOD_SWING This field controls the differential output voltage for LVDS Channel B. See the <a href="#">Electrical Characteristics table</a> for  V <sub>OD</sub>   for each setting: 00, 01 (default), 10, 11.	01	RW

**Table 8. CSR Bit Field Definitions – LVDS Registers (continued)**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x1A	6	EVEN_ODD_SWAP 0 – Odd pixels routed to LVDS Channel A and Even pixels routed to LVDS Channel B (default) 1 – Odd pixels routed to LVDS Channel B and Even pixels routed to LVDS Channel A Note: When the SN65DSI84 is in two stream mode (CSR 0x10.6:5 = '10'), setting this bit to '1' will cause the video stream from DSI Channel A to be routed to LVDS Channel B and the video stream from DSI Channel B to be routed to LVDS Channel A.	0	RW
	5	CHA_REVERSE_LVDS This bit controls the order of the LVDS pins for Channel A. 0 – Normal LVDS Channel A pin order. LVDS Channel A pin order is the same as listed in the Terminal Assignments Section. (default) 1 – Reversed LVDS Channel A pin order. LVDS Channel A pin order is remapped as follows: <ul style="list-style-type: none"> <li>• A_Y0P → A_Y3P</li> <li>• A_Y0N → A_Y3N</li> <li>• A_Y1P → A_CLKP</li> <li>• A_Y1N → A_CLKN</li> <li>• A_Y2P → A_Y2P</li> <li>• A_Y2N → A_Y2N</li> <li>• A_CLKP → A_Y1P</li> <li>• A_CLKN → A_Y1N</li> <li>• A_Y3P → A_Y0P</li> <li>• A_Y3N → A_Y0N</li> </ul>	0	RW
	4	CHB_REVERSE_LVDS This bit controls the order of the LVDS pins for Channel B. 0 – Normal LVDS Channel B pin order. LVDS Channel B pin order is the same as listed in the Terminal Assignments Section. (default) 1 – Reversed LVDS Channel B pin order. LVDS Channel B pin order is remapped as follows: <ul style="list-style-type: none"> <li>• B_Y0P → B_Y3P</li> <li>• B_Y0N → B_Y3N</li> <li>• B_Y1P → B_CLKP</li> <li>• B_Y1N → B_CLKN</li> <li>• B_Y2P → B_Y2P</li> <li>• B_Y2N → B_Y2N</li> <li>• B_CLKP → B_Y1P</li> <li>• B_CLKN → B_Y1N</li> <li>• B_Y3P → B_Y0P</li> <li>• B_Y3N → B_Y0N</li> </ul>	0	RW
	1	CHA_LVDS_TERM This bit controls the near end differential termination for LVDS Channel A. This bit also affects the output voltage for LVDS Channel A. 0 – 100Ω differential termination 1 – 200Ω differential termination (default)	1	RW
	0	CHB_LVDS_TERM This bit controls the near end differential termination for LVDS Channel B. This bit also affects the output voltage for LVDS Channel B. 0 – 100Ω differential termination 1 – 200Ω differential termination (default)	1	RW

**Table 8. CSR Bit Field Definitions – LVDS Registers (continued)**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x1B	5:4	<b>CHA_LVDS_CM_ADJUST</b> This field can be used to adjust the common mode output voltage for LVDS Channel A. 00 – No change to common mode voltage (default) 01 – Adjust common mode voltage down 3% 10 – Adjust common mode voltage up 3% 11 – Adjust common mode voltage up 6%	00	RW
	1:0	<b>CHB_LVDS_CM_ADJUST</b> This field can be used to adjust the common mode output voltage for LVDS Channel B. 00 – No change to common mode voltage (default) 01 – Adjust common mode voltage down 3% 10 – Adjust common mode voltage up 3% 11 – Adjust common mode voltage up 6%	00	RW

Note for all video registers:

1. TEST PATTERN GENERATION PURPOSE ONLY registers are for test pattern generation use only. Others are for normal operation unless the test pattern generation feature is enabled.

**Table 9. CSR Bit Field Definitions – Video Registers**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x20	7:0	<b>CHA_ACTIVE_LINE_LENGTH_LOW</b> This field controls the length in pixels of the active horizontal line that are received on DSI Channel A and output to LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 12-bit value for the horizontal line length.	0	RW
0x21	3:0	<b>CHA_ACTIVE_LINE_LENGTH_HIGH</b> This field controls the length in pixels of the active horizontal line that are received on DSI Channel A and output to LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 4 bits of the 12-bit value for the horizontal line length.	0	RW
0x24	7:0	<b>CHA_VERTICAL_DISPLAY_SIZE_LOW</b> TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 12-bit value for the vertical display size.	0	RW
0x25	3:0	<b>CHA_VERTICAL_DISPLAY_SIZE_HIGH</b> TEST PATTERN GENERATION PURPOSE ONLY. This field controls the vertical display size in lines for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 4 bits of the 12-bit value for the vertical display size.	0	RW
0x28	7:0	<b>CHA_SYNC_DELAY_LOW</b> This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI84. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the lower 8 bits of the 12-bit value for the Sync delay.	0	RW
0x29	3:0	<b>CHA_SYNC_DELAY_HIGH</b> This field controls the delay in pixel clocks from when an HSync or VSync is received on the DSI to when it is transmitted on the LVDS interface for Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The delay specified by this field is in addition to the pipeline and synchronization delays in the SN65DSI84. The additional delay is approximately 10 pixel clocks. The Sync delay must be programmed to at least 32 pixel clocks to ensure proper operation. The value in this field is the upper 4 bits of the 12-bit value for the Sync delay.	0	RW
0x2C	7:0	<b>CHA_HSYNC_PULSE_WIDTH_LOW</b> This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 10-bit value for the HSync Pulse Width.	0	RW
0x2D	1:0	<b>CHA_HSYNC_PULSE_WIDTH_HIGH</b> This field controls the width in pixel clocks of the HSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 2 bits of the 10-bit value for the HSync Pulse Width.	0	RW
0x30	7:0	<b>CHA_VSYNC_PULSE_WIDTH_LOW</b> This field controls the length in lines of the VSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the lower 8 bits of the 10-bit value for the VSync Pulse Width.	0	RW

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)

**Table 9. CSR Bit Field Definitions – Video Registers (continued)**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0x31	1:0	CHA_VSYNC_PULSE_WIDTH_HIGH This field controls the length in lines of the VSync Pulse Width for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0). The value in this field is the upper 2 bits of the 10-bit value for the VSync Pulse Width.	0	RW
0x34	7:0	CHA_HORIZONTAL_BACK_PORCH This field controls the time in pixel clocks between the end of the HSync Pulse and the start of the active video data for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW
0x36	7:0	CHA_VERTICAL_BACK_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the VSync Pulse and the start of the active video data for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW
0x38	7:0	CHA_HORIZONTAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the time in pixel clocks between the end of the active video data and the start of the HSync Pulse for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW
0x3A	7:0	CHA_VERTICAL_FRONT_PORCH TEST PATTERN GENERATION PURPOSE ONLY. This field controls the number of lines between the end of the active video data and the start of the VSync Pulse for LVDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW
0x3C	4	CHA_TEST_PATTERN TEST PATTERN GENERATION PURPOSE ONLY. When this bit is set, the SN65DSI84 will generate a video test pattern based on the values programmed into the Video Registers for LDS Channel A in single LVDS Channel mode(CSR 0x18.4=1), Channel A and B in dual LVDS Channel mode(CSR 0x18.4=0).	0	RW

**Table 10. CSR Bit Field Definitions – IRQ Registers**

ADDRESS	BIT(S)	DESCRIPTION	DEFAULT	ACCESS <sup>(1)</sup>
0xE0	0	<b>IRQ_EN</b> When enabled by this field, the IRQ output is driven high to communicate IRQ events. 0 – IRQ output is high-impedance (default) 1 – IRQ output is driven high when a bit is set in registers 0xE5 that also has the corresponding IRQ_EN bit set to enable the interrupt condition	0	RW
0xE1	7	<b>CHA_SYNCH_ERR_EN</b> 0 – CHA_SYNCH_ERR is masked 1 – CHA_SYNCH_ERR is enabled to generate IRQ events	0	RW
	6	<b>CHA_CRC_ERR_EN</b> 0 – CHA_CRC_ERR is masked 1 – CHA_CRC_ERR is enabled to generate IRQ events	0	RW
	5	<b>CHA_UNC_ECC_ERR_EN</b> 0 – CHA_UNC_ECC_ERR is masked 1 – CHA_UNC_ECC_ERR is enabled to generate IRQ events	0	RW
	4	<b>CHA_COR_ECC_ERR_EN</b> 0 – CHA_COR_ECC_ERR is masked 1 – CHA_COR_ECC_ERR is enabled to generate IRQ events	0	RW
	3	<b>CHA_LL_P_ERR_EN</b> 0 – CHA_LL_P_ERR is masked 1 – CHA_LL_P_ERR is enabled to generate IRQ events	0	RW
	2	<b>CHA_SOT_BIT_ERR_EN</b> 0 – CHA_SOT_BIT_ERR is masked 1 – CHA_SOT_BIT_ERR is enabled to generate IRQ events	0	RW
	0	<b>PLL_UNLOCK_EN</b> 0 – PLL_UNLOCK is masked 1 – PLL_UNLOCK is enabled to generate IRQ events	0	RW
0xE5	7	<b>CHA_SYNCH_ERR</b> When the DSI channel A packet processor detects an HS or VS synchronization error, that is, an unexpected sync packet; this bit is set; this bit is cleared by writing a '1' value.	0	RW1C
	6	<b>CHA_CRC_ERR</b> When the DSI channel A packet processor detects a data stream CRC error, this bit is set; this bit is cleared by writing a '1' value.	0	RW1C
	5	<b>CHA_UNC_ECC_ERR</b> When the DSI channel A packet processor detects an uncorrectable ECC error, this bit is set; this bit is cleared by writing a '1' value.	0	RW1C
	4	<b>CHA_COR_ECC_ERR</b> When the DSI channel A packet processor detects a correctable ECC error, this bit is set; this bit is cleared by writing a '1' value.	0	RW1C
	3	<b>CHA_LL_P_ERR</b> When the DSI channel A packet processor detects a low level protocol error, this bit is set; this bit is cleared by writing a '1' value. Low level protocol errors include SoT and EoT sync errors, Escape Mode entry command errors, LP transmission sync errors, and false control errors. Lane merge errors are reported by this status condition.	0	RW1C
	2	<b>CHA_SOT_BIT_ERR</b> When the DSI channel A packet processor detects an SoT leader sequence bit error, this bit is set; this bit is cleared by writing a '1' value.	0	RW1C
	0	<b>PLL_UNLOCK</b> This bit is set whenever the PLL Lock status transitions from LOCK to UNLOCK.	1	RW1C

(1) RO = Read Only; RW = Read/Write; RW1C = Read/Write '1' to Clear; WO = Write Only (reads return undetermined values)



## 8 Application and Implementation

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### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 8.1 Application Information

The SN65DSI84 device is primarily targeted for portable applications such as tablets and smart phones that utilize the MIPI DSI video format. The SN65DSI84 device can be used between a GPU with DSI output and a video panel with LVDS inputs

#### 8.1.1 Video Stop and Restart Sequence

When the system requires to stop outputting video to the display, it is recommended to use the following sequence for the SN65DSI84:

1. Clear the PLL\_EN bit to 0 (CSR 0x0D.0)
2. Stop video streaming on DSI inputs
3. Drive all DSI data lanes to LP11, but keep the DSI CLK lanes in HS.

When the system is ready to restart the video streaming.

1. Start video streaming on DSI inputs.
2. Set the PLL\_EN bit to 1(CSR 0x0D.0).
3. Wait for a minimum of 3 ms.
4. Set the SOFT\_RESET bit(0x09.0).

#### 8.1.2 Reverse LVDS Pin Order Option

For ease of PCB routing, the SN65DSI84 supports swapping/reversing the channel or pin order via configuration register programming. The order of the LVDS pin for LVDS Channel A or Channel B can be reversed by setting the address 0x1A bit 5 CHA\_REVERSE\_LVDS or bit 4 CHB\_REVERSE\_LVDS. The LVDS Channel A and Channel B can be swapped by setting the 0x1A.6 EVEN\_ODD\_SWAP bit. See the corresponding register bit definition for details.

#### 8.1.3 IRQ Usage

The SN65DSI84 provides an IRQ pin that can be used to indicate when certain errors occur on DSI. The IRQ output is enabled through the IRQ\_EN bit (CSR 0xE0.0). The IRQ pin will be asserted when an error occurs on DSI, the corresponding error enable bit is set, and the IRQ\_EN bit is set. An error is cleared by writing a '1' to the corresponding error status bit.

---

### NOTE

If the SOFT\_RESET bit is set while the DSI video stream is active, some of the error status bits may be set.

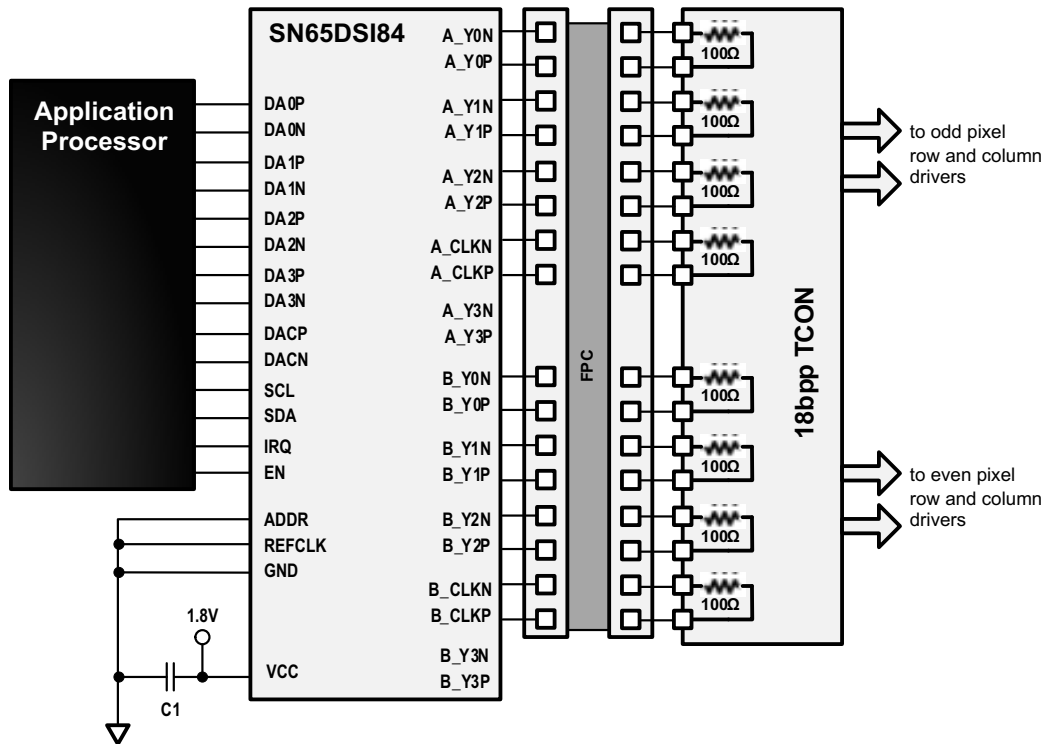
If the DSI video stream is stopped, some of the error status bits may be set. These error status bits should be cleared before restarting the video stream.

If the DSI video stream starts before the device is configured, some of the error status bits may be set. It is recommended to start streaming after the device is correctly configured as recommended in the initialization sequence in the [Initialization Sequence](#) section.

---

## 8.2 Typical Application

[Figure 18](#) illustrates a typical application using the SN65DSI84 for a single channel DSI receiver to interface a single-channel DSI application processor to an LVDS Dual-Link 18 bit-per-pixel panel supporting 1920 x 1200 WUXGA resolutions at 60 frames per second.

**Typical Application (continued)**

**Figure 18. Typical 1920 x 1200 WUXGA 18-bpp Panel Application**
**8.2.1 Design Requirements**

 For the 1920 x 1200 WUXGA 18-bpp Panel typical application design parameters, see [Table 11](#).

**Table 11. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
VCC	1.8V ( $\pm 5\%$ )
CLOCK	DSIA_CLK
REFCKL Frequency	N/A
DSIA Clock Frequency	490 MHz
<b>PANEL INFORMATION</b>	
LVDS Output Clock Frequency	81 MHz
Resolution	1920 x 1200
Horizontal Active (pixels)	960
Horizontal Blanking (pixels)	144
Vertical Active (lines)	1200
Vertical Blanking (lines)	20
Horizontal Sync Offset (pixels)	50
Horizontal Sync Pulse Width (pixels)	50
Vertical Sync Offset (lines)	1
Vertical Sync Pulse Width (lines)	5
Horizontal Sync Pulse Polarity	Negative
Vertical Sync Pulse Polarity	Negative
Color Bit Depth (6bpc or 8bpc)	6-bit
Number of LVDS Lanes	2 X [3 Data Lanes + 1 Clock Lane]

## Typical Application (continued)

**Table 11. Design Parameters (continued)**

DESIGN PARAMETER	EXAMPLE VALUE
<b>DSI INFORMATION</b>	
Number of DSI Lanes	1 X [4 Data Lanes + 1 Clock Lane]
DSI Input Clock Frequency	490MHz
Dual DSI Configuration(Odd/Even or Left/Right)	N/A

### 8.2.2 Detailed Design Procedure

The video resolution parameters required by the panel need to be programmed into the SN65DSI84. For this example, the parameters programmed would be the following:

Horizontal active = 1920 or 0x780  
 CHA\_ACTIVE\_LINE\_LENGTH\_LOW = 0x80  
 CHA\_ACTIVE\_LINE\_LENGTH\_HIGH = 0x07

Horizontal pulse Width = 50 or 0x32  
 CHA\_HSYNC\_PULSE\_WIDTH\_LOW = 0x32  
 CHA\_HSYNC\_PULSE\_WIDTH\_HIGH = 0x00

Horizontal back porch = Horizontal blanking – (Horizontal sync offset + Horizontal sync pulse width)  
 Horizontal back porch = 144 – (50 + 50)  
 Horizontal back porch = 44 or 0x2C  
 CHA\_HORIZONTAL\_BACK\_PORCH = 0x2C

Vertical pulse width = 5  
 CHA\_VSYNC\_PULSE\_WIDTH\_LOW = 0x05  
 CHA\_VSYNC\_PULSE\_WIDTH\_HIGH = 0x00

The pattern generation feature can be enabled by setting the CHA\_TEST\_PATTERN bit at address 0x3C and configuring the following TEST PATTERN GENERATION PURPOSE ONLY registers.

Vertical active = 1200 or 0x4B0  
 CHA\_VERTICAL\_DISPLAY\_SIZE\_LOW = 0xB0  
 CHA\_VERTICAL\_DISPLAY\_SIZE\_HIGH = 0x04

Vertical back porch = Vertical blanking – (Vertical sync offset + Vertical sync pulse width)  
 Vertical back porch = 20 – (1 + 5)  
 Vertical back porch = 14 or 0x0E  
 CHA\_VERTICAL\_BACK\_PORCH = 0x0E

Horizontal front porch = Horizontal sync offset  
 Horizontal front porch = 50 or 0x32  
 CHA\_HORIZONTAL\_FRONT\_PORCH = 0x32

Vertical front porch = Vertical sync offset  
 Vertical front porch = 1  
 CHA\_VERTICAL\_FRONT\_PORCH = 0x01

In this example, the clock source for the SN65DSI84 is the DSI clock. When the MIPI D-PHY clock is used as the LVDS clock source, it is divided by the factor in DSI\_CLK\_DIVIDER (CSR 0x0B.7:3) to generate the FlatLink LVDS output clock. Additionally, LVDS\_CLK\_RANGE (CSR 0x0A.3:1) and CH\_DSI\_CLK\_RANGE(CSR 0x12) must be set to the frequency range of the FlatLink LVDS output clock and DSI Channel A input clock respectively for the internal PLL to operate correctly. After these settings are programmed, PLL\_EN (CSR 0x0D.0) should be set to enable the internal PLL.

```

LVDS_CLK_RANGE = 010b-62.5 MHz ≤ LVDS_CLK < 87.5 MHz
HS_CLK_SRC = 1 – LVDS pixel clock derived from MIPI D-PHY channel A HS continuous clock
DSI_CLK_DIVIDER = 0010b – Divide by 6
CHA_DSI_LANES = 00 – Four lanes are enabled
CHA_DSI_CLK_RANGE = 0x62 – 490 MHz ≤ frequency < 495 MHz
  
```

### 8.2.2.1 Example Script

This example configures the SN65DSI84 for the following configuration:

```

<aardvark>
  <configure i2c="1" spi="1" gpio="0" tpower="1" pullups="1"/>
  <i2c_birate khz="100"/>

=====SOFTRESET=====
  <i2c_write addr="0x2D" count="1" radix="16"gt;09 01</i2c_writegt;
  <sleep ms="10"/>

=====ADDR 0D=====
=====PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured=====
  <i2c_write addr="0x2D" count="1" radix="16"gt;0D 00</i2c_writegt;
  <sleep ms="10"/>

=====ADDR 0A=====
=====HS_CLK_SRC bit0=====
=====LVDS_CLK_Range bit 3:1=====
  <i2c_write addr="0x2D" count="1" radix="16"gt;0A 05</i2c_writegt;
  <sleep ms="10"/>

=====ADDR 0B=====
=====DSI_CLK_DIVIDER bit7:3=====
=====RefCLK multiplier(bit1:0)===== =====00 - LVDSclk=source clk, 01 - x2, 10 -x3, 11 - x4=====
  <i2c_write addr="0x2D" count="1" radix="16"gt;0B 28</i2c_writegt;
  <sleep ms="10"/>

=====ADDR 10=====
=====DSI Ch Cnfg Left_Right Pixels(bit7 - 0 for A ODD, B EVEN, 1 for the other config)=====
=====DSI Ch Mode(bit6:5) 00 - Dual, 01 - single, 10 - two single =====
=====CHA_DSI_Lanes(bit4:3), CHB_DSI_Lanes(bit2:1), 00 - 4, 01 - 3, 10 - 2, 11 - 1
=====SOT_ERR_TOL_DIS(bit0)=====
  <i2c_write addr="0x2D" count="1" radix="16"gt;10 26</i2c_writegt;
  <sleep ms="10"/>

=====ADDR 12=====
  <i2c_write addr="0x2D" count="1" radix="16"gt;12 62</i2c_writegt;
  <sleep ms="10"/>

=====ADDR 18=====
=====bit7: DE_Pol, bit6:HS_Pol, bit5:VS_Pol, bit4: LVDS Link Cfg, bit3:CHA 24bpp, bit2: CHB 24bpp,
bit1: CHA 24bpp fmt1, bit0: CHB 24bpp fmt1=====
  <i2c_write addr="0x2D" count="1" radix="16"gt;18 63</i2c_writegt;
  <sleep ms="10"/>

=====ADDR 19=====
  <i2c_write addr="0x2D" count="1" radix="16"gt;19 00</i2c_writegt;
  <sleep ms="10"/>

=====ADDR 1A=====
  <i2c_write addr="0x2D" count="1" radix="16"gt;1A 03</i2c_writegt;
  <sleep ms="10"/>

=====ADDR 20=====
  
```

```

=====CHA_LINE_LENGTH_LOW=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;20 80</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 21=====
=====CHA_LINE_LENGTH_HIGH=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;21 07</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 22=====
=====CHB_LINE_LENGTH_LOW=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;22 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 23=====
=====CHB_LINE_LENGTH_HIGH=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;23 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 24=====
=====CHA_VERTICAL_DISPLAY_SIZE_LOW=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;24 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 25=====
=====CHA_VERTICAL_DISPLAY_SIZE_HIGH=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;25 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 26=====
=====CHB_VERTICAL_DISPLAY_SIZE_LOW=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;26 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 27=====
=====CHB_VERTICAL_DISPLAY_SIZE_HIGH=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;27 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 28=====
=====CHA_SYNC_DELAY_LOW=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;28 20</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 29=====
=====CHA_SYNC_DELAY_HIGH=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;29 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 2A=====
=====CHB_SYNC_DELAY_LOW=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;2A 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 2B=====
=====CHB_SYNC_DELAY_HIGH=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;2B 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 2C=====
=====CHA_HSYNC_PULSE_WIDTH_LOW=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;2C 32</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 2D=====
=====CHA_HSYNC_PULSE_WIDTH_HIGH=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;2D 00</i2c_writeglT;
    <sleep ms="10"/>

=====ADDR 2E=====
=====CHB_HSYNC_PULSE_WIDTH_LOW=====
    <i2c_write addr="0x2D" count="1" radix="16"glT;2E 00</i2c_writeglT;
    <sleep ms="10"/>
    
```

```

=====ADDR 2F=====
=====CHB_HSYNC_PULSE_WIDTH_HIGH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;2F 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 30=====
=====CHA_VSYNC_PULSE_WIDTH_LOW=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;30 05</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 31=====
=====CHA_VSYNC_PULSE_WIDTH_HIGH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;31 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 32=====
=====CHB_VSYNC_PULSE_WIDTH_LOW=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;32 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 33=====
=====CHB_VSYNC_PULSE_WIDTH_HIGH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;33 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 34=====
=====CHA_HOR_BACK_PORCH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;34 2C</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 35=====
=====CHB_HOR_BACK_PORCH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;35 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 36=====
=====CHA_VER_BACK_PORCH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;36 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 37=====
=====CHB_VER_BACK_PORCH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;37 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 38=====
=====CHA_HOR_FRONT_PORCH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;38 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 39=====
=====CHB_HOR_FRONT_PORCH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;39 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 3A=====
=====CHA_VER_FRONT_PORCH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;3A 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 3B=====
=====CHB_VER_FRONT_PORCH=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;3B 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 3C=====
=====CHA/CHB TEST PATTERN(bit4 CHA, bit0 CHB)=====
      <i2c_write addr="0x2D" count="1" radix="16"gt;3C 00</i2c_writegt;
      <sleep ms="10"/>

=====ADDR 0D=====
=====PLL_EN(bit 0) - Enable LAST after addr 0A and 0B configured=====

```

```

<i2c_write addr="0x2D" count="1" radix="16"gl;0D 0l</i2c_writegl;
<sleep ms="10"/>

=====SOFTRESET=====
<i2c_write addr="0x2D" count="1" radix="16"gl;09 00</i2c_writegl;
<sleep ms="10"/>

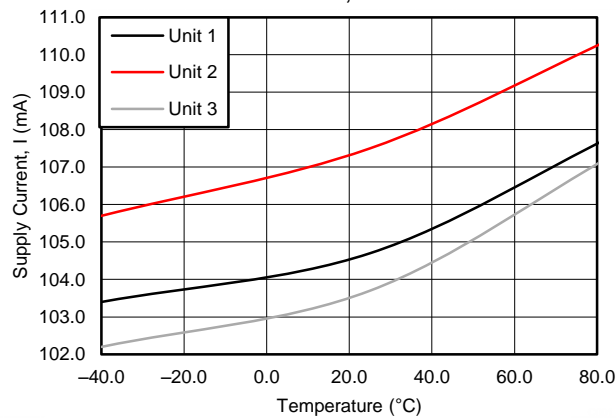
=====write=====
<i2c_write addr="0x2D" count="196" radix="16"gl;00</i2c_writegl;
<sleep ms="10"/>

=====Read=====
<i2c_read addr="0x2D" count="256" radix="16"gl;00</i2c_readgl;
<sleep ms="10"/>
</aardvark>

```

**8.2.3 Application Curve**

SN65DSI84: SINGLE Channel DSI to DUAL Channel LVDS, 1440 x 900



**Figure 19. Supply Current vs Temperature**

## 9 Power Supply Recommendations

### 9.1 V<sub>CC</sub> Power Supply

Each VCC power supply pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI83 device. It is recommended to have one bulk capacitor (1  $\mu$ F to 10  $\mu$ F) on it. It is also recommended to have the pins connected to a solid power plane.

### 9.2 V<sub>CORE</sub> Power Supply

This pin must have a 100-nF capacitor to ground connected as close as possible to the SN65DSI83 device. It is recommended to have one bulk capacitor (1  $\mu$ F to 10  $\mu$ F) on it. It is also recommended to have the pins connected to a solid power plane.

## 10 Layout

### 10.1 Layout Guidelines

#### 10.1.1 Package Specific

For the ZQE package, to minimize the power supply noise floor, provide good decoupling near the SN65DSI83 device power pins. The use of four ceramic capacitors (2  $\times$  0.1  $\mu$ F and 2  $\times$  0.01  $\mu$ F) provides good performance. At the least, TI recommends to install one 0.1- $\mu$ F and one 0.01- $\mu$ F capacitor near the SN65DSI83 device. To avoid large current loops and trace inductance, the trace length between decoupling capacitor and device power inputs pins must be minimized. Placing the capacitor underneath the SN65DSI83 device on the bottom of the PCB is often a good choice.

#### 10.1.2 Differential Pairs

- Differential pairs must be routed with controlled 100- $\Omega$  differential impedance ( $\pm$  20%) or 50- $\Omega$  single-ended impedance ( $\pm$ 15%).
- Keep away from other high speed signals
- Keep lengths to within 5 mils of each other.
- Length matching must be near the location of mismatch.
- Each pair must be separated at least by 3 times the signal trace width.
- The use of bends in differential traces must be kept to a minimum. When bends are used, the number of left and right bends must be as equal as possible and the angle of the bend must be  $\geq$  135 degrees. This arrangement minimizes any length mismatch caused by the bends and therefore minimizes the impact that bends have on EMI.
- Route all differential pairs on the same of layer.
- The number of vias must be kept to a minimum. It is recommended to keep the via count to 2 or less.
- Keep traces on layers adjacent to ground plane.
- Do NOT route differential pairs over any plane split.
- Adding Test points will cause impedance discontinuity and will therefore negatively impact signal performance. If test points are used, they must be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

#### 10.1.3 Ground

TI recommends that only one board ground plane be used in the design. This provides the best image plane for signal traces running above the plane. The thermal pad of the SN65DSI83 must be connected to this plane with vias.



## 10.2 Layout Example

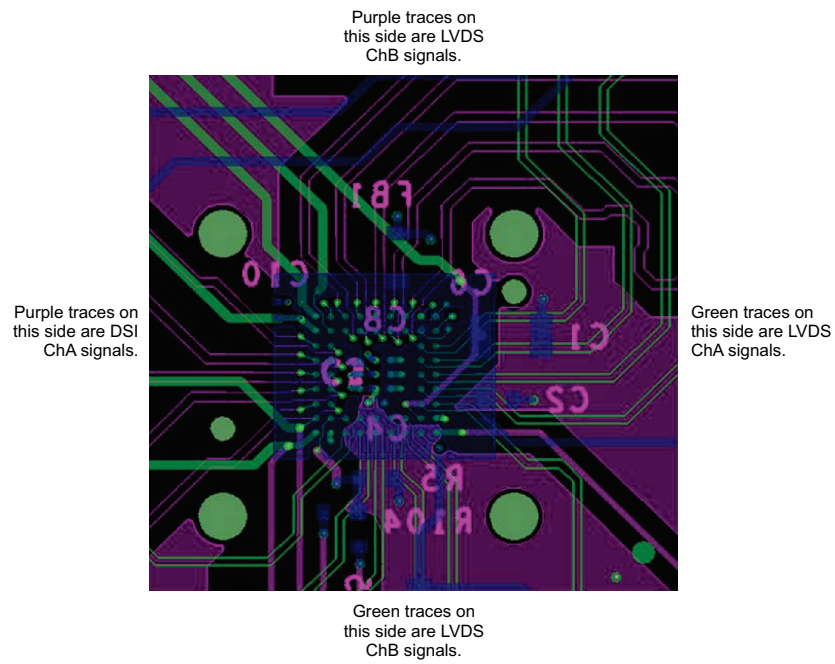


Figure 20. SN65DSI8x Layout Example

## 11 器件和文档支持

### 11.1 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。点击右上角的提醒我 (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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### 11.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.5 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65DSI84ZXHR	ACTIVE	NFBGA	ZXH	64	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	DSI84	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN65DSI84 :**

- Automotive : [SN65DSI84-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

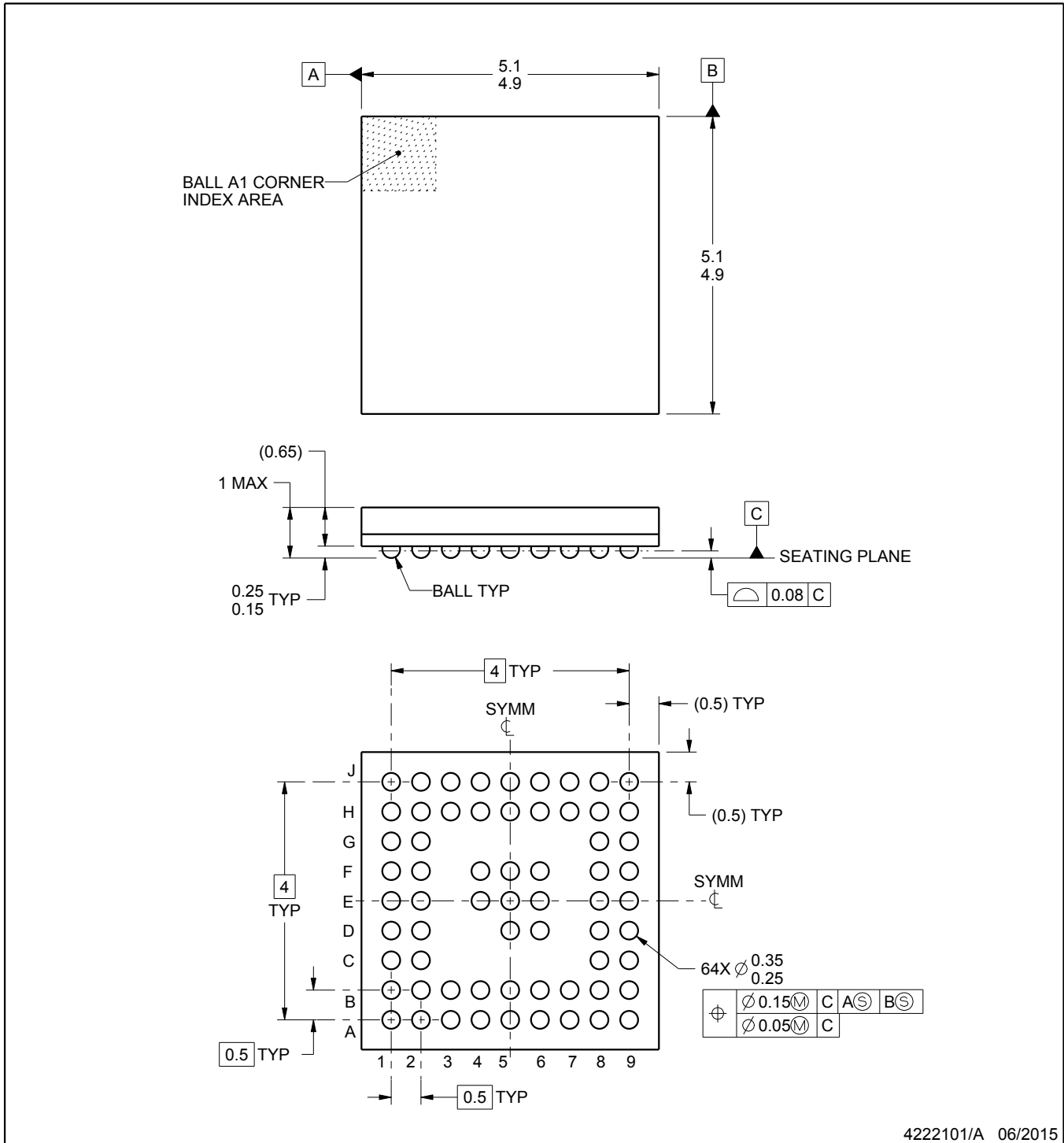

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65DSI84ZXHR	NFBGA	ZXH	64	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65DSI84ZXHR	NFBGA	ZXH	64	2500	336.6	336.6	31.8



4222101/A 06/2015

NOTES:

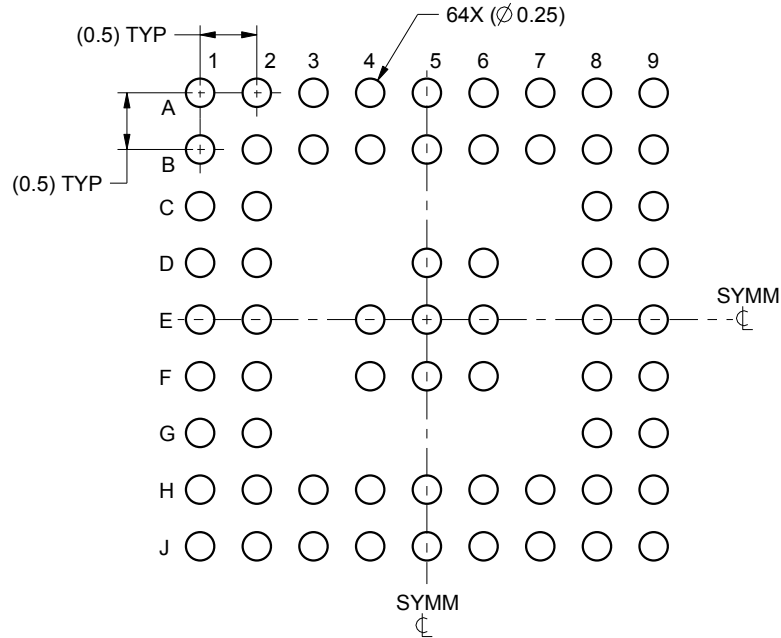
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

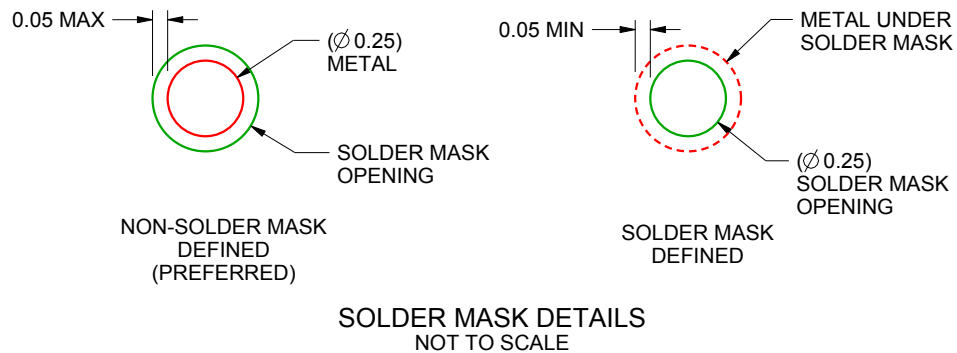
ZXH0064A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:15X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

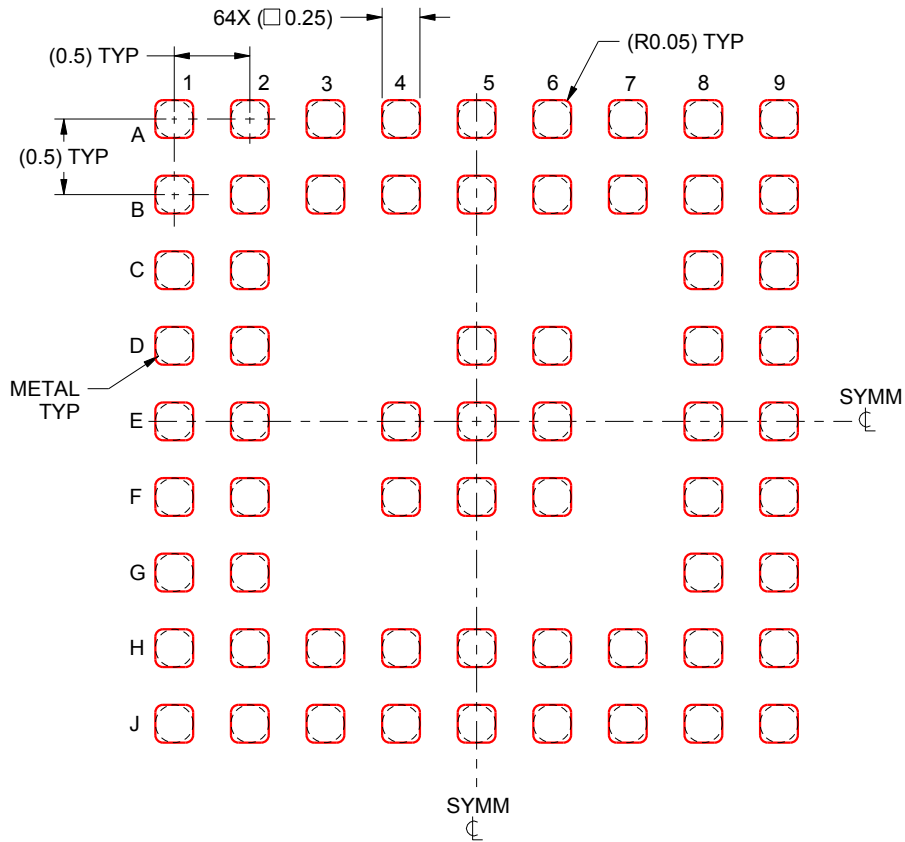


# EXAMPLE STENCIL DESIGN

ZXH0064A

NFBGA - 1 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:20X

4222101/A 06/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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