LM26480 带有独立使能和Power Good功能的车用双路 2MHz、1.5A 降压稳压器和双路 300mA LDO

1 特性

- 输入电压：2.8V 至 5.5V
- 兼容高级应用 处理器和现场可编程门阵列 (FPGA)
- 两个低压差线性稳压器 (LDO)，用于为内部处理器的运行和 I/O 供电
- 精密的内部基准电压
- 热过载保护
- 电流过载保护
- 针对 Buck1 和 Buck2 提供外部上电复位功能
- 配有欠压闭锁检测器，用于监视输入电源电压
- **降压直流/直流转换器（Buck）**
  - 1.5A 输出电流
  - V_{OUT} 范围：
  - Buck1：1.5A 时为 0.8V 至 2V
  - Buck2：1.5A 时为 1V 至 3.3V
  - 效率高达 96%
  - FB 电压精度为 ±3%
  - 2MHz 脉冲宽度调制 (PWM) 开关频率
  - 低负载条件下从 PWM 模式自动切换到脉冲频率调制 (PFM) 模式
  - 自动软启动
- **线性稳压器 (LDO)**
  - V_{OUT} 为 1V 至 3.5V
  - FB 电压精度为 ±3%
  - 300mA 输出电流
  - 25mV 压降（典型值）

2 应用

- 内核数字电源
- 应用 处理器
- 外设 I/O 电源
- 数字收音机
- 机器人驱动器
- 图像传输模块
- 低功耗数字 电感式触控不锈钢键盘参考设计

3 说明

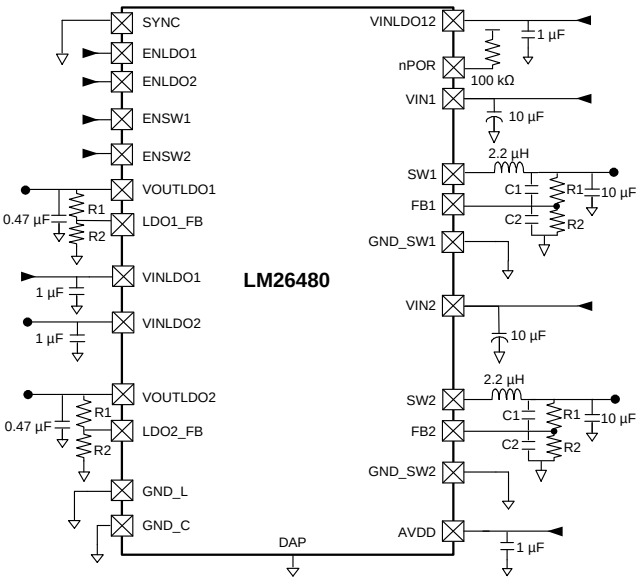
LM26480 是 多功能电源管理单元 (PMU)，针对低功耗数字应用进行了优化 。此器件集成了两个高效的 1.5A 降压直流/直流转换器和两个 300mA 线性稳压器。直流/直流降压转换器提供的典型效率为 96%，可实现最低功耗。该器件可提供 软启动、欠压锁定、电流过载保护、热过载保护功能，还具有内部开通复位 (POR) 电路，可监控降压转换器 1 和 2 上的输出电压电平。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM26480	WQFN (24)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision M (December 2016) to Revision N — **Page**

- Deleted the maximum lead temperature (soldering) from the *Absolute Maximum Ratings* table ... 5
- Changed the PBUCK1 and PBUCK2 equations in the *Junction Temperature* section ... 25
- 已更改 *静电放电注意事项* 声明 ... 33

Changes from Revision L (June 2016) to Revision M — **Page**

- 已更改 产品说明书的标题；将内容添加到*说明*部分中的第二句） ... 1
- Deleted SQ-BF option from Table 1 ... 3

Changes from Revision K (January 2015) to Revision L — **Page**

- 已添加 其他条目到*应用* ... 1
- Changed "θn" to "e_N" as symbol for supply output noise in Low Dropout Regulators EC table ... 6

Changes from Revision J (October 2014) to Revision K — **Page**

- Changed *Handling Ratings* table to *ESD Ratings* table ... 5
- Added full *Thermal Information* values. ... 5
- Added additional paragraph to *Functional Description* subsection to describe enable signal. ... 15

Changes from Revision I (May 2013) to Revision J **Page**

- 已添加 *器件信息表*，*ESD 额定值*表，*特性 描述*，*器件功能模式*，*应用和实施*，*电源相关建议*，*布局*，*器件和文档支持*以及*机械、封装和可订购信息*部分；已将一些曲线移至*应用曲线*部分。 1

5 Device Options

Table 1. Default Options

ORDER SUFFIX	SPEC	OSCILLATOR FREQUENCY	BUCK MODES	nPOR DELAY	UVLO	SYNC	AECQ
SQ-AA	NOPB	2 MHz	Auto-Mode	60 ms	Enabled	Disabled	No

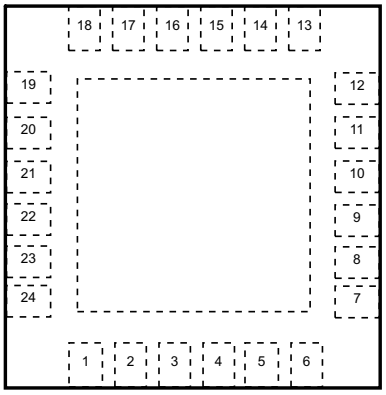
Table 2. Power Block Operation

POWER BLOCK INPUT(1)	ENABLED	DISABLED	NOTE
VINLDO12	VIN+	VIN+	Always powered
AVDD	VIN+	VIN+	Always powered
VIN1	VIN+	VIN+ or 0V	
VIN2	VIN+	VIN+ or 0V	
VINLDO1	≤ VIN+	≤ VIN+	If enabled, minimum VIN is 1.74 V
VINLDO2	≤ VIN+	≤ VIN+	If enabled, minimum VIN is 1.74 V

(1) VIN+ is the largest potential voltage on the device.

6 Pin Configuration and Functions

RTW Package
24-Pin WQFN
Top View



Pin Functions

PIN		I/O	TYPE(1)	DESCRIPTION
NO.	NAME			
1	VINLDO12	I	P	Analog power for internal functions (VREF, BIAS, I^2C, Logic)
2	SYNC	I	G/(D)	Frequency synchronization pin, which allows the user to connect an external clock signal to synchronize the PMIC internal oscillator. Default OFF and must be grounded when not used. Part number LM26480SQ-BF has this feature enabled. Contact Texas Instruments Sales Office/Distributors for availability of LM26480SQ-BF.
3	NPOR	O	D	nPOR Power on reset pin for both Buck1 and Buck 2. Open drain logic output 100-kΩ pullup resistor. nPOR is pulled to ground when the voltages on these supplies are not good. See *Flexible Power-On Reset (Power Good with Delay)* for more information.
4	GND_SW1	G	G	Buck1 NMOS power ground
5	SW1	O	P	Buck1 switcher output pin
6	VIN1	I	P	Power in from either DC source or battery to Buck1
7	ENSW1	I	D	Enable pin for Buck1 switcher, a logic HIGH enables Buck1. Pin cannot be left floating.
8	FB1	I	A	Buck1 input feedback terminal
9	GND_C	G	G	Non-switching core ground pin
10	AVDD	I	P	Analog Power for Buck converters
11	FB2	I	A	Buck2 input feedback terminal
12	ENSW2	I	D	Enable pin for Buck2 switcher, a logic HIGH enables Buck2. Pin cannot be left floating.
13	VIN2	I	P	Power in from either DC source or Battery to Buck2
14	SW2	O	P	Buck2 switcher output pin
15	GND_SW2	G	G	Buck2 NMOS
16	ENLDO2	I	D	LDO2 enable pin, a logic HIGH enables LDO2. Pin cannot be left floating.
17	ENLDO1	I	D	LDO1 enable pin, a logic HIGH enables LDO1. Pin cannot be left floating.
18	GND_L	G	G	LDO ground
19	VINLDO1	I	P	Power in from either DC source or battery to LDO1
20	LDO1	O	P	LDO1 Output
21	FBL1	I	A	LDO1 feedback terminal
22	FBL2	I	A	LDO2 feedback terminal
23	LDO2	O	P	LDO output
24	VINLDO2	I	P	Power in from either DC source or battery to LDO2.
DAP	DAP	G	G	Connection is not necessary for electrical performance, but it is recommended for better thermal dissipation.

(1) A: Analog Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin, D: Digital.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

	MIN	MAX	UNIT
VINLDO12, VIN1, AVDD, VIN2, VINLDO1, VINLDO2, ENSW1, FB1, FB2, ENSW2, ENLDO1, ENLDO2, SYNC, FBL1, FBL2	−0.3	6	V
GND to GND SLUG		±0.3	
Power dissipation, P_{D_MAX} (T_A = 85°C, T_{MAX} = 125°C)(3)		1.17	W
Junction temperature, T_{J-MAX}		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions: Bucks*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})$. See *Application and Implementation*.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions: Bucks

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{IN}	2.8		5.5	V
V_{EN}	0		(V_{IN} + 0.3 V)	
Junction temperature, T_J	–40		125	°C
Ambient temperature, T_A(1)	–40		85	°C

(1) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

7.4 Thermal Information

THERMAL METRIC(1)		LM26480 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 General Electrical Characteristics

Unless otherwise noted, V_{IN} = 3.6 V. Values and limits apply for T_J = 25°C.(1)(2)(3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	VINLDO12 shutdown current	V_{IN} = 3.6 V		0.5		µA
V_{POR}	Power-on reset threshold	V_{DD} falling edge(4)		1.9		V
T_{SD}	Thermal shutdown threshold	See(5)		160		°C
T_{SDH}	Thermal shutdown hysteresis	See(5)		20		
UVLO	Undervoltage lockout	Rising		2.9		V
		Failing		2.7		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical numbers represent the most likely norm.
(4) VPOR is voltage at which the EPROM resets. This is different from the UVLO on VINLDO12, which is the voltage at which the regulators shut off; and is also different from the nPOR function, which signals if the regulators are in a specified range.
(5) Specified by design. Not production tested.

7.6 Low Dropout Regulators, LDO1 and LDO2

Unless otherwise noted, V_{IN} = 3.6 V, C_{IN} = 1 µF, C_{OUT} = 0.47 µF, and values and limits apply for T_J = 25°C, unless otherwise specified. (1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operational voltage range	VINLDO1 and VINLDO2 PMOS pins(5) T_J = −40°C to 125°C	1.74		5.5	V
V_{FB}	FB voltage accuracy	T_J = −40°C to 125°C	–3%		3%	
ΔV_{OUT}	Line regulation	V_{IN} = (V_{OUT} + 0.3 V) to 5 V(6) Load current = 1 mA T_J = −40°C to 125°C			0.15	%/V
	Load regulation	V_{IN} = 3.6 V, T_J = −40°C to 125°C Load current = 1 mA to I_{MAX}			0.011	%/mA
I_{SC}	Short circuit current limit	LDO1-2, V_{OUT} = 0 V		500		mA
$V_{IN} - V_{OUT}$	Dropout voltage	Load current = 50 mA(7)		25		mV
		Load current = 50 mA(7) T_J = −40°C to 125°C			200	
PSRR	Power supply ripple rejection	F = 10 kHz, load current = I_{MAX}		45		dB
e_N	Supply output noise	10 Hz < F < 100 kHz		150		μV_{RMS}
I_Q	Quiescent current on	I_{OUT} = 0 mA		40		µA
		I_{OUT} = 0 mA, −40°C ≤ T_J ≤ 125°C			150	
	Quiescent current on	I_{OUT} = 300 mA		60		
		I_{OUT} = 300 mA, −40°C ≤ T_J ≤ 125°C			200	
	Quiescent current off	EN is de-asserted		0.03	1	µA
T_{ON}	Turnon time	Start-up from shutdown		300		µsec

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers represent the most likely norm.
(3) C_{IN}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) The device maintains a stable, regulated output voltage without a load.
(5) Pins 24, 19 can operate from V_{IN} min of 1.74 V to a V_{IN} max of 5.5 V. This rating is only for the series pass PMOS power FET. It allows the system design to use a lower voltage rating if the input voltage comes from a buck output.
(6) V_{IN} minimum for line regulation values is 1.8 V.
(7) Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

Low Dropout Regulators, LDO1 and LDO2 (continued)

Unless otherwise noted, V_{IN} = 3.6 V, C_{IN} = 1 µF, C_{OUT} = 0.47 µF, and values and limits apply for T_J = 25°C, unless otherwise specified. (1)(2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{OUT}	Output capacitor	Capacitance for stability 0°C ≤ T_J ≤ 125°C		0.47		µF
		−40°C ≤ T_J ≤ 125°C	0.33			
		−40°C ≤ T_J ≤ 125°C	0.68	1		
		Equivalent series resistance (ESR) T_J = −40°C to 125°C	5		500	mΩ

7.7 Buck Converters SW1, SW2

Unless otherwise noted, V_{IN} = 3.6 V, C_{IN} = 10 µF, C_{OUT} = 10 µF, L_{OUT} = 2.2 µH, and limits apply for T_J = 25°C, unless otherwise specified. (1) (2)(3)(4)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB} (5)	Feedback voltage		−3%		3%	
V_{OUT}	Line regulation	2.8 V < V_{IN} < 5.5 V I_{OUT} = 10 mA		0.089		%/V
	Load regulation	100 mA < I_{OUT} < I_{MAX}		0.0013		%/mA
Eff	Efficiency	Load current = 250 mA		96%		
I_{SHDN}	Shutdown supply current	EN is de-asserted		0.01	1	µA
f_{OSC}	Internal oscillator frequency	Default oscillator frequency = 2 MHz	1.6	2	2.4	MHz
		Default oscillator frequency = 2.1 MHz		2.1	2.5	
		Default oscillator frequency = 2.1 MHz T_J = −40°C to 125°C	1.7			
I_{PEAK}	Buck1 peak switching current limit			2	2.4	A
	Buck2 peak switching current limit			2	2.4	
I_Q	Quiescent current on (6)	No load PFM mode		33		µA
		No load PWM mode (forced PWM)		2		mA
R_{DSON} (P)	Pin-pin resistance PFET			200	400	mΩ
R_{DSON} (N)	Pin-pin resistance NFET			180	400	
T_{ON}	Turnon time	Start-up from shutdown		500		µsec
C_{IN}	Input capacitor	Capacitance for stability	10			µF
C_{OUT}	Output capacitor	Capacitance for stability	10			

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum (MIN) and maximum (MAX) limits are specified by design, test, or statistical analysis. Typical (TYP) numbers represent the most likely norm.
(3) C_{IN}, C_{OUT}: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.
(4) The device maintains a stable, regulated output voltage without a load.
(5) $V_{IN} \geq V_{OUT} + R_{DSON}(P) (I_{OUT} + 1/2\ I_{RIPPLE})$. If these conditions are not met, voltage regulation will degrade as load increases.
(6) Quiescent current is defined here as the difference in current between the input voltage source and the load at V_{OUT}.

7.8 I/O Electrical Characteristics

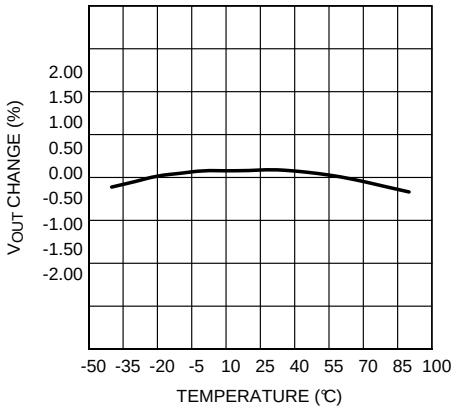
Limits apply over the entire junction temperature range for operation, T_J = −40°C to +125°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Input low level				0.4	V
V_{IH}	Input high level		0.7 × V_{DD}			

7.9 Power On Reset Threshold/Function (POR)

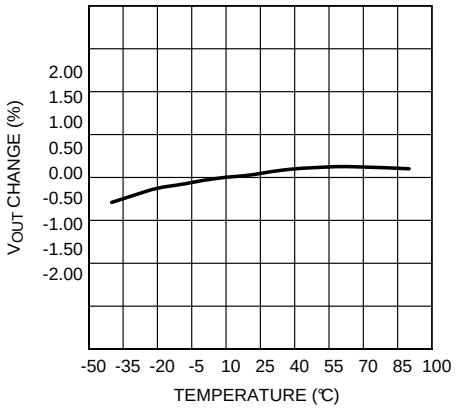
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
nPOR	nPOR = Power-on reset for Buck1 and Buck2	Default = 60 ms		60		ms
		Default = 130 µs		130		µs
nPOR Threshold	Percentage of target voltage Buck1 or Buck2	V_{BUCK1} AND V_{BUCK2} rising		92%		
		V_{BUCK1} OR V_{BUCK2} falling		82%		
V_{OL}	Output level low	Load = I_{OL} = 500 µA		0.23	0.5	V

7.10 Typical Characteristics — LDO



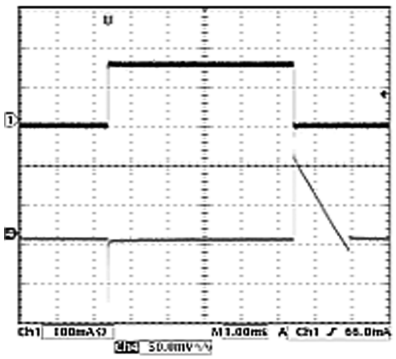
V_{IN} = 3.6 V V_{OUT} = 2.5 V Load = 100 mA

Figure 1. Output Voltage Change vs Temperature (LDO1)



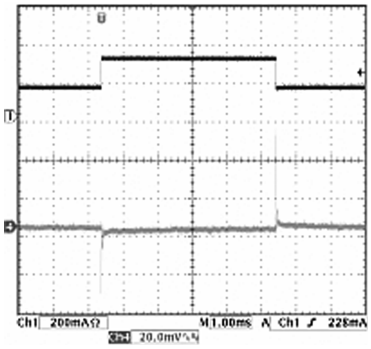
V_{IN} = 3.6 V V_{OUT} = 1.8 V Load = 100 mA

Figure 2. Output Voltage Change vs Temperature (LDO2)



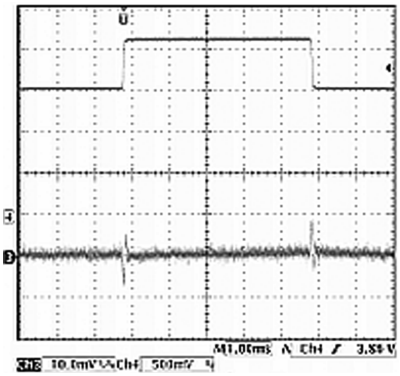
V_{IN} = 3.6 V V_{OUT} = 2.5 V Load = 0 to 150 mA

Figure 3. Load Transient



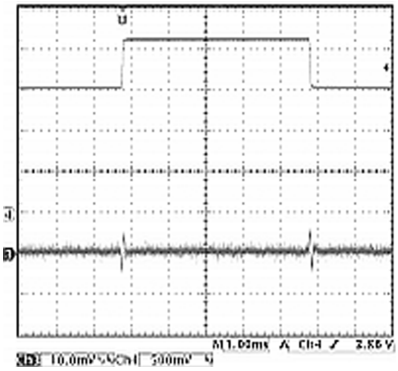
V_{IN} = 3.6 V V_{OUT} = 2.5 V Load = 150 to 300 mA

Figure 4. Load Transient



V_{IN} = 3.6 to 4.2 V V_{OUT} = 2.5 V Load = 100 mA

Figure 5. Line Transient (LDO1)



V_{IN} = 3.6 to 4.2 V V_{OUT} = 1.8 V Load = 150 mA

Figure 6. Line Transient (LDO2)

7.11 Typical Characteristics — Buck 2.8 V to 5.5 V

V_{IN} = 2.8 V to 5.5 V, T_A = 25°C

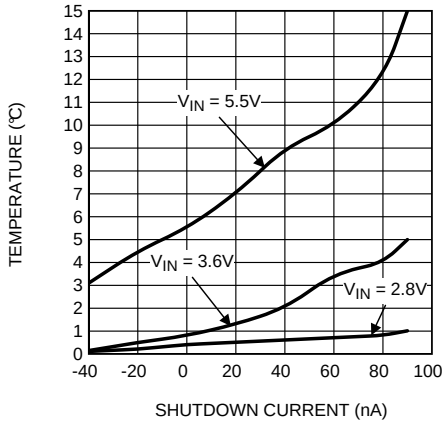
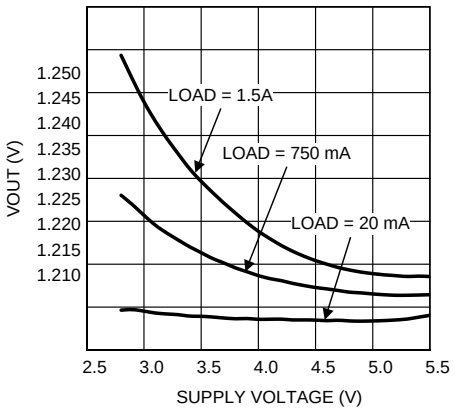
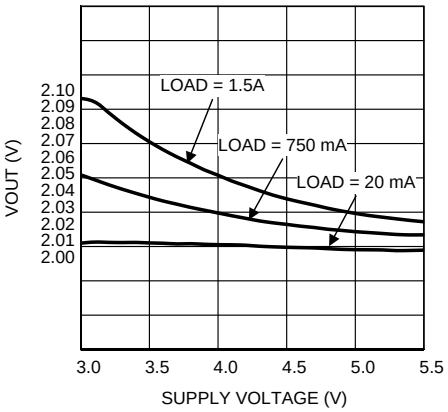


Figure 7. Shutdown Current vs. Temp



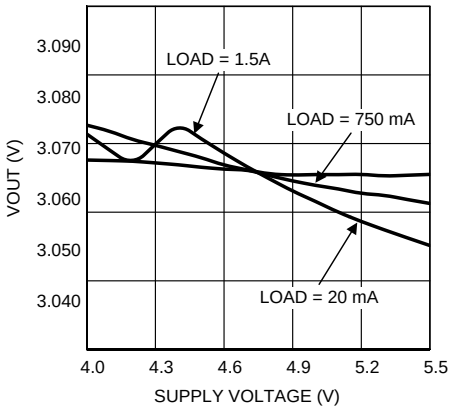
V_{OUT} = 1.2 V

Figure 8. Output Voltage vs. Supply Voltage



V_{OUT} = 2 V

Figure 9. Output Voltage vs. Supply Voltage

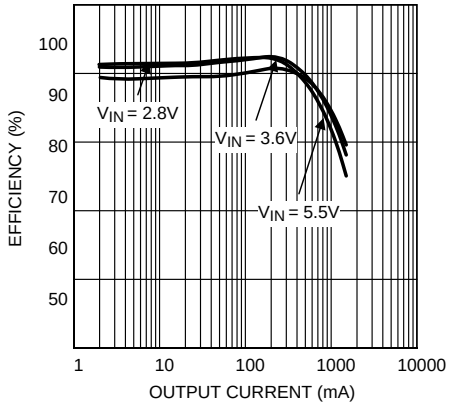


V_{OUT} = 3 V

Figure 10. Output Voltage vs. Supply Voltage

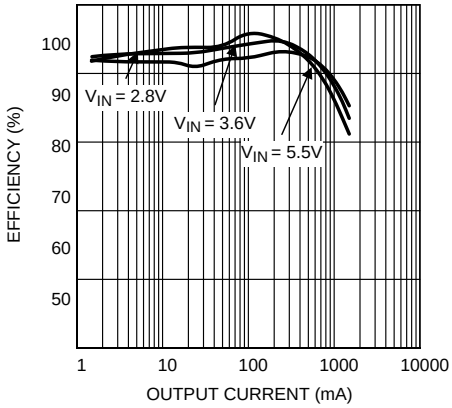
7.12 Typical Characteristics — Bucks 1 and 2

Output current transitions from PFM mode to PWM mode for Buck 1.



V_{OUT} = 1.2 V L = 2.2 µH

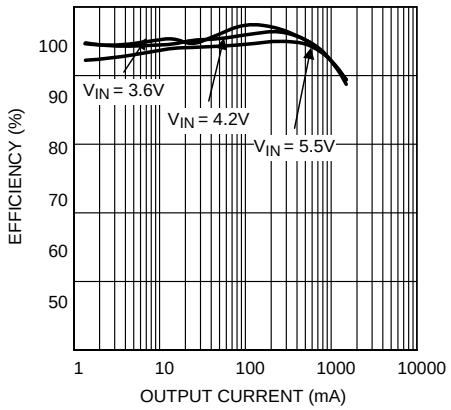
Figure 11. Efficiency vs. Output Current



V_{OUT} = 2 V L = 2.2 µH

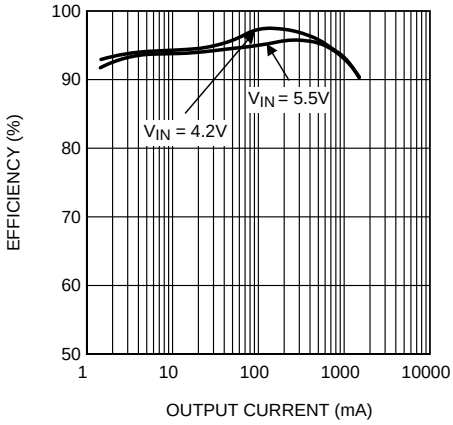
Figure 12. Efficiency vs. Output Current

Output Current transitions from PWM mode to PFM mode for Buck 2.



V_{OUT} = 3 V L = 2.2 µH

Figure 13. Efficiency vs. Output Current

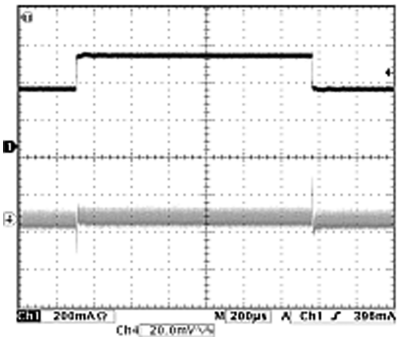


V_{OUT} = 3.5 V L = 2.2 µH

Figure 14. Efficiency vs. Output Current

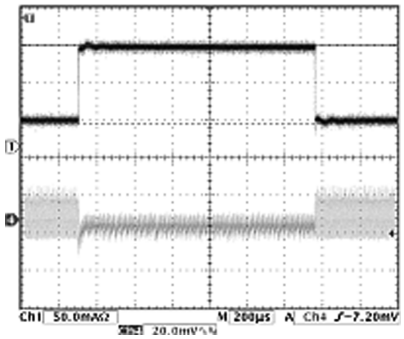
7.13 Typical Characteristics — Buck 3.6 V

V_{IN}= 3.6 V, T_A = 25°C, V_{OUT} = 1.2 V unless otherwise noted



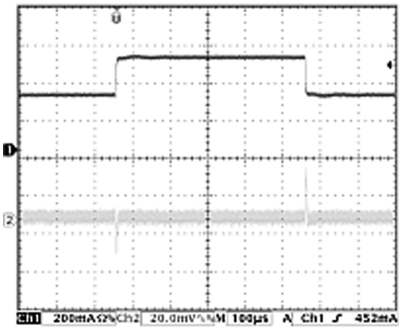
V_{OUT} = 1.2 V (PWM Mode)

Figure 15. Load Transient Response



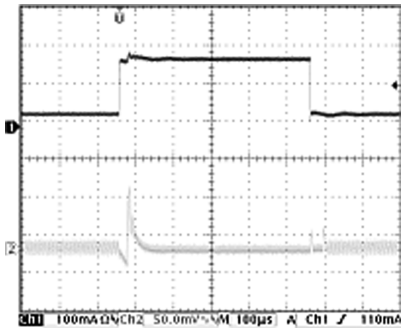
V_{OUT} = 1.2 V (PWM To PFM)

Figure 16. Mode Change By Load Transients



V_{IN} = 3.6 to 4.2 V V_{OUT} = 1.2 V Load = 250 mA

Figure 17. Line Transient Response



V_{IN} = 3 to 3.6 V V_{OUT} = 3 V Load = 250 mA

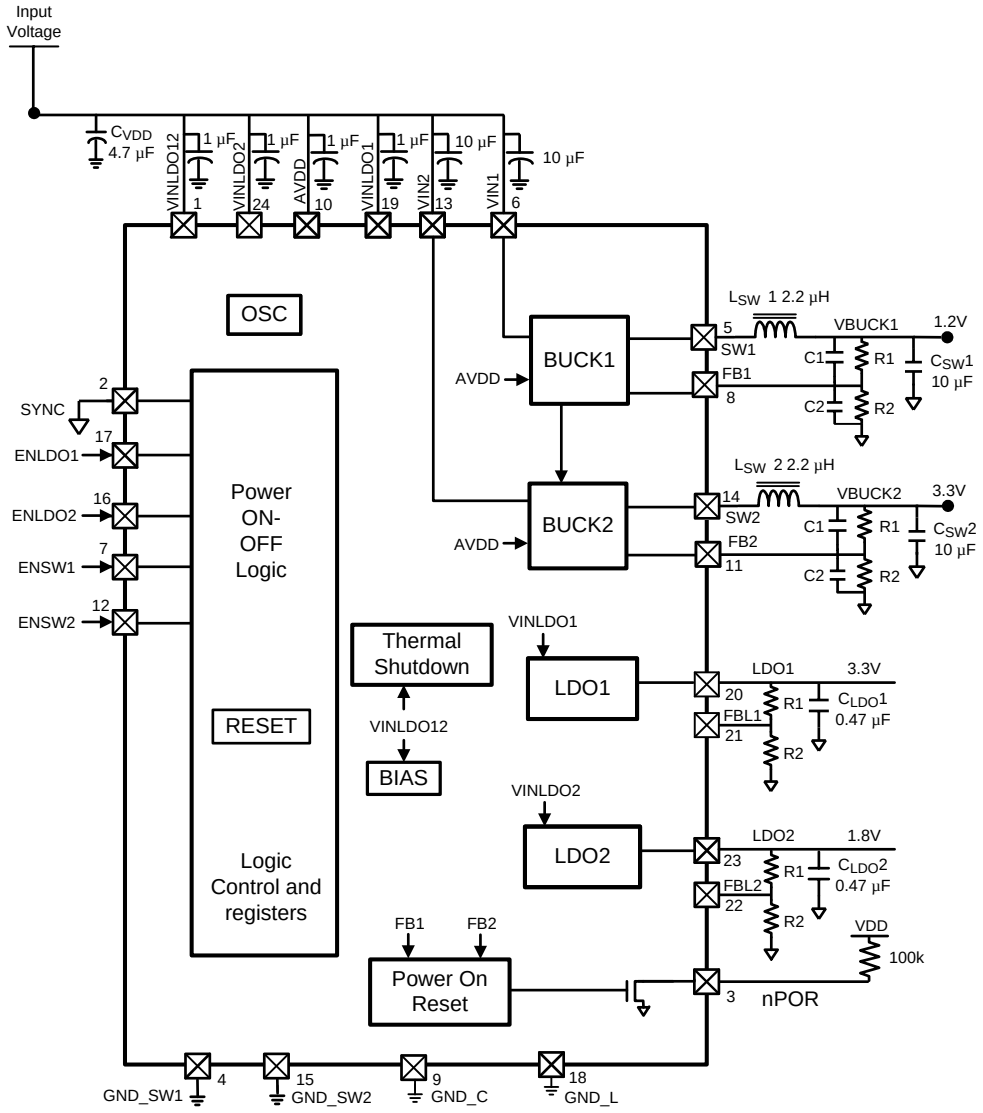
Figure 18. Line Transient Response

8 Detailed Description

8.1 Overview

The LM26480 is a multi-functional power management unit (PMU), optimized for low-power digital applications. This device integrates two highly efficient 1.5-A step-down DC-DC converters and two 300-mA linear regulators.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 DC-DC Converters

The LM26480 provides the DC-DC converters that supply the various power needs of the application by means of two linear low dropout regulators, LDO1 and LDO2, and two buck converters, SW1 and SW2. Table 3 lists the output characteristics of the various regulators.

Table 3. Supply Specification

SUPPLY	LOAD	OUTPUT	
		V_{OUT} RANGE (V)	I_{MAX} MAXIMUM OUTPUT CURRENT (mA)
LDO1	analog	1 to 3.5	300
LDO2	analog	1 to 3.5	300
SW1	digital	0.8 to 2	1500
SW2	digital	1 to 3.3	1500

8.3.1.1 Linear Low Dropout Regulators (LDOs)

LDO1 and LDO2 are identical linear regulators targeting analog loads characterized by low noise requirements. LDO1 and LDO2 are enabled through the ENLDO pin.

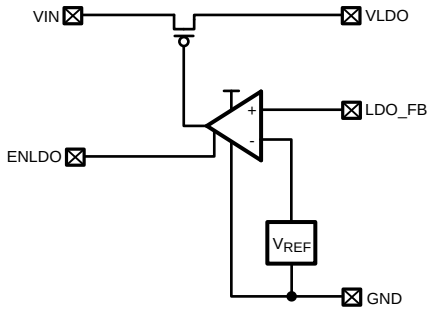


Figure 19. LDO Block Diagram

8.3.1.1.1 No-Load Stability

The LDOs remain stable and in regulation with no external load. This is an important consideration in some circuits, for example, CMOS RAM keep-alive applications.

8.3.1.2 SW1, SW2: Synchronous Step-Down Magnetic DC-DC Converters

8.3.1.2.1 Functional Description

The LM26480 incorporates two high-efficiency synchronous switching buck regulators, SW1 and SW2, that deliver a constant voltage from a single Li-Ion battery to the portable system processors. Using a voltage mode architecture with synchronous rectification, both bucks have the ability to deliver up to 1500 mA depending on the input voltage and output voltage (voltage headroom), and the inductor chosen (maximum current capability).

There are three modes of operation depending on the current required: PWM, PFM, and shutdown. PWM mode handles current loads of approximately 70 mA or higher, delivering voltage precision of ±3% with 90% efficiency or better. Lighter output current loads cause the device to automatically switch into PFM for reduced current consumption (I_Q = 33 µA typical) and a longer battery life. The Standby operating mode turns off the device, offering the lowest current consumption. PWM or PFM mode is selected automatically or PWM mode can be forced through the setting of the buck control register.

Both SW1 and SW2 can operate up to a 100% duty cycle (PMOS switch always on) for low drop out control of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage.

Additional features include soft-start, undervoltage lockout, current overload protection, and thermal overload protection.

The enable signal may be employed immediately after V_{IN} is applied to the device. However, V_{IN} must be stable for approximately 8 ms before enable single be asserted high to ensure internal bias, reference, and the flexible POR timing are stabilized. This initial delay is necessary only upon first time device power on.

8.3.1.2.2 Circuit Operation Description

A buck converter contains a control block, a switching PFET connected between input and output, a synchronous rectifying NFET connected between the output and ground (BCKGND pin) and a feedback path. During the first portion of each switching cycle, the control block turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of

$$\frac{V_{IN} - V_{OUT}}{L} \quad (1)$$

by storing energy in a magnetic field. During the second portion of each cycle, the control block turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. The inductor draws current from ground through the NFET to the output filter capacitor and load, which ramps the inductor current down with a slope of

$$\frac{-V_{OUT}}{L} \quad (2)$$

The output filter stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

8.3.1.2.3 Sync Function

The LM26480SQ-BF is the only version of the part that has the ability to use an external oscillator. The source must be 13 MHz nominal and operate within a range of 15.6 MHz and 10.4 MHz, proportionally the same limits as the 2-MHz internal oscillator. The LM26480SQ-BF has an internal divider which will divide the speed down by 6.5 to the nominal 2 MHz and use it for the regulators. This SYNC function replaces the internal oscillator and works in forced PWM only. The buck regulators no longer have the PFM function enabled. When the LM26480SQ-BF is sold with this feature enabled, the part will not function without the external oscillator present. Contact Texas Instruments Sales Office/Distributors for availability of LM26480SQ-BF.

8.3.1.2.4 PWM Operation

During PWM operation the converter operates as a voltage-mode controller with input voltage feed forward. This allows the converter to achieve excellent load and line regulation. The DC gain of the power stage is proportional to the input voltage. To eliminate this dependence, feed forward voltage inversely proportional to the input voltage is introduced.

8.3.1.2.5 Internal Synchronous Rectification

While in PWM mode, the buck uses an internal NFET as a synchronous rectifier to reduce rectifier forward voltage drop and associated power loss. Synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

8.3.1.2.6 Current Limiting

A current limit feature allows the converter to protect itself and external components during overload conditions. PWM mode implements current limiting using an internal comparator that trips at 2 A for both bucks (typical). If the output is shorted to ground the device enters a timed current limit mode where the NFET is turned on for a longer duration until the inductor current falls below a low threshold, ensuring inductor current has more time to decay, thereby preventing runaway.

8.3.1.2.7 PFM Operation

At very light loads, the converter enters PFM mode and operates with reduced switching frequency and supply current to maintain high efficiency.

The part will automatically transition into PFM mode when either of two conditions occurs for a duration of 32 or more clock cycles:

1. The inductor current becomes discontinuous, or

2. The peak PMOS switch current drops below the I_{MODE} level.

$$(\text{Typically } I_{MODE} < 66\text{ mA} + \frac{V_{IN}}{160\Omega}) \quad (3)$$

During PFM operation, the converter positions the output voltage slightly higher than the nominal output voltage during PWM operation, allowing additional headroom for voltage drop during a load transient from light to heavy load. The PFM comparators sense the output voltage via the feedback pin and control the switching of the output FETs such that the output voltage ramps between 0.8% and 1.6% (typical) above the nominal PWM output voltage. If the output voltage is below the 'high' PFM comparator threshold, the PMOS power switch is turned on. It remains on until the output voltage exceeds the *high* PFM threshold or the peak current exceeds the I_{PFM} level set for PFM mode. The typical peak current in PFM mode is:

$$I_{PFM} = 66\text{ mA} + \frac{V_{IN}}{80\Omega} \quad (4)$$

Once the PMOS power switch is turned off, the NMOS power switch is turned on until the inductor current ramps to zero. When the NMOS zero-current condition is detected, the NMOS power switch is turned off. If the output voltage is below the 'high' PFM comparator threshold (see Figure 20), the PMOS switch is again turned on and the cycle is repeated until the output reaches the desired level. Once the output reaches the 'high' PFM threshold, the NMOS switch is turned on briefly to ramp the inductor current to zero and then both output switches are turned off and the part enters an extremely low power mode. Quiescent supply current during this 'sleep' mode is less than 30 µA, which allows the part to achieve high efficiencies under extremely light load conditions. When the output drops below the *low* PFM threshold, the cycle repeats to restore the output voltage to approximately 1.6% above the nominal PWM output voltage.

If the load current should increase during PFM mode (see Figure 20) causing the output voltage to fall below the 'low2' PFM threshold, the part will automatically transition into fixed-frequency PWM mode.

8.3.1.2.8 SW1, SW2 Control

SW1 and SW2 are enabled/disabled through the external enable pins.

The Modulation mode PWM/PFM is by default automatic and depends on the load (see *Functional Description*). The modulation mode can be factory trimmed, forcing the buck to operate in PWM mode regardless of the load condition.

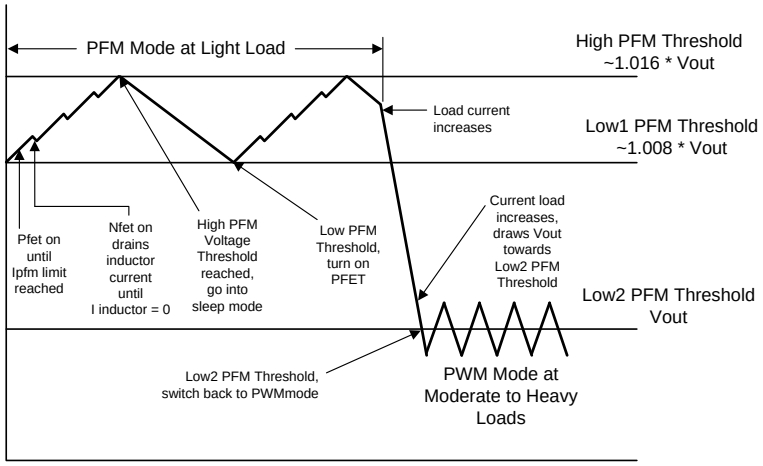


Figure 20. PWM/PFM Modulation

8.3.1.2.9 Shutdown Mode

During shutdown the PFET switch, reference, control and bias circuitry of the converters are turned off. The NFET switch will be on in shutdown to discharge the output. When the converter is enabled, soft start is activated. Disabling the converter during the system power up and undervoltage conditions is recommended when the supply is less than 2.8 V.

8.3.1.2.10 Soft Start

The soft-start feature allows the power converter to gradually reach the initial steady state operating point, thus reducing start-up stresses and surges. The two LM26480 buck converters have a soft-start circuit that limits in-rush current during start-up. During start-up the switch current limit is increased in steps. Soft start is activated only if EN goes from logic low to logic high after V_{IN} reaches 2.8 V. Soft start is implemented by increasing switch current limit in steps of 250 mA, 500 mA, 950 mA, and 2 A for both bucks (typical switch current limit). The start-up time thereby depends on the output capacitor and load current demanded at start-up.

8.3.1.2.11 Low Dropout Operation

The LM26480 can operate at 100% duty cycle (no switching; PMOS switch completely on) for low dropout support of the output voltage. In this way the output voltage will be controlled down to the lowest possible input voltage. When the device operates near 100% duty cycle, output voltage ripple is approximately 25 mV. The minimum input voltage needed to support the output voltage is

$$V_{IN,\ MIN} = I_{LOAD} \times (R_{DSON,\ PFET} + R_{INDUCTOR}) + V_{OUT} \quad (5)$$

where

- I_{LOAD} = Load current
- $R_{DSON,\ PFET}$ = Drain to source resistance of PFET switch in the triode region
- $R_{INDUCTOR}$ = Inductor resistance

8.3.1.2.12 Flexible Power-On Reset (Power Good with Delay)

The LM26480 is equipped with an internal Power-On-Reset (POR) circuit which monitors the output voltage levels on bucks 1 and 2. The nPOR is an open drain logic output which is logic LOW when either of the buck outputs are below 92% of the rising value, or when one or both outputs fall below 82% of the desired value. The time delay between output voltage level and nPOR is enabled is (130 µs, 60 ms, 100 ms, 200 ms), 60 ms by default. For any other delay option, other than the default, please consult a Texas Instruments Sales Representative. The system designer can choose the external pull-up resistor (value such as 100 kΩ) for the nPOR pin.

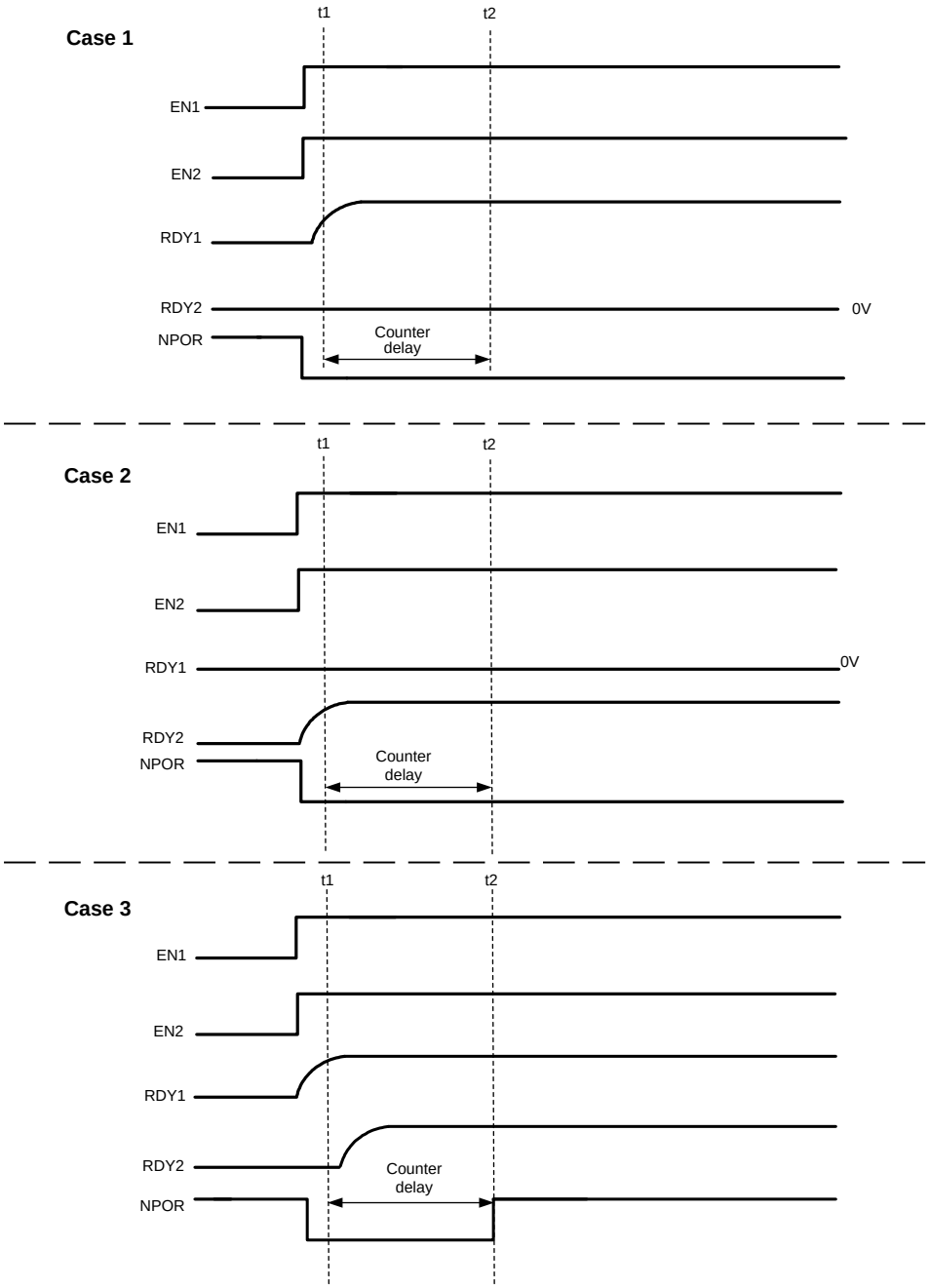


Figure 21. nPOR with Counter Delay

Figure 21 shows the simplest application of the POR where both switcher enables are tied together. In Case 1, EN1 causes nPOR to transition LOW and triggers the nPOR delay counter. If the power supply for Buck2 does not come on within that period, nPOR will stay LOW, indicating a power fail mode. Case 2 indicates the vice versa scenario if Buck1 supply did not come on. In both cases the nPOR remains LOW. Case 3 shows a typical application of the POR, where both switcher enables are tied together. Even if RDY1 ramps up slightly faster than RDY2 (or vice versa), the nPOR signal will trigger a programmable delay before going HIGH, as explained below.

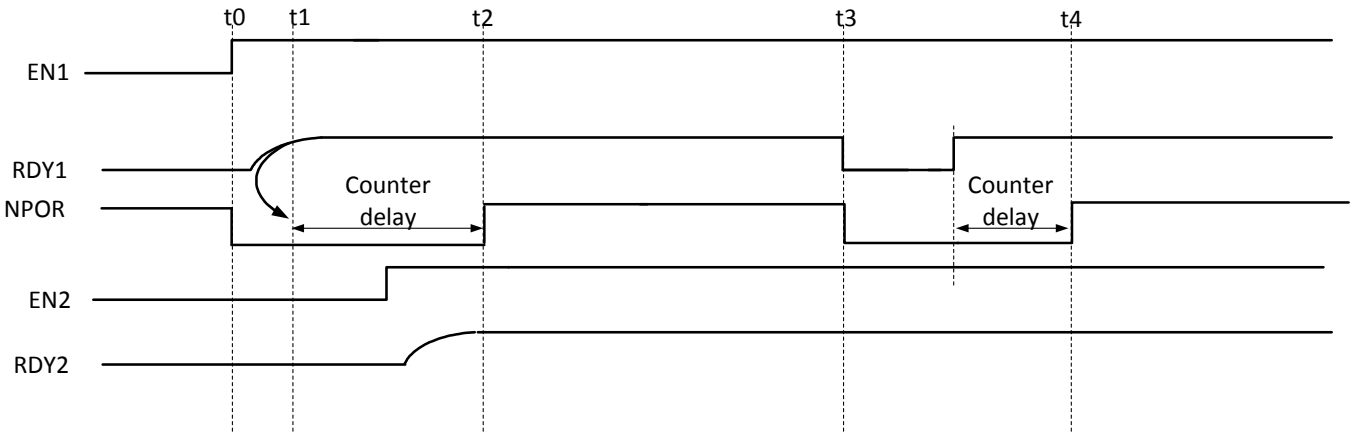


Figure 22. Faults Occurring in Counter Delay after Start-Up

Figure 22 details the Power Good with delay with respect to the enable signals EN1, and EN2. The RDY1, RDY2 are internal signals derived from the output of two comparators. Each comparator has been trimmed as follows:

Table 4. Comparator Trim

COMPARATOR LEVEL	BUCK SUPPLY LEVEL
HIGH	Greater than 92%
LOW	Less than 82%

The circuits for EN1 and RDY1 are symmetrical to EN2 and RDY2, so each reference to EN1 and RDY1 will also work for EN2 and RDY2 and vice versa.

If EN1 and RDY1 signals are High at time t1, then the RDY1 signal rising edge triggers the programmable delay counter (130 μs, 60 ms, 100 ms, 200 ms). This delay forces nPOR LOW between time interval t1 and t2. NPOR is then pulled high after the programmable delay is completed. Now if EN2 and RDY2 are initiated during this interval the nPOR signal ignores this event.

If either RDY1or RDY2 were to go LOW at t3 then the programmable delay is triggered again.

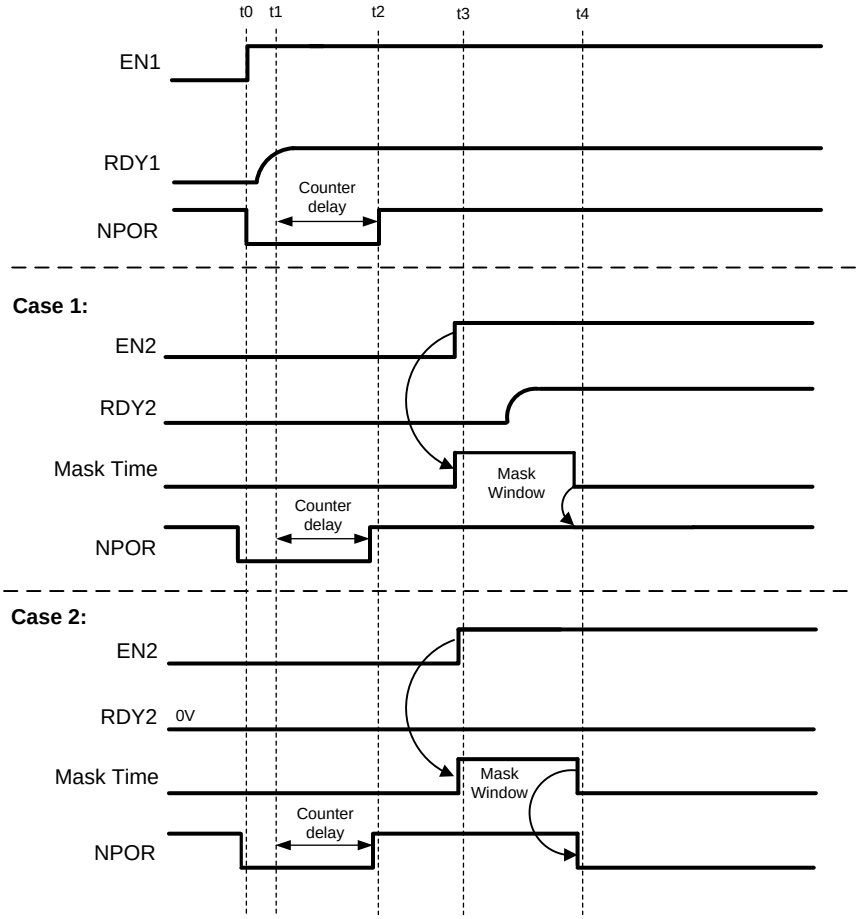


Figure 23. nPOR Mask Window

In Case 1 (Figure 23), we see that case where EN2 and RDY2 are initiated after triggered programmable delay. To prevent the nPOR being asserted again, a masked window (5 ms) counter delay is triggered off the EN2 rising edge. NPOR is still held HIGH for the duration of the mask, whereupon the nPOR status afterwards will depend on the status of both RDY1 and RDY2 lines.

In Case 2, we see the case where EN2 is initiated after the RDY1 triggered programmable delay, but RDY2 never goes HIGH (Buck2 never turns on). Normal operation operation of nPOR occurs wilth respect to EN1 and RDY1, and the nPOR signal is held HIGH for the duration of the mask window. We see that nPOR goes LOW after the masking window has timed out because it is now dependent on RDY1 and RDY2, where RDY2 is LOW.

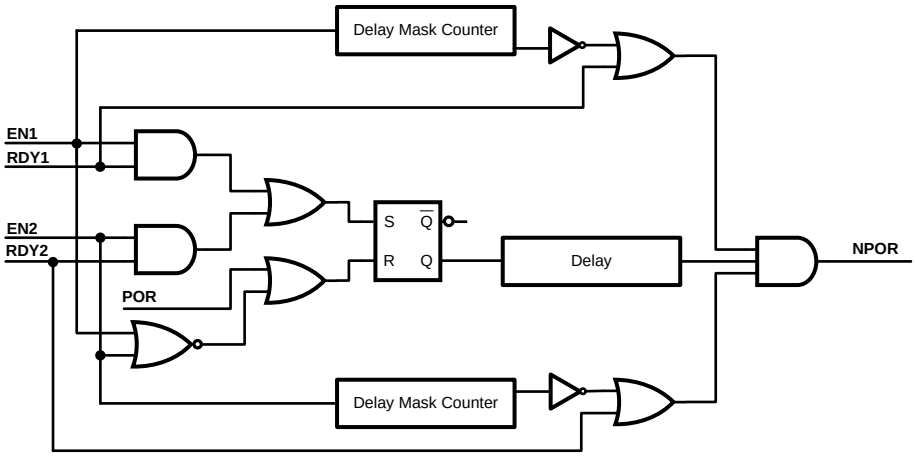


Figure 24. Design Implementation of the Flexible Power-On Reset

Design implementation of the flexible power-on reset. An internal power-on reset of the IC is used with EN1 and EN2 to produce a reset signal (LOW) to the delay timer nPOR. EN1 and RDY1 or EN2 and RDY2 are used to generate the set signal (HIGH) to the delay timer. S = R = 1 never occurs. The mask timers are triggered off EN1 and EN2 which are gated with RDY1, and RDY2 to generate outputs to the final AND gate to generate the nPOR.

8.3.1.2.13 Undervoltage Lockout

The LM26480 features an undervoltage lockout circuit. The function of this circuit is to continuously monitor the raw input supply voltage (VINLDO12) and automatically disable the four voltage regulators whenever this supply voltage is less than 2.8 VDC.

The circuit incorporates a bandgap based circuit that establishes the reference used to determine the 2.8 VDC trip point for a V_{IN} OK – Not OK detector. This V_{IN} OK signal is then used to gate the enable signals to the four regulators of the LM26480. When VINLDO12 is greater than 2.8 VDC the four **enables** control the four regulators; when VINLDO12 is less than 2.8 VDC the four regulators are **disabled** by the V_{IN} detector being in the *Not OK* state. The circuit has built-in hysteresis to prevent undesired signal variations.

8.4 Device Functional Modes

- External Programmable Output
- Up to 1.5 A output current for both Bucks
- External Power-on-Reset function for Buck1 and Buck2

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 External Component Selection

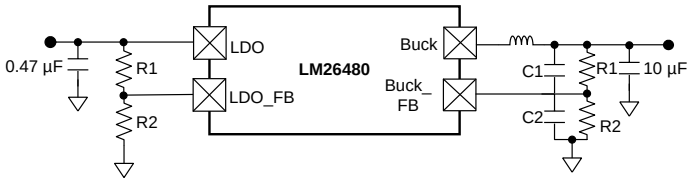


Figure 25. LDO Block Diagram

Table 5. Buck External Component Selection

TARGET V_{OUT} (V)	IDEAL RESISTOR VALUES		COMMON R VALUES		ACTUAL V_{OUT} w/ COM/R (V)	ACTUAL V_{OUT} DELTA FROM TARGET (V)	FEEDBACK CAPACITORS		POWER RAIL
	R1 (KΩ)	R2 (KΩ)	R1 (KΩ)	R2 (KΩ)			C1 (pF)	C2 (pF)	
0.8	120	200	121	200	0.803	0.002	15	none	Buck1
0.9	160	200	162	200	0.905	0.005	15	none	Only
1	200	200	200	200	1	0	15	none	^
1.1	240	200	240	200	1.1	0	15	none	|
1.2	280	200	280	200	1.2	0	12	none	|
1.3	320	200	324	200	1.31	0.01	12	none	Buck1
1.4	360	200	357	200	1.393	-0.008	10	none	And
1.5	400	200	402	200	1.505	0.005	10	none	Buck2
1.6	440	200	442	200	1.605	0.005	8.2	none	|
1.7	427	178	432	178	1.713	0.013	8.2	none	|
1.8	463	178	464	178	1.803	0.003	8.2	none	|
1.9	498	178	499	178	1.902	0.002	8.2	none	|
2	450	150	453	150	2.01	0.01	8.2	none	>
2.1	480	150	475	150	2.083	-0.017	8.2	none	^
2.2	422	124	422	124	2.202	0.002	8.2	none	|
2.3	446	124	442	124	2.282	-0.018	8.2	none	|
2.4	471	124	475	124	2.415	0.015	8.2	none	|
2.5	400	100	402	100	2.51	0.01	8.2	none	|
2.6	420	100	422	100	2.61	0.01	8.2	none	|
2.7	440	100	442	100	2.71	0.01	8.2	33	Buck2
2.8	460	100	464	100	2.82	0.02	8.2	33	Only
2.9	480	100	475	100	2.875	-0.025	8.2	33	|
3	500	100	499	100	2.995	-0.005	6.8	33	|
3.1	520	100	523	100	3.115	0.015	6.8	33	|
3.2	540	100	536	100	3.18	-0.02	6.8	33	|
3.3	560	100	562	100	3.31	0.01	6.8	33	|

The output voltages of the bucks of the LM26480 are established by the feedback resistor dividers R1 and R2 shown on the application circuit above. Equation 6 shows how to determine what value of V is:

$$V_{OUT} = V_{FB} (R1+R2)/R2 \quad (6)$$

where

- V_{FB} is the voltage on the Buck FBx pin.

The Buck control loop will force the voltage on V_{FB} to be 0.50 V ±3%.

Table 5 shows ideal resistor values to establish buck voltages from 0.8 V to 3.3 V along with common resistor values to establish these voltages. Common resistors do not always produce the target value, error is given in the delta column.

In addition to the resistor feedback, capacitor feedback C1 is always required, and depending on the output voltage capacitor C2 is also required.

INDUCTOR	VALUE	UNIT	DESCRIPTION	NOTES
$L_{SW}1,2$	2.2	µH	SW1,2 inductor	DCR 70 mΩ

9.1.2 Feedback Resistors for LDOs

See Figure 25.

Table 6. LDO External Component Selection

TARGET V_{OUT} (V)	IDEAL RESISTOR VALUES		COMMON R VALUES		ACTUAl V_{OUT} W/Com/R (V)
	R1 (KΩ)	R2 (KΩ)	R1 (KΩ)	R2 (KΩ)	
1	200	200	200	200	1
1.1	240	200	240	200	1.1
1.2	280	200	280	200	1.2
1.3	320	200	324	200	1.31
1.4	360	200	357	200	1.393
1.5	400	200	402	200	1.505
1.6	440	200	442	200	1.605
1.7	480	200	562	232	1.711
1.8	520	200	604	232	1.802
1.9	560	200	562	200	1.905
2	600	200	604	200	2.01
2.1	640	200	715	221	2.118
2.2	680	200	681	200	2.203
2.3	720	200	806	226	2.283
2.4	760	200	845	221	2.412
2.5	800	200	750	187	2.505
2.6	840	200	909	215	2.614
2.7	880	200	1100	249	2.709
2.8	920	200	1150	249	2.809
2.9	960	200	1210	255	2.873
3	1000	200	1000	200	3
3.1	1040	200	1000	191	3.118
3.2	1080	200	1000	187	3.174
3.3	1120	200	1210	215	3.314
3.4	1160	200	1210	210	3.381
3.5	1200	200	1210	200	3.525

The output voltages of the LDOs of the LM26480 are established by the feedback resistor dividers R1 and R2 shown on Figure 25 above. Equation 7 shows calculation for V_{OUT}:

$$V_{OUT} = V_{FB}(R1+R2)/R2 \quad (7)$$

where

- VFB is the voltage on the LDOX_FB pin.

The LDO control loop will force the voltage on VFB to be 0.50 V ±3%. The above table shows ideal resistor values to establish LDO voltages from 1 V to 3.5 V along with common resistor values to establish these voltages. Common resistors do not always produce the target value, error is given in the final column.

To keep the power consumed by the feedback network low it is recommended that R2 be established as about 200 kΩ. Lesser values of R2 are okay at the users discretion.

9.2 Typical Application

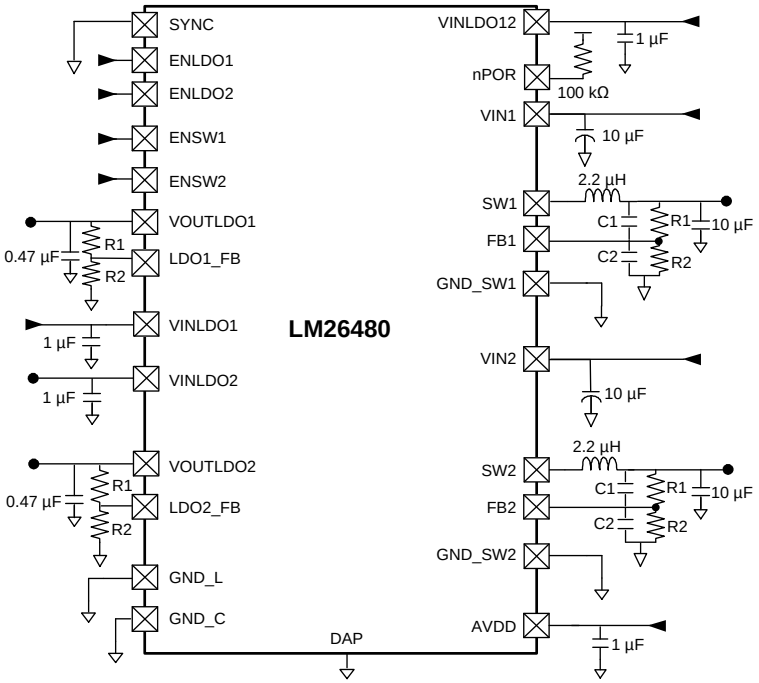


Figure 26. LM26480 Application Circuit

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 High V_{IN}- High Load Operation

Additional information is provided when the device is operated at extremes of V_{IN} and regulator loads. These are described in terms of the junction temperature and buck output ripple management.

9.2.1.2 Junction Temperature

The maximum junction temperature $T_{J\text{-}MAX\text{-}OP}$ of 125°C of the device package.

Equation 8 and Equation 9 demonstrate junction temperature determination, ambient temperature $T_{A\text{-}MAX}$, and total chip power must be controlled to keep T_J below this maximum:

$$T_{J\text{-}MAX\text{-}OP} = T_{A\text{-}MAX} + (R_{\theta JA}) \text{ [°C/Watt]} \times (P_{D\text{-}MAX}) \text{ [Watts]} \quad (8)$$

Total IC power dissipation $P_{D\text{-}MAX}$ is the sum of the individual power dissipation of the four regulators plus a minor amount for chip overhead. Chip overhead is bias, TSD, and LDO analog.

$$P_{D-MAX} = PLDO1 + PLDO2 + PBUCK1 + PBUCK2 + (0.0001A * VIN) \text{ [Watts]}$$

$$\text{Power dissipation of LDO1 (PLDO1)} = (VINLDO1 - VOUTLDO1) * IOUTLDO1 \text{ [V * A]}$$

$$\text{Power dissipation of LDO2 (PLDO2)} = (VINLDO2 - VOUTLDO2) * IOUTLDO2 \text{ [V * A]}$$

$$\text{Power dissipation of Buck1 (PBuck1)} = PIN - POUT = VOUTBUCK1 * IOUTBUCK1 * (1/\eta 1 - 1) \text{ [V * A]}$$

$\eta 1$ = efficiency of Buck1

$$\text{Power dissipation of Buck2 (PBuck2)} = PIN - POUT = VOUTBUCK2 * IOUTBUCK2 * (1/\eta 2 - 1) \text{ [V * A]}$$

$\eta 2$ = efficiency of Buck2

where

- η is the efficiency for the specific condition is taken from efficiency graphs. (9)

If V_{IN} and I_{LOAD} increase, the output ripple associated with the buck regulators also increases. This mainly occurs with V_{IN} > 5.2 V and a load current greater than 1.2 A. To ensure operation in this area of operation, TI recommends that the system designer circumvents the output ripple issues by installing Schottky diodes on the bucks(s) that are expected to perform under these extreme conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Output Inductors and Capacitors for SW1 AND SW2

There are several design considerations related to the selection of output inductors and capacitors:

- Load transient response;
- Stability;
- Efficiency;
- Output ripple voltage; and
- Overcurrent ruggedness.

The LM26480 has been optimized for use with nominal values 2.2 µH and 10 µF. If other values are needed for the design, please contact Texas Instruments sales with any concerns.

9.2.2.1.1 Inductor Selection for SW1 and SW2

TI recommends a nominal inductor value of 2.2 µH. It is important to ensure the inductor core does not saturate during any foreseeable operational situation.

Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

There are two methods to choose the inductor saturation current rating:

Recommended method:

Typical Application (continued)

The best way to ensure the inductor does not saturate is to choose an inductor that has saturation current rating greater than the maximum LM26480 current limit of 2.4 A. In this case the device prevents inductor saturation.

Alternate method:

If the recommended approach cannot be used, care must be taken to ensure that the saturation current is greater than the peak inductor current:

$$I_{SAT} > IL_{PEAK}$$

$$IL_{PEAK} = I_{OUTMAX} + \frac{I_{RIPPLE}}{2}$$

$$I_{RIPPLE} = \frac{D \times (V_{IN} - V_{OUT})}{L \times F}$$

$$D = \frac{V_{OUT}}{V_{IN} \times EFF}$$

- I_{SAT}: Inductor saturation current at operating temperature
- I_{LPEAK}: Peak inductor current during worst case conditions
- I_{OUTMAX}: Maximum average inductor current
- I_{RIPPLE}: Peak-to-peak inductor current
- V_{OUT}: Output voltage
- V_{IN}: Input voltage
- L: Inductor value in Henries at I_{OUTMAX}
- F: Switching frequency, Hertz
- D: Estimated duty factor
- EFF: Estimated power supply efficiency (10)

I_{SAT} may not be exceeded during any operation, including transients, start-up, high temperature, worst-case conditions, etc.

9.2.2.1.2 Suggested Inductors and Their Suppliers

MODEL	MANUFACTURER	DIMENSIONS (mm)	DCR (max) (mΩ)	$I_{SATURATION}$ (A) (values approx.)
DO3314-222MX	Coilcraft	3.3 × 3.3 × 1.4	200	1.8
LPO3310-222MX	Coilcraft	3.3 × 3.3 × 1	150	1.3
ELL6PG2R2N	Panasonic	6 × 6 × 2	37	2.2
ELC6GN2R2N	Panasonic	6 × 6 × 1.5	53	1.9
CDRH2D14NP-2R2NC	Sumida	3.2 × 3.2 × 1.5	94	1.5

9.2.2.2 Output Capacitor Selection for SW1 and SW2

TI recommends a ceramic output capacitor of 10 µF, 6.3 V with an ESR of less than 500 mΩ.

Output ripple can be estimated from the vector sum of the reactive (capacitor) voltage component and the real (ESR) voltage component of the output capacitor.

$$V_{COUT} = \frac{I_{RIPPLE}}{8 \times F \times C_{OUT}}$$

$$V_{ROUT} = I_{RIPPLE} \times ESR_{COUT}$$

$$V_{PPOUT} = \sqrt{V_{COUT}^2 + V_{ROUT}^2}$$

- V_{COUT}: Estimated reactive output ripple
- V_{ROUT}: Estimated real output ripple
- V_{PPOUT}: Estimated peak-to-peak output ripple (11)

The output capacitor needs to be mounted as close as possible to the output pin of the device. For better temperature performance, X7R or X5R types are recommended. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0805 and 0603.

DC bias characteristics vary from manufacturer to manufacturer and by case size. DC bias curves should be requested from them as part of the capacitor selection process. ESR is typically higher for smaller packages.

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

Note that the output voltage ripple is dependent on the inductor current ripple and the equivalent series resistance of the output capacitor (ESR_{COUT}). ESR_{COUT} is frequency dependent as well as temperature dependent. The R_{ESR} should be calculated with the applicable switching frequency and ambient temperature.

9.2.2.3 Input Capacitor Selection for SW1 and SW2

It is required to use a ceramic input capacitor of at least 4.7 µF and 6.3 V with an ESR of less than 500 mΩ.

The input power source supplies average current continuously. During the PFET switch on-time, however, the demanded di/dt is higher than can be typically supplied by the input power source. This delta is supplied by the input capacitor.

A simplified “worst case” assumption is that all of the PFET current is supplied by the input capacitor. This will result in conservative estimates of input ripple voltage and capacitor RMS current. Input ripple voltage is estimated in Equation 12:

$$V_{PPIN} = \frac{I_{OUT} \times D}{C_{IN} \times F} + I_{OUT} \times ESR_{CIN}$$

- V_{PPIN}: Estimated peak-to-peak input ripple voltage
- I_{OUT}: Output current, Amps
- $C_{IN:}$ Input capacitor value, Farads
- $ESR_{IN:}$ Input capacitor ESR, Ohms (12)

This capacitor is exposed to significant RMS current, so it is important to select a capacitor with an adequate RMS current rating. Capacitor RMS current estimated as follows:

$$I_{RMSCIN} = \sqrt{D \times \left(I_{OUT}^2 + \frac{I_{RIPPLE}}{12}\right)^2}$$

- I_{RSCIN}: Estimated input capacitor RMS current (13)

Table 7. Suggested Capacitors and Their Suppliers

MODEL	TYPE	VENDOR	VOLTAGE RATING (V)	CASE SIZE
4.7 µF for CIN				
C2012X5R0J475K	Ceramic, X5R	TDK	6.3	0805, (2012)
JMK212BJ475K	Ceramic, X5R	Taiyo-Yuden	6.3	0805, (2012)
GRM21BR60J475K	Ceramic, X5R	Murata	6.3	0805, (2012)
C1608X5R0J475K	Ceramic, X5R	TDK	6.3	0603, (1608)
10 µF for COUT				
GRM21BR60J106K	Ceramic, X5R	Murata	6.3	0805, (2012)
JMK212BJ106K	Ceramic, X5R	Taiyo-Yuden	6.3	0805, (2012)
C2012X5R0J106K	Ceramic, X5R	TDK	6.3	0805, (2012)
C1608X5R0J106K	Ceramic, X5R	TDK	6.3	0603, (1608)

9.2.2.4 LDO Capacitor Selection

9.2.2.4.1 Input Capacitor

An input capacitor is required for stability. TI recommends that a 1-µF capacitor be connected between the LDO input pin and ground (this capacitance value may be increased without limit). This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

CAUTION

Tantalum capacitors can suffer catastrophic failures due to surge currents when connected to a low impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be specified by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1 µF over the entire operating temperature range.

9.2.2.4.2 Output Capacitor

The LDOs on the LM26480 are designed specifically to work with very small ceramic output capacitors. A 1-µF ceramic capacitor (temperature types Z5U, Y5V, or X7R) with ESR between 5 mΩ to 500 mΩ, are suitable in the application circuit. It is also possible to use tantalum or film capacitors at the device output C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost. The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

9.2.2.4.3 Capacitor Characteristics

The LDOs are designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest, least expensive and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1-µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LDOs.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependent on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 27 shows a typical graph comparing different capacitor case sizes in a capacitance vs. DC bias plot.

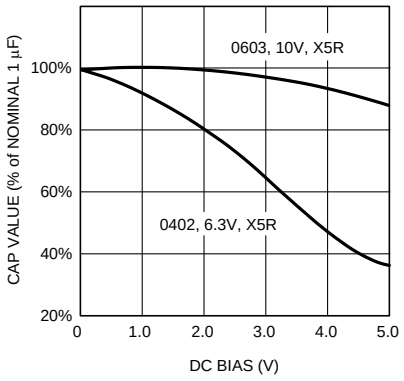


Figure 27. Capacitance vs DC Bias

As shown in Figure 27, increasing the DC bias condition can result in the capacitance value that falls below the minimum value given in the recommended capacitor specifications table. Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (such as 0402) may not be suitable in the actual application.

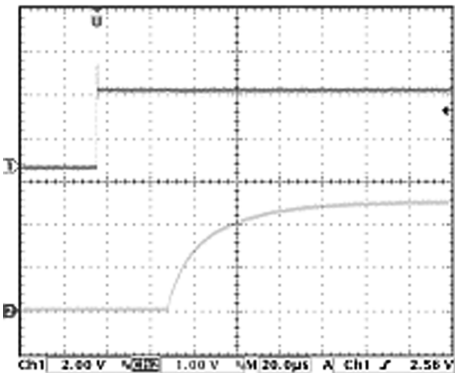
The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to 125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to 85°C. Many large value ceramic capacitors, larger than 1 μF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47-μF to 4.7-μF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

Table 8. Capacitor Characteristics

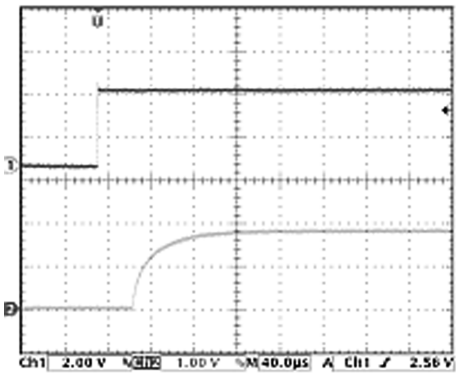
CAPACITOR	MIN VALUE (μF)	DESCRIPTION	RECOMMENDED TYPE
CLDO1	0.47	LDO1 output capacitor	Ceramic, 6.3V, X5R
CLDO2	0.47	LDO2 output capacitor	
CSW1	10	SW1 output capacitor	
CSW2	10	SW2 output capacitor	

9.2.3 Application Curves



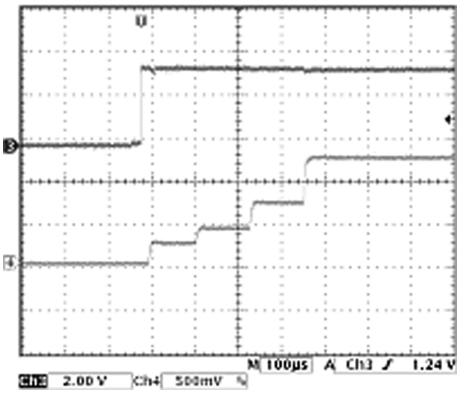
V_{IN} = 0 to 3.6 V V_{OUT} = 2.5 V Load = 1 mA

Figure 28. Enable Start-Up Time (LDO1)



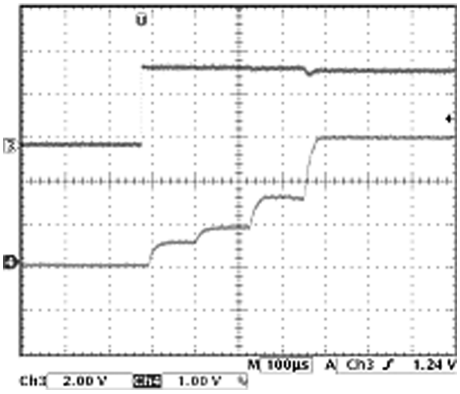
V_{IN} = 0 to 3.6 V V_{OUT} = 1.8 V Load = 1 mA

Figure 29. Enable Start-Up Time (LDO2)



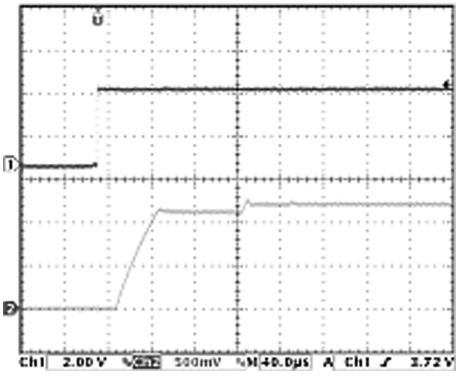
V_{IN} = 1.2 V Load = 1.5 A

Figure 30. Start-Up Into PWM Mode



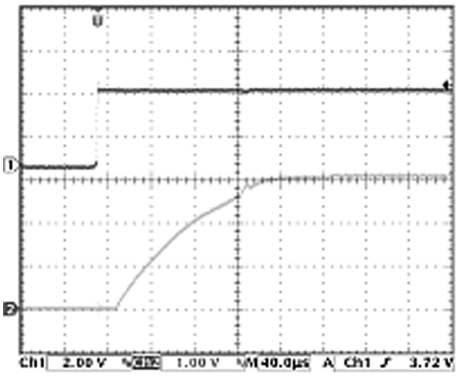
V_{IN} = 3 V Load = 1.5 A

Figure 31. Start-Up Into PWM Mode



V_{IN} = 1.2 V Load = 30 mA

Figure 32. Start-Up Into PFM Mode



V_{IN} = 3 V Load = 30 mA

Figure 33. Start-Up Into PFM Mode

10 Power Supply Recommendations

All power inputs should be tied to the main VDD source (that is, a battery), unless the user wishes to power it from another source. (that is, powering LDO from Buck output).

The analog VDD inputs power the internal bias and error amplifiers, so they should be tied to the main VDD. The analog VDD inputs must have an input voltage between 2.8 V and 5.5 V, as specified in the *Recommended Operating Conditions: Bucks* section of this datasheet.

The other V_{IN} pins (VINLDO1, VINLDO2, VIN1, VIN2) can actually have inputs lower than 2.8 V, as long as they are higher than the programmed output (0.3 V). The analog and digital grounds should be tied together outside of the chip to reduce noise coupling.

11 Layout

11.1 Layout Guidelines

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss ii the traces. These can send erroneous signals to the DC-DC converter device, resulting in poor regulation or instability. Poor layout can also result in re-flow problems leading to poor solder joints, which can result in erratic or degraded performance.

Good layout for the LM26480 bucks can be implemented by following a few simple design rules, as shown in Figure 34.

1. Place the buck inductor and filter capacitors close together and make the trace short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor close to the buck.
2. Arrange the components so that the switching current loops curl in the same direction. During the first halt of each cycle, current flows from the input filter capacitor, through the buck and inductor to the output filter capacitor and back through ground, forming a current loop. In the second half of each cycle, current is pulled up from ground, through the buck by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two half-cycles and reduces radiated noise.
3. Connect the ground pins of the buck, and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground–plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the buck by giving it a low-impedance ground connection.
4. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces
5. R_{OUT} noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the buck circuit and should be routed directly from FB to VOUT at the output capacitor and must be routed opposite to noise components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (because this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

For more information on board layout techniques, refer to *AN-1187 Leadless Leadframe Package (LLP)* on TI's website. This application note also discusses package handling, solder stencil, and the assembly process.

11.2 Layout Example

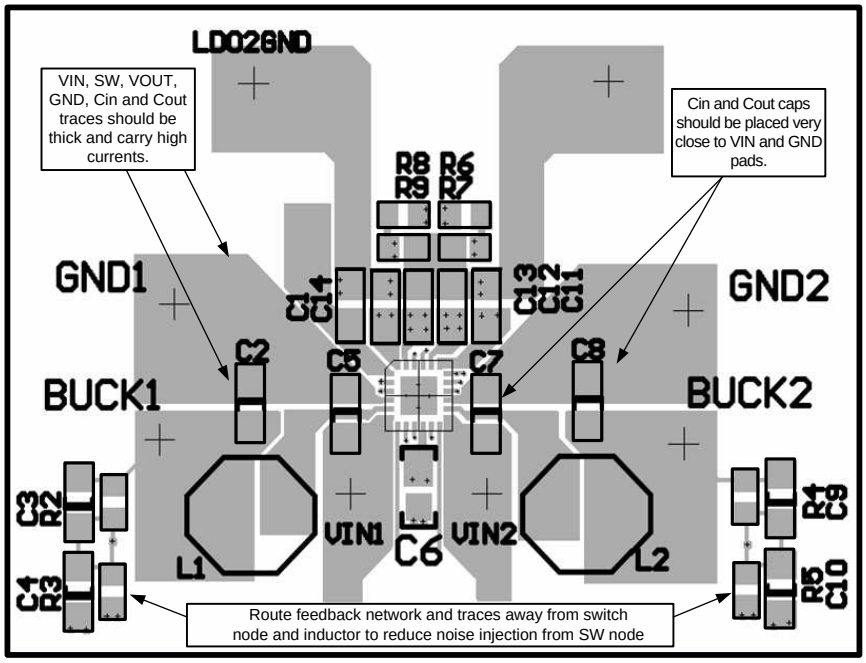


Figure 34. Board Layout Design Rules for the LM26480

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.2 文档支持

12.2.1 相关文档

相关文档如下：

- *《AN-1187 无引线框架封装 (LLP)》*
- *《优化国防/工业 应用的按位取反恢复能力和 PMU 设计》*
- *《先进 FPGA 电源设计的注意事项》*
- *《AN-1800 适用于LM26480 的评估套件 - 具有双路低噪音线性稳压器的双路直流/直流降压稳压器》*

12.3 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM26480SQ-AA/NOPB	ACTIVE	WQFN	RTW	24	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	26480AA	Samples
LM26480SQX-AA/NOPB	ACTIVE	WQFN	RTW	24	4500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	26480AA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

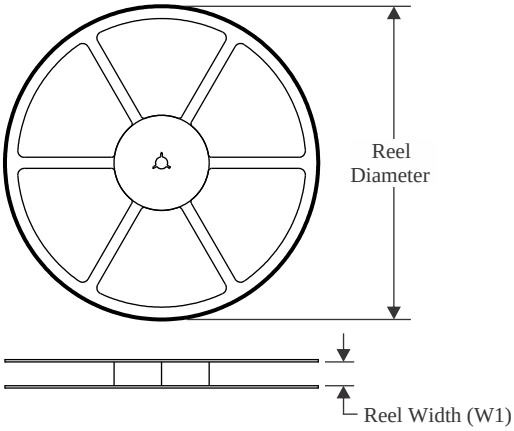
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

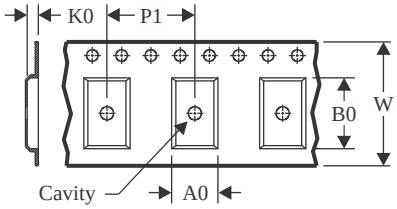
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

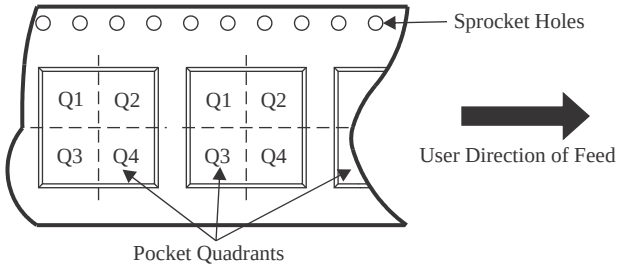


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

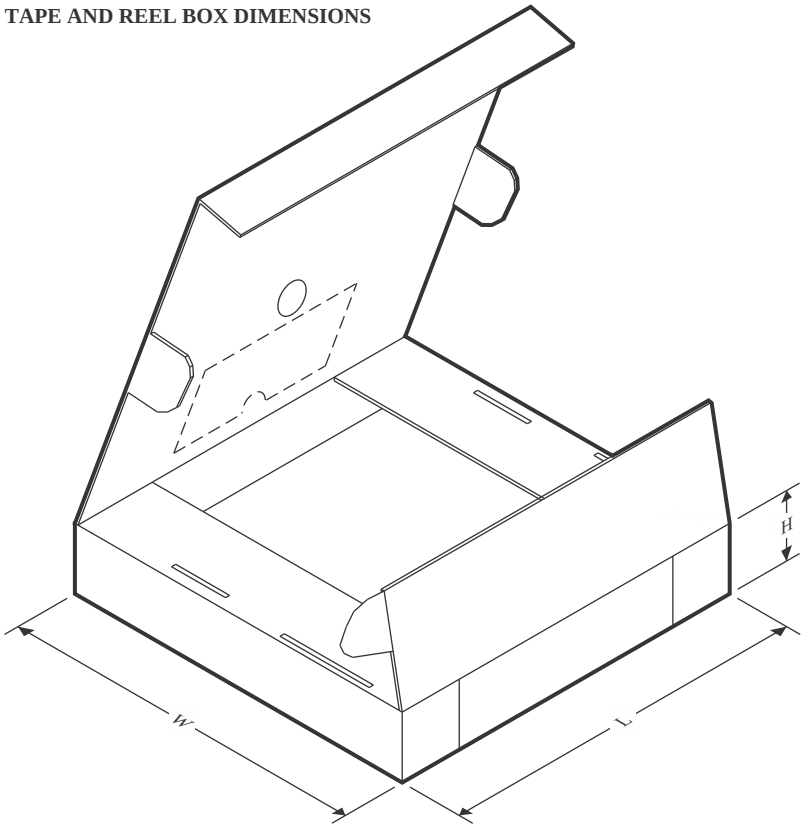
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM26480SQ-AA/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM26480SQX-AA/NOPB	WQFN	RTW	24	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

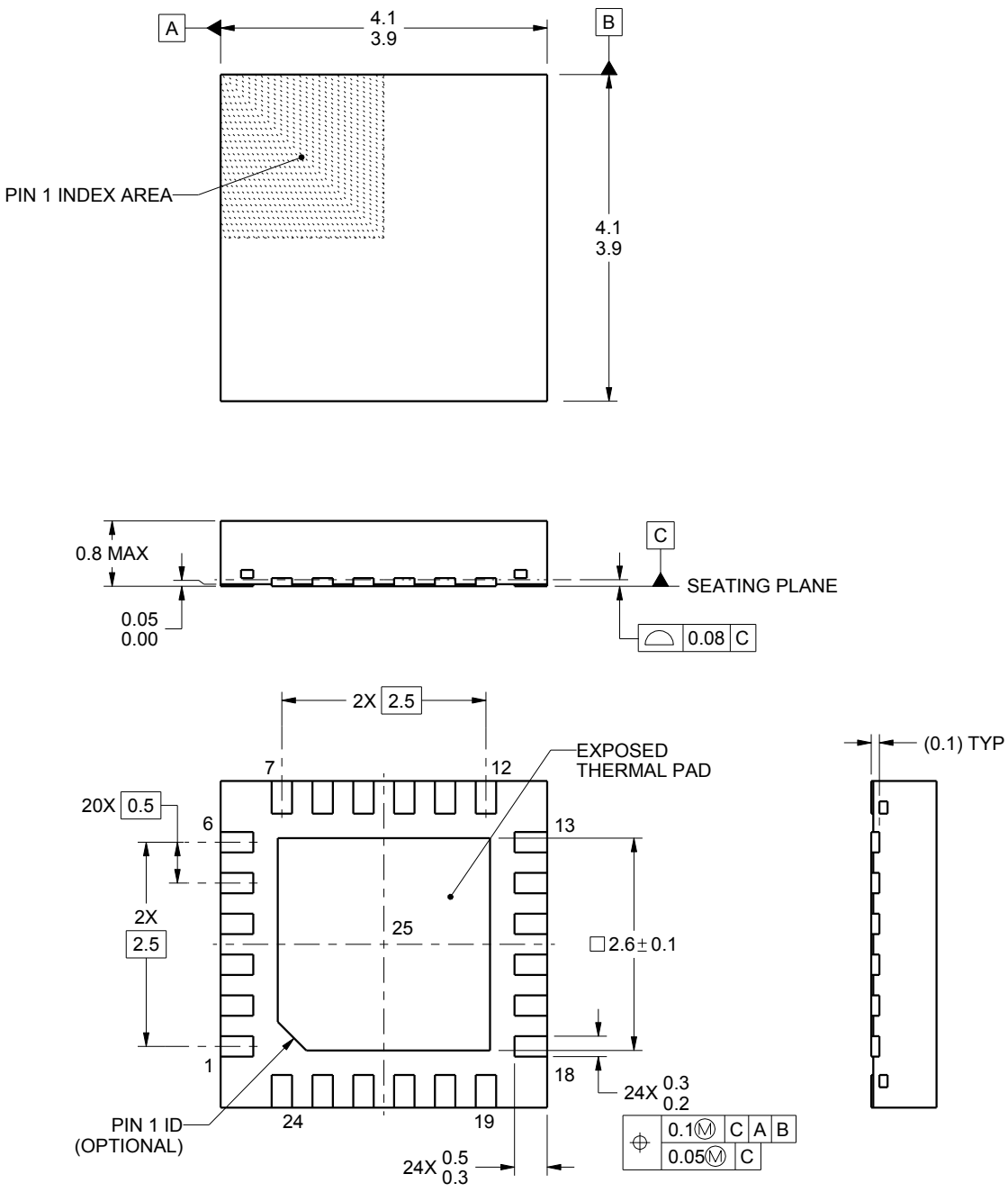
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM26480SQ-AA/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0
LM26480SQX-AA/NOPB	WQFN	RTW	24	4500	367.0	367.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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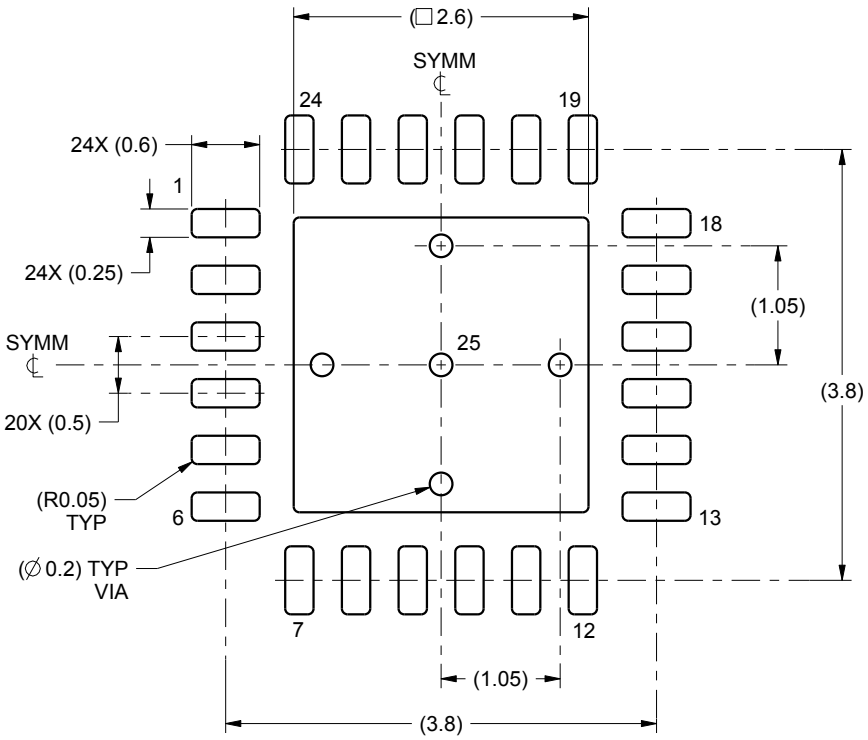
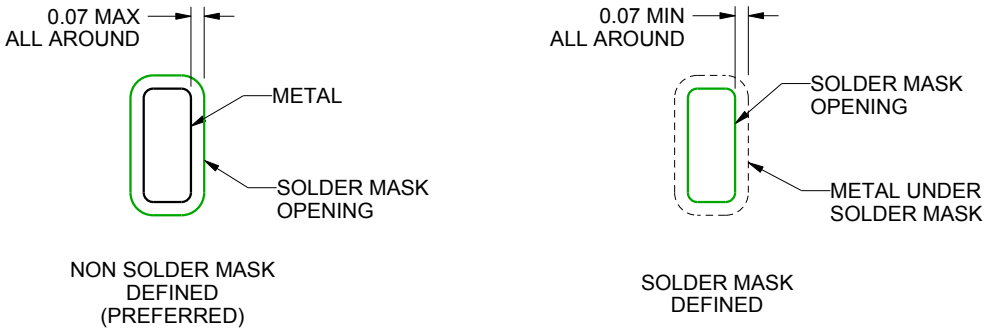
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

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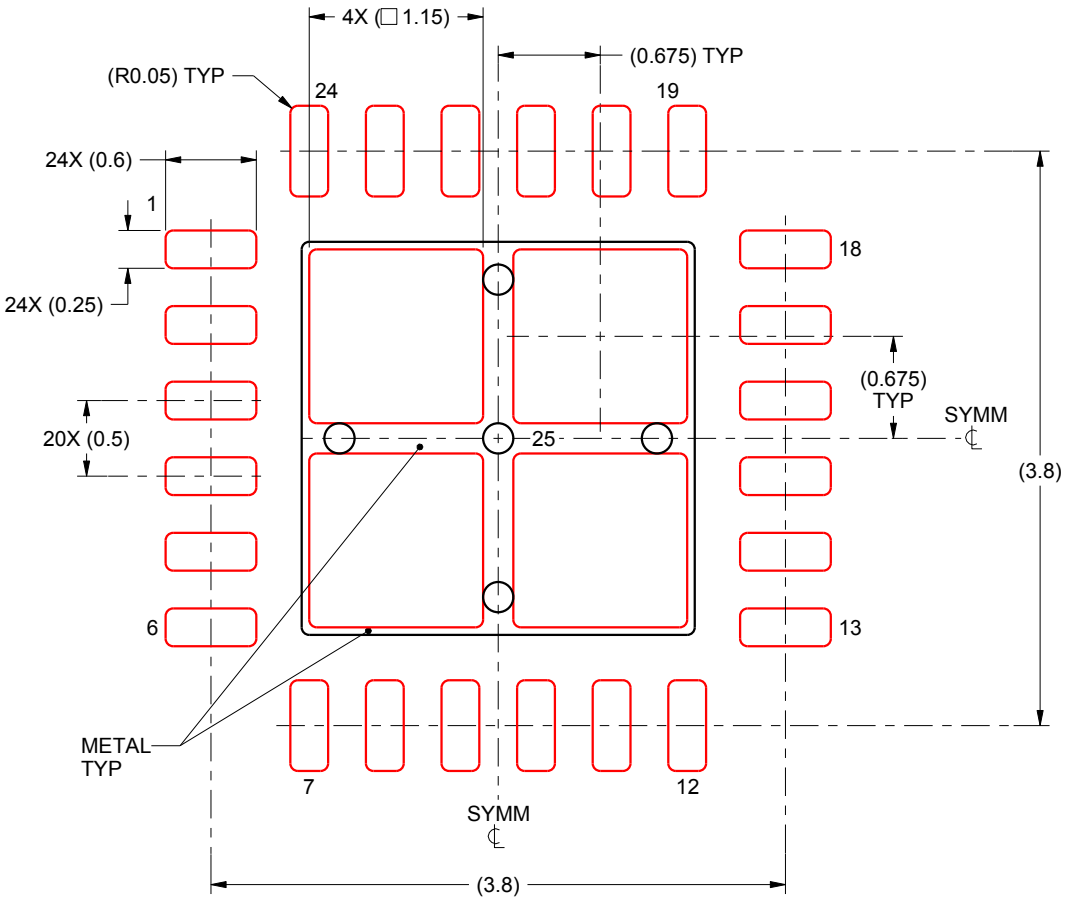
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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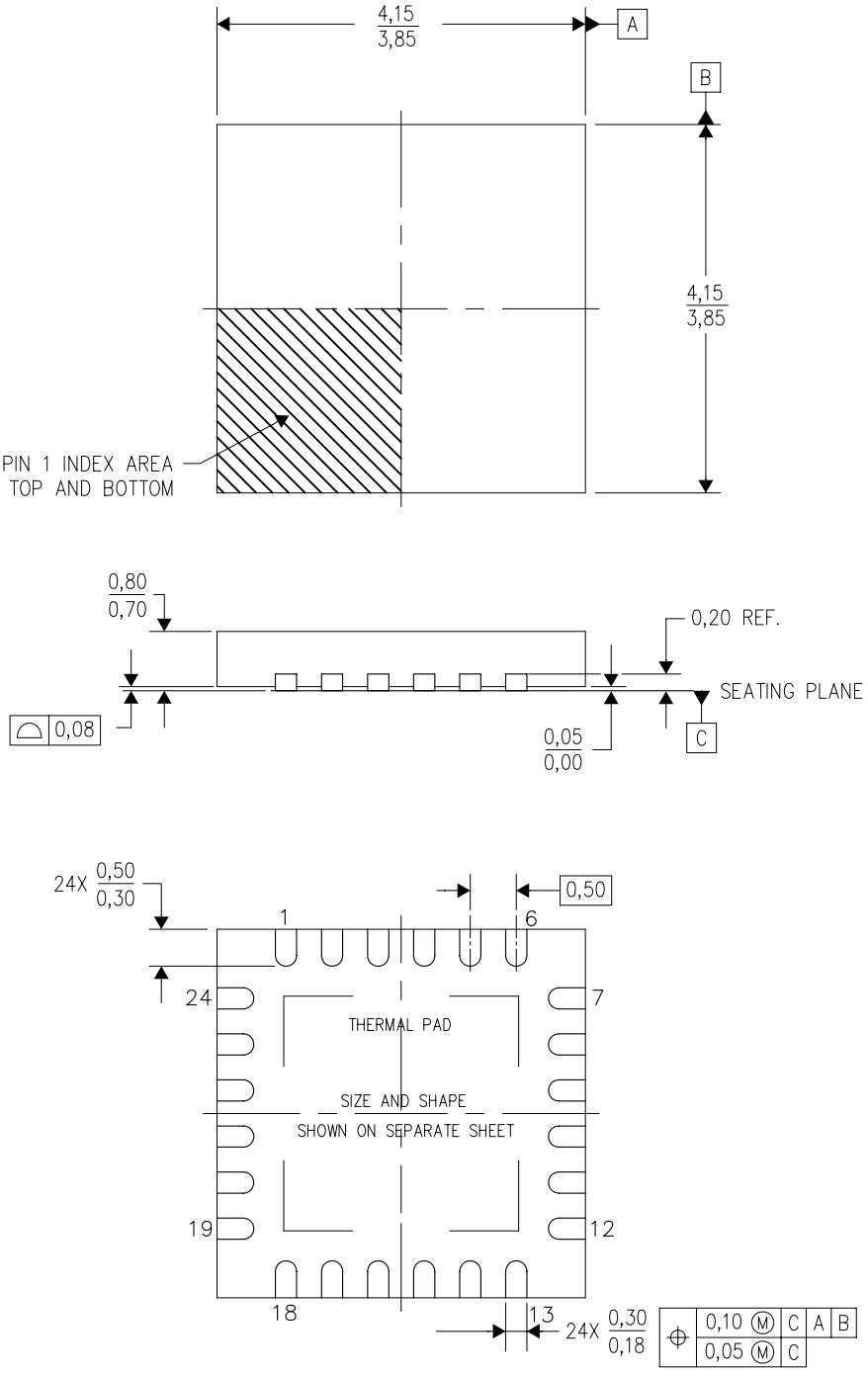
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

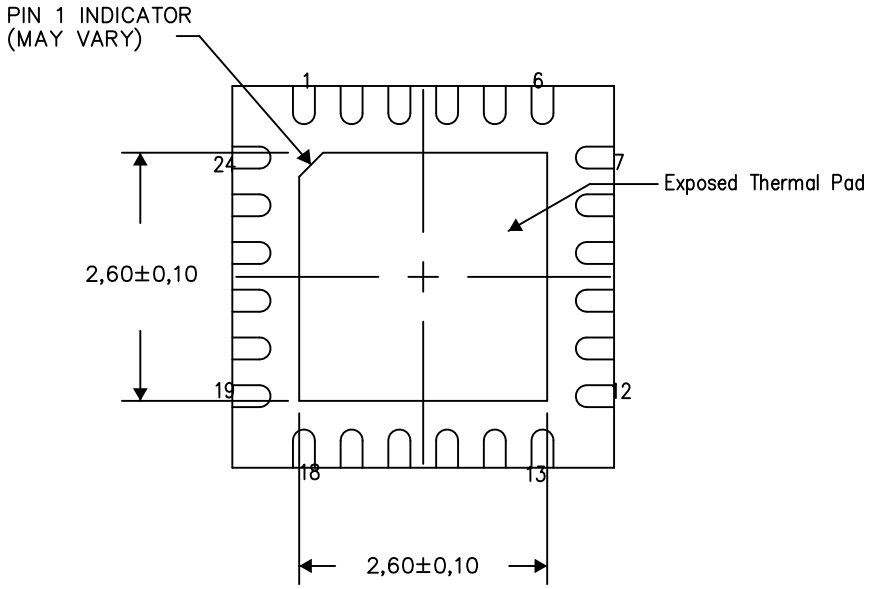
RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206249–8/P 05/15

NOTES: A. All linear dimensions are in millimeters

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