

CSD18512Q5B 40V N 通道 NexFET™ 功率 MOSFET

1 特性

- 低 $R_{DS(ON)}$
- 低热阻
- 雪崩级
- 逻辑电平
- 无铅端子镀层
- 符合 RoHS
- 无卤素
- SON 5mm x 6mm 塑料封装

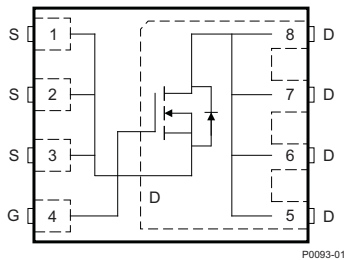
2 应用

- 直流/直流转换
- 次级侧同步整流器
- 电机控制

3 说明

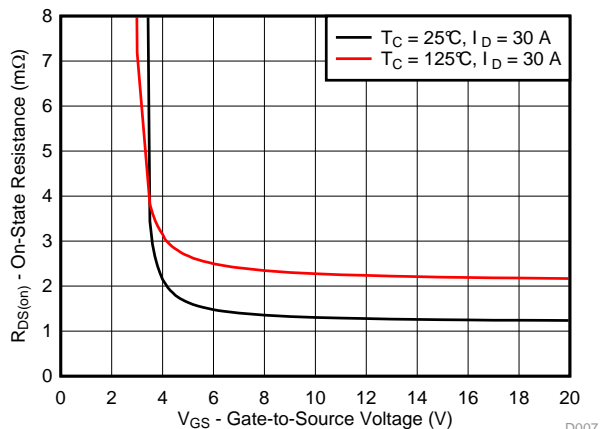
这款 40V、1.3m Ω 、5mm x 6mm NexFET™ 功率 MOSFET 旨在用于最大程度降低功率转换应用中的损耗。

俯视图



P0093-01

$R_{DS(on)}$ 与 V_{GS} 对比



D007

产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	40		V
Q_g	栅极电荷总量 (10V)	75		nC
Q_{gd}	栅漏栅极电荷	13.3		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	1.8	m Ω
		$V_{GS} = 10\text{V}$	1.3	m Ω
$V_{GS(th)}$	阈值电压	1.6		V

订购信息⁽¹⁾

器件	数量	包装介质	封装	配送
CSD18512Q5B	2500	13 英寸卷带	SON 5mm x 6mm 塑料封装	卷带封装
CSD18512Q5BT	250	7 英寸卷带		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

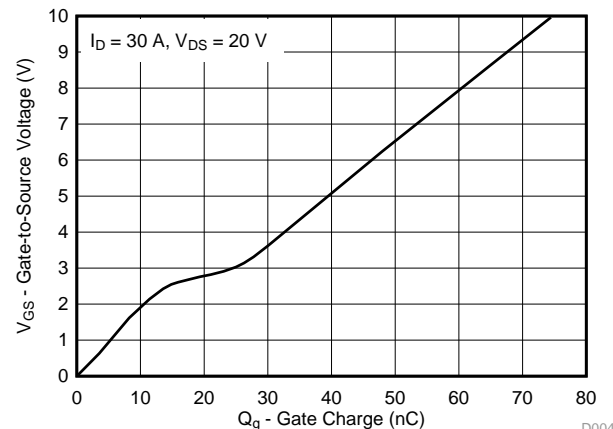
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	40	V
V_{GS}	栅源电压	± 20	V
I_D	持续漏极电流 (受封装限制)	100	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	211	
	持续漏极电流 ⁽¹⁾	32	
I_{DM}	脉冲漏极电流 ⁽²⁾	400	A
P_D	功耗 ⁽¹⁾	3.1	W
	功耗, $T_C = 25^\circ\text{C}$	139	
T_J , T_{stg}	工作结温、贮存温度	-55 至 150	$^\circ\text{C}$
E_{AS}	雪崩能量, 单一脉冲 $I_D = 64\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	205	mJ

(1) $R_{\theta JA} = 40^\circ\text{C}/\text{W}$ ，这是在厚度为 0.06 英寸的环氧板 (FR4) 印刷电路板 (PCB) 上的 1 英寸² 2 盎司的铜焊盘上测得的典型值。

(2) 最大 $R_{\theta JC} = 0.9^\circ\text{C}/\text{W}$ ，脉冲持续时间 $\leq 100\mu\text{s}$ ，占空比 $\leq 1\%$

栅极电荷



D004



目录

<p>1 特性 1</p> <p>2 应用 1</p> <p>3 说明 1</p> <p>4 修订历史记录 2</p> <p>5 Specifications 3</p> <p style="padding-left: 20px;">5.1 Electrical Characteristics 3</p> <p style="padding-left: 20px;">5.2 Thermal Information 3</p> <p style="padding-left: 20px;">5.3 Typical MOSFET Characteristics 4</p> <p>6 器件和文档支持 7</p>	<p>6.1 社区资源 7</p> <p>6.2 商标 7</p> <p>6.3 静电放电警告 7</p> <p>6.4 术语表 7</p> <p>7 "机械、封装和可订购信息" 8</p> <p style="padding-left: 20px;">7.1 Q5B 封装尺寸 8</p> <p style="padding-left: 20px;">7.2 建议 PCB 布局 9</p> <p style="padding-left: 20px;">7.3 建议模板布局 9</p> <p style="padding-left: 20px;">7.4 Q5B 卷带信息 10</p>
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4 修订历史记录

Changes from Original (December 2016) to Revision A	Page
<ul style="list-style-type: none"> • Corrected the SOA in Figure 10 5 	5

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

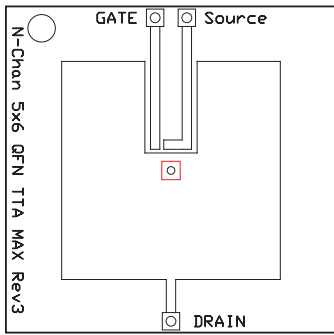
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V _{DSS}	Drain to source voltage	V _{GS} = 0 V, I _D = 250 μA	40			V
I _{DSS}	Drain to source leakage current	V _{GS} = 0 V, V _{DS} = 32 V			1	μA
I _{GSS}	Gate to source leakage current	V _{DS} = 0 V, V _{GS} = 20 V			100	nA
V _{GS(th)}	Gate to source threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.3	1.6	2.2	V
R _{DS(on)}	Drain to source on resistance	V _{GS} = 4.5 V, I _D = 30 A		1.8	2.3	mΩ
		V _{GS} = 10 V, I _D = 30 A		1.3	1.6	mΩ
g _{fs}	Transconductance	V _{DS} = 20 V, I _D = 30 A		136		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 20 V, f = 1 MHz		5480	7120	pF
C _{oss}	Output capacitance			537	699	pF
C _{rss}	Reverse transfer capacitance			256	333	pF
R _G	Series gate resistance			1.0	2.0	Ω
Q _g	Gate charge total (4.5 V)	V _{DS} = 20 V, I _D = 30 A		37	48	nC
Q _g	Gate charge total (10 V)			75	98	nC
Q _{gd}	Gate charge gate to drain			13.3		nC
Q _{gs}	Gate charge gate to source			15.1		nC
Q _{g(th)}	Gate charge at V _{th}			8.2		nC
Q _{oss}	Output charge		V _{DS} = 20 V, V _{GS} = 0 V		23	
t _{d(on)}	Turn on delay time	V _{DS} = 20 V, V _{GS} = 10 V, I _{DS} = 30 A, R _G = 0 Ω		7		ns
t _r	Rise time			16		ns
t _{d(off)}	Turn off delay time			31		ns
t _f	Fall time			7		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode forward voltage	I _{SD} = 30 A, V _{GS} = 0 V		0.75	1.0	V
Q _{rr}	Reverse recovery charge	V _{DS} = 20 V, I _F = 30 A, di/dt = 300 A/μs		22		nC
t _{rr}	Reverse recovery time			17		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

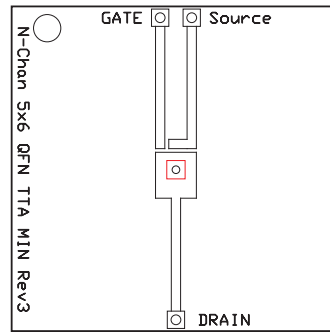
THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-case (top of package) thermal resistance ⁽¹⁾			0.9	°C/W
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			50	°C/W

- (1) R_{θJC} is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.



M0137-01

Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2
oz. (0.071 mm thick)
Cu.

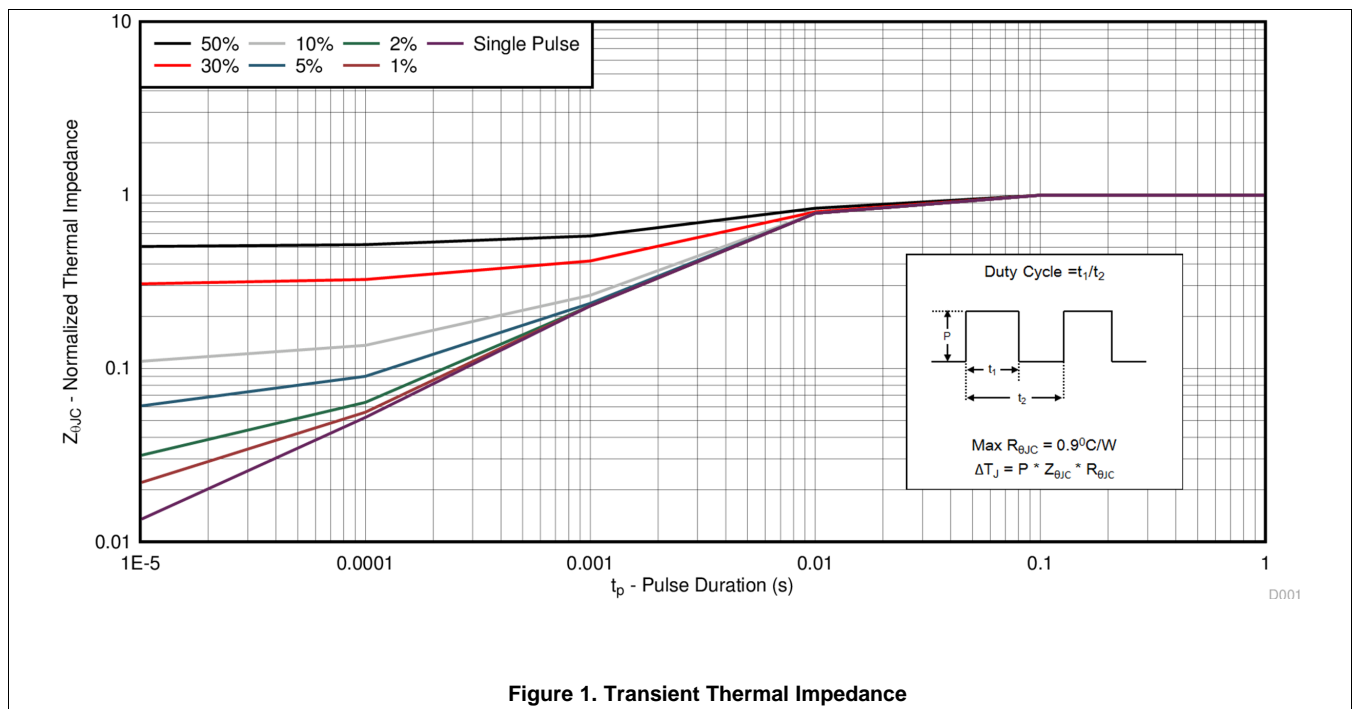


M0137-02

Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of 2
oz. (0.071 mm thick)
Cu.

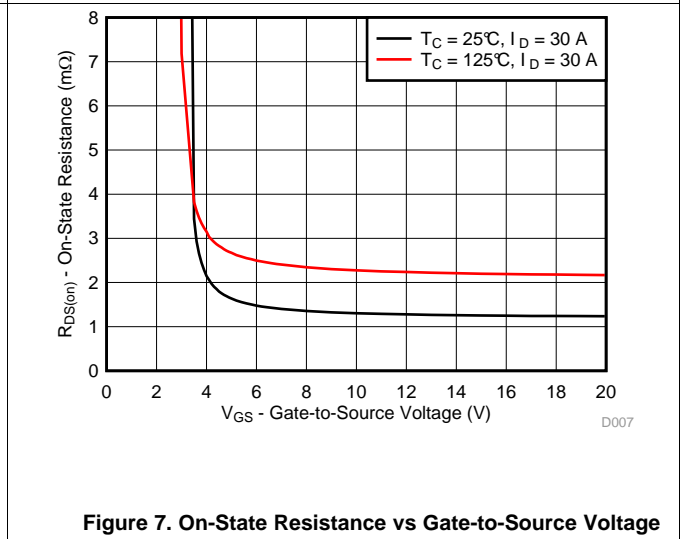
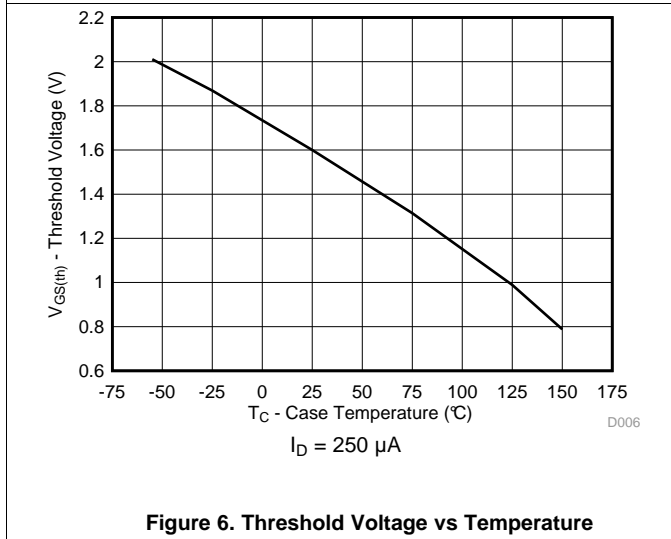
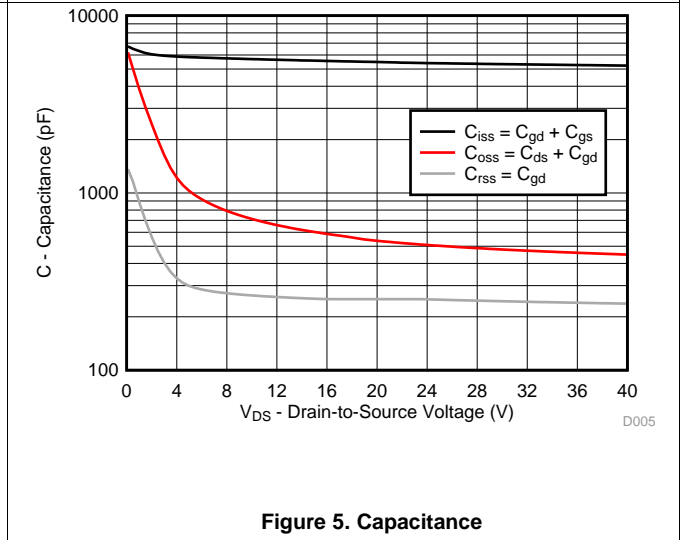
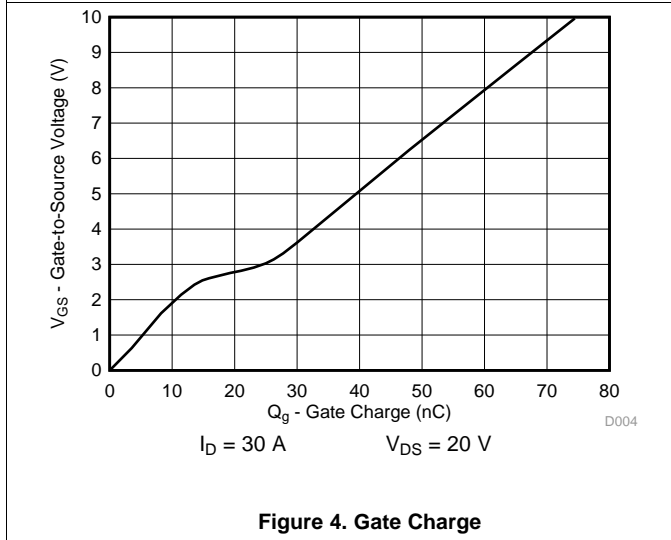
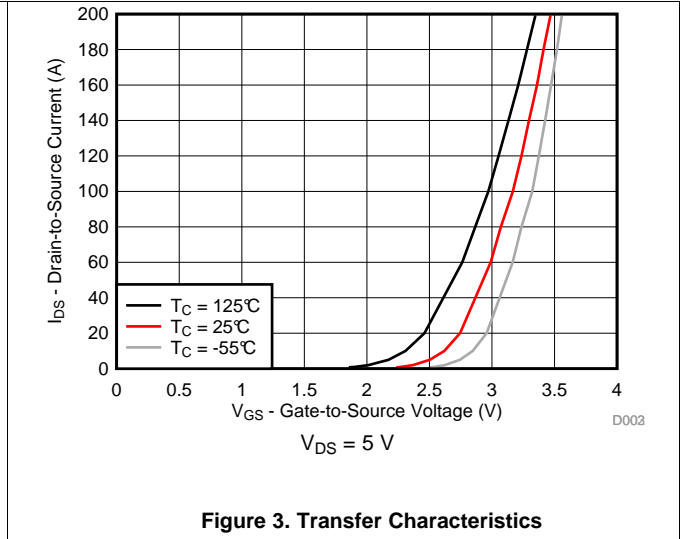
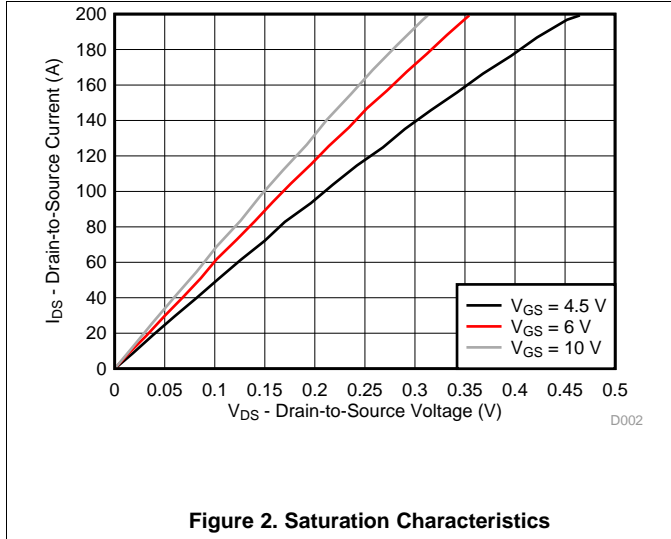
5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$ (unless otherwise stated)



Typical MOSFET Characteristics (continued)

T_A = 25°C (unless otherwise stated)



Typical MOSFET Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

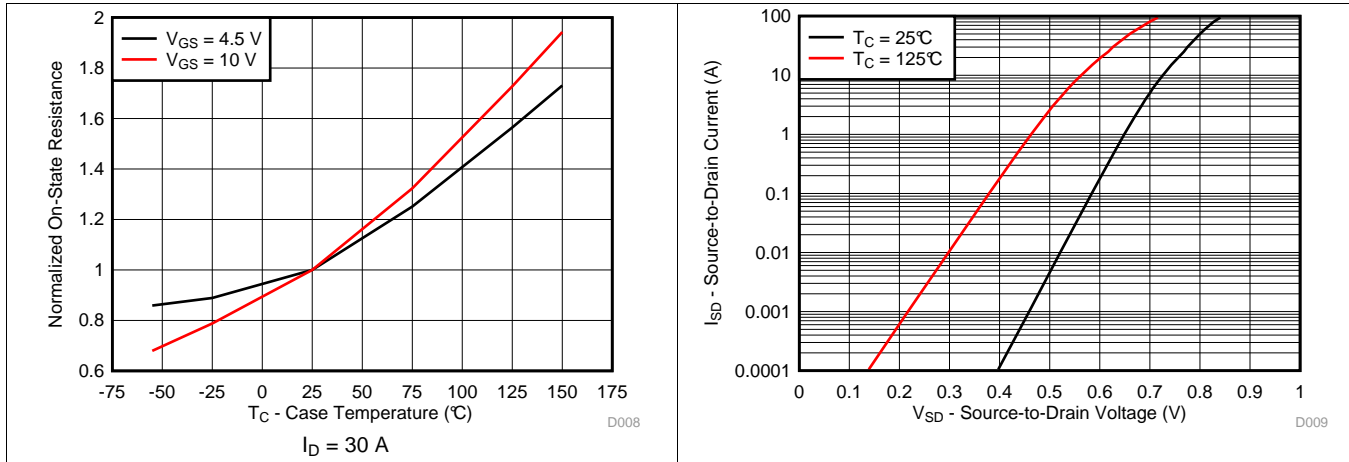


Figure 8. Normalized On-State Resistance vs Temperature

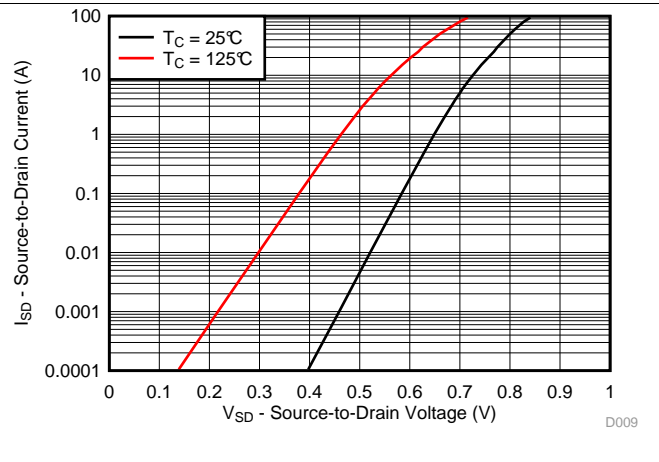


Figure 9. Typical Diode Forward Voltage

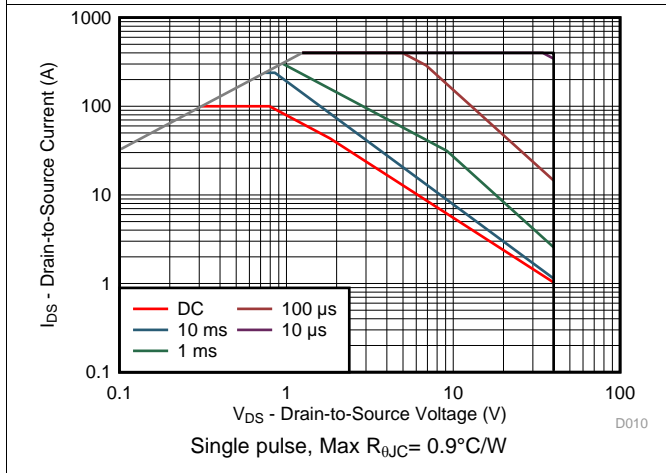


Figure 10. Maximum Safe Operating Area

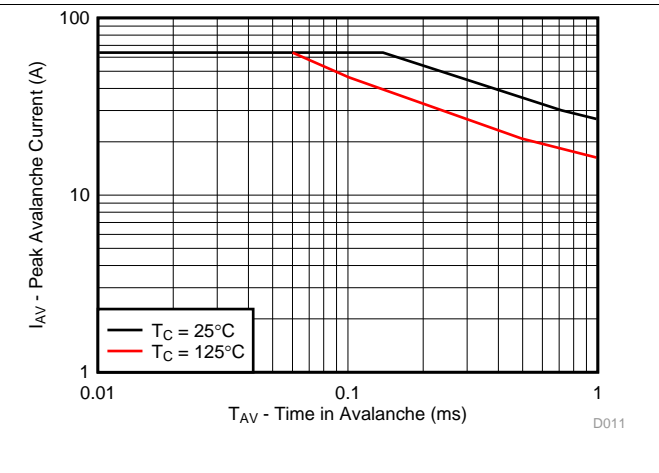


Figure 11. Single Pulse Unclamped Inductive Switching

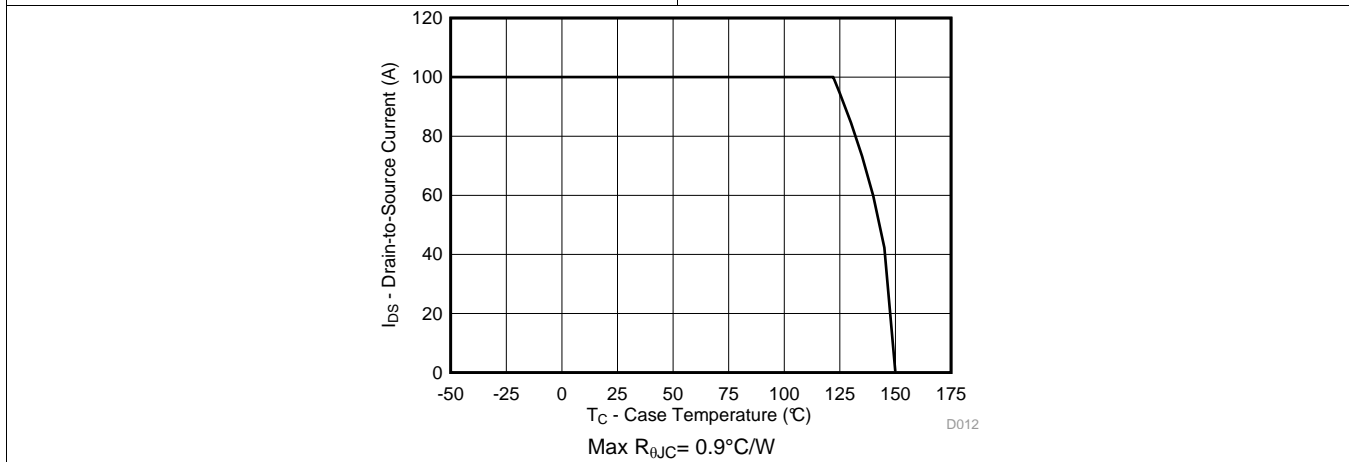


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.2 商标

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6.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

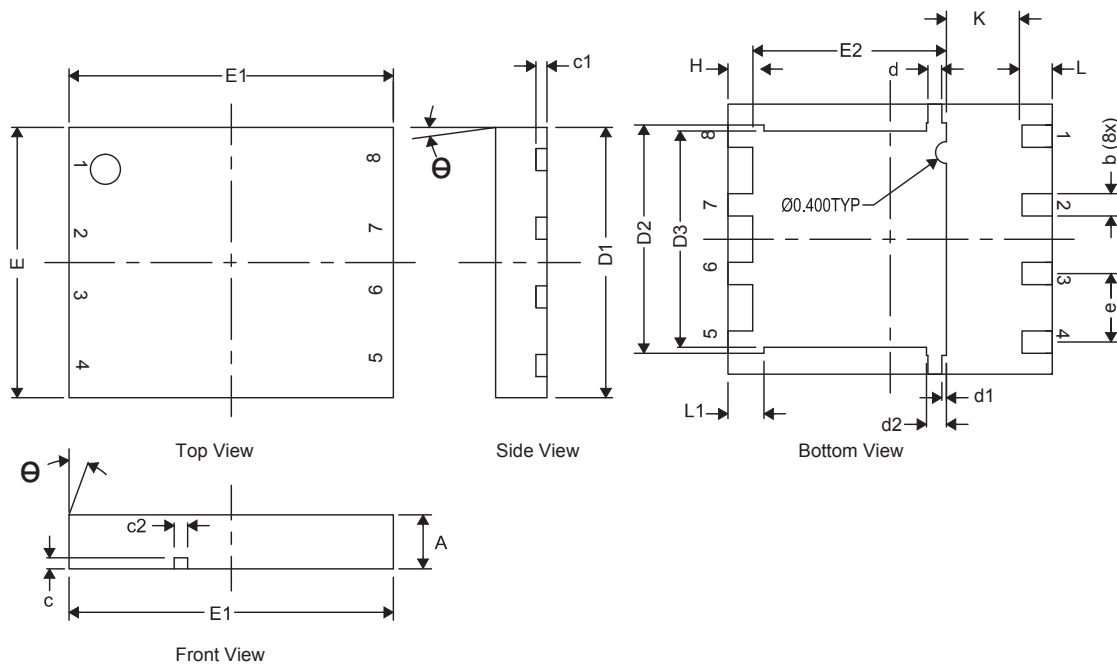
6.4 术语表

SLYZ022 — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

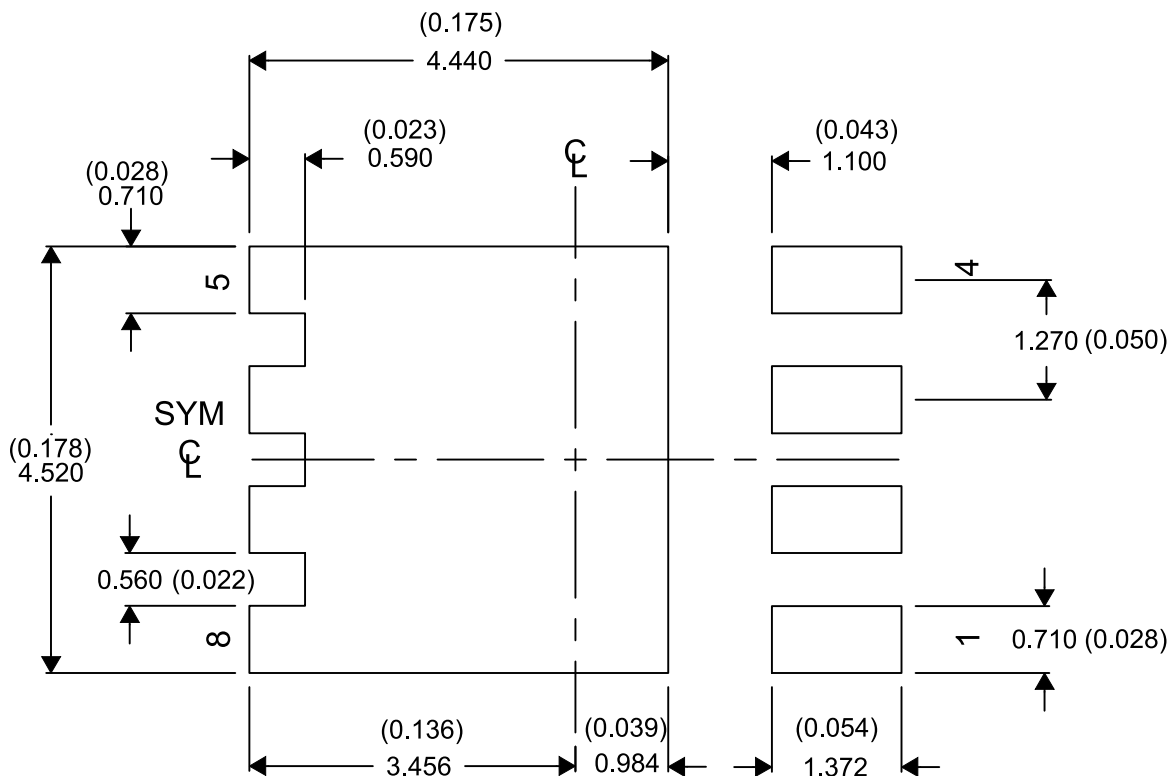
7 "机械、封装和可订购信息

7.1 Q5B 封装尺寸



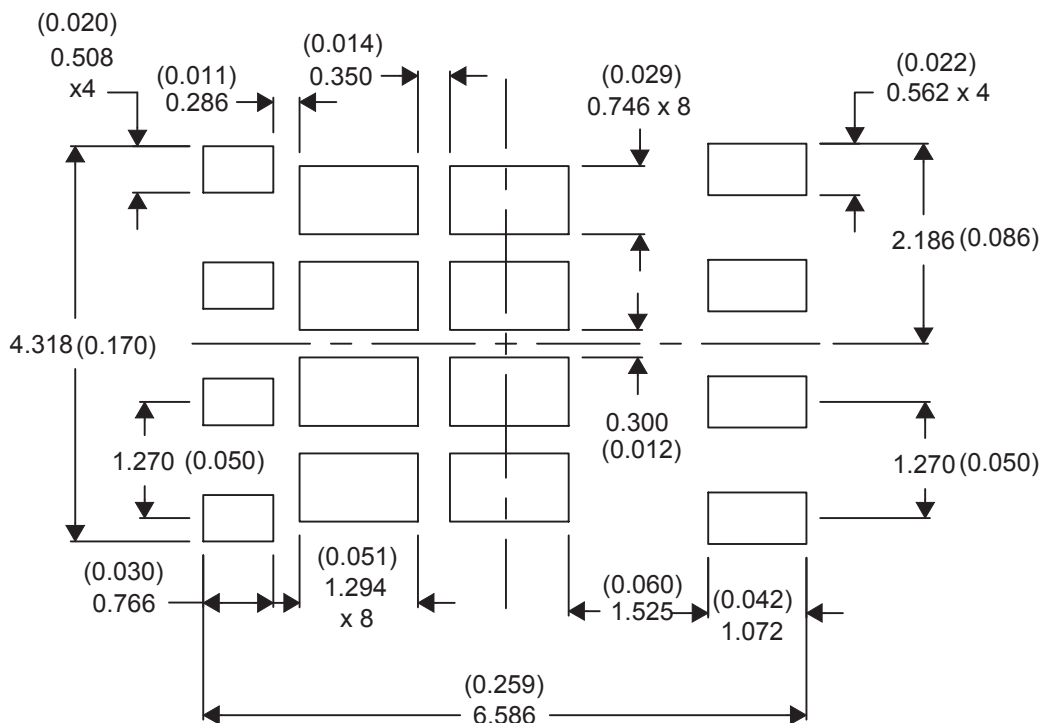
DIM	毫米		
	最小值	标称值	最大值
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 典型值		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 典型值		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	-	-
K	1.40 典型值		

7.2 建议 PCB 布局

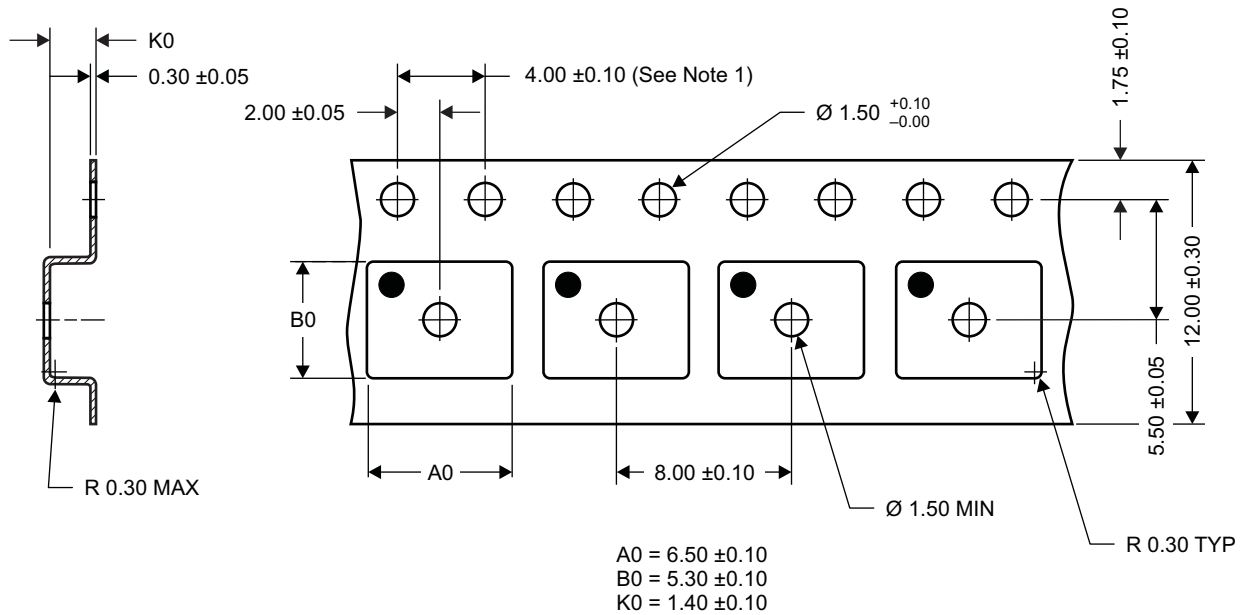


要获得与印刷电路板 (PCB) 设计相关的建议电路布局布线, 请参阅《应用说明》[SLPA005 - 通过 PCB 布局布线技巧来减少振铃](#)。

7.3 建议模板布局



7.4 Q5B 卷带信息



M0138-01

注释:

1. 10 个链齿孔的累积容差为 ± 0.2 。
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。
3. 材料：黑色抗静电聚苯乙烯。
4. 全部尺寸为 mm（除非另外注明）。
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18512Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	RoHS-Exempt & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18512	
CSD18512Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	RoHS-Exempt & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	CSD18512	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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