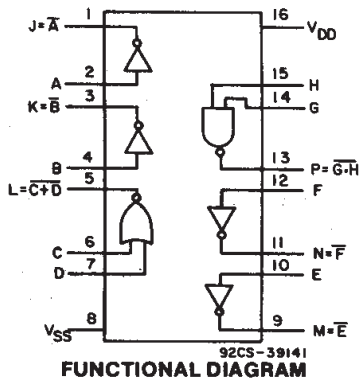


CMOS Hex Gate

Four Inverters, One 2-Input NOR Gate, One 2-Input NAND Gate



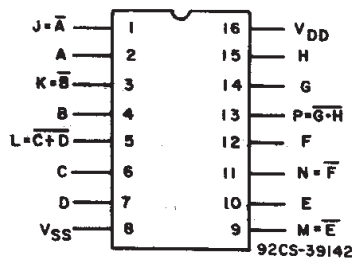
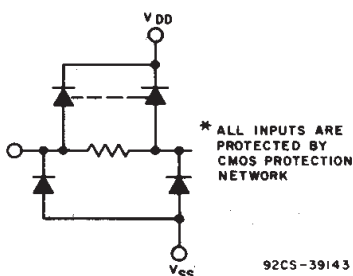
Features:

- Pin 7 NOR input positioned adjacent to V_{SS} for easy use of gate as an inverter
- Pin 15 NAND input positioned adjacent to V_{DD} for easy use of gate as an inverter
- Standard symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range: 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

■ CD4572UB Hex Gate provides the system designer with direct implementation of inverter, NAND, and NOR functions and supplements the existing family of CMOS gates.

The CD4572UB devices meet all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."

The CD4572UB types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



TERMINAL ASSIGNMENT

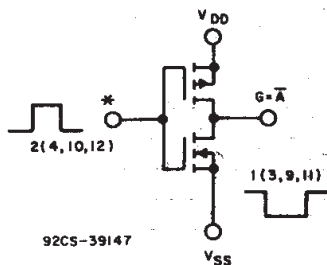


Fig. 1 - Schematic diagram of one of four identical inverters.

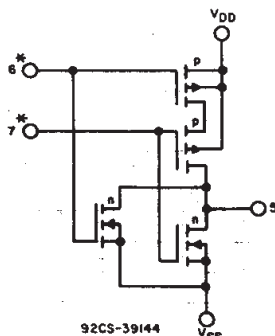


Fig. 2 - Schematic diagram for the 2-input NOR gate.

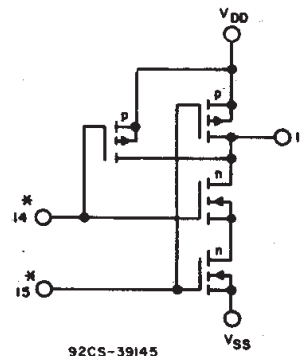


Fig. 3 - Schematic diagram for the 2-input NAND gate.

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

CD4572UB Types

MAXIMUM RATINGS, Absolute-Maximum Values:

| | |
|------------------------------------------------------------------------------------------------|--------------------------------------|
| DC SUPPLY-VOLTAGE RANGE, (V _{DD}) Voltages referenced to V _{SS} Terminal | -0.5V to +20V |
| INPUT VOLTAGE RANGE, ALL INPUTS | -0.5V to V _{DD} +0.5V |
| DC INPUT CURRENT, ANY ONE INPUT | ±10mA |
| POWER DISSIPATION PER PACKAGE (P _D): | |
| For T _A = -55°C to +100°C | 500mW |
| For T _A = +100°C to +125°C | Derate Linearity at 12mW/°C to 200mW |
| DEVICE DISSIPATION PER OUTPUT TRANSISTOR | |
| FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) | 100mW |
| OPERATING-TEMPERATURE RANGE (T _A) | -55°C to +125°C |
| STORAGE TEMPERATURE RANGE (T _{stg}) | -65°C to +150°C |
| LEAD TEMPERATURE (DURING SOLDERING): | |
| At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max | +265°C |

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | LIMITS | | UNITS |
|---------------------------------------------------------------------------|--------|------|-------|
| | Min. | Max. | |
| Supply-Voltage Range (For T _A =Full Package-Temperature Range) | 3 | 18 | V |

STATIC ELECTRICAL CHARACTERISTICS

| CHARACTERISTIC | CONDITIONS | | | LIMITS AT INDICATED TEMPERATURES (°C) | | | | | | | UNITS |
|----------------------------------------------------|-----------------------|------------------------|------------------------|---------------------------------------|-------|-------|-------|-------|-------------------|------|-------|
| | V _O (V) | V _{IN} (V) | V _{DD} (V) | +25 | | | | | | | |
| | | | | -55 | -40 | +85 | +125 | Min. | Typ. | Max. | |
| Quiescent Device Current, I _{DD} Max. | — | 0, 5 | 5 | 0.25 | 0.25 | 7.5 | 7.5 | — | 0.01 | 0.25 | μA |
| | — | 0, 10 | 10 | 0.5 | 0.5 | 15 | 15 | — | 0.01 | 0.5 | |
| | — | 0, 15 | 15 | 1 | 1 | 30 | 30 | — | 0.01 | 1 | |
| | — | 0, 20 | 20 | 5 | 5 | 150 | 150 | — | 0.02 | 5 | |
| Output Low (Sink) Current, I _{OL} Min. | 0.4 | 0, 5 | 5 | 0.64 | 0.61 | 0.42 | 0.36 | 0.51 | 1 | — | mA |
| | 0.5 | 0, 10 | 10 | 1.6 | 1.5 | 1.1 | 0.9 | 1.3 | 2.6 | — | |
| | 1.5 | 0, 15 | 15 | 4.2 | 4 | 2.8 | 2.4 | 3.4 | 6.8 | — | |
| Output High (Source) Current, I _{OH} Min. | 4.6 | 0, 5 | 5 | -0.64 | -0.61 | -0.42 | -0.36 | -0.51 | -1 | — | mA |
| | 2.5 | 0, 5 | 5 | -2 | -1.8 | -1.3 | -1.15 | -1.6 | -3.2 | — | |
| | 9.5 | 0, 10 | 10 | -1.6 | -1.5 | -1.1 | -0.9 | -1.3 | -2.6 | — | |
| | 13.5 | 0, 15 | 15 | -4.2 | -4 | -2.8 | -2.4 | -3.4 | -6.8 | — | |
| Output Voltage: Low-Level, V _{OL} Max. | — | 0, 5 | 5 | 0.05 | | | | — | 0 | 0.05 | V |
| | — | 0, 10 | 10 | 0.05 | | | | — | 0 | 0.05 | |
| | — | 0, 15 | 15 | 0.05 | | | | — | 0 | 0.05 | |
| Output Voltage: High-Level, V _{OH} Min. | — | 0, 5 | 5 | 4.95 | | | | 4.95 | 5 | — | V |
| | — | 0, 10 | 10 | 9.95 | | | | 9.95 | 10 | — | |
| | — | 0, 15 | 15 | 14.95 | | | | 14.95 | 15 | — | |
| Input Low Voltage, V _{IL} Max. | 0.5, 4.5 | — | 5 | 1 | | | | — | — | 1 | V |
| | 1, 9 | — | 10 | 2 | | | | — | — | 2 | |
| | 1.5, 13.5 | — | 15 | 2.5 | | | | — | — | 2.5 | |
| Input High Voltage, V _{IH} Min. | 0.5, 4.5 | — | 5 | 4 | | | | 4 | — | — | V |
| | 1, 9 | — | 10 | 8 | | | | 8 | — | — | |
| | 1.5, 13.5 | — | 15 | 12.5 | | | | 12.5 | — | — | |
| Input Current, I _{IN} Max. | — | 0, 18 | 18 | ±0.1 | ±0.1 | ±1 | ±1 | — | ±10 ⁻⁵ | ±0.1 | μA |

CD4572UB Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A=25^\circ\text{C}$, Input $t_r, t_f=20\text{ ns}$, $C_L=50\text{ pF}$, $R_L=200\text{ K}\Omega$

| CHARACTERISTIC | SYMBOL | TEST CONDITIONS | | | LIMITS | | | UNITS |
|------------------------|--------------------|---------------------|--|--|--------|------|------|-------|
| | | V _{DD} (V) | | | Min. | Typ. | Max. | |
| Propagation Delay Time | t_{PHL}, t_{PLH} | 5 | | | — | 100 | 200 | ns |
| | | 10 | | | — | 55 | 110 | |
| | | 15 | | | — | 40 | 85 | |
| Transition Time | t_{THL}, t_{TLH} | 5 | | | — | 100 | 200 | |
| | | 10 | | | — | 50 | 100 | |
| | | 15 | | | — | 40 | 80 | |
| Input Capacitance | C_{IN} | Any Input | | | — | 10 | 15 | pF |

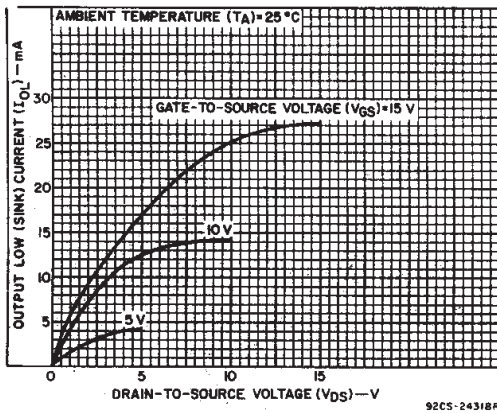


Fig. 4 - Typical output low (sink) current characteristics.

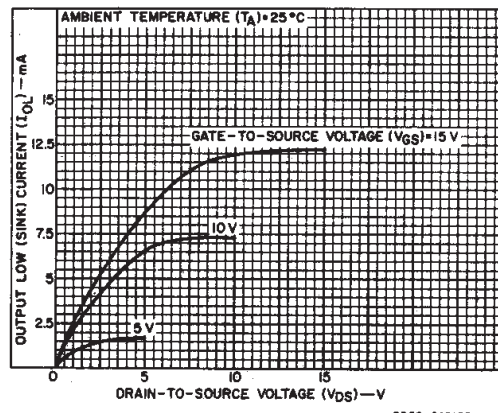


Fig. 5 - Minimum output low (sink) current characteristics.

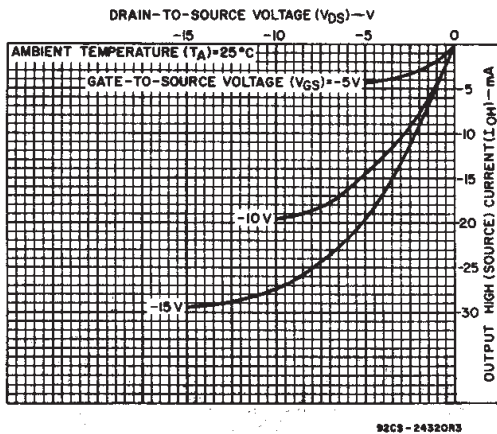


Fig. 6 - Typical output high (source) current characteristics.

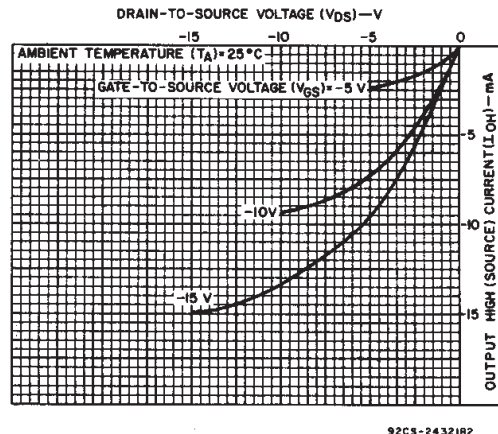


Fig. 7 - Minimum output high (source) current characteristics.

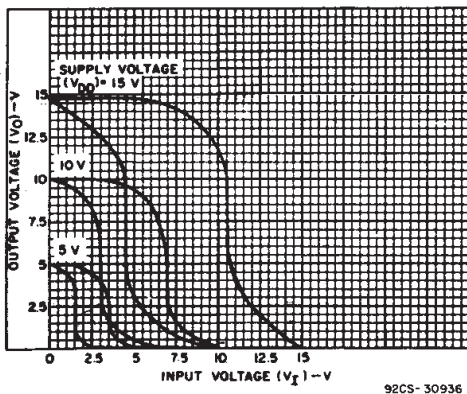


Fig. 8 - Minimum and maximum inverter voltage transfer characteristics.

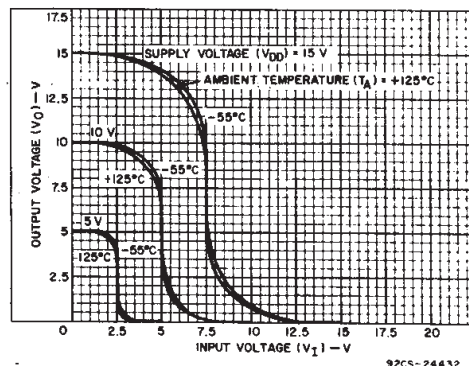


Fig. 9 - Typical inverter voltage transfer characteristics as a function of temperature.

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HIGH VOLTAGE ICs

CD4572UB Types

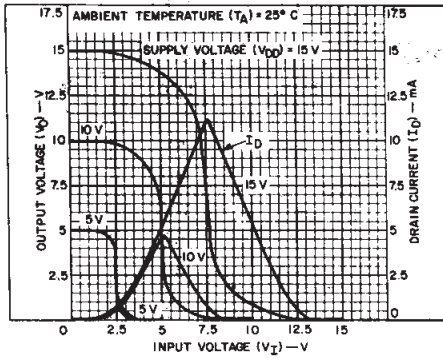


Fig. 10 - Typical inverter current and voltage transfer characteristics.

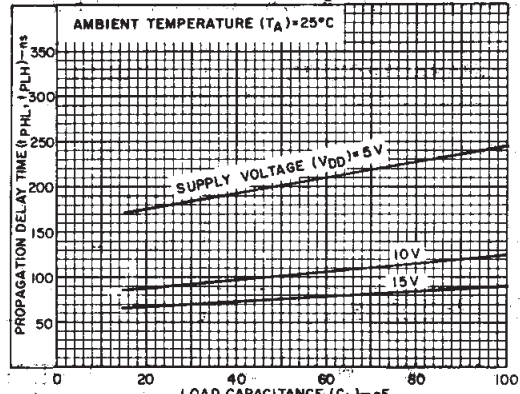


Fig. 11 - Typical propagation delay time as a function of load capacitance.

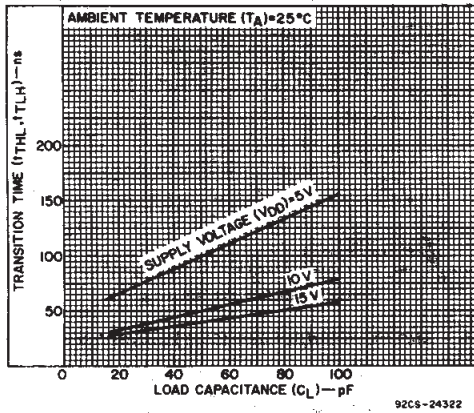


Fig. 12 - Typical transition time vs. load capacitance.

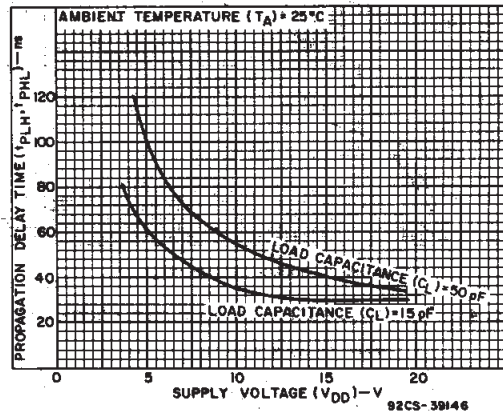


Fig. 13 - Typical propagation delay time vs. supply voltage.

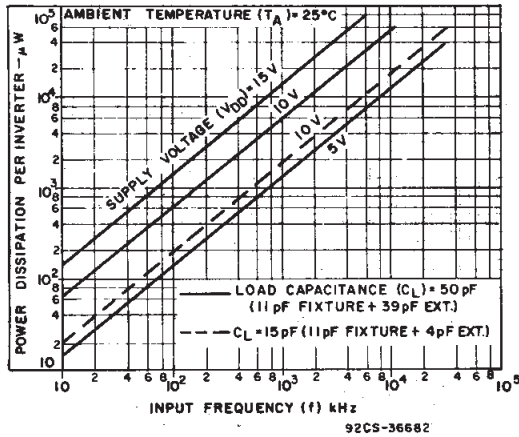


Fig. 14 - Typical dynamic power dissipation vs. frequency.

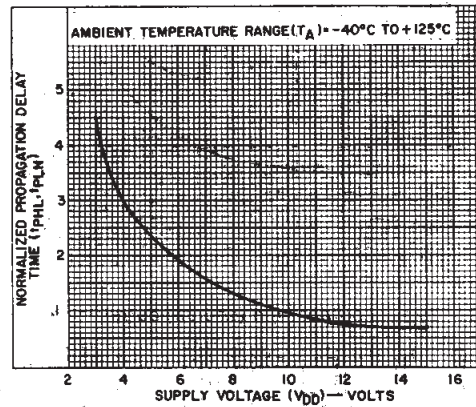


Fig. 15 - Variation of normalized propagation delay time (t_{PHL} and t_{PLN}) with supply voltage.

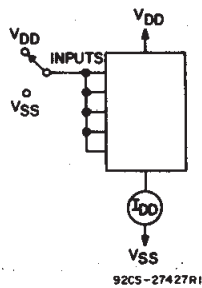


Fig. 16 - Quiescent device current test circuit.

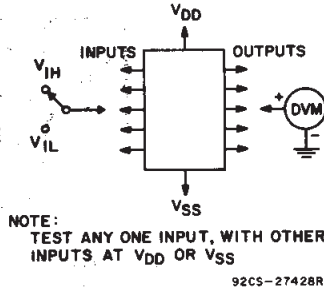


Fig. 17 - Noise immunity test circuit.

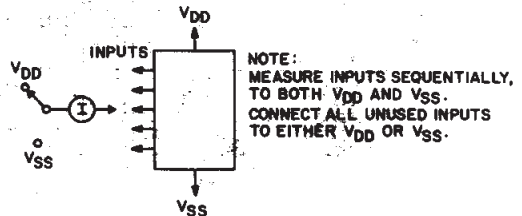


Fig. 18 - Input leakage current test circuit.

CD4572UB Types

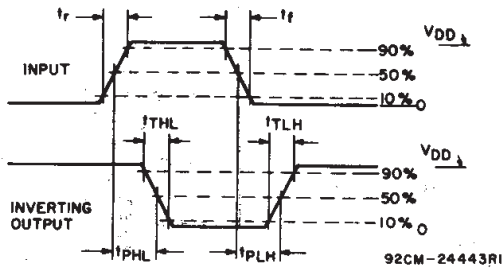
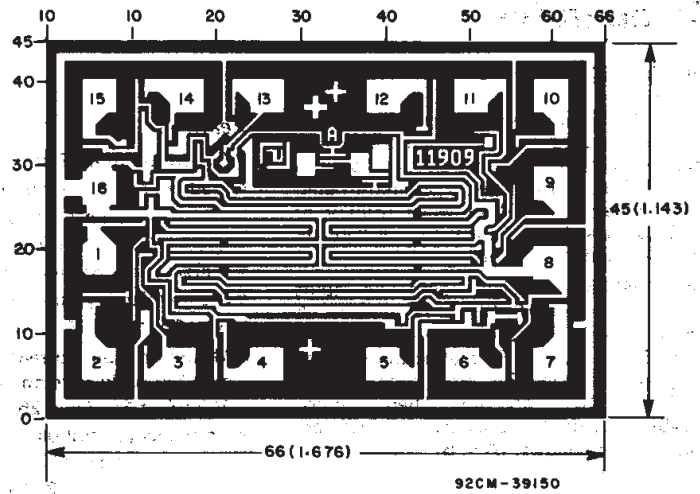


Fig. 19 - Transition times and propagation delay times, combination logic.



Dimensions and pad layout for CD4572UBH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

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COMMERCIAL CMOS
HIGH VOLTAGE ICs

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CD4572UBE | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD4572UBE | Samples |
| CD4572UBEE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD4572UBE | Samples |
| CD4572UBM | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4572UBM | Samples |
| CD4572UBNSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CD4572UB | Samples |
| CD4572UBPWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | CM572UB | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CD4572UBNSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD4572UBPWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CD4572UBNSR | SO | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| CD4572UBPWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal



| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CD4572UBE | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4572UBE | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4572UBEE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4572UBEE4 | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| CD4572UBM | D | SOIC | 16 | 40 | 507 | 8 | 3940 | 4.32 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.



PACKAGE OUTLINE

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

EXAMPLE BOARD LAYOUT

NS0016A

SOP - 2.00 mm max height

SOP



4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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