

具有 $\pm 15\text{kV}$ IEC ESD 保护功能的 TRSF3243E 3V 至 5.5V 多通道 RS-232 兼容线路驱动器和接收器

1 特性

- 为 RS-232 总线引脚提供 ESD 保护
 - $\pm 15\text{kV}$ 人体放电模型 (HBM)
 - $\pm 8\text{kV}$ IEC61000-4-2 接触放电
 - $\pm 15\text{kV}$ IEC61000-4-2 气隙放电
- 由单个 3V 至 5.5V V_{CC} 电源供电
- 始终有效同相接收器输出 (ROUT2B)
- 低待机电流: $1\ \mu\text{A}$ (典型值)
- 外部电容器: $4 \times 0.1\ \mu\text{F}$
- 接受 5V 逻辑输入及 3.3V 电源
- 串行鼠标驱动能力
- 支持高达 1Mbit/s 的运行速度
- 自动断电功能, 在没有检测到有效 RS-232 信号时禁用驱动器输出
- 采用节省空间的 RHB (5mm x 5mm QFN-32) 封装

2 应用

- 工业 PC
- 有线网络
- 数据中心和网络设备
- 笔记本电脑
- 手持设备

3 说明

TRSF3243E 由三个线路驱动器、五个线路接收器和一个双电荷泵电路组成, 在串行端口连接引脚上具有

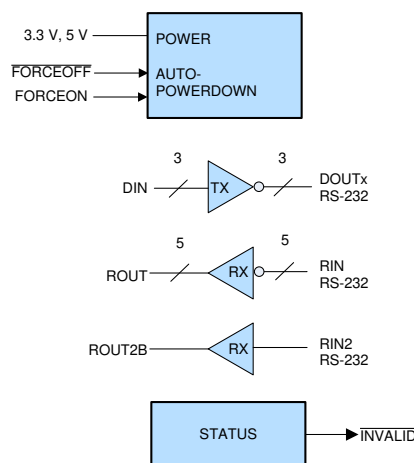
$\pm 15\text{kV}$ ESD (HBM 和 IEC61000-4-2, 空气间隙放电) 和 $\pm 8\text{kV}$ ESD (IEC61000-4-2, 接触放电) 保护。该器件可在异步通信控制器和串行端口连接器之间提供电气接口。电荷泵和四个小型外部电容器支持由 3V 至 5.5V 单电源供电。另外, 该器件包括一个始终有效同相输出 (ROUT2B), 这使得使用振铃指示的应用能够在器件断电的情况下发送数据。该器件以高达 1Mbit/s 的数据信号传输速率运行, 具有从 $18\text{V}/\mu\text{s}$ 至 $150\text{V}/\mu\text{s}$ 的更高压摆率范围。

串行端口处于非活动状态时, 可提供灵活的电源管理控制选项。当 FORCEON 为低电平且 FORCEOFF 为高电平时, 自动断电功能启用。在这种运行模式下, 如果器件未检测到有效的 RS-232 信号, 则禁用驱动器输出。如果 FORCEOFF 设定为低电平, 则驱动器和接收器 (ROUT2B 除外) 均关闭, 且电源电流降低至 $1\ \mu\text{A}$ 。断开串行端口的连接或关闭外围驱动器会导致发生自动断电情况。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TRSF3243E	VQFN (RHB) (32)	5,00mm × 5,00mm
	TSSOP (PW) (28)	9,70mm × 4,40mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



简化版电路

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (November 2021) to Revision A (September 2022)	Page
• 删除了封装信息表中的 TSSOP (PW) 产品预发布说明.....	1

5 Pin Configuration and Functions

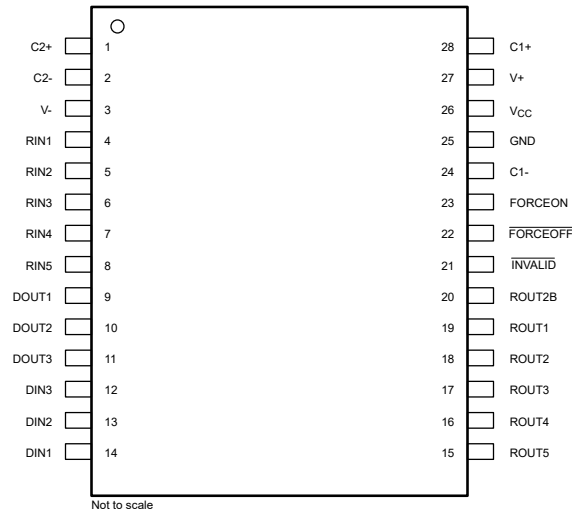


图 5-1. PW (TSSOP) Packages, 28 Pin, Top View

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the charge-pump capacitor
2	C2-	—	Negative terminal of the charge-pump capacitor
3	V-	—	Negative charge-pump rail
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver logic inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver logic outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active non-inverting receiver logic output
21	INVALID	O	Invalid Output Pin
22	FORCEOFF	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the charge-pump capacitor
25	GND	—	Ground
26	V _{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge-pump rail
28	C1+	—	Positive terminal of the charge-pump capacitor

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

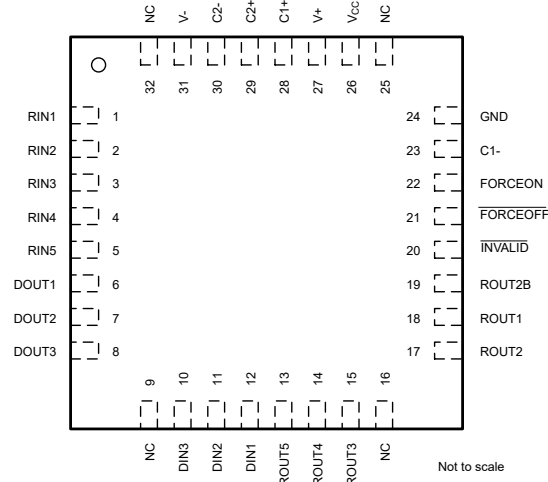


图 5-2. RHB (VQFN) Package, 32 Pin, Top View

表 5-2. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	RIN1	I	RS-232 receiver inputs
2	RIN2		
3	RIN3		
4	RIN4		
5	RIN5		
6	DOUT1	O	RS-232 driver outputs
7	DOUT2		
8	DOUT3		
9	NC	—	No internal connection
10	DIN3	I	Driver logic inputs
11	DIN2		
12	DIN1		
13	ROUT5	O	Receiver logic outputs
14	ROUT4		
15	ROUT3		
16	NC	—	No internal connection
17	ROUT2	O	Receiver outputs
18	ROUT1		
19	ROUT2B	O	Always-active non-inverting receiver output
20	INVALID	O	Invalid Output Pin
21	FORCEOFF	I	Auto Powerdown Control input (Refer to Truth Table)
22	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
23	C1-	—	Negative terminal of the charge-pump capacitor
24	GND	—	Ground
25	NC	—	No internal connection
26	V _{CC}	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge-pump rail
28	C1+	—	Positive terminal of the charge-pump capacitor
29	C2+	—	Negative terminal of the charge-pump capacitor
30	C2-	—	Negative terminal of the charge-pump capacitor
31	V-	—	Negative charge-pump rail
32	NC	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage range ⁽²⁾	- 0.3	6	V	
V+	Positive-output supply voltage range ⁽²⁾	- 0.3	7	V	
V-	Negative-output supply voltage range ⁽²⁾	0.3	- 7	V	
V+ - V-	Supply voltage difference ⁽²⁾		13	V	
V _I	Input voltage range	Driver (FORCEOFF, FORCEON)	- 0.3	6	V
		Receiver	- 25	25	
V _O	Output voltage range	Driver	- 13.2	13.2	V
T _J	Operating virtual junction temperature		150	°C	
T _{stg}	Storage temperature range	- 65	150	°C	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	All pins except RIN1, RIN2, RIN3, RIN4, RIN5, DOUT1, DOUT2 and DOUT3 pins	±3000	V
			RIN1, RIN2, RIN3, RIN4, RIN5, DOUT1, DOUT2 and DOUT3 pins to GND	±15000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	All pins	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	IEC 61000-4-2 Contact Discharge ⁽¹⁾	RIN1, RIN2, RIN3, RIN4, RIN5, DOUT1, DOUT2 and DOUT3 pins	±8,000	V
		IEC 61000-4-2 Air-gap Discharge ⁽¹⁾		±15,000	

- (1) A minimum of 1-μF capacitor between V_{CC} and GND is required to meet the specified IEC 61000-4-2 rating.

6.4 Recommended Operating Conditions

see (1)

			MIN	NOM	MAX	UNIT
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
		$V_{CC} = 5\text{ V}$	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON	$V_{CC} = 3.3\text{ V}$	2		V
			$V_{CC} = 5\text{ V}$	2.4		
V_{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON			0.8	V
V_I	Driver and control input voltage	DIN, FORCEOFF, FORCEON	0		5.5	V
V_I	Receiver input voltage		- 25		25	V
T_A	Operating free-air temperature		- 40		85	°C

(1) Test conditions are $C1 - C4 = 0.1\ \mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\ \mu\text{F}$, $C2 - C4 = 0.33\ \mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TRSF3243E		UNIT
		VQFN (RHB)	TSSOP (PW)	
		32 PINS	28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.1	70.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.9	21.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.6	29.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.6	28.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.1	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
I_I	Input leakage current	FORCEOFF, FORCEON		±0.01	±1	μA
I_{CC}	Supply current	Auto-powerdown disabled	No load, FORCEOFF and FORCEON = V_{CC}	0.3	1.2	mA
		Powered off	No load, FORCEOFF = GND	1	10	
		Auto-powerdown enabled	No load, FORCEOFF = V_{CC} , FORCEON = GND, All RIN are open or grounded, All DIN are grounded	1	10	μA

(1) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

(2) Test conditions are $C1 - C4 = 0.1\ \mu\text{F}$ at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; $C1 = 0.047\ \mu\text{F}$, $C2 - C4 = 0.33\ \mu\text{F}$ at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.7 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	All DOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL}	Low-level output voltage	All DOUT at R _L = 3 kΩ to GND		-5.4	-5	V
V _O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V _{CC} , 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	±5			V
I _{IH}	High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL}	Low-level input current	V _I = GND		±0.01	±1	μA
I _{OS}	Short-circuit output current ⁽²⁾	V _{CC} = 3.6 V, V _O = 0 V V _{CC} = 5.5 V, V _O = 0 V		±35	±60	mA
r _o	Output resistance	V _{CC} , V ₊ , and V ₋ = 0 V, V _O = ±2 V	300	10M		Ω
I _{off}	Output leakage current	FORCEOFF = GND V _O = ±12 V, V _{CC} = 3 V to 3.6 V V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V			±25 ±25	μA

- (1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
- (2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
- (3) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.8 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽³⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
Maximum data rate (see Fig 7-1)	R _L = 3 kΩ, One DOUT switching	C _L = 1000 pF		250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V		1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V		1000		
t _{sk(p)}	Pulse skew ⁽²⁾	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Fig 7-2		25		ns
SR(tr)	Slew rate, transition region (see Fig 7-1)	C _L = 150 pF to 1000 pF, R _L = 3 kΩ to 7 kΩ, V _{CC} = 3.3 V		18	150	V/μs

- (1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.
- (2) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.
- (3) Test conditions are C1 - C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2 - C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.9 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽²⁾	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current (except ROUT2B)	FORCEOFF = 0 V		±0.05	±10	μA
r _i	Input resistance	V _I = ±3 V to ±25 V	3	5	7	kΩ

- (1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(2) Test conditions are C1 - C4 = 0.1 μ F at $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; C1 = 0.047 μ F, C2 - C4 = 0.33 μ F at $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$.

6.10 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽³⁾	TYP ⁽¹⁾	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 150 \text{ pF}$, See 图 7-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output	$C_L = 150 \text{ pF}$, See 图 7-3	150	ns
t_{en}	Output enable time	$C_L = 150 \text{ pF}$, $R_L = 3 \text{ k}\Omega$, See 图 7-4	200	ns
t_{dis}	Output disable time	$C_L = 150 \text{ pF}$, $R_L = 3 \text{ k}\Omega$, See 图 7-4	200	ns
$t_{sk(p)}$	Pulse skew ⁽²⁾	See 图 7-3	50	ns

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

(3) Test conditions are C1 - C4 = 0.1 μ F at $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$; C1 = 0.047 μ F, C2 - C4 = 0.33 μ F at $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$.

6.11 Electrical Characteristics: Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 7-5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	- 2.7		V
$V_{T(invalid)}$	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	- 0.3	0.3	V
V_{OH}	INVALID high-level output voltage	$I_{OH} = - 1 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}	$V_{CC} - 0.6$		V
V_{OL}	INVALID low-level output voltage	$I_{OL} = 1.6 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}		0.4	V

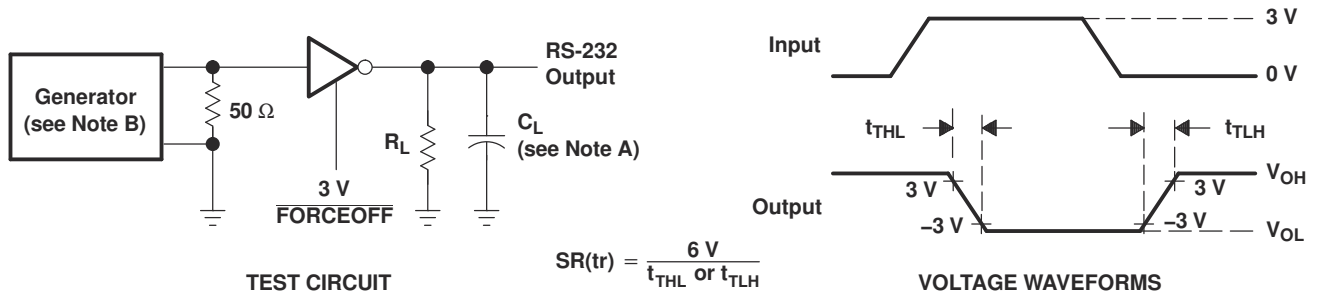
6.12 Switching Characteristics: Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [图 7-5](#))

PARAMETER		TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	μ s
$t_{invalid}$	Propagation delay time, high- to low-level output	30	μ s
t_{en}	Supply enable time	100	μ s

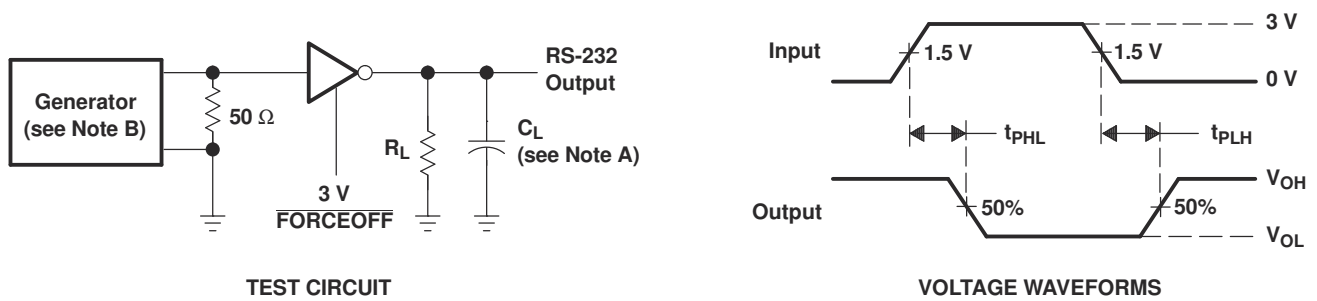
(1) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

Parameter Measurement Information



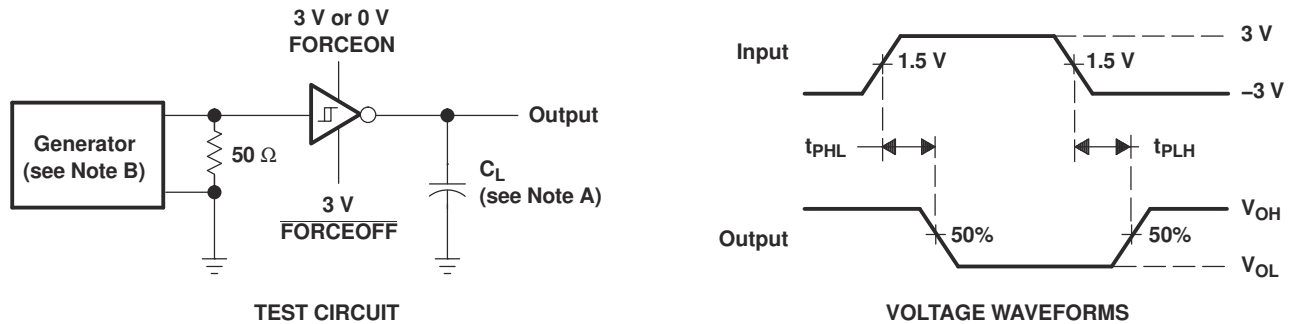
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 7-1. Driver Slew Rate



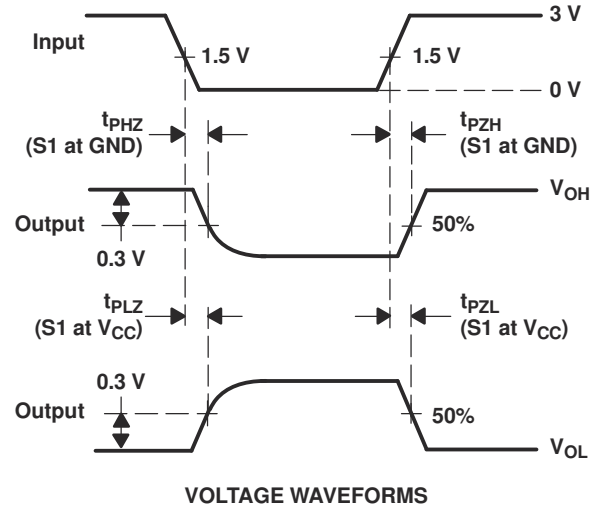
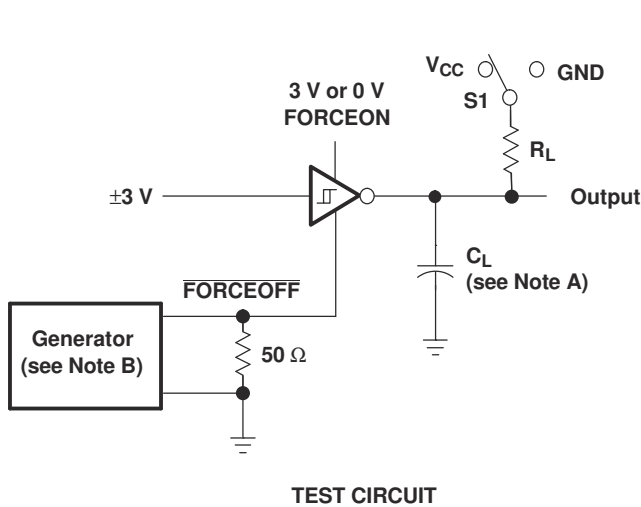
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 1 Mbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 7-2. Driver Pulse Skew



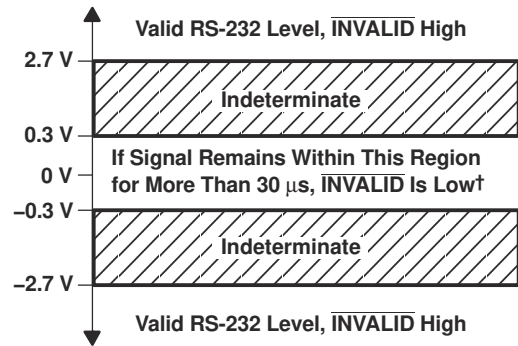
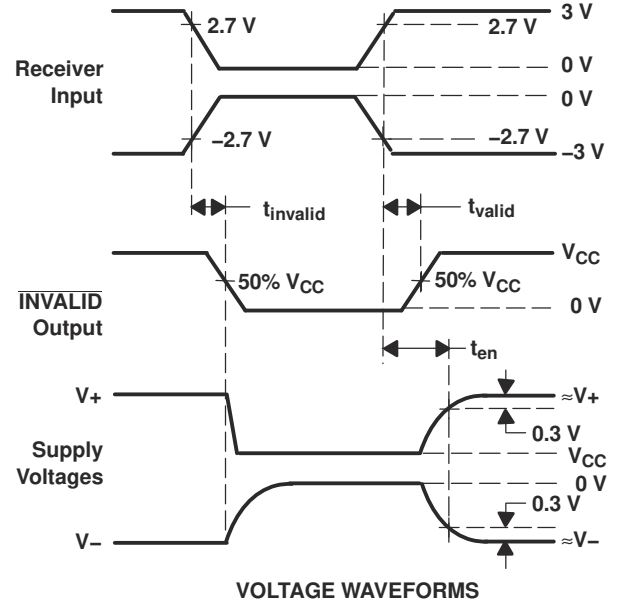
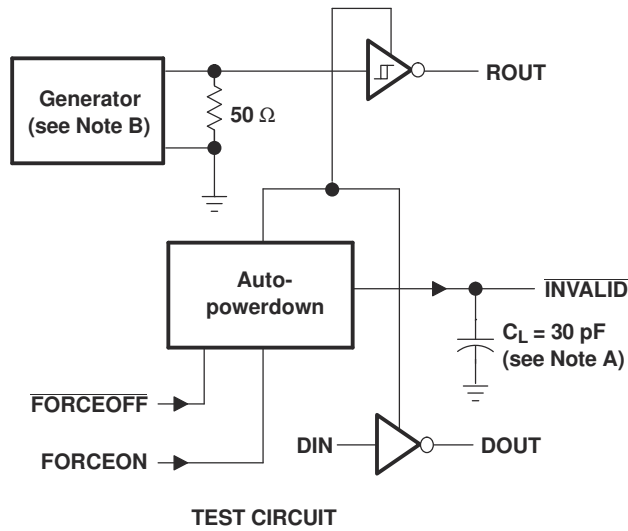
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

图 7-3. Receiver Propagation Delay Times



- NOTES: A. C_L includes probe and jig capacitance.
 B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
 C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 D. t_{PZL} and t_{PZH} are the same as t_{en} .

图 7-4. Receiver Enable and Disable Times



† Auto-powerdown disables drivers and reduces supply current to 1 μ A.

- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

图 7-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

7 Detailed Description

7.1 Overview

The TRSF3243E device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ± 15 -kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ± 8 -kV ESD (IEC61000-4-2, Contact Discharge) protection on serial-port connection pins. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector.

The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 500 kbit/s and a maximum of 30-V/ μ s driver output slew rate.

Functional Block Diagram

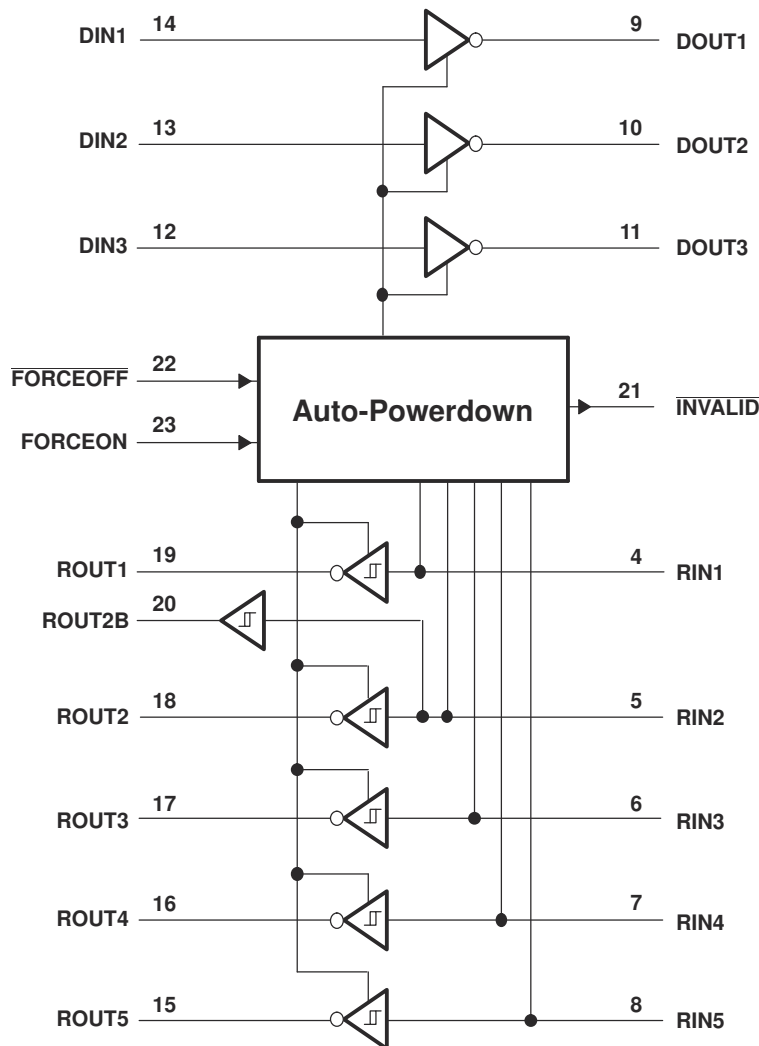


图 7-1. Logic Diagram

7.2 Feature Description

Auto-powerdown can be disabled when FORCEON and FORCEOFF are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30 μs. INVALID is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 μs. Refer to [Figure 7-5](#) for receiver input levels.

7.3 Device Functional Modes

[Table 7-1](#) through [Table 7-3](#) show the device functional modes.

Table 7-1. Each Driver

INPUTS ⁽¹⁾				OUTPUT		DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL	DOUT		
X	X	L	X	Z	Powered off	
L	H	H	X	H	Normal operation with auto-powerdown disabled	
H	H	H	X	L		
L	L	H	Yes	H	Normal operation with auto-powerdown enabled	
H	L	H	Yes	L		
X	L	H	No	Z	Powered off by auto-powerdown feature	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Table 7-2. Each Receiver

INPUTS ⁽¹⁾			OUTPUT		RECEIVER STATUS
RIN	FORCEON	FORCEOFF	ROUT		
X	X	L	Z	Powered off	
L	X	H	H	Normal operation with auto-powerdown disabled/enabled	
H	X	H	L		
Open	X	H	H		

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Table 7-3. ROUT2B And Outputs INVALID

INPUTS ⁽¹⁾				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	FORCEOFF	INVALID	ROUT2B	
Yes	L	X	X	H	L	Always active
Yes	H	X	X	H	H	
Yes	Open	X	X	H	L	
No	Open	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

8 Application and Implementation

备注

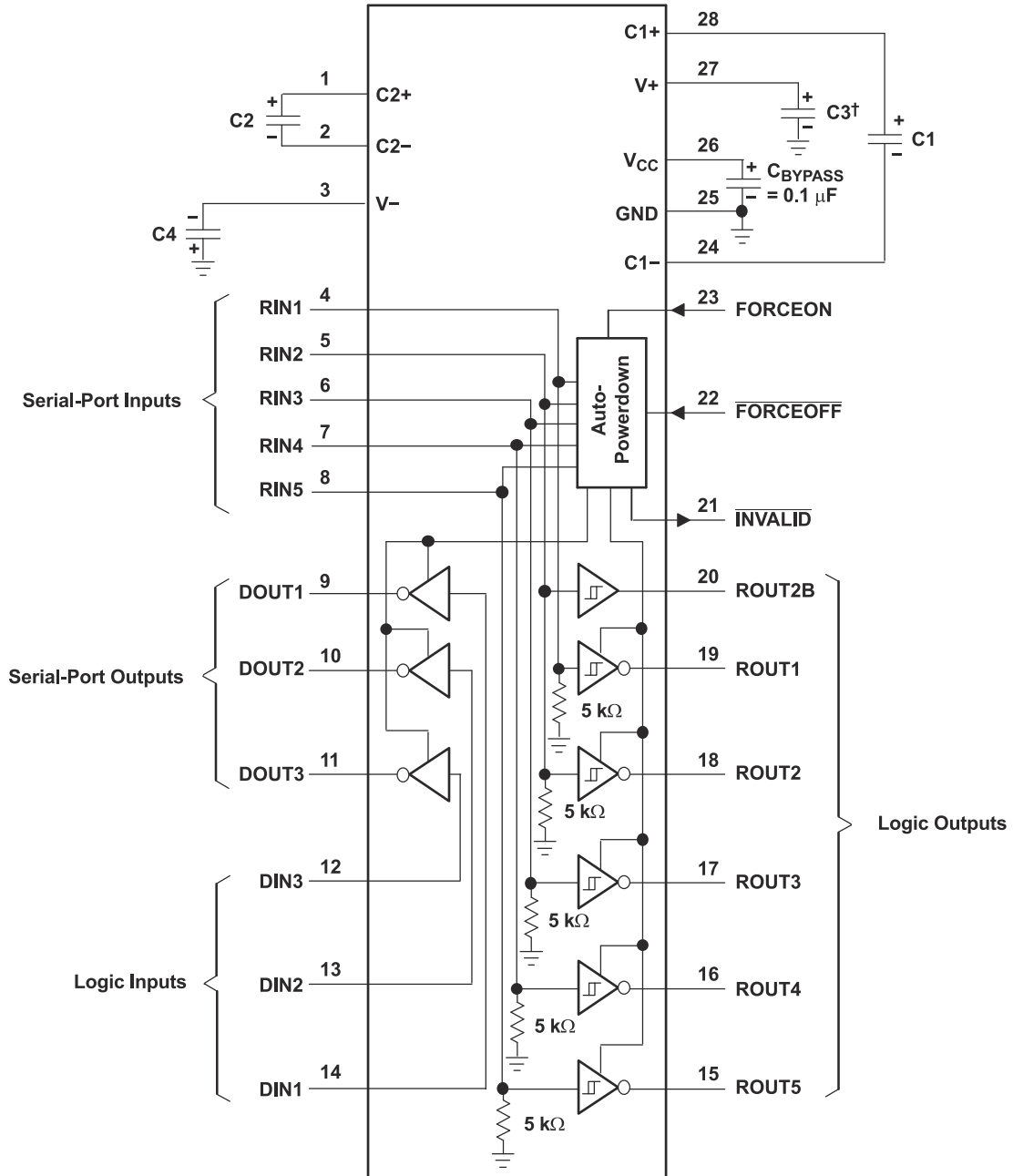
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8.1 Application Information

For proper operation, add capacitors as shown in [图 8-1](#). Pins 12 through 23 connect to UART or general-purpose logic lines. RS-232 lines on Pins 4 through 11 connect to a connector or cable.

8.2 Typical Application

Three driver and five receiver channels are supported for full duplex transmission with hardware flow control. The five 5-k Ω resistors are internal to the device.



- A. C3 can be connected to V_{CC} or GND
- B. Resistor values shown are nominal.

图 8-1. Typical Operating Circuit and Capacitor Values

8.3 Design Requirements

For this design example, use the values in [V_{CC} vs Capacitor Values](#).

- V_{CC} minimum is 3 V and maximum is 5.5 V.
- Maximum recommended bit rate is 1 Mbps.

表 8-1. V_{CC} vs Capacitor Values

V _{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

8.4 Detailed Design Procedure

TRSF3243E has integrated charge-pump that generates positive and negative rails needed for RS-232 signal levels. Main design requirement is that charge-pump capacitor terminals must be connected with recommended capacitor values. Charge-pump rail voltages and device supply pin must be properly bypassed with ceramic capacitors.

9 Power Supply Recommendations

The V_{CC} voltage must be connected to the same power source used for logic device connected to DIN and ROUT pins. V_{CC} must be between 3 V and 5.5 V.

10 Layout

10.1 Layout Guidelines

As shown in [Layout Example](#), charge-pump and supply voltage capacitors must be located very close to device pins. Non-polarized ceramic capacitors are recommended. If polarized tantalum or electrolytic capacitors are used, they should be connected as per [Typical Operating Circuit and Capacitor Values](#).

10.2 Layout Example

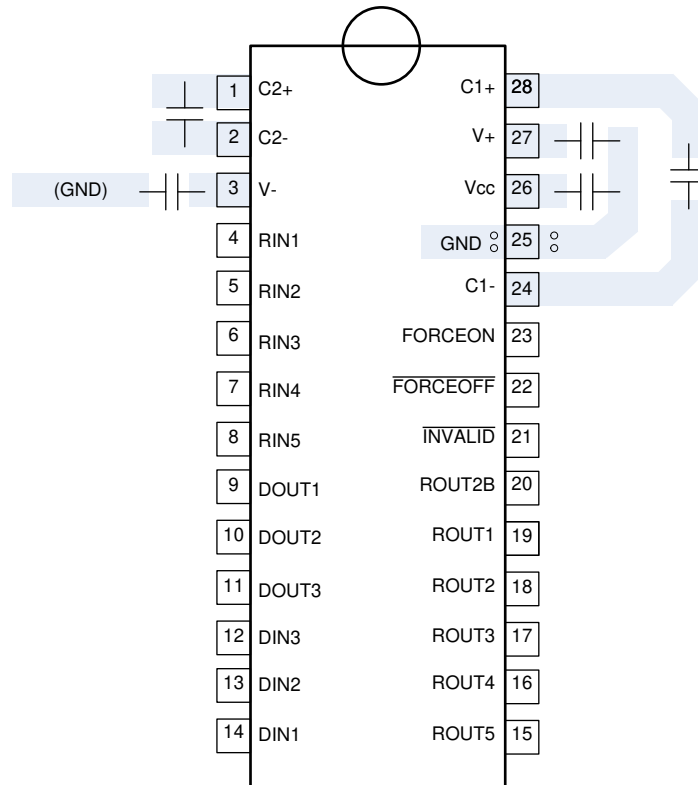


图 10-1. Example Layout

Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.3 商标

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRSF3243EIPWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F3243	Samples
TRSF3243EIRHBR	ACTIVE	VQFN	RHB	32	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TRSF 3243	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3243EIPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRSF3243EIRHBR	VQFN	RHB	32	5000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3243EIPWR	TSSOP	PW	28	2000	356.0	356.0	35.0
TRSF3243EIRHBR	VQFN	RHB	32	5000	367.0	367.0	35.0

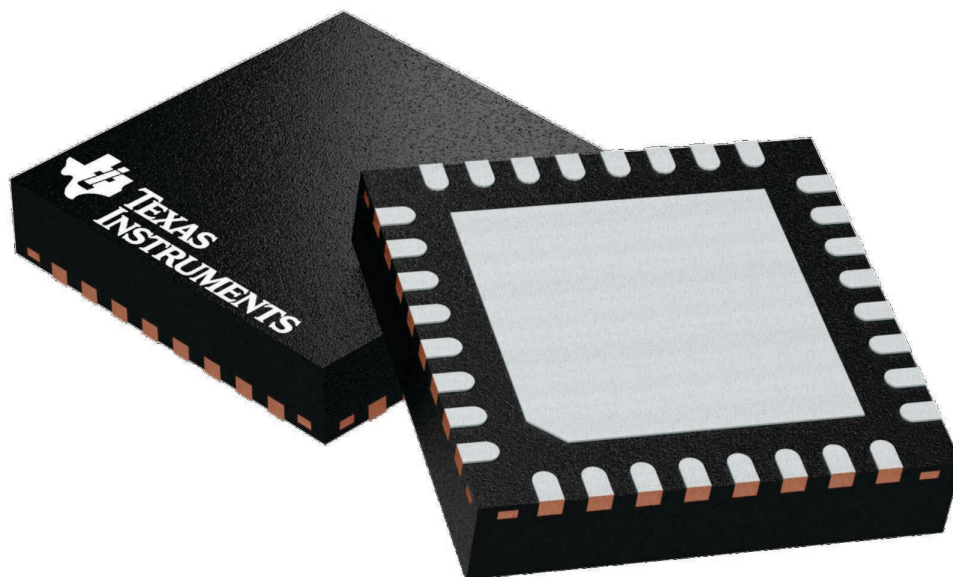
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224745/A



4223442/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

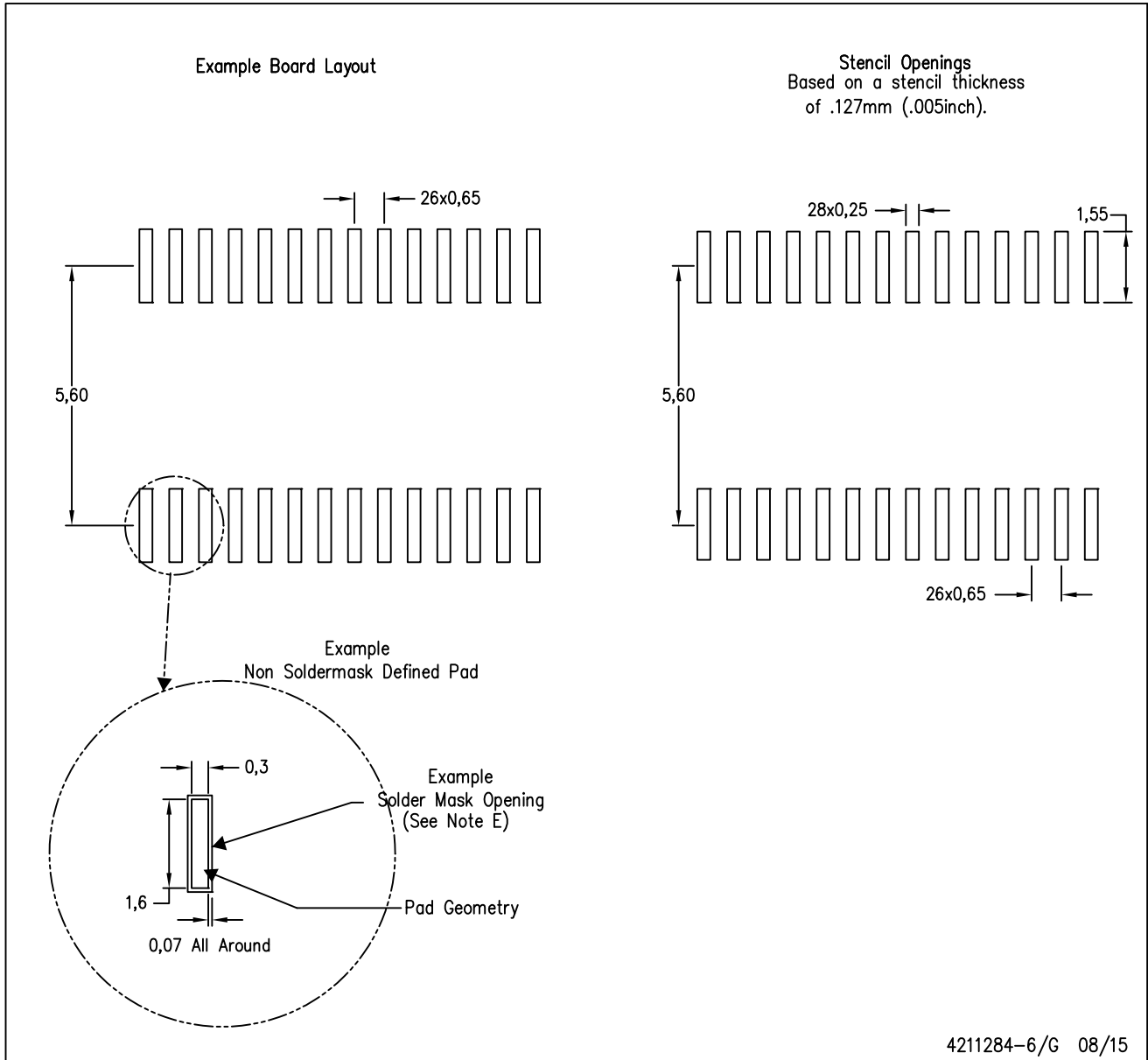


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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