

## TUSB216I 具有 BC 1.2 控制器的 USB 2.0 高速信号调节器

### 1 特性

- 宽电源电压范围：2.3V 至 6.5V
- 超低 USB 断开和关断功耗
- 可提供 USB 2.0 高速信号调节
- 与 USB 2.0、OTG 2.0 和 BC 1.2 兼容
- 支持低速、全速和高速信号传输
- 集成了 BC 1.2 CDP 电池充电控制器
- 主机/器件无关
- 支持长达 5m 的电缆
  - 通过外部下拉电阻器值实现四种可选的信号增强（边沿升压与直流升压）设置
  - 通过上拉或下拉实现三种可选的 RX 灵敏度设置，以补偿高损耗应用中的 ISI 抖动
- TUSB216I 支持长达 10m 的电缆和两台器件
- 可扩展解决方案 - 器件可通过菊花链连接，以用于高损耗应用
- 与 TUSB211/212/214 引脚兼容 (3.3V)

### 2 应用

- 笔记本电脑/台式机/扩展坞
- [便携式电子产品](#)
- [平板电脑](#)
- 手机
- 电视
- 有源电缆、电缆扩展器、背板

### 3 说明

TUSB216I 是第三代 USB 2.0 高速信号调节器，旨在补偿传输通道中的交流损失（由于电容性负载）和直流损失（由于电阻性负载）。

TUSB216I 采用了专利设计，可通过边缘加速器来对 USB 2.0 高速信号的传输边缘进行加速，并通过直流升压功能来提高静态电平。

TUSB216I 此外，还具有预均衡功能，可提高接收器的灵敏度并补偿较长线缆应用中的码间串扰 (ISI) 抖动。TUSB216IUSB 低速和全速信号特征不受的影响。

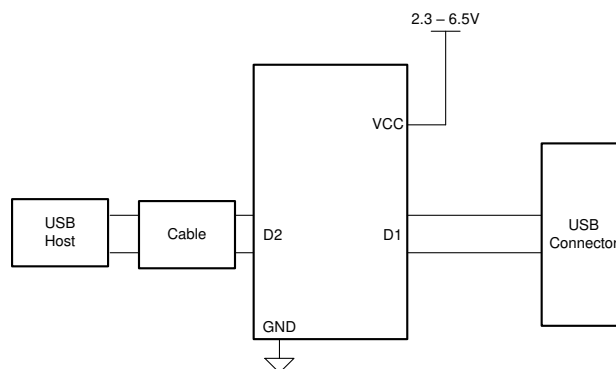
TUSB216I 可在不改变数据包计时或不增加传播延迟的情况下提高信号质量。

TUSB216I 可使用长达 5 米的线缆帮助系统通过 USB 2.0 高速近端眼图合规性测试。

TUSB216I 与 USB On-The-Go (OTG) 和电池充电 (BC 1.2) 协议兼容。集成的 BC 1.2 电池充电控制器可通过控制引脚启用。

#### 器件信息

器件型号	封装	OP TEMP (TA) °C	封装尺寸 (标称值)
TUSB216I	X2QFN (12)	-40 至 85	1.60mm x 1.60mm



简化版原理图



## Table of Contents

<b>1 特性</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>9</b>
<b>2 应用</b> .....	<b>1</b>	7.5 TUSB216 Registers.....	<b>10</b>
<b>3 说明</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>14</b>
<b>4 Revision History</b> .....	<b>2</b>	8.1 Application Information.....	14
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.2 Typical Application.....	14
<b>6 Specifications</b> .....	<b>5</b>	<b>9 Power Supply Recommendations</b> .....	<b>22</b>
6.1 Absolute Maximum Ratings .....	5	<b>10 Layout</b> .....	<b>23</b>
6.2 ESD Ratings .....	5	10.1 Layout Guidelines.....	23
6.3 Recommended Operating Conditions .....	5	10.2 Layout Example.....	23
6.4 Thermal Information .....	5	<b>11 Device and Documentation Support</b> .....	<b>24</b>
6.5 Electrical Characteristics .....	6	11.1 接收文档更新通知.....	24
6.6 Switching Characteristics .....	7	11.2 支持资源.....	24
6.7 Timing Requirements .....	8	11.3 Trademarks.....	24
<b>7 Detailed Description</b> .....	<b>9</b>	11.4 静电放电警告.....	24
7.1 Overview.....	9	11.5 术语表.....	24
7.2 Functional Block Diagram.....	9	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>24</b>
7.3 Feature Description.....	9		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
March 2021	*	Initial Release

## 5 Pin Configuration and Functions

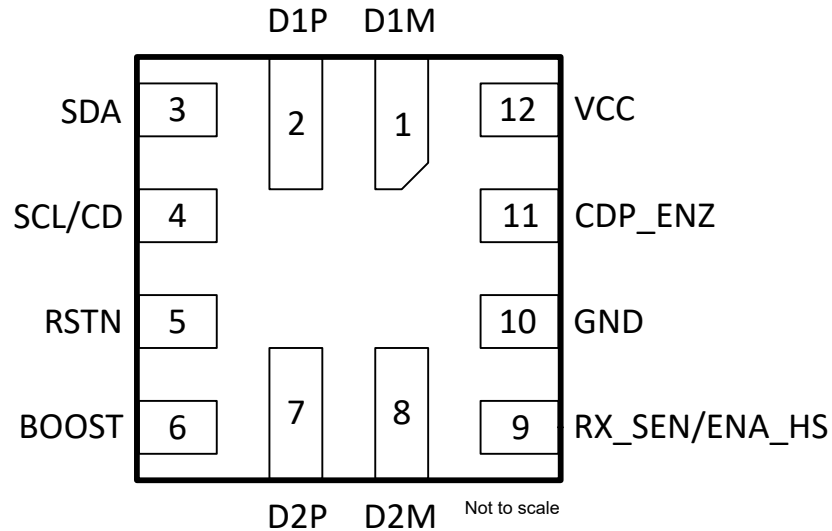


图 5-1. TUSB216I RWB 12-Pin X2QFN Top View

表 5-1. Pin Functions

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
BOOST	6	I	N/A	USB High-speed boost select via external pull down resistor. Both edge boost and DC boost are controlled by a single pin in non-I2C mode. In I2C mode edge boost and DC boost can be individually controlled. Sampled upon power up. Does not recognize real time adjustments. Auto selects BOOST LEVEL = 3 when left floating.
CDP_ENZ	11	I	500 k $\Omega$ PU	Set CDP_ENZ is low to enable BC 1.2 CDP controller
RX_SEN2/ENA_HS	9	I/O	N/A	In I2C mode: Reserved for TI test purpose. In non-I2C mode: At reset: 3-level input signal RX_SEN. USB High-speed RX Sensitivity Setting to Compensate ISI Jitter H (pin is pulled high) - high RX sensitivity (high loss channel) M (pin is left floating) - medium RX sensitivity (medium loss channel) L (pin is pulled low) - low RX sensitivity (low loss channel) After reset: Output signal ENA_HS. Flag indicating that channel is in High-speed mode. Asserted upon: 1. Detection of USB-IF High-speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 $\mu$ s - 128 $\mu$ s].

表 5-1. Pin Functions (continued)

PIN		I/O	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
D2P	7	I/O	N/A	USB High-speed positive port.
D2M	8	I/O	N/A	USB High-speed negative port.
GND	10	P	N/A	Ground
D1M	1	I/O	N/A	USB High-speed negative port..
D1P	2	I/O	N/A	USB High-speed positive port.
SDA1	3	I/O	500 k $\Omega$ PU 1.8 M $\Omega$ PD	I2C Mode: Bidirectional I2C data pin [7-bit I2C slave address = 0x2C]. In non I2C mode: Reserved for TI test purpose.
VCC	12	P	N/A	Supply power
RSTN	5	I	500 k $\Omega$ PU 1.8 M $\Omega$ PD	Device disable/enable. Low - Device is at reset and in shutdown, and High - Normal operation. Recommend 0.1- $\mu$ F external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.
SCL1/CD	4	I/O	When RSTN asserted there is a 500 k $\Omega$ PD	In I2C mode: I2C clock pin [I2C address = 0x2C]. Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.

1. Pull-up resistors for SDA and SCL pins in I<sup>2</sup>C mode should be  $R_{\text{Pull-up}}$  (depending on I2C bus voltage). If both SDA and SCL are pulled up at power-up the device enters into I<sup>2</sup>C mode.
2. Pull-down and pull-up resistors for RX\_SEN pin must follow  $R_{\text{RXSEN1}}$  and  $R_{\text{RXSEN2}}$  resistor recommendations in non I<sup>2</sup>C mode.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range	VCC	- 0.3	7	V
Voltage range USB data	DxP, DxM	- 0.3	5.5	V
Voltage range on BOOST pin	BOOST	-0.3	1.98	V
Voltage range other pins	RX_SEN, CDP_ENZ, SDA, SCL, RSTN	-0.3	5.5	V
Storage temperature, T <sub>stg</sub>		- 65	150	°C
Maximum junction temperature, T <sub>J(max)</sub>			125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per	±2000	V
		Charged-device model (CDM), per	±750	

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.3	5	6.5	V
T <sub>A</sub>	Operating free-air temperature (Industrial)	- 40		85	°C
T <sub>J</sub>	Junction temperature (Industrial)			105	°C
V <sub>I2C_BUS</sub>	I2C Bus Voltage	1.62		3.6	V
DxP, DxM	Voltage range USB data	0		3.6	V
BOOST	Voltage range BOOST pin	0		1.98	V
CDP_ENZ	Voltage range other pins (SCL, SDA, RSTN, CDP_ENZ)	0		3.6	V
RX_SEN	Voltage range RX_SEN pin	0		5.0	V

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		RWB (X2QFN)	UNIT
		12 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	137.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	62	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	67.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	67.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>POWER</b>						
I <sub>ACTIVE_HS</sub>	High Speed Active Current	USB channel = HS mode. 480 Mbps traffic. V <sub>CC</sub> supply stable, with Boost = Max		22	36	mA
I <sub>IDLE_HS</sub>	High Speed Idle Current	USB channel = HS mode, no traffic. V <sub>CC</sub> supply stable, Boost = Max		22	36	mA
I <sub>HS_SUSPEND</sub>	High Speed Suspend Current	USB channel = HS Suspend mode. V <sub>CC</sub> supply stable		0.75	1.4	mA
I <sub>FS</sub>	Full-Speed Current	USB channel = FS mode, 12 Mbps traffic, V <sub>CC</sub> supply stable		0.75	1.4	mA
I <sub>DISCONN</sub>	Disconnect Power	Host side application. No device attachment.		0.80	1.4	mA
I <sub>SHUTDOWN</sub>	Shutdown Power	RSTN driven low, V <sub>CC</sub> supply stable		60	115	μA
<b>CONTROL PIN LEAKAGE</b>						
I <sub>LKG_FS</sub>	Pin failsafe leakage current for SDA, RSTN	V <sub>CC</sub> = 0 V, pin at V <sub>IH, max</sub>		10	15	μA
I <sub>LKG_FS</sub>	Pin failsafe leakage current for RX_SEN	V <sub>CC</sub> = 0 V, pin at V <sub>IH, max</sub>		6	15	μA
I <sub>LKG_FS</sub>	Pin failsafe leakage current for SCL	V <sub>CC</sub> = 0 V, pin at V <sub>IH, max</sub>			70	nA
<b>INPUT RSTN</b>						
V <sub>IH</sub>	High level input voltage		1.5		3.6	V
V <sub>IL</sub>	Low-level input voltage		0		0.5	V
I <sub>IH</sub>	High level input current	V <sub>IH</sub> = 3.6 V, R <sub>PU</sub> enabled			±15	μA
I <sub>IL</sub>	Low level input current	V <sub>IL</sub> = 0V, R <sub>PU</sub> enabled			±20	μA
<b>INPUT DIGITAL</b>						
V <sub>IH</sub>	High level input voltage (CDP_ENZ)		1.5		3.6	V
V <sub>IL</sub>	Low-level input voltage (CDP_ENZ)		0		0.5	V
I <sub>IL</sub>	Low level input current	V <sub>IL</sub> = 0V			±20	μA
I <sub>IH</sub>	High level input current	V <sub>IH</sub> = 3.6 V			±15	μA
<b>INPUT RX_SEN (3-level input, for mid level leave pin floating)</b>						
V <sub>IH(Max)</sub>	Maximum High level input voltage	V <sub>CC</sub> = 2.3V to 6.5V			5.0	V
V <sub>IH(Min)</sub>	Minimum High level input voltage	V <sub>CC</sub> = 2.3V to 6.5V (% of V <sub>CC</sub> )	75			%
V <sub>IL</sub>	Low level input voltage				0.75	V
<b>INPUT BOOST</b>						
R <sub>BOOST_LVL0</sub>	External pulldown resistor for BOOST Level 0				160	Ω
R <sub>BOOST_LVL1</sub>	External pulldown resistor for BOOST Level 1		1.5	1.8	2	kΩ
R <sub>BOOST_LVL2</sub>	External pulldown resistor for BOOST Level 2		3.4	3.6	3.96	kΩ
R <sub>BOOST_LVL3</sub>	External pulldown resistor for BOOST Level 3 to remove upper limit for resistor value, can be left open		7.5			kΩ
<b>OUTPUTS CD, ENA_HS</b>						
V <sub>OH</sub>	High level output voltage for CD and ENA_HS	I <sub>O</sub> = - 50 μA, V <sub>CC</sub> ≥ 3.0V	2.5			V
V <sub>OH</sub>	High level output voltage for CD	I <sub>O</sub> = - 25 μA, V <sub>CC</sub> = 2.3V	1.7			V

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	High level output voltage for ENA_HS	I <sub>O</sub> = - 25 μA, VCC = 2.3V	1.8			V
V <sub>OL</sub>	Low level output voltage for CD and ENA_HS	I <sub>O</sub> = 50 μA			0.3	V
<b>I<sup>2</sup>C</b>						
C <sub>I2C_BUS</sub>	I <sup>2</sup> C Bus Capacitance		4		150	pF
I <sub>OL</sub>	I <sup>2</sup> C open drain output current	V <sub>OL</sub> = 0.4V	1.5			mA
V <sub>IL</sub>	2.3V ≤ VCC ≤ 4.3V, V <sub>I2C_BUS</sub> = 1.8V +/-10%	R <sub>Pull-up</sub> = 1.6kΩ to 2.5kΩ, % of V <sub>I2C_BUS</sub>			25	%
V <sub>IL</sub>	V <sub>I2C_BUS</sub> = 3.3V +/-10%	R <sub>Pull-up</sub> = 2.8kΩ to 7kΩ, % of V <sub>I2C_BUS</sub>			25	%
V <sub>IH</sub>	2.3V ≤ VCC ≤ 4.3V, V <sub>I2C_BUS</sub> = 1.8V +/-10%	R <sub>Pull-up</sub> = 1.6kΩ to 2.5kΩ, % of V <sub>I2C_BUS</sub>	80			%
V <sub>IH</sub>	V <sub>I2C_BUS</sub> = 3.3V +/-10%	R <sub>Pull-up</sub> = 2.8kΩ to 7kΩ, % of V <sub>I2C_BUS</sub>	75			%
R <sub>Pull-up</sub>	V <sub>I2C_BUS</sub> = 1.8V +/-10%		1.6	2	2.5	kΩ
R <sub>Pull-up</sub>	V <sub>I2C_BUS</sub> = 3.3V +/-10%		2.8	4.7	7	kΩ
SCL Frequency					100	kHz
<b>DxP, DxM</b>						
C <sub>IO_DXX</sub>	Capacitance to GND	Measured with VNA at 240 MHz, VCC supply stable, Redriver off		2.5		pF

(1) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
<b>DxP, DxM USB Signals</b>						
F <sub>BR_DXX</sub>	Bit Rate	USB channel = HS mode. 480 Mbps traffic. VCC supply stable			480	Mbps
t <sub>R/F_DXX</sub>	Rise/Fall time		100			ps

(1) All typical values are at V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
<b>POWER UP TIMING</b>					
$T_{RSTN\_PW}$	Minimum width to detect a valid RSTN signal assert when the pin is actively driven low	100			$\mu$ s
$T_{STABLE}$	VCC must be stable before RSTN de-assertion	300			$\mu$ s
$T_{READY}$	Maximum time needed for the device to be ready after RSTN is de-asserted.			500	$\mu$ s
$T_{RAMP}$	$V_{CC}$ ramp time			100	ms
$T_{RAMP}$	$V_{CC}$ ramp time	0.2			ms
<b>I2C (STD)</b>					
$t_{SUSTO}$	Stop setup time, SCL ( $T_r=600$ ns-1000ns), SDA ( $T_f=6.5$ ns-106.5ns), 100kHz STD	4			$\mu$ s
$t_{HDSTA}$	Start hold time, SCL ( $T_r=600$ ns-1000ns), SDA ( $T_f=6.5$ ns-106.5ns), 100kHz STD	4			$\mu$ s
$t_{SUSTA}$	Start setup time, SCL ( $T_r=600$ ns-1000ns), SDA ( $T_f=6.5$ ns-106.5ns), 100kHz STD	4.7			$\mu$ s
$t_{SUDAT}$	Data input or False start/stop, setup time, SCL ( $T_r=600$ ns-1000ns), SDA ( $T_f=6.5$ ns-106.5ns), 100kHz STD	250			ns
$t_{HDDAT}$	Data input or False start/stop, hold time, SCL ( $T_r=600$ ns-1000ns), SDA ( $T_f=6.5$ ns-106.5ns), 100kHz STD	5			$\mu$ s
$t_{BUF}$	Bus free time between START and STOP conditions	4.7			$\mu$ s
$t_{LOW}$	Low period of the I <sub>2</sub> C clock	4.7			$\mu$ s
$t_{HIGH}$	High period of the I <sub>2</sub> C clock	4			$\mu$ s
$t_F$	Fall time of both SDA and SCL signals			300	ns
$t_R$	Rise time of both SDA and SCL signals			1000	ns



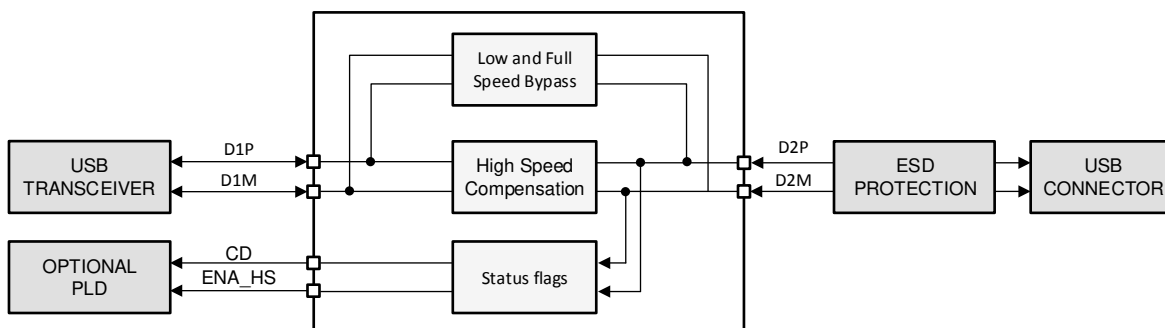
## 7 Detailed Description

### 7.1 Overview

The TUSB216I is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB216I has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. Additional RX sensitivity, tuned by external pull-up resistor and pull-down resistor, allows to overcome attenuation in cables. The TUSB216I allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

### 7.2 Functional Block Diagram



Copyright © 2018, Texas Instruments Incorporated

### 7.3 Feature Description

#### 7.3.1 High-speed Boost

The high-speed booster (combination of edge boost and DC boost) improves the eye width for USB2.0 high-speed signals. It is direction independent and by that is compatible to OTG systems. The BOOST pin is configuring the booster strength with different values of pull down resistors to set 4 levels of boosts, alternatively the boost level can be set via I2C register according to [节 7.4.6](#). Internal circuitry of the signal conditioner reduces possible overshoot.

#### 7.3.2 RX Sensitivity

The RX\_SEN pin is a tri-level pin. It is used to set the gain of the device according to system channel loss. RX sensitivity can be increased to recover incoming signals with low vertical eye opening to be able to boost weak signals and helps overcoming high attenuation.

### 7.4 Device Functional Modes

#### 7.4.1 Low-speed (LS) Mode

TUSB216I automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high but ENA\_HS will be low.

#### 7.4.2 Full-speed (FS) Mode

TUSB216I automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high but ENA\_HS will be low

#### 7.4.3 High-speed (HS) Mode

TUSB216I automatically detects a HS connection and will enable signal compensation as determined by the configuration of the RX\_SEN pin and the external pull down resistance on its BOOST pin.

CD pin and ENA\_HS pin are asserted high when high-speed boost is active.

#### 7.4.4 High-speed Downstream Port Electrical Compliance Test Mode

TUSB216I will detect HS compliance test fixture and enter downstream port high-speed eye diagram test mode. CD pin will be low and ENA\_HS pin is asserted high when TUSB216I is in HS eye compliance test mode.

If RSTN pin is asserted low and de-asserted high while TUSB216I is operating in HS functional mode, TUSB216I will transition to HS eye compliance test mode and CD asserts low and ENA\_HS remains high. When this occurs signal compensation is enabled.

#### 7.4.5 Shutdown Mode

TUSB216I can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

表 7-1. CD and ENA\_HS Pins in Different Modes

MODE	CD	ENA_HS
Low-speed	HIGH	LOW
Full-speed	HIGH	LOW
High-speed	HIGH	HIGH
High-speed downstream port electrical test	LOW	HIGH
Shutdown	LOW	LOW

#### 7.4.6 I<sup>2</sup>C Mode

TUSB216I supports 100 KHz I<sup>2</sup>C for device configuration, status read back and test purposes. For detail electrical and functional specifications refer to I<sup>2</sup>C Bus Specification 2.1, 2001 - STANDARD MODE. This controller is enabled after SCL and SDA pins are sampled high shortly after return from shutdown. In this mode, the CSR can be accessed by I<sup>2</sup>C read/write transaction to 7-bit slave address 0x2C. It is advised to set CFG\_ACTIVE bit before changing values. This halts the FSM, and reset it after all changes are made. This ensure proper startup into high-speed mode.

#### 7.4.7 BC 1.2 Battery Charging Controller

The TUSB216I main function is a signal conditioner offering the boost and pre-equalization features to the incoming DP/DM signals. For applications in which USB host or hub does not provide USB BC charging controller functionality, the TUSB216I can perform this task when CDP\_ENZ is low and BC 1.2 CDP Controller is enabled. When battery charging CDP controller feature is enabled (CDP\_ENZ=low) TUSB216I supports CDP charging downstream port functionality. CDP\_ENZ has an internal pull up when the pin is left unconnected CDP controller will be disabled.

表 7-2. TUSB216I Battery Charging Controller Modes

Pin 11 (CDP_ENZ)	CDP
High	NO
Low	YES

### 7.5 TUSB216 Registers

表 7-3 lists the memory-mapped registers for the TUSB216 registers. All register offset addresses not listed in 表 7-3 should be considered as reserved locations and the register contents should not be modified.

表 7-3. TUSB216 Registers

Offset	Acronym	Register Name	Section
0x1	EDGE_BOOST	This register is setting EDGE BOOST level.	<a href="#">Go</a>
0x3	CONFIGURATION	This register is selecting device mode.	<a href="#">Go</a>
0xE	DC_BOOST	This register is setting DC BOOST level.	<a href="#">Go</a>
0x25	RX_SEN	This register is setting RX Sensitivity level.	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. 表 7-4 shows the codes that are used for access types in this section.

**表 7-4. TUSB216 Access Type Codes**

Access Type	Code	Description
Read Type		
RH	H R	Set or cleared by hardware Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

### 7.5.1 EDGE\_BOOST Register (Offset = 0x1) [reset = X]

EDGE\_BOOST is shown in 图 7-1 and described in 表 7-5.

Return to [Summary Table](#).

This register is setting EDGE BOOST level.

**图 7-1. EDGE\_BOOST Register**

7	6	5	4	3	2	1	0
ACB_LVL				RESERVED			
RH/W-X				RH/W-X			

**表 7-5. EDGE\_BOOST Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	ACB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range  0x0 = BOOST PIN LEVEL 0 (lowest edge boost setting)  0x3 = BOOST PIN LEVEL 1  0x6 = BOOST PIN LEVEL 2  0xA = BOOST PIN LEVEL 3  0xF = (highest edge boost setting)
3-0	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values

### 7.5.2 CONFIGURATION Register (Offset = 0x3) [reset = X]

CONFIGURATION is shown in 图 7-2 and described in 表 7-6.

Return to [Summary Table](#).

This register is selecting device mode.

**图 7-2. CONFIGURATION Register**

7	6	5	4	3	2	1	0
RESERVED						CFG_ACTIVE	
RH/W-X						RH/W-0x1	

图 7-2. CONFIGURATION Register (continued)

表 7-6. CONFIGURATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values
0	CFG_ACTIVE	RH/W	0x1	Configuration mode After reset, if I2C mode is true (SCL and SDA are both pulled high) set the bit to get into configuration mode and clear to return to normal mode.  0x0 = NORMAL MODE 0x1 = CONFIGURATION MODE

### 7.5.3 DC\_BOOST Register (Offset = 0xE) [reset = X]

DC\_BOOST is shown in 图 7-3 and described in 表 7-7.

Return to [Summary Table](#).

This register is setting DC BOOST level.

图 7-3. DC\_BOOST Register

7	6	5	4	3	2	1	0
RESERVED				DCB_LVL			
RH/W-X				RH/W-X			

表 7-7. DC\_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values
3-0	DCB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range  0x0 = BOOST PIN LEVEL 0 (lowest dc boost setting)  0x2 = BOOST PIN LEVEL 1 and 2  0x6 = BOOST PIN LEVEL 3  0xF = (highest dc boost setting)

### 7.5.4 RX\_SEN Register (Offset = 0x25) [reset = X]

RX\_SEN is shown in 图 7-4 and described in 表 7-8.

Return to [Summary Table](#).

This register is setting RX Sensitivity level.

图 7-4. RX\_SEN Register

7	6	5	4	3	2	1	0
RX_SEN							
RH/W-X							

图 7-4. RX\_SEN Register (continued)

表 7-8. RX\_SEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RX_SEN	RH/W	X	XXXXb (sampled at startup from RX_SEN pin) 00000000b to 11111111b range  0x0 = RX_SEN LEVEL LOW  0x33 = RX_SEN LEVEL MID  0x66 = RX_SEN LEVEL HIGH  0xFF = (highest setting)

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

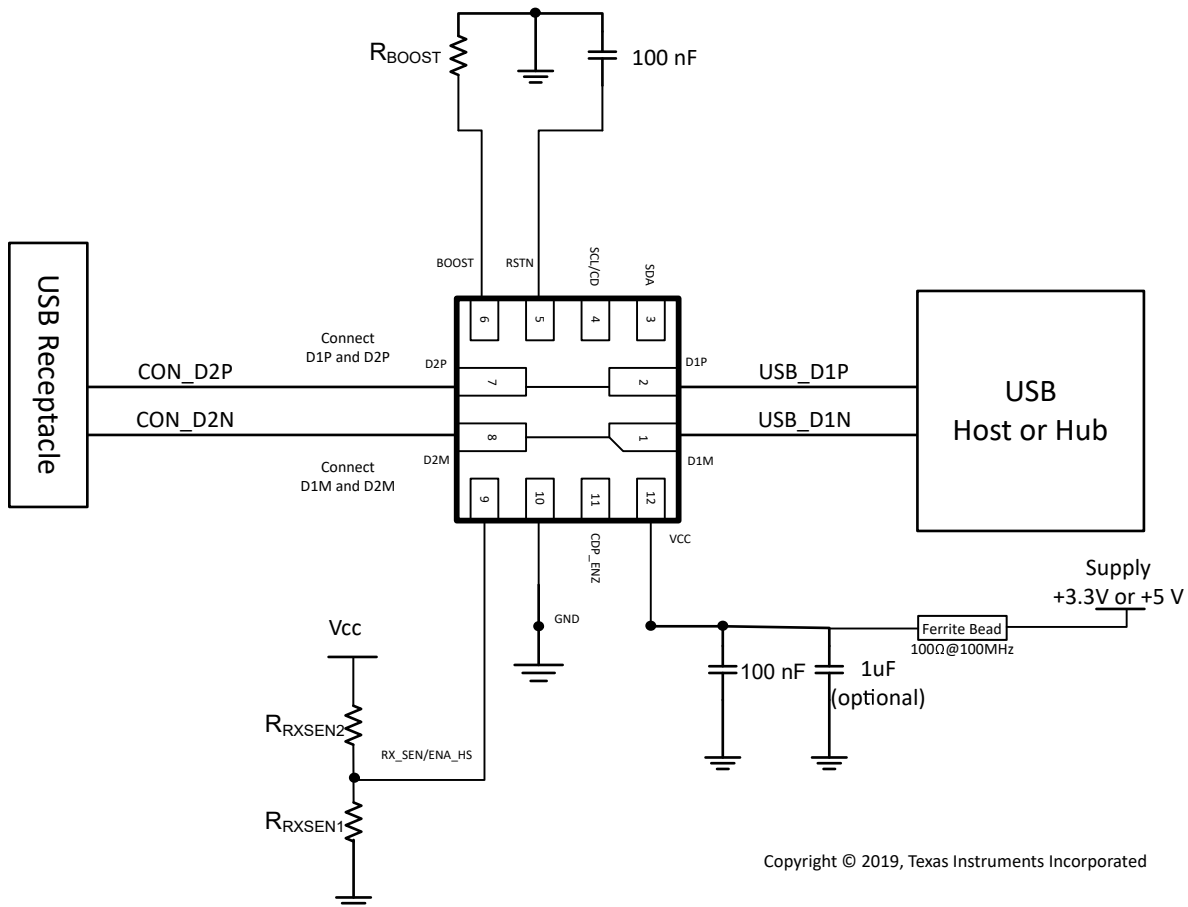
### 8.1 Application Information

The purpose of the TUSB216I is to re-store the signal integrity of a USB High-speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB216I can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB216I to control other blocks on the customer platform, if so desired.

### 8.2 Typical Application

A typical application for TUSB216I is shown in [Figure 8-1](#). In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].



Copyright © 2019, Texas Instruments Incorporated

**Figure 8-1. TUSB216I Reference Schematic (Design Example with CDP disabled), CDP\_ENZ can be left floating but an option for a decoupling capacitor of 0.1uF is recommended so the design is compatible with older devices: TUSB211, TUSB212, TUSB214**

### 8.2.1 Design Requirements

TUSB216I requires a valid reset signal as described in the *power supply recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters shown in [表 8-1](#), [表 8-2](#) and [表 8-3](#)

**表 8-1. Design Parameters for 5-V Supply With High Loss System**

PARAMETER				VALUE <sup>(1)</sup>
V <sub>CC</sub>				5 V ±10%
I <sup>2</sup> C support required in system (Yes/No)				No
Edge and DC Boost		<b>R<sub>BOOST</sub></b>	<b>BOOST Level</b>	Boost Level 1: R <sub>BOOST</sub> = 1.8 kΩ
		0-Ω	0	
		1.8 kΩ ±1%	1	
		3.6 kΩ ±1%	2	
		Do Not Install (DNI)	3	
RX Sensitivity	<b>R<sub>RXSEN1</sub></b>	<b>R<sub>RXSEN2</sub></b>	<b>RX_SEN Level</b>	High RX Sensitivity Level: R <sub>RXSEN1</sub> = 37.5 kΩ R <sub>RXSEN2</sub> = 12.5 kΩ
	22 kΩ - 40 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37.5 kΩ <sup>(2)</sup>	12.5 kΩ	High	

- (1) These parameters are starting values for a high loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 5V supply system could be applicable to 3.3V supply system as well.
- (2) This resistor is needed for a 5V supply to divide the voltage down so the RX\_SEN pin voltage does not exceed 5.0V

**表 8-2. Design Parameters for 3.3-V Supply With Low to Medium Loss System**

PARAMETER				VALUE <sup>(1)</sup>
V <sub>CC</sub>				3.3 V ±10%
I <sup>2</sup> C support required in system (Yes/No)				No
Edge and DC Boost		<b>R<sub>BOOST</sub></b>	<b>BOOST Level</b>	Boost Level 0: R <sub>BOOST</sub> = 0-Ω
		0-Ω	0	
		1.8 kΩ ±1%	1	
		3.6 kΩ ±1%	2	
		Do Not Install (DNI)	3	
RX Sensitivity	<b>R<sub>RXSEN1</sub></b>	<b>R<sub>RXSEN2</sub></b>	<b>RX_SEN Level</b>	Medium RX Sensitivity Level: R <sub>RXSEN1</sub> = DNI R <sub>RXSEN2</sub> = DNI
	22 kΩ - 40 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	Do Not Install (DNI)	22 kΩ - 40 kΩ (27 kΩ typical)	High	

- (1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 3.3V supply system could be applicable to 5V supply system as well.

表 8-3. Design Parameters for 2.3-V to 4.3-V VBAT Supply With Low to Medium Loss System

PARAMETER			VALUE <sup>(1)</sup>
V <sub>CC</sub>			2.3 V to 4.3V
I <sup>2</sup> C support required in system (Yes/No)			No
Edge and DC Boost	<b>R<sub>BOOST</sub></b>	<b>BOOST Level</b>	Boost Level 0: R <sub>BOOST</sub> = 0-Ω
	0-Ω	0	
	1.8 kΩ ±1%	1	
	3.6 kΩ ±1%	2	
	Do Not Install (DNI)	3	
RX Sensitivity	<b>R<sub>RXSEN1</sub></b>	<b>R<sub>RXSEN2</sub></b>	<b>RX_SEN Level</b>
	22 kΩ - 40 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low
	Do Not Install (DNI)	Do Not Install (DNI)	Medium
	37.5 kΩ <sup>(2)</sup>	12.5 kΩ	High
			Medium RX Sensitivity Level: R <sub>RXSEN1</sub> = DNI R <sub>RXSEN2</sub> = DNI

- (1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host and/or device as well as cable length and loss profile. These settings are not specific to a 2.3V-4.3V supply system could be applicable to 5V supply system as well.
- (2) This resistor is needed for a VBAT supply (2.3V - 4.3V) to divide the voltage down so the RX\_SEN pin voltage does not exceed 5.0V

### 8.2.2 Detailed Design Procedure

The ideal BOOST setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with BOOST level 0, and then increment to BOOST level 1, and so on. Same applies to the RX sensitivity setting where it is recommended to plan for the required pads or connections to change boost settings, but to start with RX sensitivity level Low.

In order for the TUSB216I to recognize any change to the BOOST setting, the RSTN pin must be toggled. This is because the BOOST pin is latched on power up and the pin is ignored thereafter.

#### Note

The TUSB216I compensates for extra attenuation in the signal path according to the configuration of the RX\_SEN pin. This maximum recommended voltage for this pin is 5 V when selecting the highest RX sensitivity level.

Placement of the device is also dependent on the application goal. 表 8-4 summarizes our recommendations.

表 8-4. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB216I PLACEMENT
Pass USB Near End Mask at the receptacle	Close to measurement point (connector)
Pass USB Far End Eye Mask at the plug	Close to USB PHY
Cascade multiple TUSB216s to improve device enumeration	Midway between each USB interconnect

表 8-5. Table of Recommended Settings

BOOST and RX_SEN settings <sup>(1)</sup> for channel loss		
Pre-channel cable length (Between USB PHY and TUSB216I)	BOOST	RX_SEN
0-3 meter	Level 0	Medium or High
2-5 meter	Level 1	Medium or High
Post-channel cable length (Between TUSB216I and inter-connect)	BOOST	RX_SEN
0-2 meter	Level 0	Medium or High
1-4 meter	Level 1	Medium or High

- (1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host and/or device as well as cable length and loss profile.



### 8.2.2.1 Test Procedure to Construct USB High-speed Eye Diagram

---

#### Note

USB-IF certification tests for High-speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

---

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High-speed Eye Mask:

#### 8.2.2.1.1 For a Host Side Application

1. Configure the TUSB216I to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB216I
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB216I
4. Enable the host to transmit USB TEST\_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB216I with a different BOOST setting (must reset to change)

#### 8.2.2.1.2 For a Device Side Application

1. Configure the TUSB216I to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB216I
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB216I. Ensure that the USB-IF device test fixture is configured to the 'INIT' position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST\_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the 'TEST' position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB216I with a different BOOST setting (must reset to change)

### 8.2.3 Application Curves

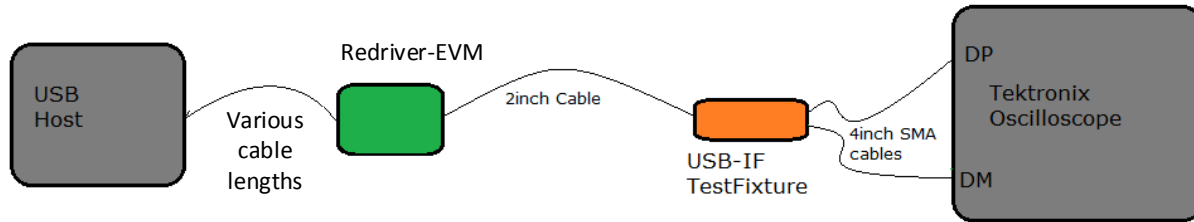


图 8-2. Near End Eye Measurement Set-Up With Pre-Channel Cable

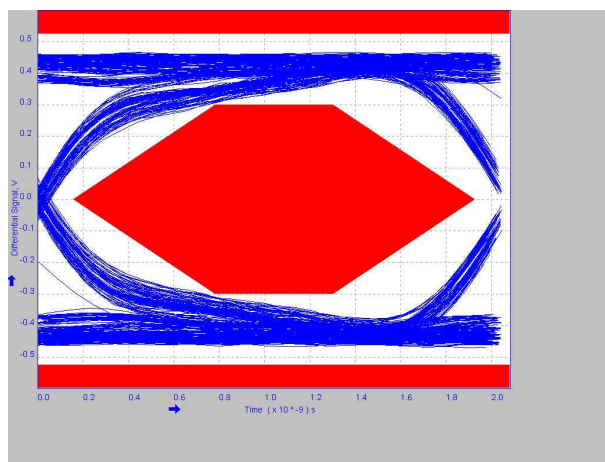


图 8-3. 2 Meter Pre-Channel Without TUSB216

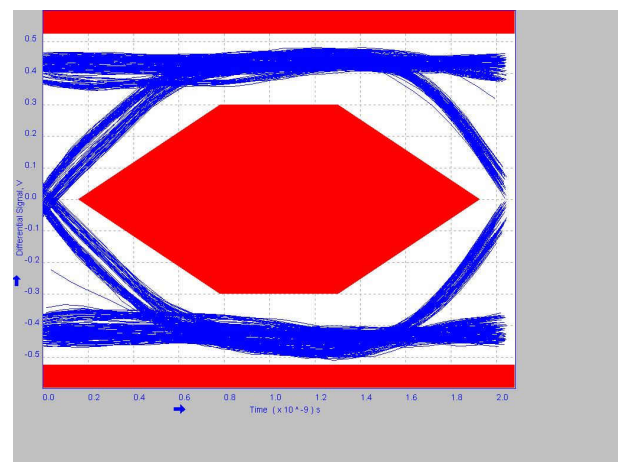


图 8-4. 2 Meter Pre-Channel With TUSB216  
BOOST=1 RX\_SEN=MED

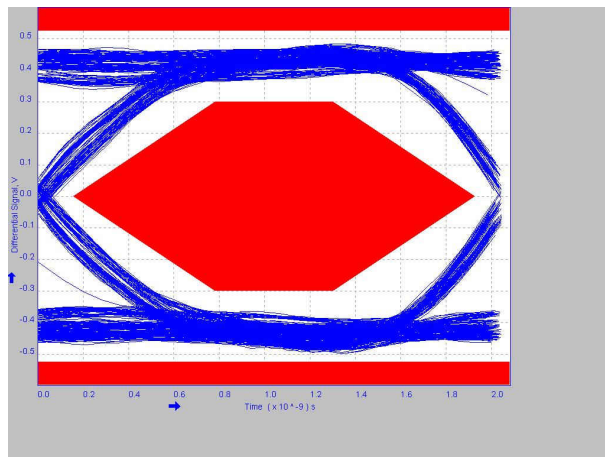


图 8-5. 2 Meter Pre-Channel With TUSB216  
BOOST=0 RX\_SEN=HIGH

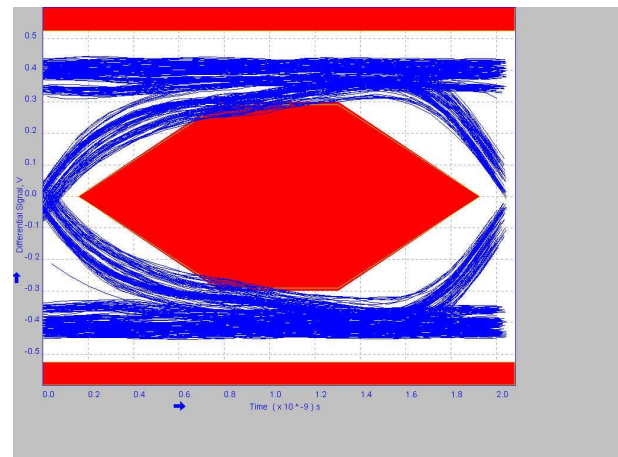


图 8-6. 3 Meter Pre-Channel Without TUSB216

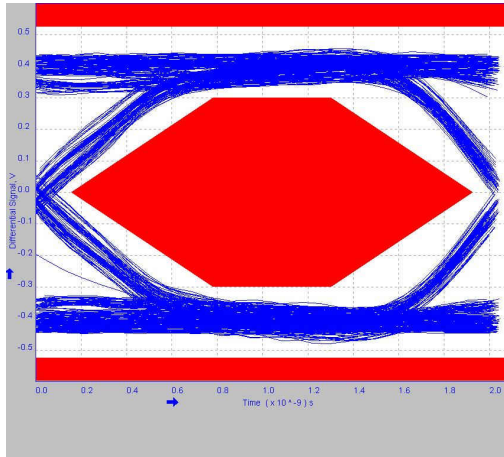


图 8-7. 3 Meter Pre-Channel With TUSB2161  
BOOST=0 RX\_SEN=HIGH

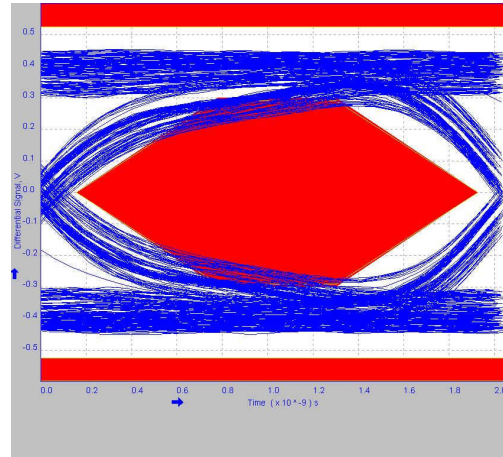


图 8-8. 5 Meter Without TUSB2161

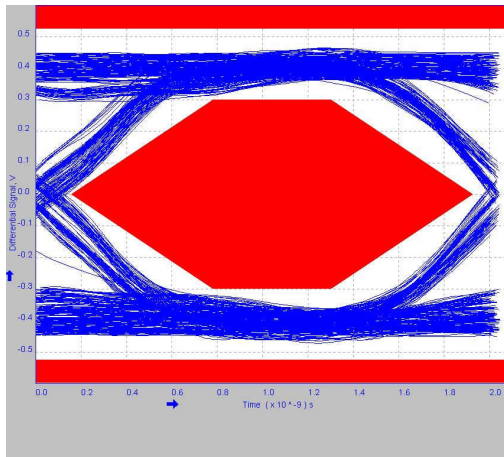


图 8-9. 5 Meter Pre-Channel With TUSB2161  
BOOST=1 RX\_SEN=MED

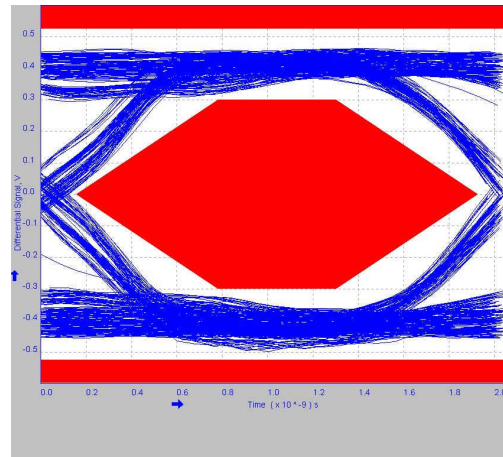


图 8-10. 5 Meter Pre-Channel With TUSB2161  
BOOST=2 RX\_SEN=MED

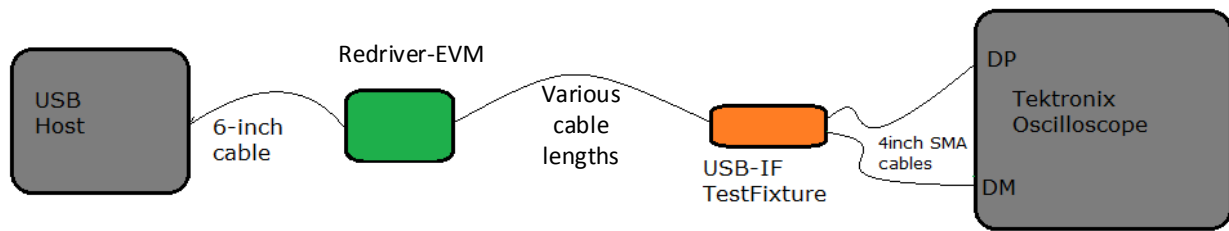


图 8-11. Near End Eye Measurement Set-Up With Post-Channel Cable

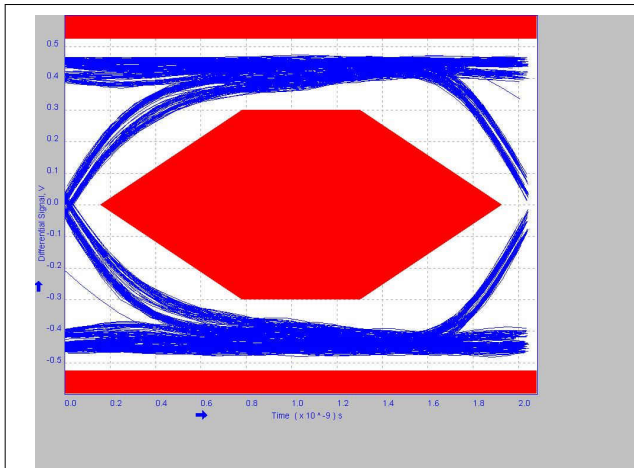


图 8-12. 6 Inches Post Channel Without TUSB216I

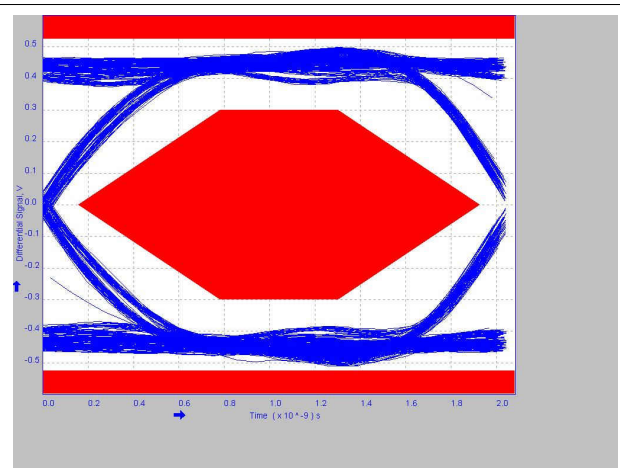


图 8-13. 6 Inches Post-Channel With TUSB216I  
BOOST=0 RX\_SEN=HIGH

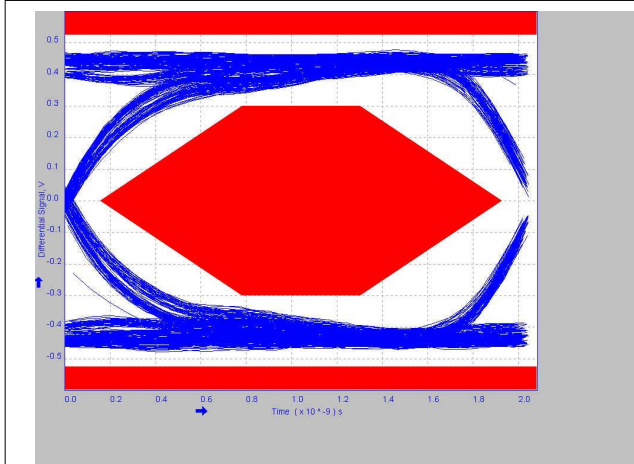


图 8-14. 1 Meter Post-Channel Without TUSB216I

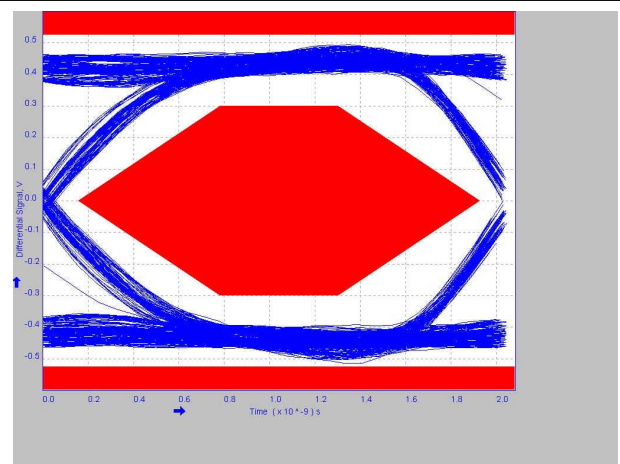


图 8-15. 1 Meter Post-Channel With TUSB216I  
BOOST=0 RX\_SEN=MED

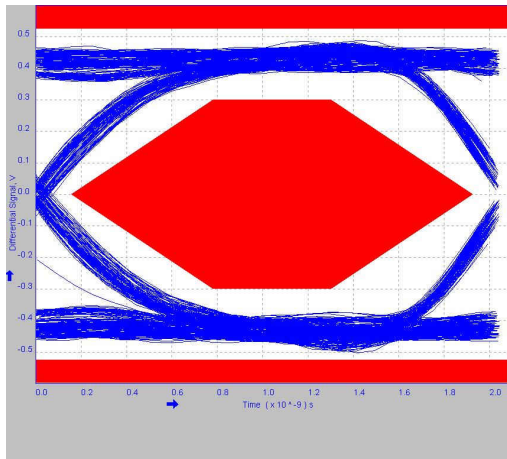


图 8-16. 1 Meter Post-Channel With TUSB216  
BOOST=0 RX\_SEN=HIGH

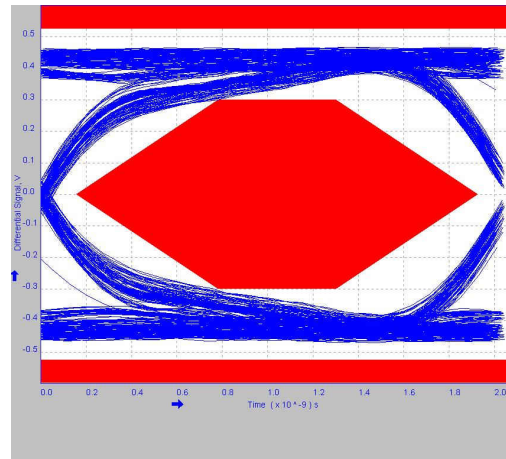


图 8-17. 2 Meter Post-Channel Without TUSB216

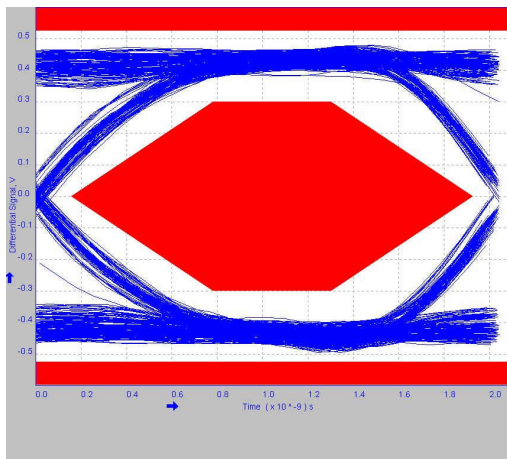


图 8-18. 2 Meter Post-Channel With TUSB216  
BOOST=1 RX\_SEN=MED

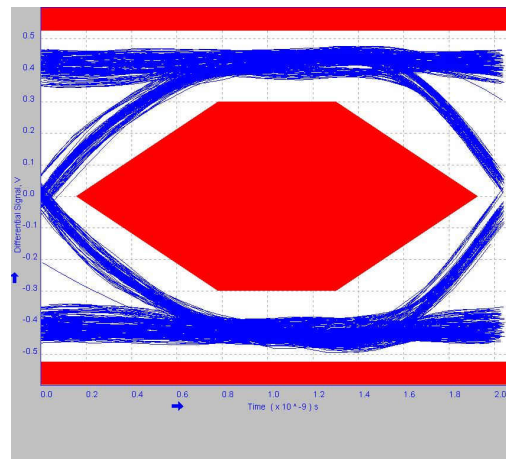


图 8-19. 2 Meter Post-Channel With TUSB216  
BOOST=1 RX\_SEN=HIGH

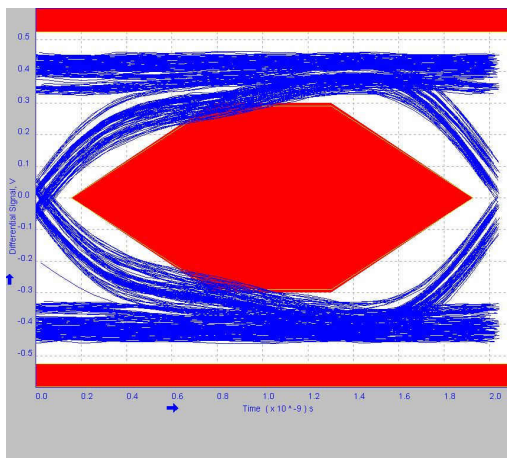


图 8-20. 4 Meter Post-Channel Without TUSB216

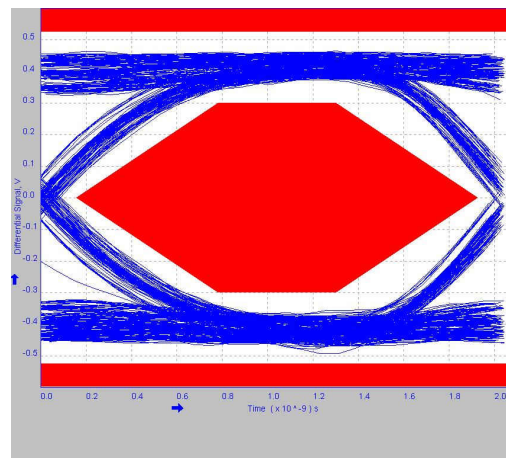


图 8-21. 4 Meter Post-Channel With TUSB216  
BOOST=2 RX\_SEN=MED



## 9 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to minimum recommended supply voltage or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to  $V_{CC}$ ). With a typical internal pullup resistance of  $500\text{ k}\Omega$ , the recommended minimum external capacitance is calculated as:

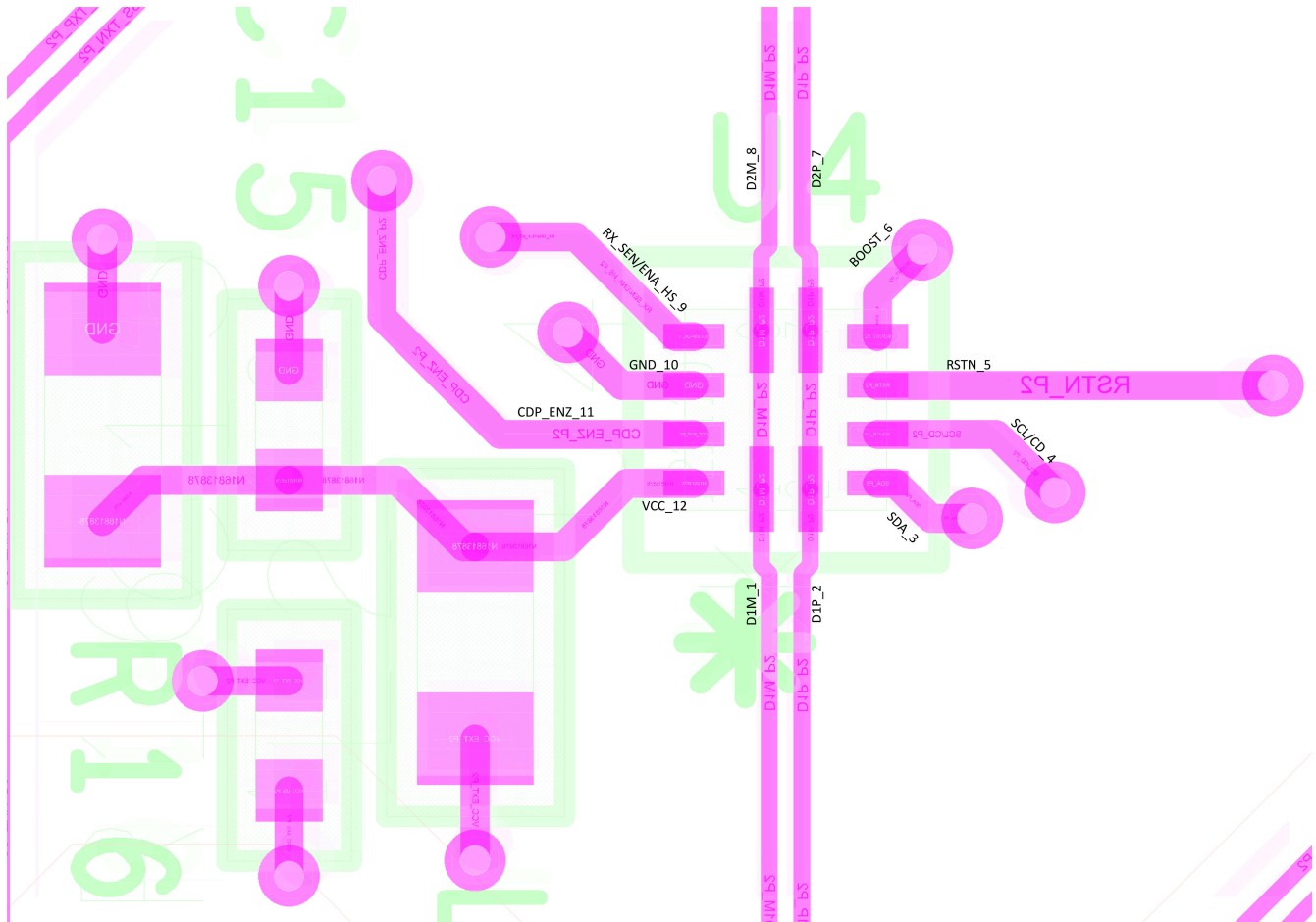
$$[\text{Ramp Time} \times 5] \div [500\text{ k}\Omega] \tag{1}$$

## 10 Layout

### 10.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90 Ω differential routing underneath the device.

### 10.2 Layout Example



**10-1. Layout Example**

## 11 Device and Documentation Support

### 11.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 11.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB2161RWBR	ACTIVE	X2QFN	RWB	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6I	<a href="#">Samples</a>
TUSB2161RWB	ACTIVE	X2QFN	RWB	12	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

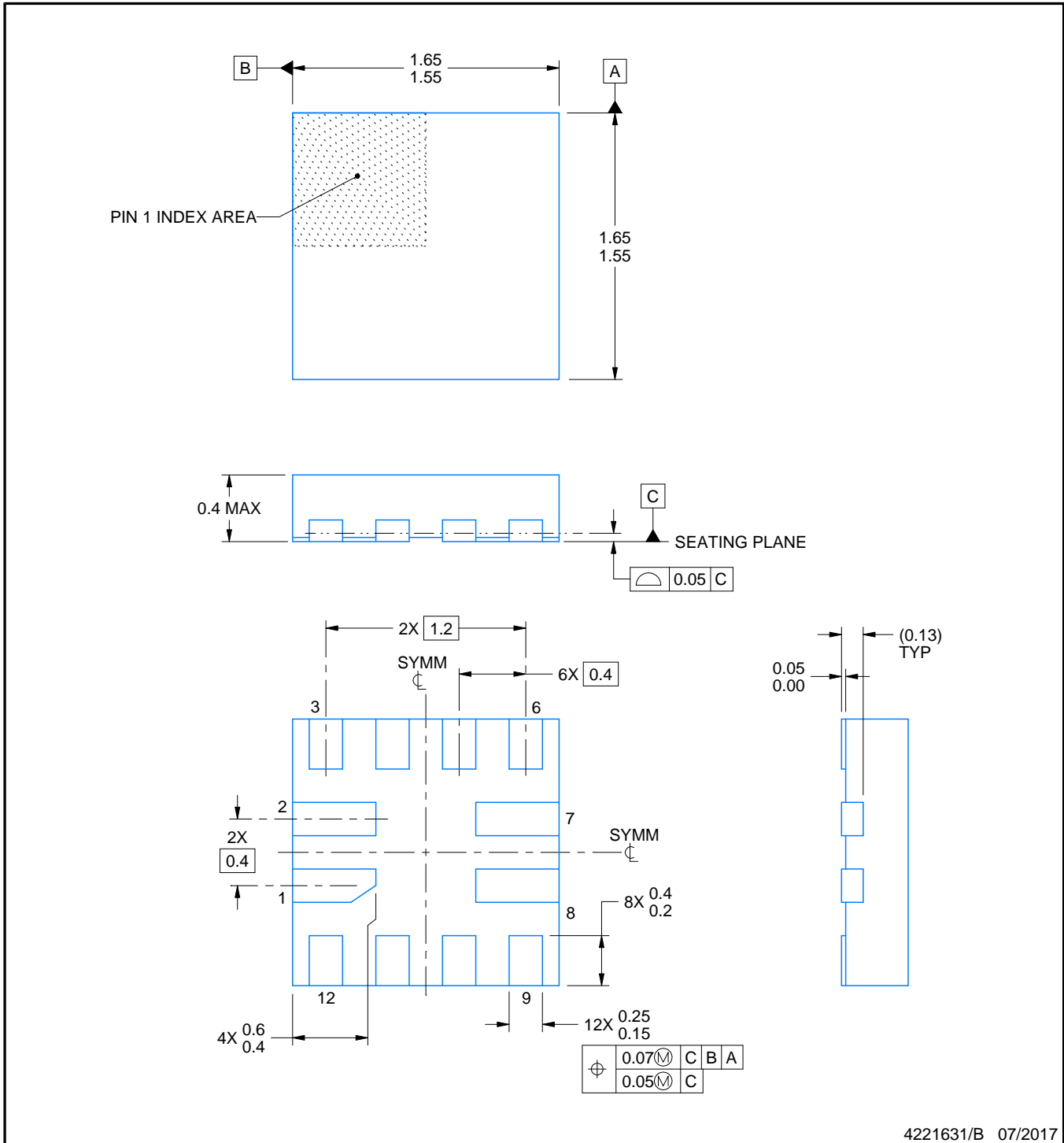
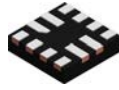
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.





4221631/B 07/2017

NOTES:

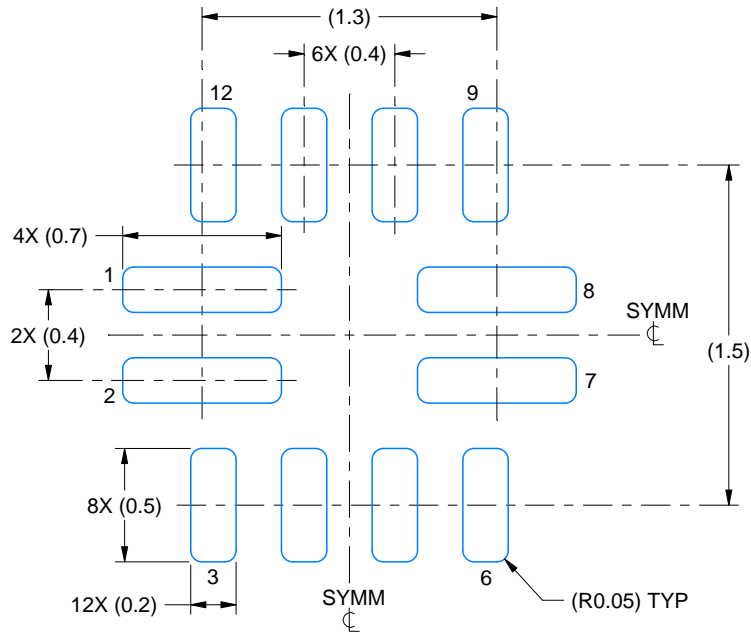
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

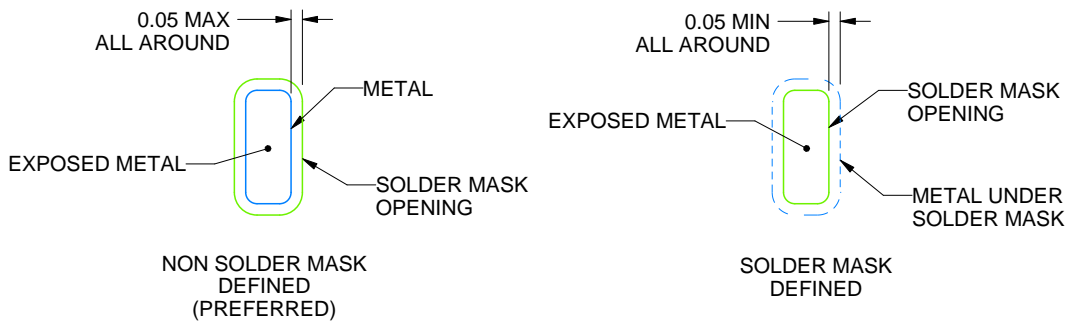
RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDER MASK DETAILS

4221631/B 07/2017

NOTES: (continued)

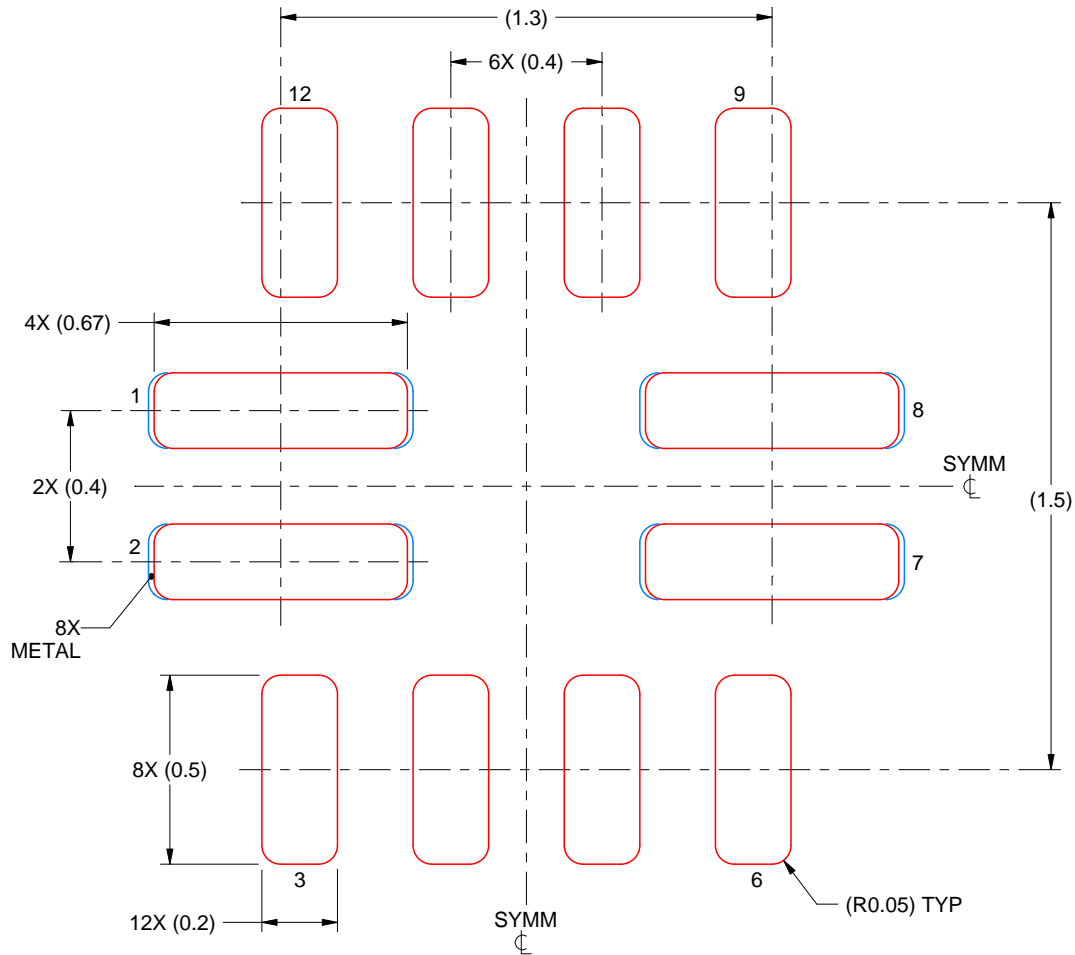
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RWB0012A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8  
96% PRINTED SOLDER COVERAGE BY AREA  
SCALE:50X

4221631/B 07/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (<https://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 或 [ti.com.cn](https://www.ti.com.cn) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

Copyright © 2021 德州仪器半导体技术（上海）有限公司