TPS61288 18V、15A 全集成同步升压转换器

1 特性

- 具有 HotRod™ Lite 选项的 2.5mm × 3.0mm QFN 封装
  - TPS61288 HotRod
  - TPS61288L HotRod Lite
  - 建议使用 TPS61288L 进行热性能改进
- 宽输入电压和输出电压范围
  - V_{IN}：2.0 V 至 18 V
  - 启动时的最小输入电压为 2.4V
  - V_{OUT}：4.5V 至 18V
- 较高的效率和功率容量
  - 开关电流峰值限制：15A
  - 两个 6.5mΩ (LS)/8.5mΩ (HS) MOSFET
  - 开关频率：500kHz
  - 效率高达 94.7%（V_{IN} = 3.6V、V_{OUT} = 13V 且 I_{OUT} = 2A 时）
  - 效率高达 96.9%（V_{IN} = 7.2V、V_{OUT} = 16V 且 I_{OUT} = 2.5A 时）
- 延长系统运行时间
  - VOUT 引脚静态电流典型值为 110μA
  - 关断期间，VIN 引脚的电流最大值为 2.1μA
  - 在轻负载和低占空比下平滑导通时间/关断时间 (SOO) 调制，并且 PFM 和 PWM 之间没有直流失调电压
- 丰富的保护特性
  - 19 V 输出过压保护
  - 逐周期过流保护
  - 热关断

2 应用

- Bluetooth™ 扬声器
- LCD 显示屏的电源驱动器
- USB Type-C 电力输送

3 说明

TPS61288 是一款高功率密度的全集成同步升压转换器，配有一个 6.5mΩ 功率开关和一个 8.5mΩ 整流器开关，可为便携式系统提供高效的小尺寸解决方案。TPS61288 具有 2V（2.4V 上升）至 18V 的宽输入电压范围，可支持由单芯或两芯锂电池供电的应用。该器件具备 15A 开关电流能力，并且能够提供高达 18V 的输出电压。

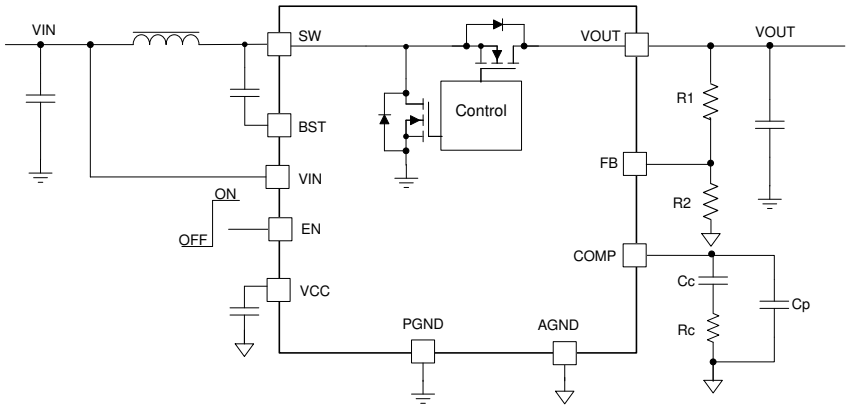
TPS61288 使用具有 SOO 调制的峰值电流控制拓扑来调节输出电压。在中等到重负载条件下，该器件以脉宽调制 (PWM) 模式工作。在轻负载和低占空比条件下，它会自动在脉冲频率调制 (PFM) 模式下运行。SOO 调制可在宽负载/VIN 范围内实现精确调节，同时保持高效率和低输出纹波。PWM 模式下的开关频率为 500kHz。TPS61288 提供 19V 输出过压保护、逐周期过流保护和热关断保护。

TPS61288 采用 2.5mm x 3.0mm QFN 封装。

器件信息

器件型号	封装[1]	封装尺寸（标称值）
TPS61288	四方扁平无引线 (QFN) (11)	2.5mm × 3.0mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用电路

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (December 2021) to Revision C (May 2022)	Page
• 添加了 HotRod Lite 选项	1

Changes from Revision A (December 2020) to Revision B (December 2021)	Page
• 将文档状态从“预告信息”更改为“量产数据”	1

5 Device Comparison

DEVICE NAME	PACKAGE
TPS61288	HotRod
TPS61288L	HotRod Lite

6 Pin Configuration and Functions

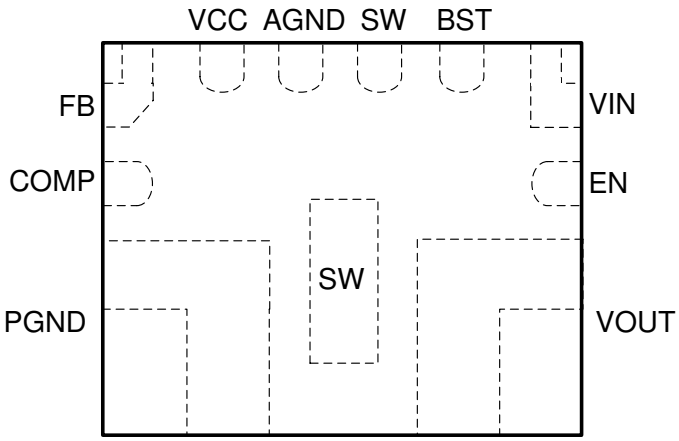


图 6-1. 11-Pin RQQ VQFN Package (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
FB	1	I	Voltage feedback. Connect to the center tape of a resistor divider to program the output voltage.
COMP	2	O	Output of the internal error amplifier, the loop compensation network should be connected between this pin and the AGND pin.
PGND	3	PWR	Power ground of the IC. It is connected to the source of the low-side MOSFET.
SW	4,9	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.
VOUT	5	PWR	Boost converter output
EN	6	I	Enable logic input. Logic high level enables the device. Logic low level disables the device and turns it into shutdown mode.
VIN	7	I	IC power supply input
BST	8	O	Power supply for high-side MOSFET gate driver. A ceramic capacitor of 0.1 µF must be connected between this pin and the SW pin.
AGND	10	-	Signal ground of the IC
VCC	11	O	Output of the internal regulator. A ceramic capacitor of more than 1.0 µF is required between this pin and ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	BST	–0.3	SW+6	V
Voltage	VIN, VOUT, SW	–0.3	20	V
Voltage	Other pins	–0.3	6	V
T_J	Operating Junction Temperature	-40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.0		18	V
V_{OUT}	Output voltage range	4.5		18	V
L	Effective inductance range	0.8		5.6	µH
C_{IN}	Effective input capacitance range	1	10		µF
C_{OUT}	Effective output capacitance range	10		1000	µF
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS61288 RQQ (VQFN) - 11 PINS EVM(2)	TPS61288 RQQ (VQFN) - 11 PINS Standard	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.6	71.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	n/a	n/a	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	n/a	n/a	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	2.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.4	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured on TPS61288EVM, 4-layer, 2oz copper PCB.

7.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 2.5 V to 9 V and V_{OUT} = 16 V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{UVLO}	Input voltage under voltage lockout (UVLO) threshold	VIN rising		2.3	2.4	V
	Input voltage under voltage lockout (UVLO) threshold	VIN falling, V_{OUT} > 3 V	1.8	1.9	2	V
	under voltage lock out hysteresis	V_{UVLO} rising - V_{UVLO} falling		400		mV
V_{CC}	Vcc regulated votlage	I_{CC} = 5 mA, V_{IN} = 9 V		4.8		V
V_{CC_UVLO}	Vcc falling threshold	V_{CC} falling	1.9	2		V
I_{Q_IN}	Quiescent current into VIN pin	EN = High, No switching, 2.4 V < V_{IN} < 16 V, V_{OUT} > 1.1 V_{IN}, -40°C ⩽ T_J ⩽ 85 °C		3	10	uA
I_{Q_OUT}	Quiescent current into VOUT pin	EN = High, No switching, 2.4 V < V_{IN} < 16 V, V_{OUT} > 1.1 V_{IN}, -40 °C ⩽ T_J ⩽ 85 °C		110	165	uA
I_{SD}	Shutdown current into VIN pin	EN = Low, No switching, 2.4 V < V_{IN} < 18 V, -40 °C ⩽ T_J ⩽ 85 °C			2.1	uA
I_{SD_SW}	Reverse leakage current into SW	EN = Low, No switching, V_{SW} = 0V, 4.5 V < V_{OUT} < 18 V, -40 °C ⩽ T_J ⩽ 85°C			1	uA
OUTPUT						
V_{REF}	Feedback regulation reference voltage	PWM Operation	0.588	0.6	0.612	V
I_{FB}	Feedback input bias current				20	nA
V_{OVP}	Over Voltage Protection	Rising threshold	18.3	19	19.5	V
V_{OVP_HYS}	Over Voltage Protection Hysteresis			600		mV
POWER SWITCH						
$R_{DS(on)}$	High-side FET on resistance	V_{CC} = 5 V		8.5		mΩ
$R_{DS(on)}$	Low-side FET on resistance	V_{CC} = 5 V		6.5		mΩ
CURRENT LIMIT						
I_{LIM}	Switching Peak Current Limit	V_{IN} = 7.2 V, V_{OUT} = 16 V, L = 2.2 uH, -20 °C ⩽ T_J ⩽ 125 °C	12	15	17.1	A
LOGIC INTERFACE						
V_{IH}	EN High-level input voltage				1.2	V
V_{IL}	EN Low-level input voltage		0.4			V
V_{HYS}	Hysteresis of the control logic		50			mV
R_{EN}	Pull down resistor for control pin			850	1100	kΩ
ERROR AMPLIFIER						
V_{COMP_H}	COMP output high voltage	V_{FB} = V_{REF} - 200 mV		1.88		V
V_{COMP_L}	COMP output low voltage	V_{FB} = V_{REF} + 200 mV		0.55		V
Gm	Error amplifier trans conductance			180		μS
K_{COMP}	Power stage trans-conductance(inductor peak current / comp voltage)			13.5		A / V
I_{SINK}	Comp pin sink current	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1.5 V		20		μA
I_{SOURCE}	Comp pin source current	V_{FB} = V_{REF} + 200 mV, V_{COMP} = 1.5 V		20		μA
SWITCHING TIME						
T_{SS}	Soft start time	V_{IN} = 7.2V, V_{OUT} = 16V; L = 2.2 uH, $C_{out(eff)}$ = 50 uF		3		ms
f_{SW}	Switching frequency	V_{IN} = 7.2V, V_{OUT} = 16V; V_{IN} = 3.6V, V_{OUT} = 13V	440	500	600	kHz
t_{ON_MIN}	Minimum on-time			60	110	ns

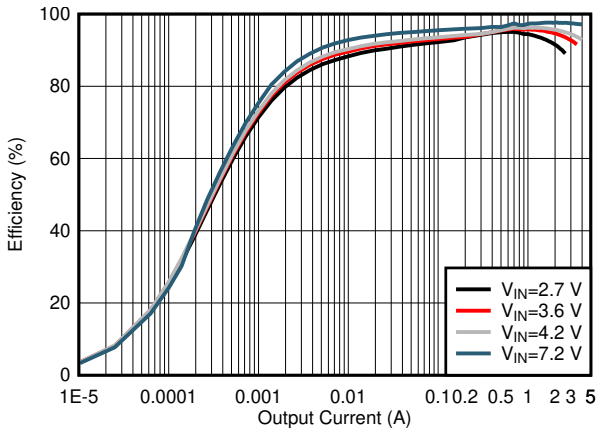
7.5 Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 2.5 V to 9 V and V_{OUT} = 16 V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION						
T_{SD}	Thermal shutdown	Junction temperature rising		160		°C
T_{SD_HYS}	Thermal shutdown hysteresis			20		°C

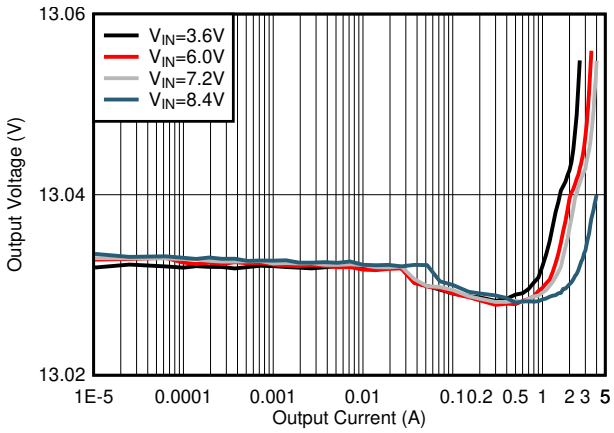
7.6 Typical Characteristics

T_A = 25°C, f_{SW} = 500 kHz, unless otherwise noted.



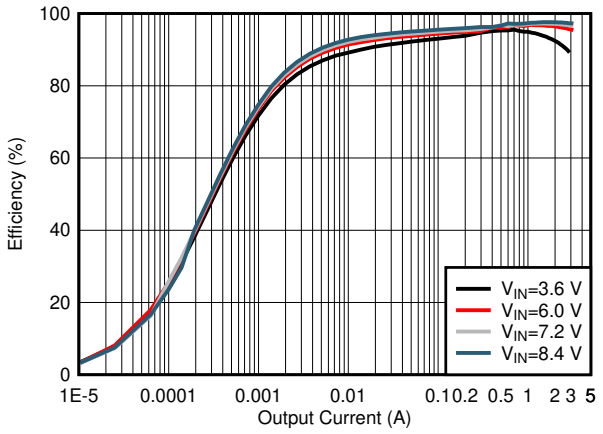
V_{IN} = 2.7 V; 3.6 V; 4.2 V; 7.2 V V_{OUT} = 13 V

图 7-1. Efficiency vs Output Current V_{OUT} = 13 V



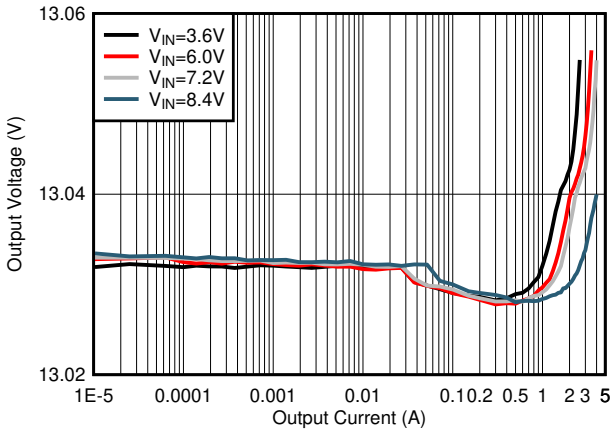
V_{IN} = 2.7 V; 3.6 V; 4.2 V; 7.2 V V_{OUT} = 13 V

图 7-2. Output Voltage vs Output Current, V_{OUT} = 13 V



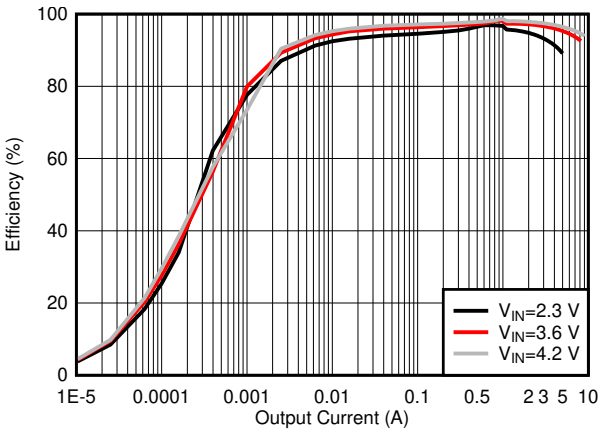
V_{IN} = 3.6 V; 6 V; 7.2 V; 8.4 V V_{OUT} = 16 V

图 7-3. Efficiency vs Output Current, V_{OUT} = 16 V



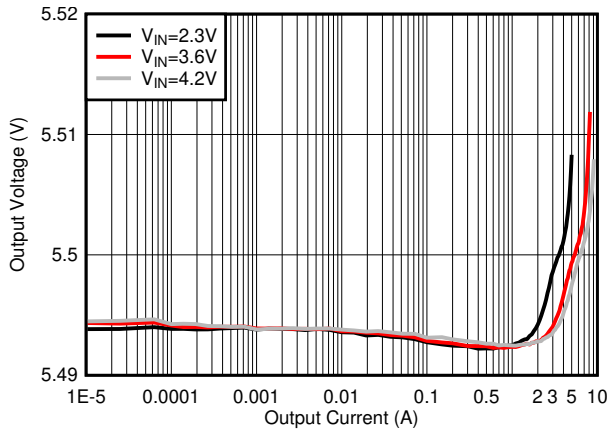
V_{IN} = 3.6 V; 6 V; 7.2 V; 8.4 V V_{OUT} = 16 V

图 7-4. Output Voltage vs Output Current, V_{OUT} = 16 V



Separate power V_{IN} and 3.3 V signal V_{IN} V_{OUT} = 5.5 V

图 7-5. Efficiency vs Output Current, V_{OUT} = 5.5 V



Separate power V_{IN} and 3.3 V signal V_{IN} V_{OUT} = 5.5 V

图 7-6. Output Voltage vs Output Current, V_{OUT} = 5.5 V

7.6 Typical Characteristics (continued)

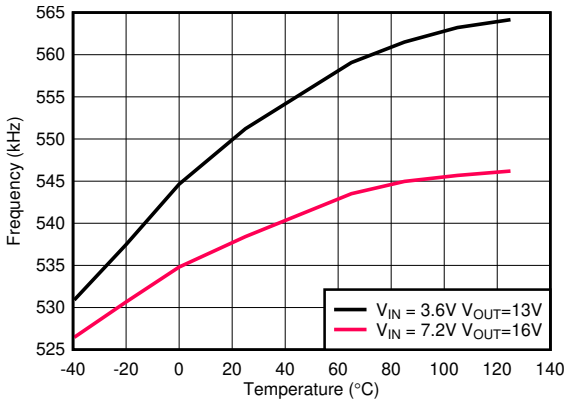


图 7-7. Switching Frequency vs Temperature

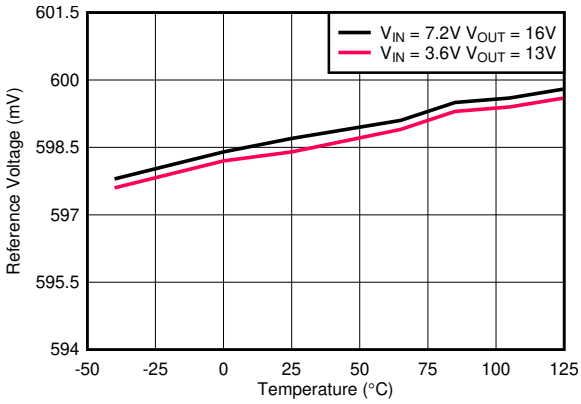
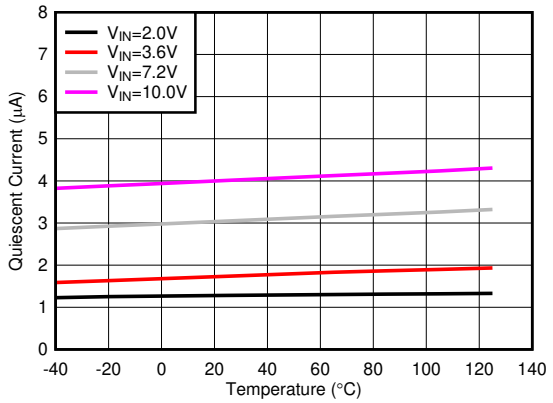
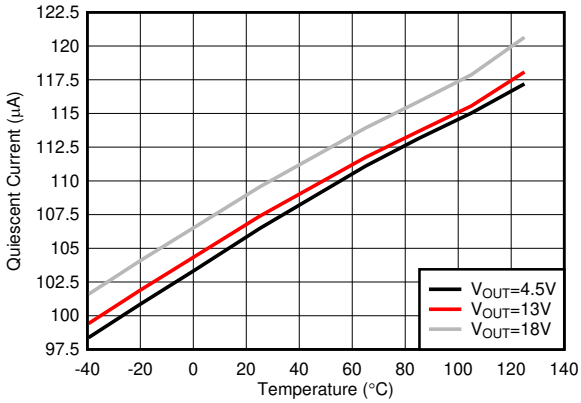


图 7-8. Reference Voltage vs Temperature



V_{IN} = 2.0 V; 3.6 V; 7.2 V; 10 V V_{OUT} = 13 V

图 7-9. Quiescent Current into VIN vs Temperature



V_{IN} = 3.6 V V_{OUT} = 4.5 V; 13 V; 18 V

图 7-10. Quiescent Current into VOUT vs Temperature

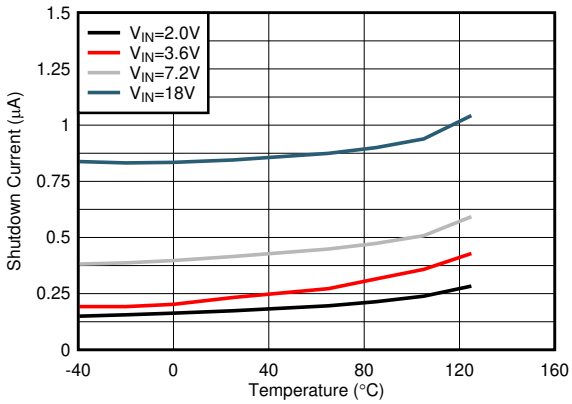


图 7-11. Shutdown Current vs Temperature

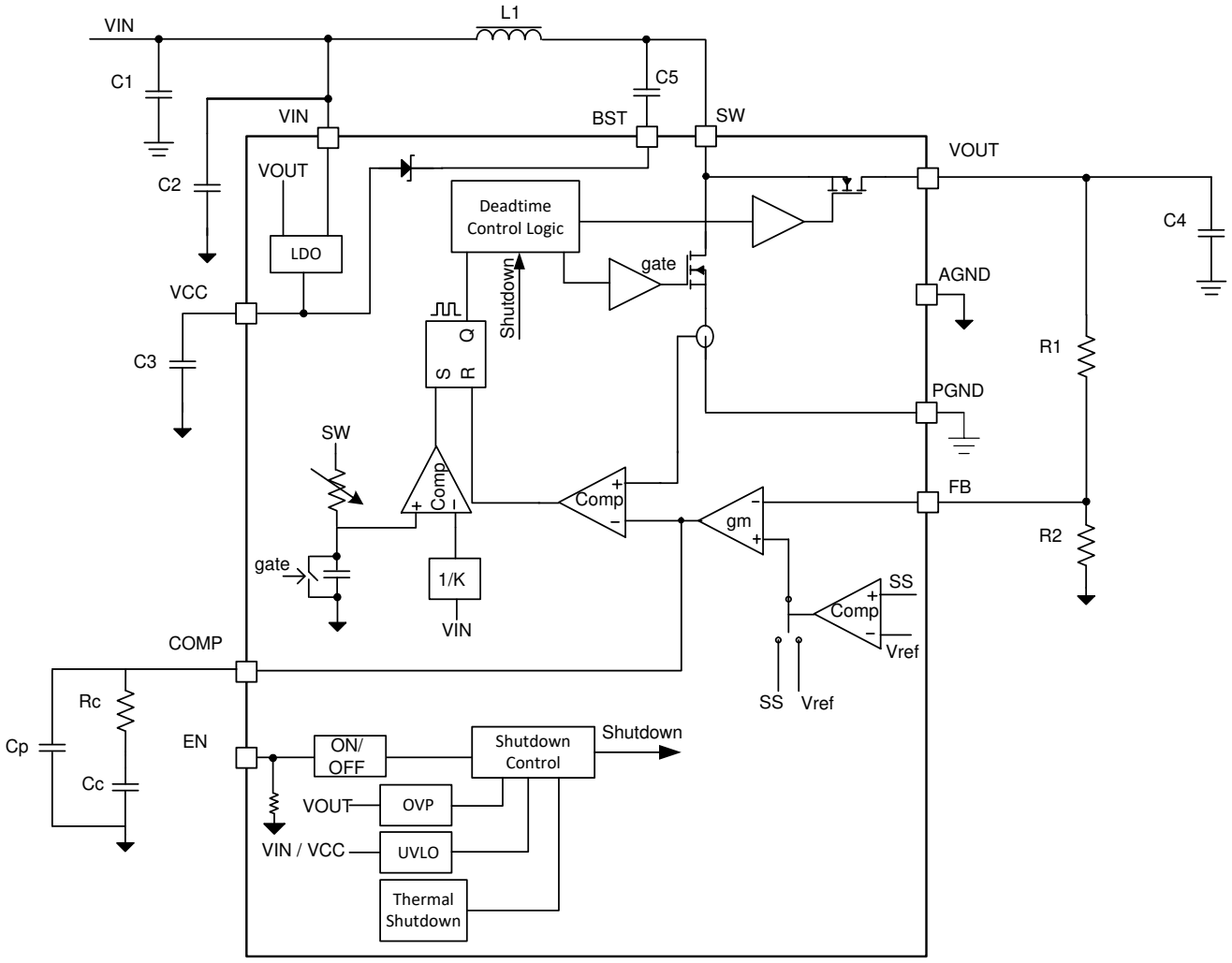
8 Detailed Description

8.1 Overview

The TPS61288 is a fully-integrated synchronous boost converter with a 6.5-mΩ power switch and a 8.5-mΩ rectifier switch to output high power from a single cell or two-cell Lithium batteries. The device is capable of providing an output voltage of 18 V and delivering up to 35-W power from a single cell Lithium battery and 45-W power from a two cells Lithium battery.

The TPS61288 employs the peak current control topology with the SOO modulation to regulate the output voltage. In the moderate-to-heavy load condition, the TPS61288 operates in the quasi-constant frequency pulse width modulation (PWM) mode. As conventional adaptive off-time converters, the device varies the off-time as a function of input and output voltage to maintain a nearly constant frequency 500 kHz. In the light load condition, the device runs in the pulse frequency modulation (PFM) mode. Off-time is modulated by the feedback loop and extended as load becoming lighter. Zero current detection in high-side N-MOSFET enables the device running in discontinuous conduction mode (DCM) to optimize light-load efficiency. The TPS61288 implements the cycle-by-cycle current limit to protect the device from overload conditions during boost switching. The typical switch peak current limit is 15 A. The TPS61288 uses external loop compensation, which provides flexibility to use different inductors and output capacitors. The peak current control scheme gives excellent transient line and load response with minimal output capacitance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable and Start-up

The TPS61288 has a soft start function to prevent high inrush current during start-up. When the EN pin is pulled high, the internal soft-start capacitor is charged with a constant current. During this time, the soft-start capacitor voltage is compared with the internal reference (0.6 V). The lower one is fed into the internal positive input of the error amplifier. The output of the error amplifier (which determines the inductor peak current value) ramps up slowly as the soft-start capacitor voltage goes up. The soft-start phase is completed after the soft-start capacitor voltage exceeds the internal reference (0.6 V). When the EN pin is pulled low, the voltage of the soft-start capacitor is discharged to ground.

8.3.2 Undervoltage Lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning at low input voltage and the battery from excessive discharge. The TPS61288 has both VIN UVLO and VCC UVLO function. It disables the device from switching when the falling voltage at the VIN pin trips the falling UVLO threshold V_{UVLO}, which is typically 1.9 V. The device starts operating when the rising voltage at the VIN pin trips the rising UVLO threshold typically 2.3 V. It also disables the device when the falling voltage at the VCC pin trips the UVLO threshold V_{CC_UVLO}, which is typically 2.1 V.

8.3.3 Switching Peak Current Limit

To avoid an accidental large peak current, the TPS61288 has an internal cycle-by-cycle current limit. The low-side switch is turned off immediately as soon as the switch current touches the typical 15-A current limit.

8.3.4 Overvoltage Protection

If the output voltage at the VOUT pin is detected above 19 V (typical value), the TPS61288 stops switching immediately until the voltage at the VOUT pin drops the hysteresis value lower than the output overvoltage protection threshold. This function prevents overvoltage on the output and secures the circuits connected to the output from excessive overvoltage.

8.3.5 Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown happens at a junction temperature of 160°C. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically 140°C, then the device starts switching again.

8.4 Device Functional Modes

8.4.1 PWM

The synchronous boost converter TPS61288 operates at a quasi-constant frequency pulse width modulation (PWM) in moderate to heavy load condition. Based on the VIN to VOUT ratio, a circuit predicts the required off-time of the switching cycle. At the beginning of each switching cycle, the low-side N-MOSFET switch, shown in 节 8.2, is turned on, and the inductor current ramps up to a peak current that is determined by the output of the internal error amplifier. After the peak current is reached, the current comparator trips, and it turns off the low-side N-MOSFET switch and the inductor current goes through the body diode of the high-side N-MOSFET in a dead-time duration. After the dead-time duration, the high-side N-MOSFET switch is turned on. Because the output voltage is higher than the input voltage, the inductor current decreases. The high-side switch is not turned off until the calculated off-time is reached. After a short dead-time duration, the low-side switch turns on again and the switching cycle is repeated.

8.4.2 PFM

The TPS61288 provides a seamless transition from PWM to PFM operation with smooth on-time/off-time (SOO) mode and enables automatic pulse-skipping mode that provides excellent efficiency over a wide load range. As load current decreasing or VIN rising, the output of the internal error amplifier decreases to lower the inductor peak current, delivering less power to the load. When the output current further decreases, the inductor current

will decrease to zero during the off-time. The converter senses inductor current and prevents negative flow by shutting off the high-side MOSFET until the beginning of the next switching cycle.

When the inductor peak current reaches to 2.6 A (typical), along with decreasing peak current, the TPS61288 extends its off-time of the switching period to deliver less energy to the output and regulate the output voltage to the target. The output of the error amplifier continuously goes down and reaches a threshold with respect to the 1.3-A (typical) peak current, the output of the error amplifier is clamped at this value and does not decrease any more.

With SOO mode, the TPS61288 keeps the output voltage equal to the setting voltage. In addition, the output voltage ripple is much smaller at light load due to low peak current. Refer to 图 8-1.

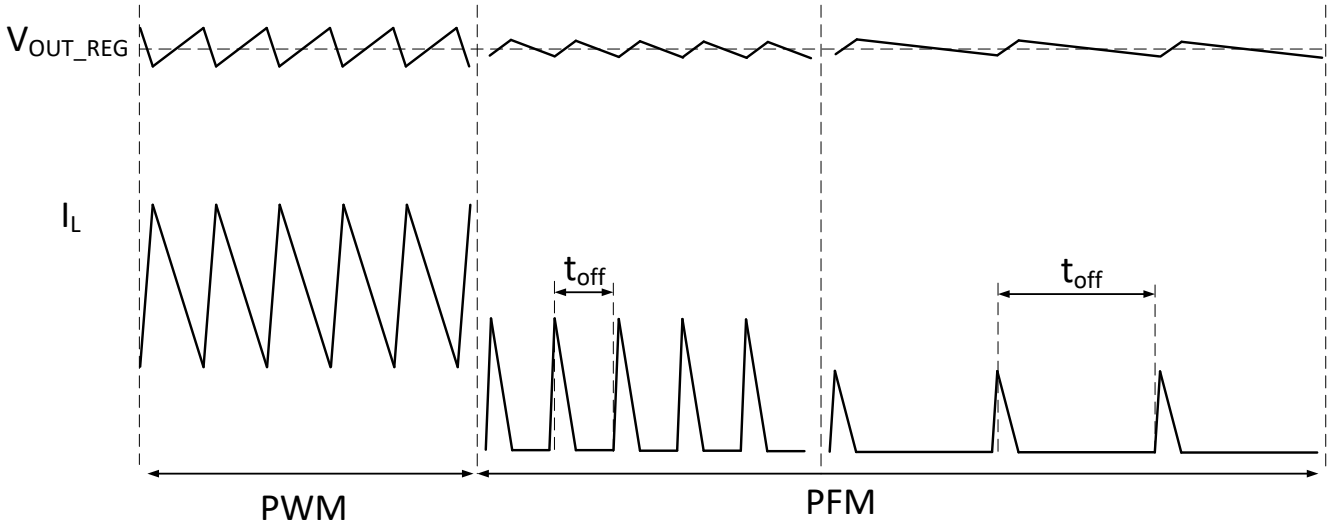


图 8-1. PFM Mode Diagram

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TPS61288 is designed for outputting voltage up to 18 V with the 15-A switch current capability. The TPS61288 operates at a quasi-constant frequency pulse-width modulation (PWM) in moderate to heavy load condition. In light load condition, the converter operates in PFM mode with single pulse. The PFM mode brings high efficiency over the entire load range. The converter uses the adaptive constant off-time peak current control scheme, which provides excellent transient line and load response with minimal output capacitance. The TPS61288 can work with different inductor and output capacitor combinations by external loop compensation.

9.2 Typical Application

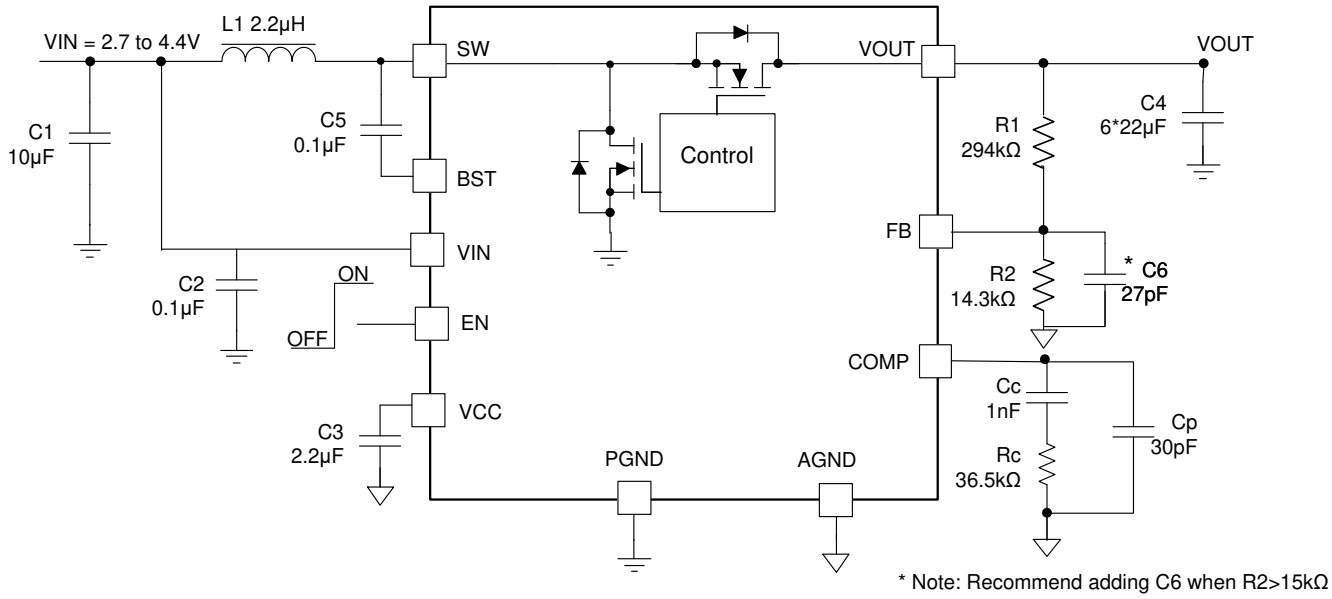


图 9-1. TPS61288 3.6-V to 13-V/2.3-A Output Converter

9.2.1 Design Requirements

表 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	2.7 to 4.4 V
Output voltage	13 V
Output voltage ripple	100 mV peak-to-peak
Output current rating	2.3 A

9.2.2 Detailed Design Procedure

9.2.2.1 Setting Output Voltage

The output voltage is set by an external resistor divider (R1, R2 in the 图 9-1 circuit diagram). For the best accuracy, R2 should be smaller than 300 kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 towards a lower value increases the immunity against noise injection. When R2 is higher than 15 kΩ, TI recommends adding a 27-pF ceramic capacitor (C6 in the 图 9-1) in parallel with the R2 for noise immunity.

The value of R1 is then calculated as:

$$R_1 = \frac{(V_{OUT} - V_{REF}) \times R_2}{V_{REF}} \quad (1)$$

9.2.2.2 Inductor Selection

Since the selection of the inductor affects the steady state of the power supply operation, transient behavior, loop stability, and boost converter efficiency, the inductor is the most important component in switching power regulator design. The three most important specifications to the performance of the inductor are the inductor value, DC resistance, and saturation current.

The TPS61288 is designed to work with inductor values between 1.0 and 4.7 µH. A 1.0-µH inductor is typically available in a smaller or lower-profile package, while a 4.7-µH inductor produces lower inductor current ripple. If the boost output current is limited by the peak current protection of the IC, using a 4.7-µH inductor can maximize the output current capability of the controller.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current, depending on how the inductor vendor defines saturation. When selecting an inductor, make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow Equation 2 to Equation 4 to calculate the peak current of the inductor. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To leave enough design margin, TI recommends using the minimum switching frequency, the inductor value with – 30% tolerance, and a low-power conversion efficiency for the calculation.

In a boost regulator, calculate the inductor DC current as in Equation 2.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (2)$$

where

- V_{OUT} is the output voltage of the boost regulator.
- I_{OUT} is the output current of the boost regulator.
- V_{IN} is the input voltage of the boost regulator.
- η is the power conversion efficiency.

Calculate the inductor current peak-to-peak ripple as in Equation 3.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}}\right) \times f_{SW}} \quad (3)$$

where

- I_{PP} is the inductor peak-to-peak ripple.
- L is the inductor value.

- f_{SW} is the switching frequency.
- V_{OUT} is the output voltage.
- V_{IN} is the input voltage.

Therefore, the peak current, I_{Lpeak}, seen by the inductor is calculated with Equation 4.

$$I_{Lpeak} = I_{DC} + \frac{I_{PP}}{2} \quad (4)$$

Set the current limit of the TPS61288 higher than the peak current, I_{Lpeak}. Then select the inductor with saturation current higher than the setting current limit.

Boost converter efficiency is dependent on the resistance of its current path, the switching loss associated with the switching MOSFETs, and the core loss of the inductor. The TPS61288 has optimized the internal switch resistance. However, the overall efficiency is affected significantly by the DC resistance (DCR) of the inductor, equivalent series resistance (ESR) at the switching frequency, and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss. Usually, a data sheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, TI would recommend an inductor with lower DCR and ESR. However, there is a tradeoff among the inductance of the inductor, DCR and ESR resistance, and its footprint. Furthermore, shielded inductors typically have higher DCR than unshielded inductors. 表 9-2 lists recommended inductors for the TPS61288. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, Cyntec's inductor, CMLE105T-2R2MS-99 is selected for its small size and low DCR.

表 9-2. Recommended Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT/HEAT RATING CURRENT (A)	SIZE MAX (L × W × H mm)	VENDOR
CMLE105T-2R2MS-99	2.2	4.5	26.0 / 19.5	10.3 x 11.5 x 5.0	Cyntec
CMLE105T-1R0MS-99	1.0	2.5	36.0 / 25.5	10.3 x 11.5 x 5.0	Cyntec
XAL1060-222ME	2.2	4.95	32.0 / 20.0	10.0 x 11.3 x 6.0	Coilcraft
104CDMCCDS-2R2MC	2.2	7.0	18.0 / 15.0	11.5 × 10.3 × 4.0	Sumida

9.2.2.3 Input Capacitor Selection

For good input voltage filtering, TI recommends low-ESR ceramic capacitors. The VIN pin is the power supply for the TPS61288. A 0.1-µF ceramic bypass capacitor is recommended as close as possible to the VIN pin of the TPS61288. The VCC pin is the output of the internal LDO. A ceramic capacitor of more than 1.0 µF is required at the VCC pin to get a stable operation of the LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasite inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100 mV. Generally, 10-µF input capacitance is sufficient for most applications.

备注

DC bias effect: High-capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore, the right capacitor value must be chosen carefully. The differences between the rated capacitor value and the effective capacitance result from package size and voltage rating in combination with material. A 10-V rated 0805 capacitor with 10 µF can have an effective capacitance of less 5 µF at an output voltage of 5 V.

9.2.2.4 Output Capacitor Selection

For small output voltage ripple, TI recommends a low-ESR output capacitor like a ceramic capacitor. Typically, three 22-μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Take care when evaluating the derating of the capacitor under DC bias. The bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the following equations to calculate the minimum required effective capacitance C_{OUT}:

$$V_{ripple\_dis} = \frac{(V_{OUT} - V_{IN\_MIN}) \times I_{OUT}}{V_{OUT} \times f_{SW} \times C_{OUT}} \quad (5)$$

$$V_{ripple\_ESR} = I_{Lpeak} \times R_{C\_ESR} \quad (6)$$

where

- V_{ripple_dis} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- R_{C_ESR} is the ESR of the output capacitors.

9.2.2.5 Loop Stability

The TPS61288 requires external compensation, which allows the loop response to be optimized for each application. The COMP pin is the output of the internal error amplifier. An external compensation network, comprised of resistor R_C, and ceramic capacitors C_C and C_P, is connected to the COMP pin.

The power stage small signal loop response of constant off-time (COT) with peak current control can be modeled by Equation 7.

$$G_{PS}(S) = K_{COMP} \times \frac{R_O \times (1-D)}{2} \times \frac{\left(1 + \frac{S}{2\pi f_{ESRZ}}\right) \times \left(1 - \frac{S}{2\pi f_{RHPZ}}\right)}{1 + \frac{S}{2\pi f_P}} \quad (7)$$

where

- D is the switching duty cycle.
- R_O is the output load resistance.
- K_{COMP} is power stage trans-conductance (inductor peak current / comp voltage), which is 13.5 A/V.

$$f_P = \frac{2}{2\pi \times R_O \times C_O} \quad (8)$$

where

- C_O is output capacitor.

$$f_{ESRZ} = \frac{1}{2\pi \times R_{ESR} \times C_O} \quad (9)$$

where

- R_{ESR} is the equivalent series resistance of the output capacitor.

$$f_{RHPZ} = \frac{R_O \times (1 - D)^2}{2\pi \times L} \tag{10}$$

The COMP pin is the output of the internal transconductance amplifier. Equation 11 shows the small signal transfer function of compensation network.

$$Gc(S) = \frac{G_{EA} \times R_{EA} \times V_{REF}}{V_{OUT}} \times \frac{\left(1 + \frac{S}{2 \times \pi \times f_{COMZ}}\right)}{\left(1 + \frac{S}{2 \times \pi \times f_{COMP1}}\right)\left(1 + \frac{S}{2 \times \pi \times f_{COMP2}}\right)} \tag{11}$$

where

- G_{EA} is the transconductance of the amplifier.
- R_{EA} is the output resistance of the amplifier.
- V_{REF} is the reference voltage at the FB pin.
- V_{OUT} is the output voltage.
- f_{COMP1}, f_{COMP2} are the frequency of the poles of the compensation network.
- f_{COMZ} is the zero's frequency of the compensation network.

The next step is to choose the loop crossover frequency, f_C. The higher frequency that the loop gain stays above zero before crossing over, the faster the loop response is. It is generally accepted that the loop gain cross over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}.

Then set the value of R_C, C_C, and C_P (in 图 9-1) by following these equations.

$$R_C = \frac{2\pi \times V_{OUT} \times C_O \times f_C}{(1\text{-}D) \times V_{REF} \times G_{EA} \times K_{COMP}} \tag{12}$$

where

- f_C is the selected crossover frequency.

The value of C_C can be set by Equation 13.

$$C_C = \frac{R_O \times C_O}{2R_C} \tag{13}$$

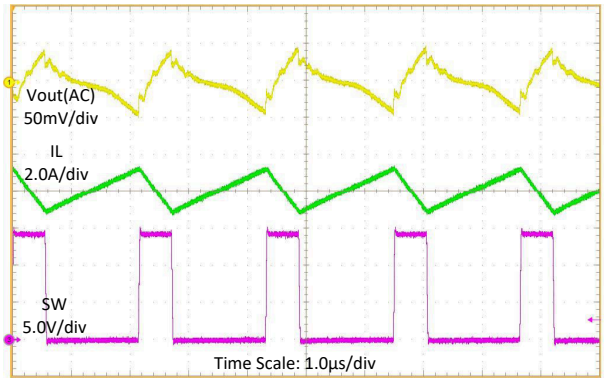
The value of C_P can be set by Equation 14.

$$C_P = \frac{R_{ESR} \times C_O}{R_C} \tag{14}$$

If the calculated value of C_P is less than 10 pF, it can be left open.

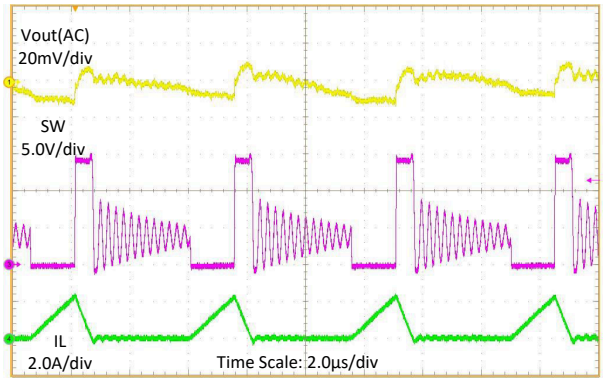
Designing the loop for greater than 45° of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

9.2.3 Application Curves



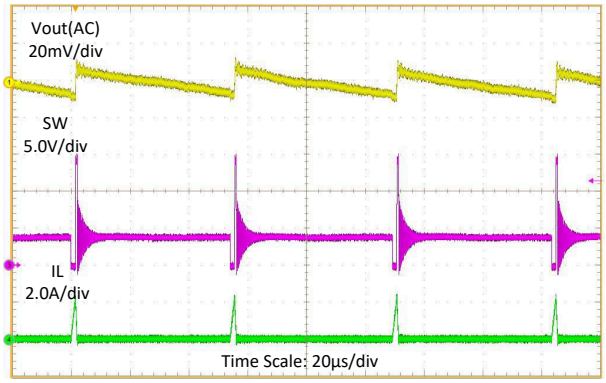
V_{IN} = 3.6 V V_{OUT} = 13 V I_{OUT} = 2.3 A

图 9-2. Switching Waveforms in CCM



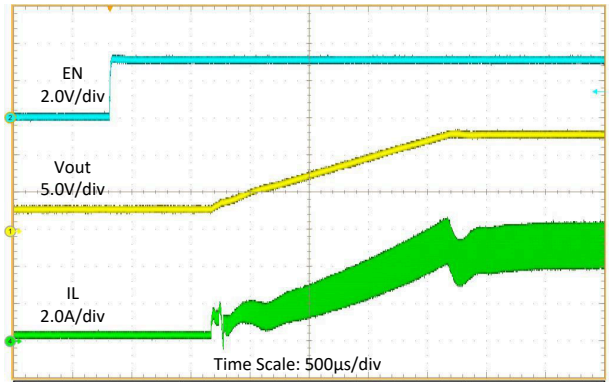
V_{IN} = 3.6 V V_{OUT} = 13 V I_{OUT} = 100 mA

图 9-3. Switching Waveforms in 100 mA load



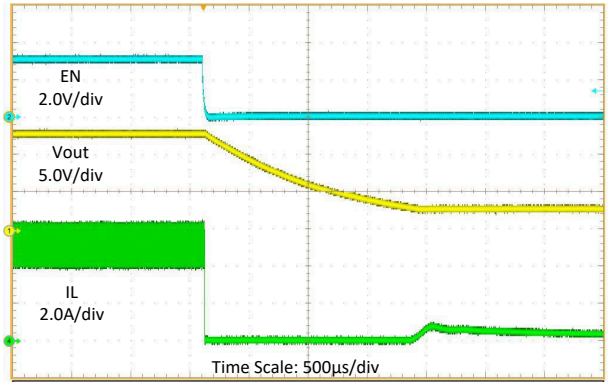
V_{IN} = 3.6 V V_{OUT} = 13 V I_{OUT} = 10 mA

图 9-4. Switching Waveforms in 10 mA load



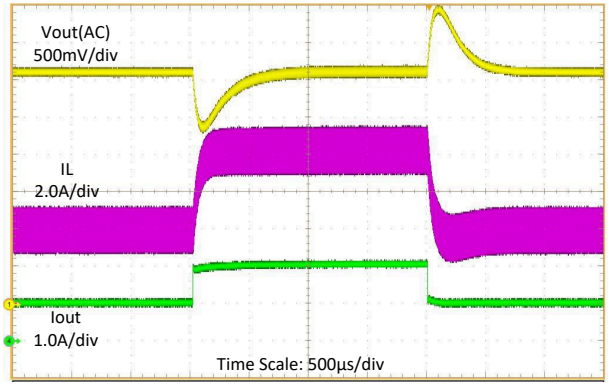
V_{IN} = 3.6 V V_{OUT} = 13 V R_{LOAD} = 10 Ω

图 9-5. Start-up Waveforms



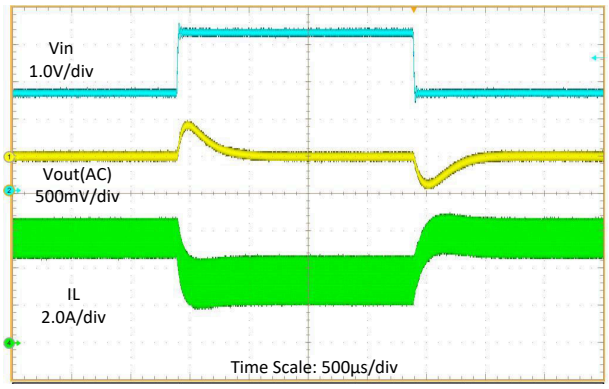
V_{IN} = 3.6 V V_{OUT} = 13 V R_{LOAD} = 10 Ω

图 9-6. Shutdown Waveforms



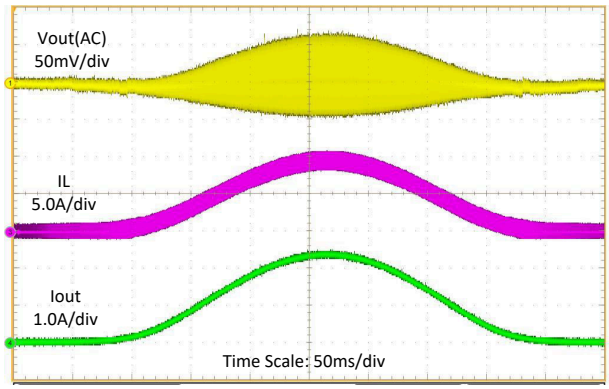
V_{IN} = 3.6 V V_{OUT} = 13 V

图 9-7. Load Transient (I_{OUT} = 1 to 2 A)



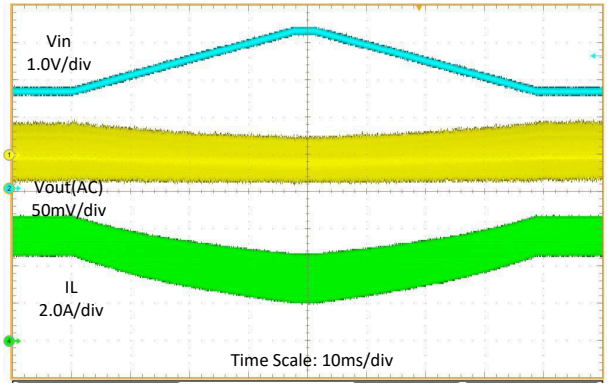
V_{OUT} = 13 V I_{OUT} = 1 A

图 9-8. Line Transient (V_{IN} = 2.7 V to 4.2 V)



V_{IN} = 3.6 V V_{OUT} = 13 V

图 9-9. Load Sweep (I_{OUT} = 0 to 2 A)



V_{OUT} = 13 V I_{OUT} = 1 A

图 9-10. Line Sweep (V_{IN} = 2.7 V to 4.2 V)

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.0 V to 18 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. A typical choice is an electrolytic or tantalum capacitor with a value of 47 μF.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator can suffer from instability and noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high-frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling.

The input capacitor needs to be close to the VIN pin and GND pin in order to reduce the I_{input} supply ripple.

The layout should also be done with well consideration of the thermal as this is a high power density device. The SW, VOUT, and PGND pins that improves the thermal capabilities of the package should be soldered with the large polygon, using thermal vias underneath the SW pin could improve thermal performance.

11.2 Layout Example

The bottom layer is a large ground plane connected to the PGND plane and AGND plane on top layer by vias.

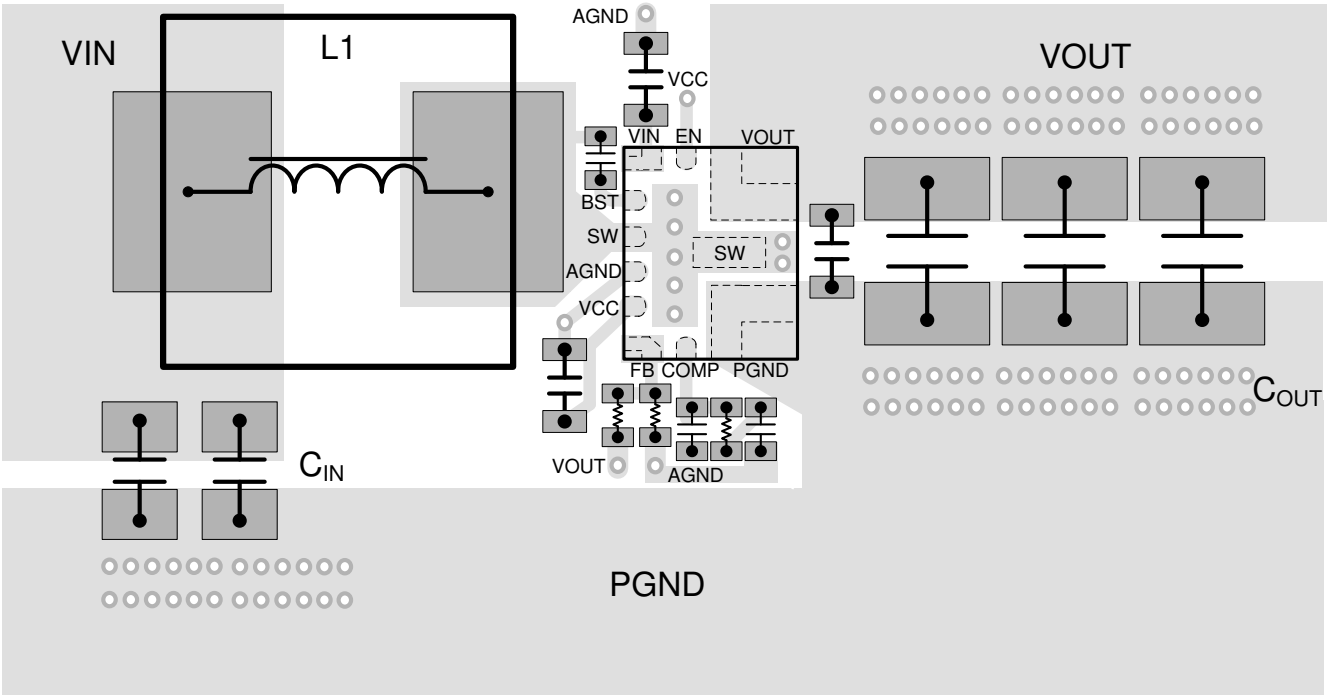


图 11-1. Layout Example

11.2.1 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 15.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{15}$$

where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in the *Thermal Information* table.

The TPS61288 comes in a thermally-enhanced VQFN package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout, and thermal pad connection. Using thick PCB copper and soldering the thermal pad to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

HotRod™ and TI E2E™ are trademarks of Texas Instruments.
Bluetooth™ is a trademark of Bluetooth SIG.
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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61288LRQQR	ACTIVE	VQFN-HR	RQQ	11	3000	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR	-40 to 125	61288L	Samples
TPS61288RQQR	ACTIVE	VQFN-HR	RQQ	11	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	61288	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

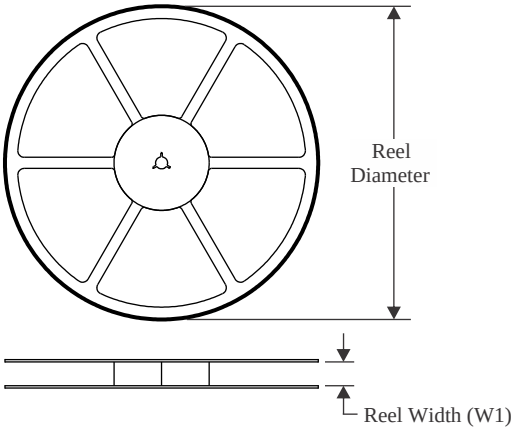
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

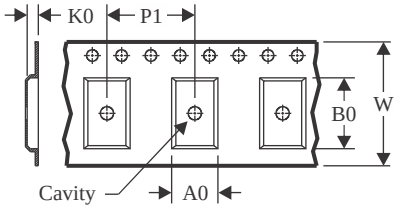
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

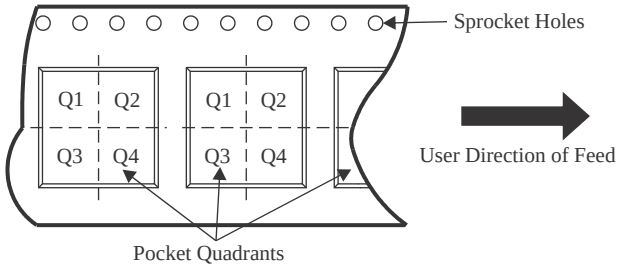


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

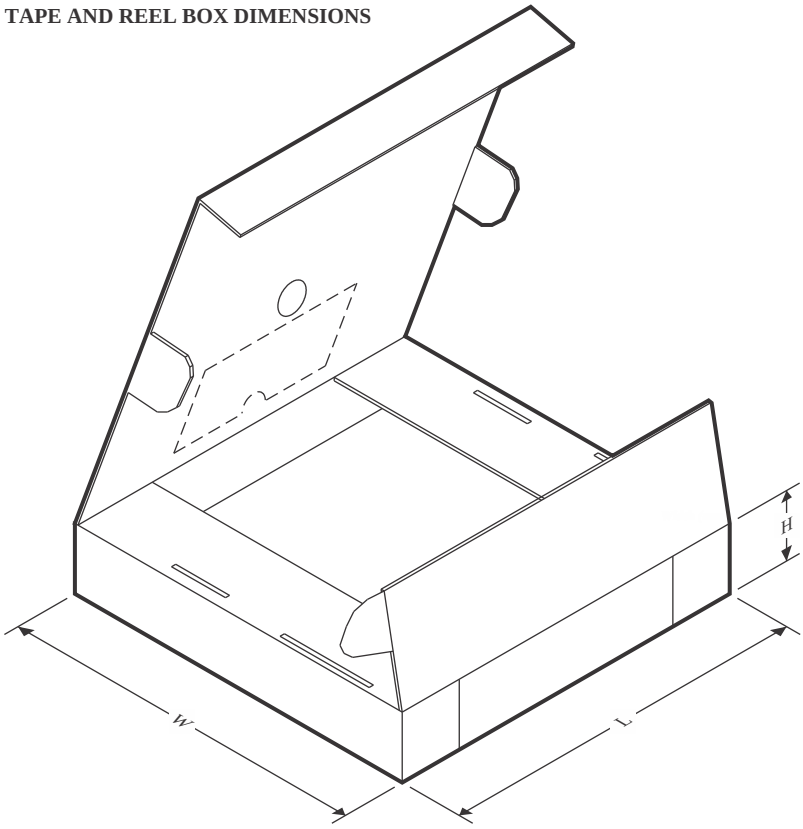
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61288RQQR	VQFN-HR	RQQ	11	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

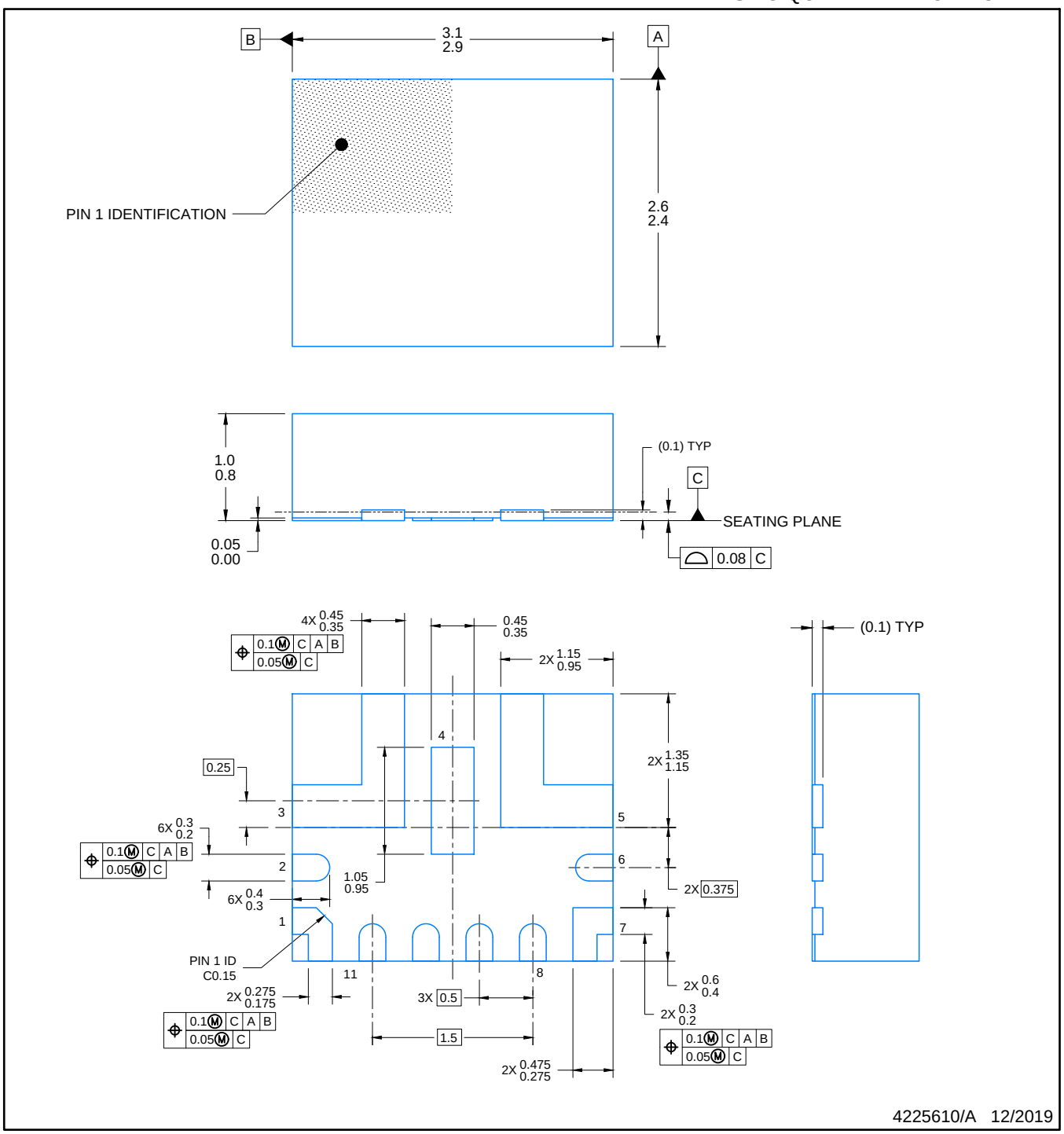
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61288RQQR	VQFN-HR	RQQ	11	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RQQ0011A

VQFN-HR - 1 mm max height

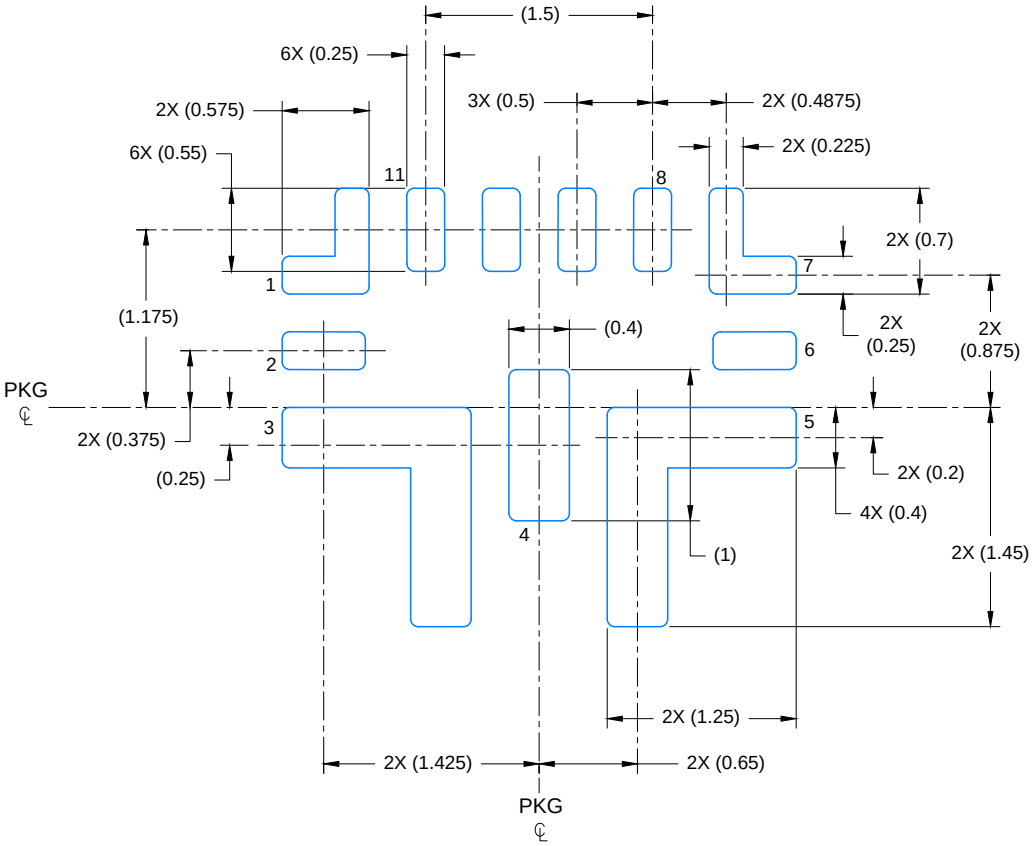
PLASTIC QUAD FLATPACK-NO LEAD



4225610/A 12/2019

NOTES:

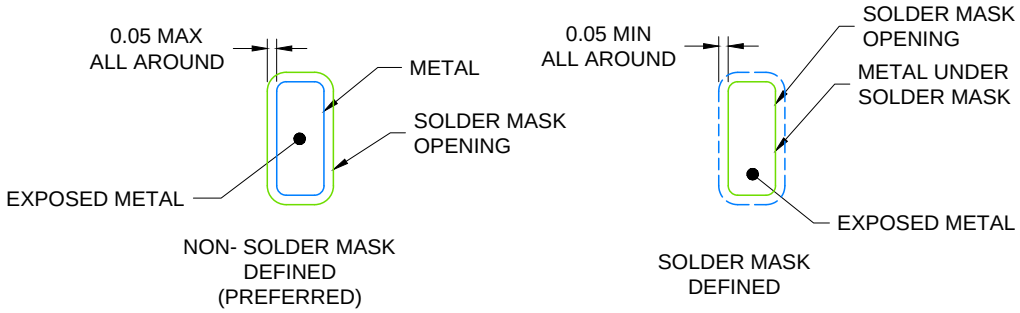
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



SOLDER MASK DETAILS

NOT TO SCALE

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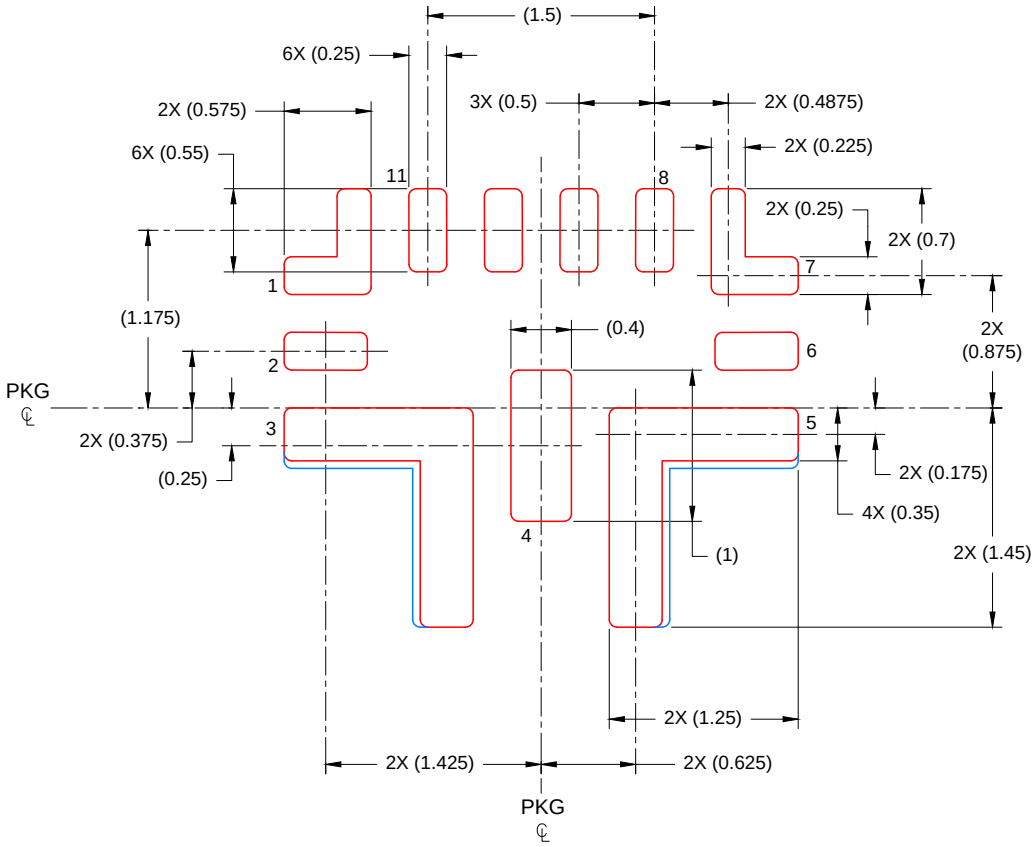
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PIN 3 & 5: 89%
SCALE: 20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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