带有电流监视器的 TPS2475x 12A 电子保险丝电路保护器

1 特性

- 2.5V 至 18V 总线运行
- 持续电流高达 12A
- 具有 3mΩ（典型值）$R_{DS(on)}$ 的集成 MOSFET
- 可编程电流限制
- 可编程 FET 安全运行区域 (SOA) 保护
- 从 10mA 至 12A 的高 I_{Limit} 精度
- 可编程故障定时器
- 用于短路保护的快速断路器
- 可编程 VOUT 转换率，欠压 (UV) 和过压 (OV)
- 电源正常和故障输出
- 模拟负载电流监视器
- 热关断
- 通过 UL 2367 认证 – 文件编号 E339631

2 应用

- 服务器
- 高电流负载开关
- 通信设备
- 插件模块
- RAID 系统
- 基站
- 风扇控制

3 说明

TPS2475x 可以为 2.5V 至 18V 应用提供高度集成的负载 保护。该器件在单个适用于小外形尺寸应用的封装内集成了一个热插拔控制器和一个 功率 MOSFET。这些器件保护电源、负载和内部 MOSFET 不受潜在损害事件的影响。在启动过程中，负载电流与 MOSFET 功率耗散被限制在用户选定值内。在启动之后，将允许超过用户选定限值的电流流动，直至设定的超时为止 — 负载与电源直接断开的极端过载情况除外。

可编程 FET SOA 保护确保内部 MOSFET 始终在其安全运行区域 (SOA) 内运行，并且负载以一个已定义的斜升速率启动。这在提升系统稳定性的同时增加了内部 MOSFET 性能。针对系统状态监视以及下游负载控制提供电源正常、故障和电流监视输出。

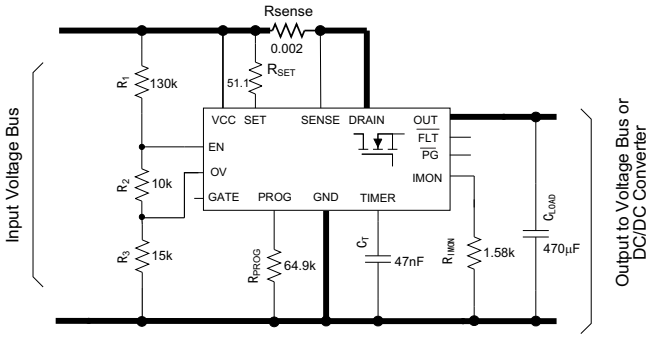
这些器件采用 36 引脚 7mm × 3.5mm QFN (RUV) 封装，额定工作结温范围为 –40°C 至 +125°C。

器件信息(1)

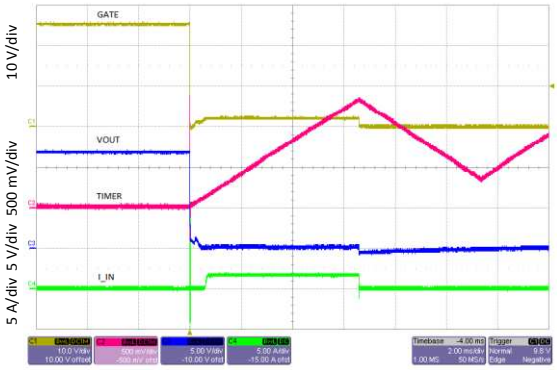
器件型号	封装	封装尺寸（标称值）
TPS24750	VQFN	7.00mm × 3.50mm
TPS24751		

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

应用原理图 (12V/10A)



瞬态输出短路响应



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (November 2016) to Revision C — **Page**

- 已添加 将“通过 UL 2367 认证 – 文件编号 E339631”添加到了*特性* 部分 ... 1

Changes from Revision A (September 2015) to Revision B — **Page**

- Added designator C1 to Figure 41 ... 26
- Updated *STEP 5. Select R_1, R_2, and R_3 for UV and OV* section ... 29

Changes from Original (October 2013) to Revision A — **Page**

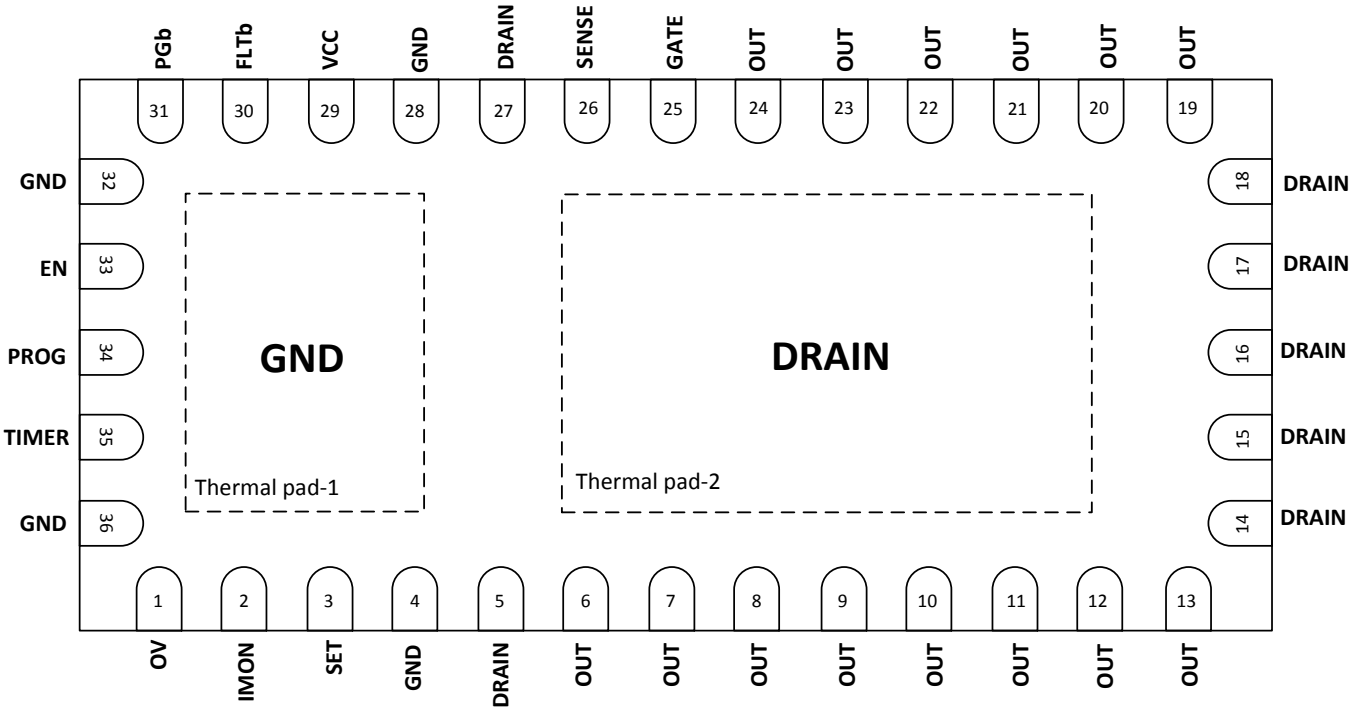
- 添加了 *ESD 额定值* 表、*详细说明*、*特性* 说明、*器件功能模式*、*应用和实施*、*电源建议*、*器件和文档支持* 以及*机械、封装和可订购信息* ... 1
- 已删除*特性*“*FET 短路检测（TPS24752，TPS24753）*” ... 1
- 已更改应用原理图。已删除 C_{VIN} 和 D1 ... 1
- Deleted devices TPS24752 and TPS24753 from the data sheet ... 3
- Deleted list item from the *Overview* section: "Internal MOSFET short detection (TPS24752/3 only)" ... 14
- Removed notes for pin 30 and 31 from the *Functional Block Diagram* ... 14
- Deleted section *Fault Detection of Internal Mosfet Short* ... 24
- Changed Figure 40. Deleted C_{VIN} and D1 ... 25
- Changed text in *STEP 3. Choose Output Voltage Rising Time, t_{ON}, and Timing Capacitor C_T* From: "maximum steady state junction temperature ($T_{JDMAX} = T_{A(MAX)} + I_{LIM}^2 \times R_{(DS)ON}$)." To: " maximum steady state junction temperature ($T_{JDMAX} = T_{A(MAX)} + I_{LIM}^2 \times R_{(DS)ON} \times R_{\theta JA}$)." ... 28
- Changed Figure 46 and Figure 47. Deleted C_{VIN} and D1 ... 32
- Added text and Figure 48 to *System Examples* ... 33
- Changed Figure 51 ... 35
- Added Figure 52 ... 36

5 Device Comparison Table

Part Number	Operating Voltage Range	Function	Fault Response	Status
TPS24750RUV	2.5 V-18 V	Integrated hot swap protector	Latch	Active
TPS24751RUV	2.5 V-18 V	Integrated hot swap protector	Auto retry	Active

6 Pin Configuration and Functions

TPS24750, TPS24751 RUV Package
36-Pin VQFN
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
DRAIN	5, 14-18, 27	I	The drain of the internal pass MOSFET. Connect to a terminal of current sense resistor in the power path
EN	33	I	Active high enable input. Logic input. Connects to resistor divider
FLTb	30	I	Active-low, open-drain output indicates overload fault timer has turned internal FET off
GATE	25	I/O	Gate driver output for the internal MOSFET
GND	4, 28, 32, 36	GND	Ground
IMON	2	O	Load current analog and current limit program point. Connect R_{IMON} to ground
OUT	6-13, 19-24	I/O	Internally connect to the source of internal pass MOSFET. Connect to output capacitors and load
OV	1	I	Overvoltage comparator input. Connects to resistor divider. GATE is pulled low when OV exceeds the threshold
Pad-1	—	—	Tied to GND
Pad-2	—	—	Tied to DRAIN
PGb	31	O	Active-low, open-drain power good indicator. Status is determined by the voltage across the MOSFET

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
PROG	34	I	Power-limiting programming pin. A resistor from this pin to GND sets the maximum power dissipation for the internal pass MOSFET
SENSE	26	I	Current sensing input for resistor shunt from VCC to SENSE. Connect to a terminal of current sense resistor
SET	3	I	Current limit programming set pin. A resistor is connected from this pin to VCC
TIMER	35	I/O	A capacitor connected from this pin to GND provides a fault timing function
VCC	29	I	Input voltage sense and power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, all voltages referred to GND (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Input voltage	DRAIN, EN, FLTb(2), GATE, OUT, PGb(2), SENSE, SET(2), VCC	–0.3	30	V
		OV	–0.3	20	
		PROG(2)	–0.3	3.6	
		[SET, SENSE] to VCC	–0.3	0.3	
		IMON, TIMER	–0.3	5	
	Sink current	FLTb, PGb		5	mA
	Source current	PROG	Internally limited		
		IMON		5	mA
T_J	Maximum junction temperature		150		°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Do not apply voltage directly to these pins.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Input voltage	OV	0	16	V
		SENSE, SET(1), VCC(2)	2.5	18	
		EN, FLTb, GATE(2), PGb, OUT(2), DRAIN(2)	0	18	
	Sink current	FLTb, PGb	0	2	mA
	Source current	IMON	0	1	mA
	Resistance	PROG	4.99	500	kΩ
	External capacitance	TIMER	1		nF
		GATE(3)		1	µF
T_J	Operating junction temperature		–40	125	°C

(1) Do not apply voltage directly to these pins.
(2) See the *Gate Clamp Diode* section for additional precaution to be taken for operating voltages >14 V.
(3) External capacitance tied to GATE must be in series with a resistor no less than 1 kΩ.

7.4 Thermal Information

THERMAL METRIC(1)		TPS2475x RUV (VQFN) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	33.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC(1)		TPS2475x RUV (VQFN) 36 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	5.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.1	°C/W

7.5 Electrical Characteristics

–40°C ≤ T_J ≤ +125°C, V_{CC} = 12 V, V_{EN} = 3 V, R_{SET} = 191 Ω, R_{IMON} = 5 kΩ, and R_{PROG} = 50 kΩ to GND. All voltages referenced to GND, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VCC						
	UVLO threshold, rising		2.20	2.32	2.45	V
	UVLO threshold, falling		2.10	2.22	2.35	V
	UVLO hysteresis(1)			0.1		V
	Supply current	Enabled — I_{OUT} + I_{VCC} + I_{SENSE}	0.5	1	1.4	mA
		Disabled(1) — EN = 0 V, I_{OUT} + I_{VCC} + I_{SENSE}		0.45		mA
OUT						
R_{ON}	On-resistance	1 A ≤ I_{OUT} ≤ 10 A at T_J = 25°C		3	3.5	mΩ
		1 A ≤ I_{OUT} ≤ 10 A at T_J = 125°C		5	6	mΩ
	Input bias current	V_{OUT} = 12 V	10	16	30	µA
	Diode forward voltage	V_{EN} = 0 V, I_{OUT} = –100 mA, V_{OUT} > V_{SENSE}		0.8	1	V
	Leakage current - DRAIN to OUT	V_{EN} = 0 V, V_{OUT} = 0 V, V_{DRAIN} = 18 V at 25°C		0	1	µA
		V_{EN} = 0 V, V_{OUT} = 0 V, V_{DRAIN} = 18 V at 125°C		2	5	µA
C_{iss}	Input capacitance	V_{GS} = 0 V, $V_{DRAIN-OUT}$ = 15 V, f = 1 MHz		2710	3250	pF
C_{oss}	Output capacitance			635	762	pF
C_{rss}	Reverse transfer capacitance			48	60	pF
Q_g	Gate charge total (4.5 V)	$V_{DRAIN-OUT}$ = 15 V, I_{OUT} = 20 A		17.5	21.5	nC
Qg(th)	Gate charge at Vth			4.1		nC
EN						
	Threshold voltage, falling		1.2	1.3	1.4	V
	Hysteresis(1)			50		mV
	Input leakage current	0 V ≤ V_{EN} ≤ 30 V	–1	0	1	µA
	Turnoff time	EN ↓ to V_{GATE} < 1 V	3	8	25	µs
	Deglitch time	EN ↑	8	14	21	µs
	Disable delay	EN ↓ to GATE ↓, C_{GATE} = 0, $t_{pff50-90}$, See Figure 28	0.1	0.4	1.8	µs
	Turnon delay	C_{OUT} = 2.2 uF, V_{EN} ↑ to V_{OUT} ↑, V_{EN}: 0 V to 3 V, V_{OUT} : 90% V_{CC}		800		µs
OV						
	Threshold voltage, rising		1.25	1.35	1.45	V
	Hysteresis(1)			60		mV
	Input leakage current	0 V ≤ V_{OV} ≤ 30 V	–1	0	1	µA
	Deglitch time	OV rising	0.5	1.2	1.5	µs
FLTb						
	Output low voltage	Sinking 2 mA		0.11	0.25	V
	Input leakage current	V_{FLTb} = 0 V, 30 V	–1	0	1	µA
PGb						
	Threshold	$V_{(SENSE - OUT)}$ rising, PGb going high	140	220	340	mV
	Hysteresis(1)	Measured $V_{(SENSE - OUT)}$ falling, PGb going low		70		mV
	Output low voltage	Sinking 2 mA		0.11	0.25	V
	Input leakage current	V_{PGb} = 0 V, 30 V	–1	0	1	µA

(1) These parameters are provided for reference only and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

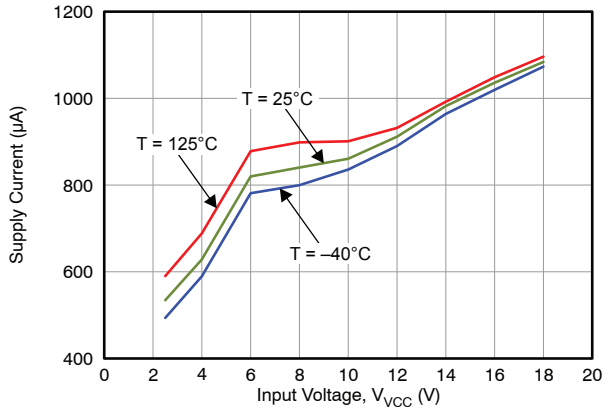
Electrical Characteristics (continued)

–40°C ≤ T_J ≤ +125°C, V_{CC} = 12 V, V_{EN} = 3 V, R_{SET} = 191 Ω, R_{IMON} = 5 kΩ, and R_{PROG} = 50 kΩ to GND. All voltages referenced to GND, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
	Delay (deglitch) time	Rising or falling edge	2	3.4	6	ms
PROG						
	Bias voltage	Sourcing 10 µA	0.65	0.675	0.7	V
	Input leakage current	V_{PROG} = 1.5 V	–0.2	0	0.2	µA
TIMER						
	Sourcing current	V_{TIMER} = 0 V	8	10	12	µA
	Sinking current	V_{TIMER} = 2 V	8	10	12	µA
		V_{EN} = 0 V, V_{TIMER} = 2 V	2	4.5	7	mA
	Upper threshold voltage		1.3	1.35	1.4	V
	Lower threshold voltage		0.33	0.35	0.37	V
	Timer activation voltage	Raise GATE until I_{TIMER} sinking, measure $V_{(GATE - VCC)}$, V_{VCC} = 12 V	5	5.8	7	V
	Retry duty cycle	During over current and short circuit conditions (TPS24751 only)		4%		
IMON						
	Circuit breaker threshold		650	675	696	mV
	Input referred offset of servo amplifier	At T_J = 25°C	–1	0	1	mV
		T_J from –40°C to +125°C	–1.5	0	1.5	mV
SET						
	Input referred offset of servo amplifier	Measure SET to SENSE	–1.5	0	1.5	mV
GATE						
	Output voltage	V_{OUT} = 12 V	23.5	25.7	28	V
	Clamp voltage	Inject 10 µA into GATE, measure $V_{(GATE - VCC)}$	12	13.9	15.5	V
	Sourcing current	V_{GATE} = 12 V	20	30	40	µA
	Sinking current	Fast turnoff, V_{GATE} = 14 V	0.4	1	1.4	A
		Sustained, V_{GATE} = 4 V to 23 V	6	11	20	mA
		In inrush current limit, V_{GATE} = 4 V to 23 V	20	30	40	µA
	Pulldown resistance	Thermal shutdown or V_{EN} = 0 V	14	20	26	kΩ
	Fast turnoff duration		8	13	18	µs
Turnon delay		V_{VCC} rising to GATE sourcing, $t_{prr50-50}$, See Figure 29		100	375	µs
SENSE						
	Input bias current	V_{SENSE} = 12 V, sinking current		30	40	µA
	Current limit threshold	V_{OUT} = 12 V	22.5	25	27.5	mV
	Power limit threshold	$V_{DRAIN–OUT}$ = 8 V, R_{PROG} = 100 kΩ		4		mV
		$V_{DRAIN–OUT}$ = 8 V, R_{PROG} = 50 kΩ	6.6	8	9.6	
		$V_{DRAIN–OUT}$ = 5.37 V, R_{PROG} = 50 kΩ	10	12	14	
		$V_{DRAIN–OUT}$ = 10.3 V, R_{PROG} = 25 kΩ	10	12.5	15	
	Fast-trip threshold		52	60	68	mV
	Fast-turnoff delay(1)	$V_{(VCC - SENSE)}$ = 80 mV, C_{GATE} = 0 pF, $t_{prf50–50}$, See Figure 30		200		ns
OTSD						
	Threshold, rising	Temperature referenced to PAD1 of the device. See(2)	130	140		°C
	Hysteresis(1)			10		°C

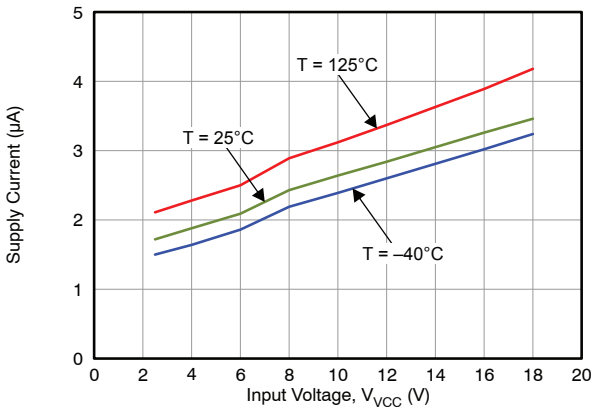
(2) The temperature difference between PAD1 and PAD2 must be minimized. See the SOA curve Figure 27 and *Power-Limited Start-Up* section for temperature limited design.

7.6 Typical Characteristics



EN = High

Figure 1. Supply Current vs Input Voltage at Normal Operation



EN = 0 V

Figure 2. Supply Current vs Input Voltage at Shutdown

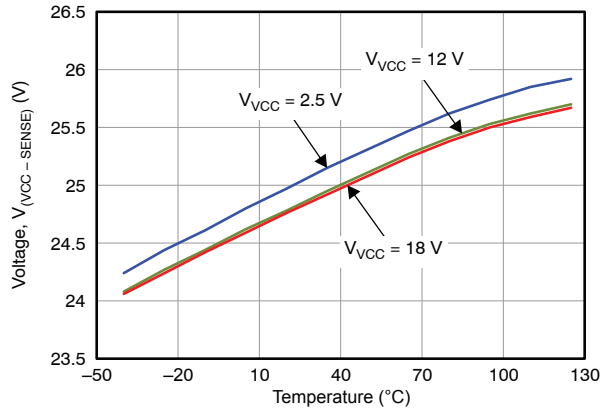


Figure 3. Voltage Across R_{SENSE} in Inrush Current Limiting vs Temperature

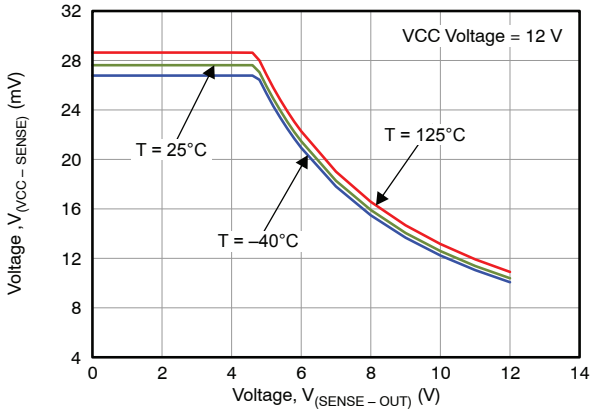


Figure 4. Voltage Across R_{SENSE} in Inrush Power Limiting vs V_{DS} of Internal FET

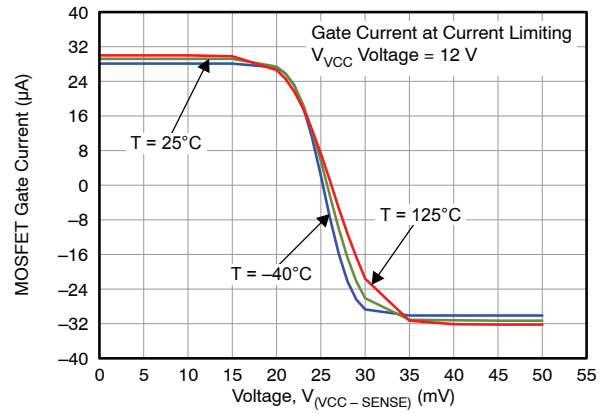
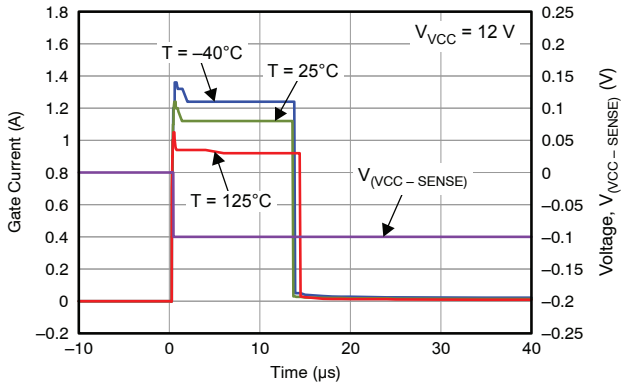


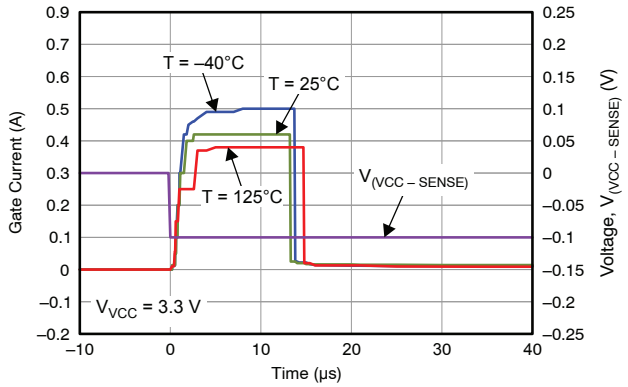
Figure 5. Internal FET Gate Current vs Voltage Across R_{SENSE} During Inrush Power Limiting



$V_{VCC} = V_{GATE} = 12$ V

Figure 6. Gate Current During Fast Trip

Typical Characteristics (continued)



$V_{VCC} = V_{GATE} = 3.3$ V

Figure 7. Gate Current During Fast Trip

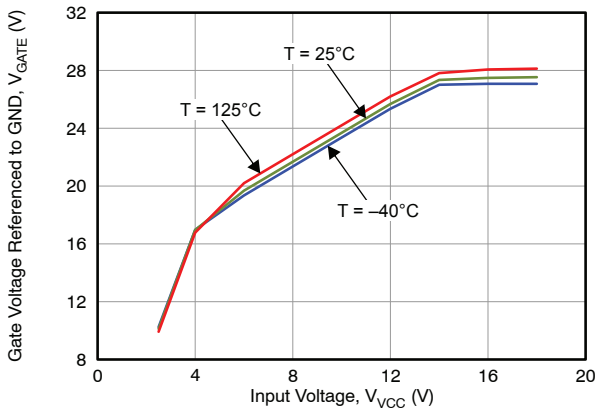


Figure 8. Gate Voltage With Zero Gate Current vs Input Voltage

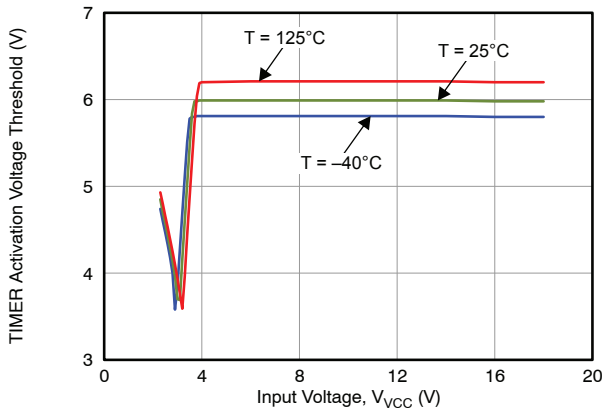


Figure 9. TIMER Activation Voltage Threshold vs Input Voltage at Various Temperatures

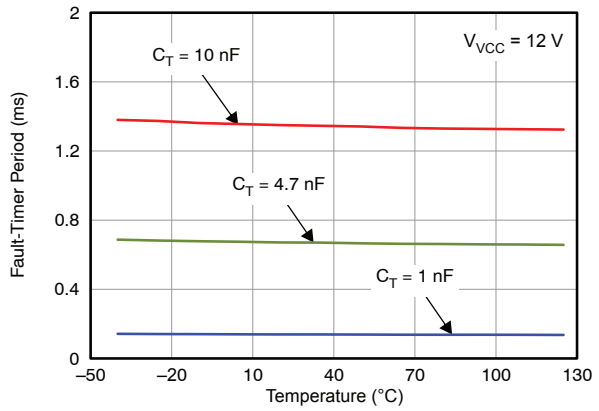


Figure 10. Fault-Timer vs Temperature with Various TIMER Capacitors

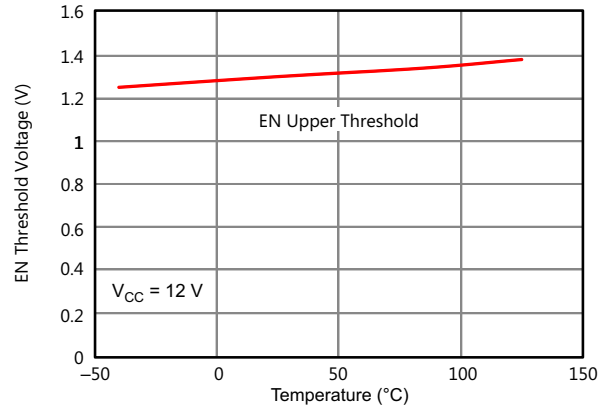


Figure 11. EN Threshold Voltage vs Temperature

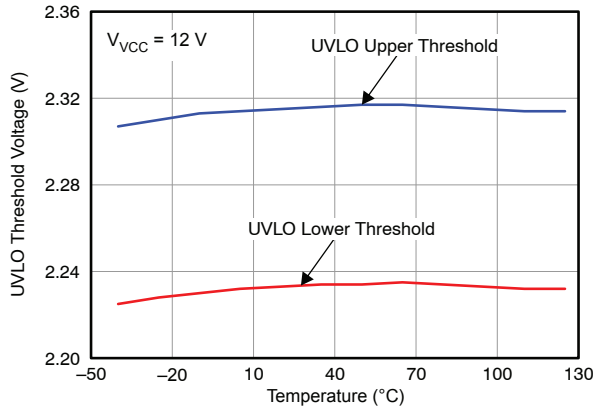


Figure 12. UVLO Threshold Voltage vs Temperature

Typical Characteristics (continued)

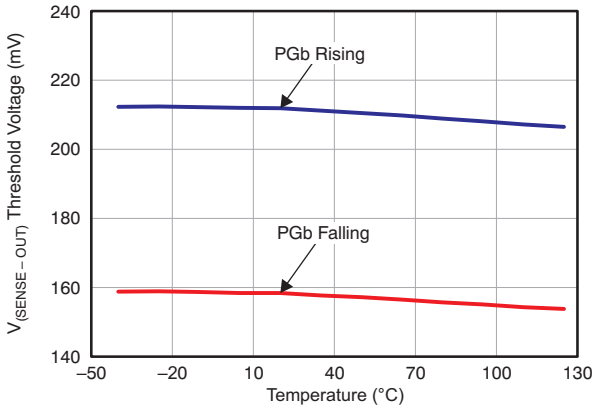


Figure 13. Threshold Voltage of V_{DS} vs Temperature, PGb Rising and Falling

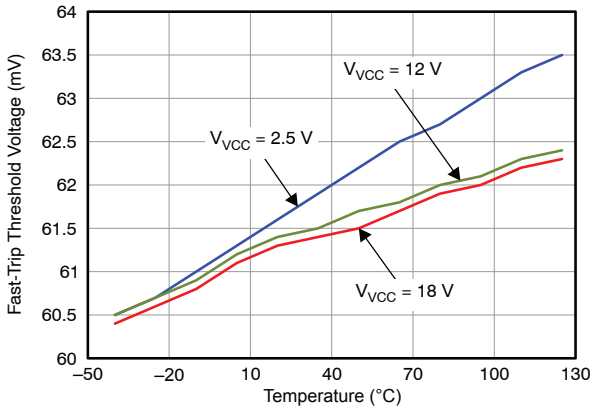


Figure 14. Fast-Trip Threshold Voltage vs Temperature

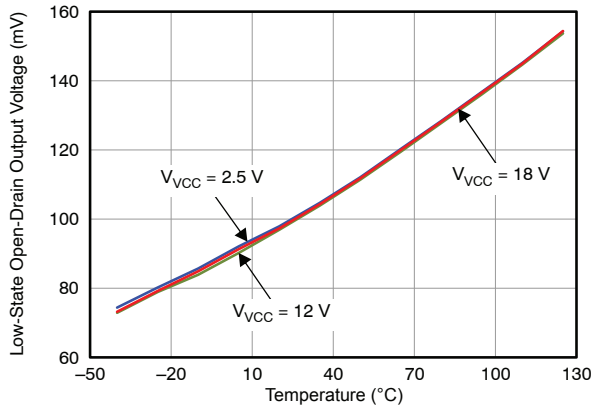


Figure 15. PGb Open-Drain Output Voltage in Low State

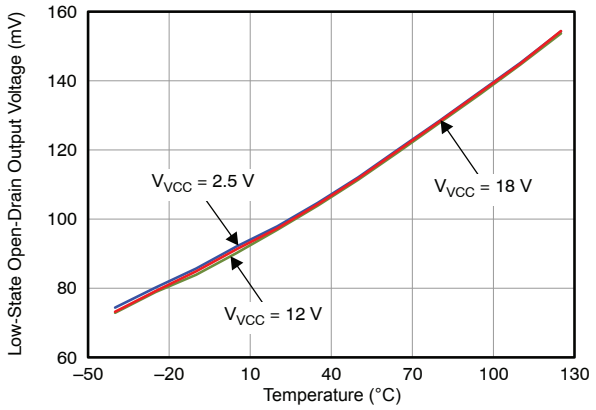


Figure 16. FLTb Open-Drain Output Voltage in Low State

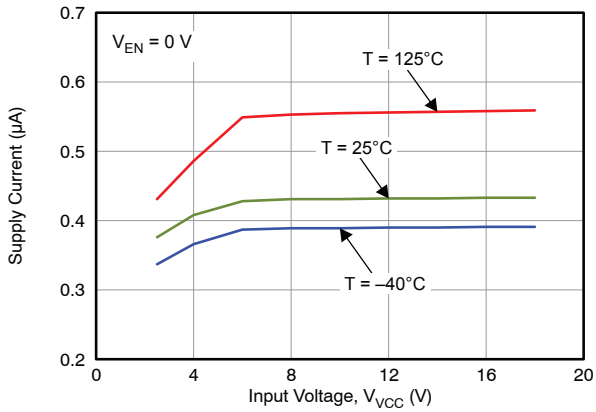


Figure 17. Supply Current vs Input Voltage at Various Temperatures when EN Pulled Low

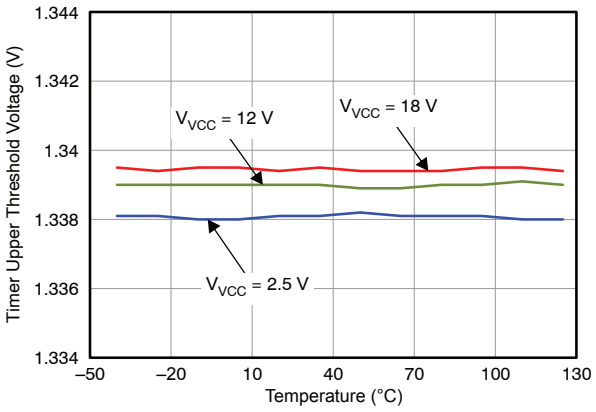


Figure 18. Timer Upper Threshold Voltage vs Temperature at Various Input Voltages

Typical Characteristics (continued)

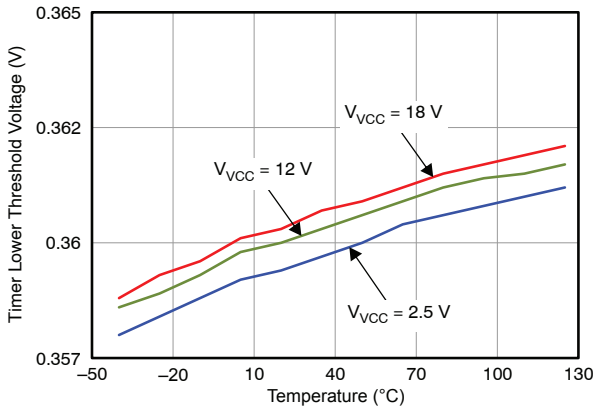


Figure 19. Timer Lower Threshold Voltage vs Temperature at Various Input Voltages

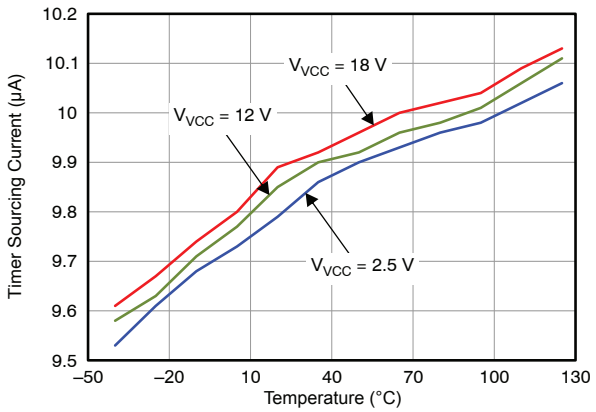


Figure 20. Timer Sourcing Current vs Temperature at Various Input Voltages

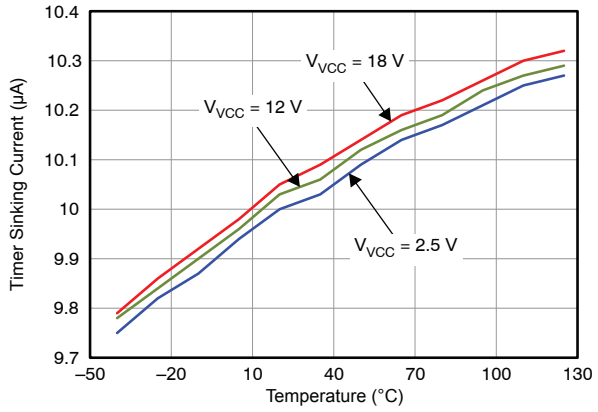


Figure 21. Timer Sinking Current vs Temperature at Various Input Voltages

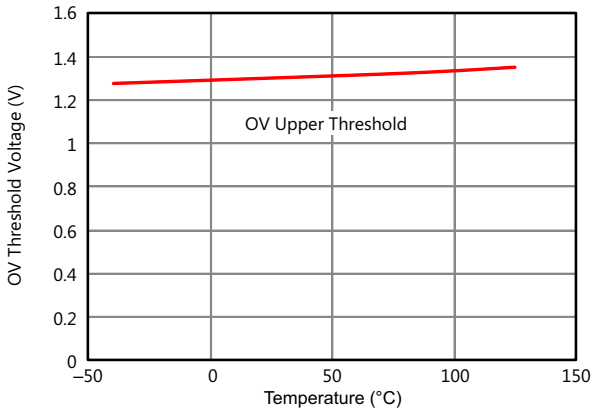


Figure 22. OV Threshold Voltage vs Temperature

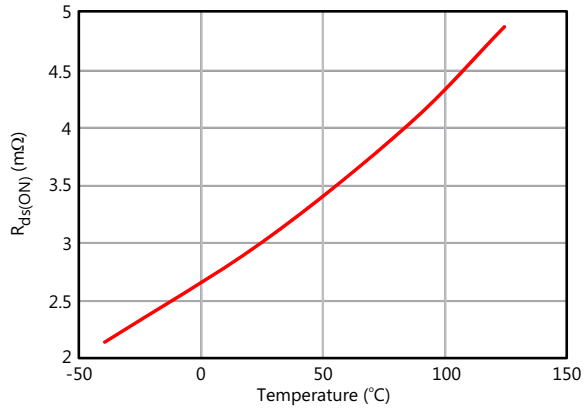


Figure 23. $R_{DS(ON)}$ vs Temperature

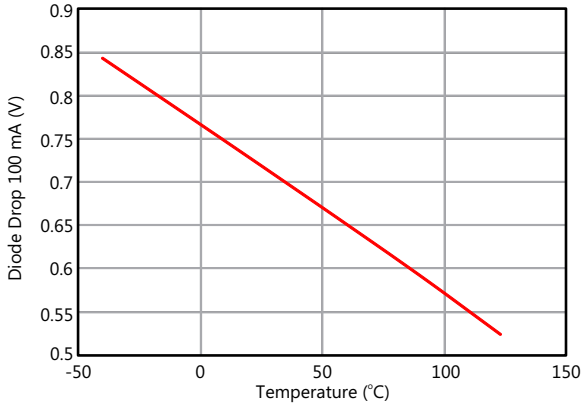


Figure 24. Diode Drop vs Temperature

Typical Characteristics (continued)

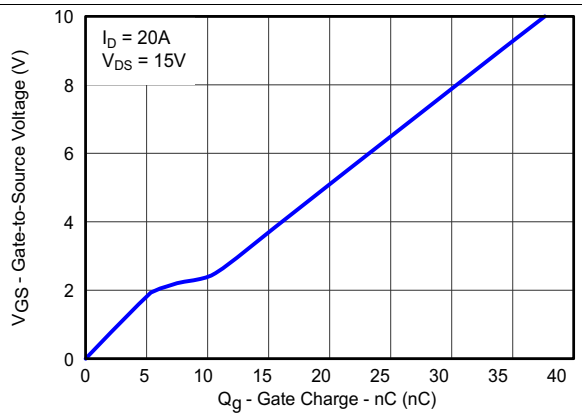


Figure 25. Gate Charge – Internal MOSFET

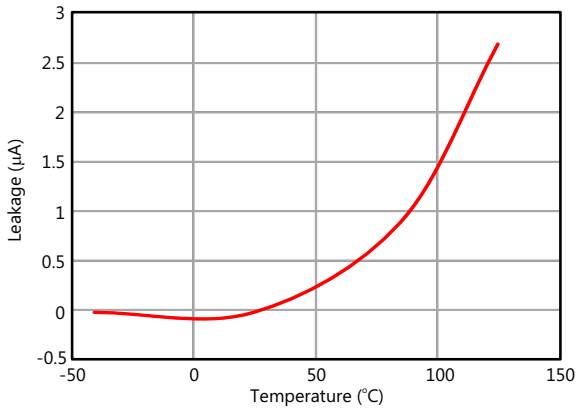


Figure 26. Leakage Current vs Temperature

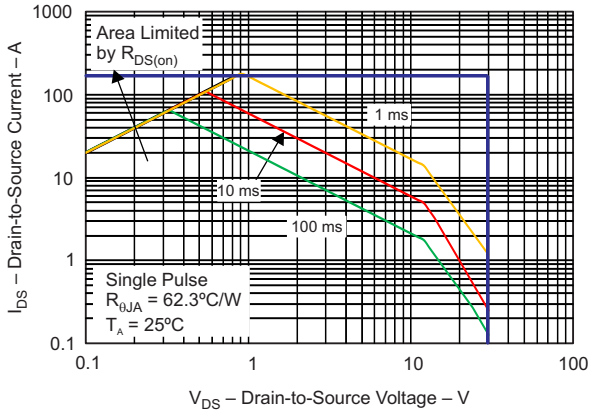


Figure 27. TPS2475x Maximum Safe Operating Area (SOA)

8 Parameter Measurement Information

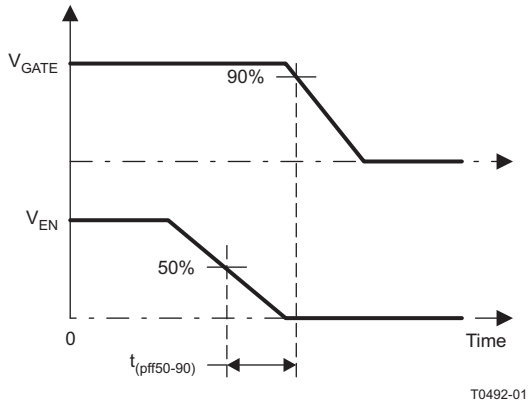


Figure 28. $t_{pff50–90}$ Timing Definition

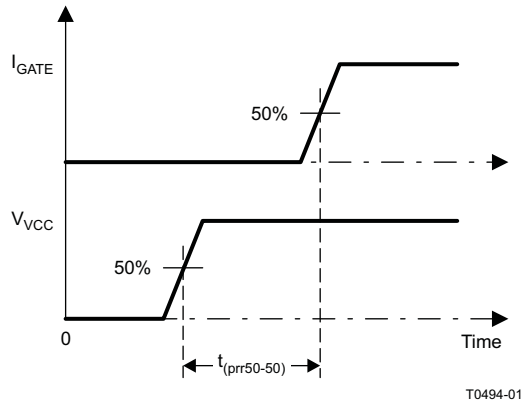


Figure 29. $t_{prr50–50}$ Timing Definition

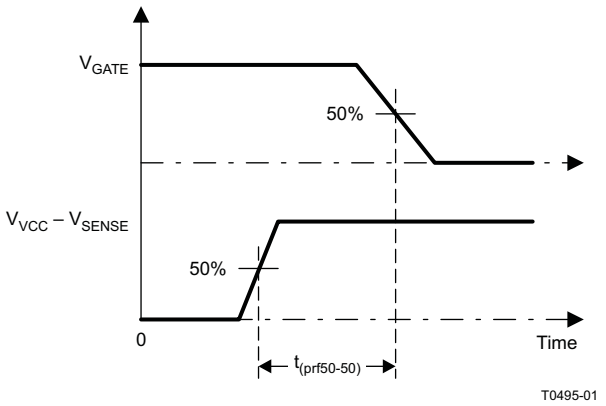


Figure 30. $t_{prf50–50}$ Timing Definition

9 Detailed Descriptions

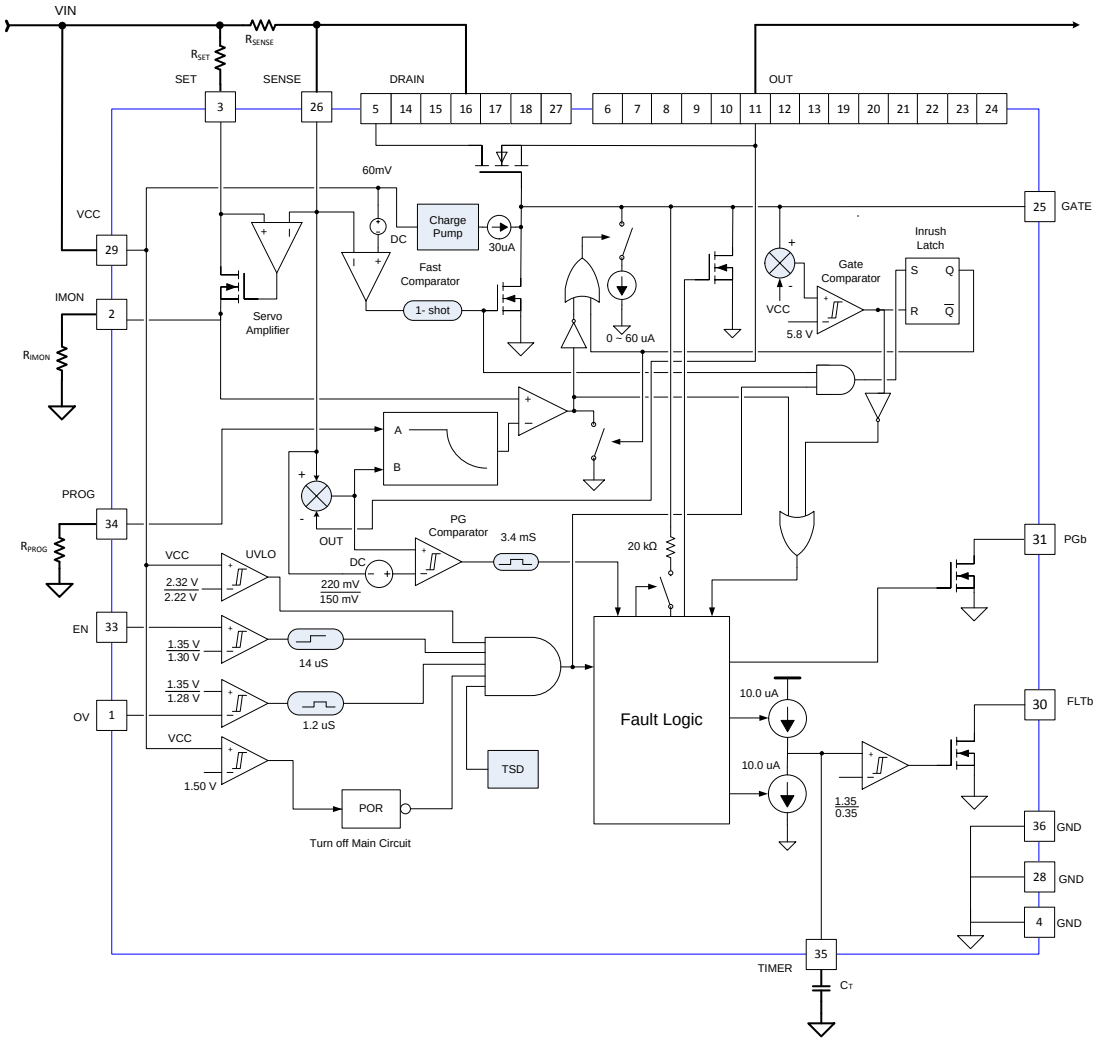
9.1 Overview

The TPS2475x provides all the features needed for a positive hot-swap protector. These features include:

- Undervoltage lockout
- Adjustable (system-level) enable
- Turnon inrush limiting
- Integrated N-channel MOSFET
- MOSFET protection by power limiting
- Electronic circuit breaker operation with adjustable overload timeout
- Charge-complete indicator for downstream converter coordination
- A choice of latch or automatic restart mode
- Load overvoltage protection
- Precise current monitor output

The typical application diagram, shown on the front page of this data sheet, and oscilloscope plots, shown in Figure 31 through Figure 33 and Figure 35 through Figure 39, demonstrate many of the functions of the device.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 DRAIN

The drain of the internal pass MOSFET. Connect to a terminal of current sense resistor in the power path.

9.3.2 EN

Applying a voltage of 1.3 V or more to this pin enables the gate driver. The addition of an external resistor divider allows the EN pin to serve as an undervoltage monitor. Cycling EN low and then back high resets the TPS24750 that has latched off due to a fault condition. This pin must not be left floating.

9.3.3 FLTb

This active-low open-drain output pulls low when the TPS2475x has remained in current limit long enough for the fault timer to expire. The TPS24750 operates in latch mode while the TPS24751 operates in retry mode. In latch mode, a fault timeout disables the internal MOSFET and holds FLTb low. The fault is reset when EN is pulled low or VCC falls under UVLO. In retry mode, a fault timeout first disables the internal MOSFET, next waits sixteen cycles of TIMER charging and discharging, and finally attempts a restart. This process repeats as long as the fault persists. In retry mode, the FLTb pin is pulled low whenever the internal MOSFET is disabled by the fault timer. In a sustained fault, the FLTb waveform becomes a train of pulses. The FLTb pin does not assert if the internal MOSFET is disabled by EN, OV, overtemperature shutdown, or UVLO. This pin can be left floating when not used.

9.3.4 GATE

This pin provides gate drive to the internal MOSFET. A charge pump sources 30 µA to enhance the internal MOSFET. A 13.9 V clamp between GATE and VCC limits the gate-to-source voltage since V_{VCC} is close to V_{OUT} in normal operation. During start up, a transconductance amplifier regulates the gate voltage of the internal FET to provide inrush current limiting. The TIMER pin charges timer capacitor C_T during the inrush. Inrush current limiting continues until the $V_{(GATE - VCC)}$ exceeds the Timer Activation Voltage 5.8 V for V_{VCC} = 12 V. Then the TPS2475x enters into circuit breaker mode. In the circuit breaker mode, the current flowing in R_{SENSE} is compared with the current limit threshold derived from the MOSFET power limit scheme (see the *PROG* definition). If the current flowing in R_{SENSE} exceeds the current limit threshold, then the internal pass MOSFET will be turned off. The GATE pin is disabled by the following three mechanisms:

1. GATE is pulled down by an 11-mA current source when
   - The fault timer expires during an overload current fault (V_{IMON} > 675 mV)
   - V_{EN} is below its falling threshold
   - V_{VCC} drops below the UVLO threshold
   - V_{OV} is above its rising threshold
2. GATE is pulled down by a 1-A current source for 13.5 µs when a hard output short circuit occurs and $V_{(VCC - SENSE)}$ is greater than 60 mV, that is, the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11-mA sustaining current ensures that the internal FET remains off.
3. GATE is discharged by a 20-kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

GATE remains low in latch mode (TPS24750) and attempts a restart periodically in retry mode (TPS24751).

Connect a capacitor from this pin to GND to control the slew rate of the output voltage at power-on. This pin can be left floating to obtain a predetermined slew rate on the output.

If used, any capacitor connecting GATE and GND must not exceed 1 µF and it must be connected in series with a resistor of no less than 1 kΩ. No external resistor must be directly connected from GATE to GND or from GATE to OUT.

9.3.5 GND

This pin is connected to system ground.

Feature Description (continued)

9.3.6 IMON

A resistor connected from this pin to GND scales the current-limit and power-limit settings, as illustrated in the *Functional Block Diagram*. The voltage present at this pin is proportional to the current flowing through sense resistor R_{SENSE}. This voltage can be used as a means of monitoring current flow through the system. The value of R_{IMON} can be calculated from Equation 3. This pin must not have a bypass capacitor or any other load except for R_{IMON}.

9.3.7 OUT

This pin is connected to the source of the internal MOSFET inside the chip. It allows the device to measure the drain-to-source voltage across the internal MOSFET. The power good indicator (PGb) relies upon this information, as does the power limiting engine. The OUT pin must be bypassed to GND with a low-impedance ceramic capacitor in the range of 10 nF to 1 μF. Connect all the OUT pins to output capacitors and load. In the presence of cable inductance, the OUT pin must be protected from negative voltage transients by using a clamping/Schottky diode.

9.3.8 OV

This pin is used to program the device overvoltage level. A voltage of more than 1.35 V on this pin turns off the internal FET. A resistor divider connected from VCC to this pin provides overvoltage protection for the downstream load. This pin must be tied to GND when not used.

9.3.9 PGb

This active low, open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits. PGb pulls low after the drain-to-source voltage of the internal FET has fallen below 150 mV and a 3.4 ms deglitch delay has elapsed. It goes open drain when V_{DS} exceeds 220 mV. PGb assumes high impedance status after a 3.4 ms deglitch delay once V_{DS} of internal FET rises up, resulting from GATE being pulled to GND at the following conditions:

- An overload current fault occurs (V_{IMON} > 675 mV) and the fault timer times out.
- A hard output short circuit occurs, leading to $V_{(VCC\ -\ SENSE)}$ greater than 60 mV, that is, the fast-trip shutdown threshold has been exceeded.
- V_{EN} is below its falling threshold.
- V_{VCC} drops below the UVLO threshold.
- V_{OV} is above its rising threshold.
- Die temperature exceeds the OTSD threshold.

This pin can be left floating when not used.

9.3.10 PROG

A resistor from this pin to GND sets the maximum power permitted in the internal MOSFET during inrush. Do not apply a voltage to this pin. If the constant power limit is not desired, use a PROG resistor of 4.99 kΩ. To set the maximum power, use Equation 1.

$$P_{LIM} = \frac{84375 \times R_{SET}}{R_{PROG} \times R_{SENSE} \times R_{IMON}} \quad (1)$$

where P_{LIM} is the allowed power limit of the internal MOSFET. R_{SENSE} is the load current monitoring resistor connected between the VCC pin and the SENSE pin. R_{PROG} is the resistor connected from the PROG pin to GND. Both R_{PROG} and R_{SENSE} are in ohms and P_{LIM} is in watts. P_{LIM} is determined by the maximum allowed thermal stress of internal MOSFET, given by Equation 2.

$$P_{LIM} < \frac{T_{J(MAX)} - T_{C(MAX)}}{R_{\theta JC(MAX)}} \quad (2)$$

where $T_{J(MAX)}$ is the maximum desired transient junction temperature and $T_{C(MAX)}$ is the maximum case temperature prior to a start or restart. $R_{\theta JC(MAX)}$ is the junction-to-case thermal impedance of the internal pass FET in units of °C/W. Both $T_{J(MAX)}$ and $T_{C(MAX)}$ are in °C.

Feature Description (continued)

9.3.11 SENSE

This pin connects to the negative terminal of R_{SENSE}. It provides a means of sensing the voltage across this resistor, as well as a way to monitor the drain-to-source voltage across the internal FET. The current limit I_{LIM} is set by Equation 3.

$$I_{LIM} = \frac{0.675\ V \times R_{SET}}{R_{IMON} \times R_{SENSE}} \quad (3)$$

A fast-trip shutdown occurs when $V_{(VCC\ -\ VSENSE)}$ exceeds 60 mV.

SET: A resistor R_{SET} is connected from this pin to the positive terminal of R_{SENSE}. This resistor scales the current limit and power limit settings. It coordinates with R_{IMON} and R_{SENSE} to determine the current limit value. The value of R_{SET} can be calculated from Equation 3 (see the *SENSE* definition).

9.3.12 TIMER

A capacitor C_T connected from the TIMER pin to GND determines the overload fault timing. TIMER sources 10 µA when an overload is present, and discharges C_T at 10 µA otherwise. Internal FET is turned off when V_{TIMER} reaches 1.35 V. In an application implementing auto-retry after a fault, this capacitor also determines the period before the internal FET is re-enabled. A minimum timing capacitance of 1 nF is recommended to ensure proper operation of the fault timer. The value of C_T can be calculated from the desired fault time t_{FLT}, using Equation 4.

$$C_T = \frac{10\ \mu A}{1.35\ V} \times t_{FLT} \quad (4)$$

Either latch mode (TPS24750) or retry mode (TPS24751) occurs if the load current exceeds the current limit threshold or the fast trip shutdown threshold. While in latch mode, the TIMER pin continues to periodically charge and discharge the attached capacitor. In retry mode, the internal MOSFET is disabled for sixteen cycles of TIMER charging and discharging. The TIMER pin is pulled to GND by a 2 mA current source at the end of the 16^{th} cycle of charging and discharging. The internal MOSFET is then re-enabled. The TIMER pin capacitor, C_T, can also be discharged to GND during latch mode or retry mode in the following way:

- A 2-mA current sinks TIMER whenever any of the following occurs:
  - V_{EN} is below its falling threshold.
  - V_{VCC} drops below the UVLO threshold.
  - V_{OV} is above its rising threshold.

TIMER is not affected when the die temperature exceeds the OTSD threshold.

9.3.13 VCC

This pin performs three functions. First, it provides biasing power to the integrated circuit. Second, it serves as an input to the power-on reset (POR) and undervoltage lockout (UVLO) functions. Bypass capacitor C_1, shown in the typical application diagram on the front page, must be connected to the positive terminal of V_{VCC}. A capacitance of at least 10 nF is recommended.

9.4 Device Functional Modes

9.4.1 Board Plug-In

Figure 31 and Figure 32 illustrate the inrush current that flows when a hot swap board under the control of the TPS2475x is plugged into a system bus. Only the bypass capacitor charge current and small bias currents are evident when a board is first plugged in. The TPS2475x is held inactive for a short period while internal voltages stabilize. In this short period, GATE, PROG, and TIMER are held low and PGb, and FLTb, are held open-drain. When the voltage on the internal VCC rail exceeds approximately 1.5 V, the power-on reset (POR) circuit initializes the TPS2475x and a start-up cycle is ready to take place.

GATE, PROG, TIMER, PGb, and FLTb are released after the internal voltages have stabilized and the external EN (enable) thresholds have been exceeded. The part begins sourcing current from the GATE pin to turnon internal FET. The TPS2475x monitors both the drain-to-source voltage across internal MOSFET and the drain current passing through it. Based on these measurements, the TPS2475x limits the drain current by controlling the gate voltage so that the power dissipation of the internal FET does not exceed the power limit programmed by the user. The current increases as the voltage across the FET decreases until finally the current reaches the current limit I_{LIM}.

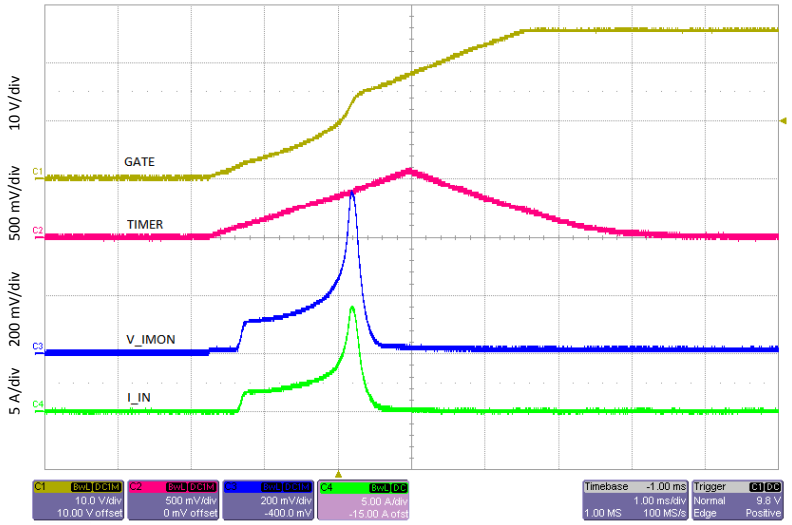


Figure 31. Inrush Mode at Hot-Swap Circuit Insertion

9.4.2 Inrush Operation

After the TPS2475x initialization is complete (as described in the *Board Plug-in section*) and EN is active, GATE is enabled (V_{GATE} starts increasing), when V_{GATE} reaches the internal FET gate threshold, a current flows into the downstream bulk storage capacitors. When this current exceeds the limit set by the power-limit engine, the gate of the internal FET is regulated by a feedback loop to make the internal FET current rise in a controlled manner. This not only limits the capacitor-charging inrush current but it also limits the power dissipation of the internal FET to safe levels. A more complete explanation of the power-limiting scheme is given in the *Action of the Constant-Power Engine* section. When the GATE is enabled, the TIMER pin begins to charge the timing capacitor C_T with a current of approximately 10 µA. The TIMER pin continues to charge C_T until $V_{(GATE-VCC)}$ reaches the timer activation voltage (5.8 V for V_{VCC} = 12V). The TIMER then begins to discharge C_T with a current of approximately 10 µA. This indicates that the inrush mode is finished. If the TIMER exceeds its upper threshold of 1.35 V before $V_{(GATE\ -\ VCC)}$ reaches the timer activation voltage, the GATE pin is pulled to GND and the hot-swap circuit enters either latch mode (TPS24750) or auto-retry mode (TPS24751).

The power limit feature is disabled once the inrush operation is finished and the hotswap circuit becomes a circuit breaker. The TPS2475x turns off the internal FET after a fault timer period once the load exceeds the current limit threshold.

Device Functional Modes (continued)

9.4.3 Action of the Constant-Power Engine

Figure 32 illustrates the operation of the constant-power engine during start-up. The circuit used to generate the waveforms of Figure 32 was programmed to a power limit of 21 W by means of the resistor connected between PROG and GND. At the moment current begins to flow through the internal FET, a voltage of 12 V appears across it (input voltage V_{VCC} = 12 V), and the constant-power engine therefore allows a current of 1.75 A (equal to 21 W divided by 12 V) to flow. This current increases in inverse ratio as the drain-to-source voltage diminishes, so as to maintain a constant dissipation of 21 W. The constant-power engine adjusts the current by altering the reference signal fed to the current limit amplifier. The lower part of Figure 32 shows the measured power dissipated in the internal FET, labeled FET PWR, remaining substantially constant during this period of operation, which ends when the current through the FET reaches the current limit I_{LIM}. This behavior can be considered a form of foldback limiting, but unlike the standard linear form of foldback limiting, it allows the power device to operate near its maximum capability, thus reducing the start-up time.

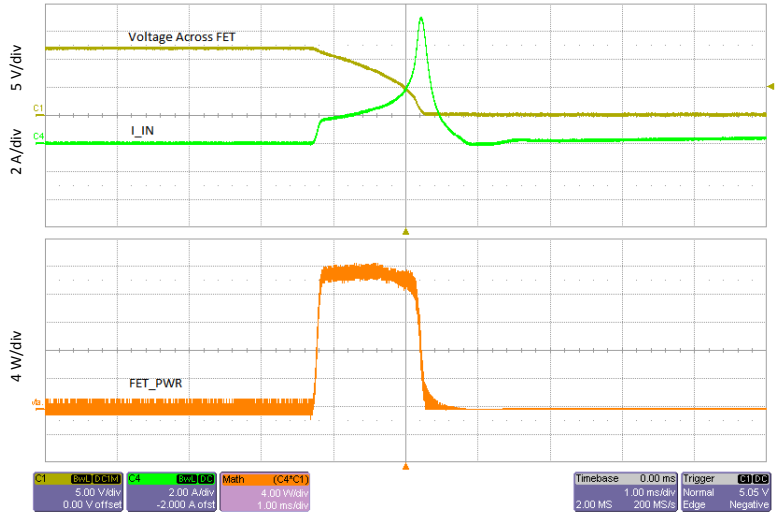


Figure 32. Computation of Power Stress During Startup

9.4.4 Circuit Breaker and Fast Trip

The TPS2475x monitors load current by sensing the voltage across R_{SENSE}. The TPS2475x incorporates two distinct thresholds: a current-limit threshold and a fast-trip threshold.

The functions of circuit breaker and fast-trip turnoff are shown in Figure 33 through Figure 36.

Figure 33 shows the behavior of the TPS2475x when a fault in the output load causes the current passing through R_{SENSE} to increase to a value above the current limit but less than the fast-trip threshold. When the current exceeds the current-limit threshold, a current of approximately 10 μA begins to charge timing capacitor C_T. If the voltage on C_T reaches 1.35 V, then the internal FET is turned off. The TPS24750 version latches off, while as the TPS24751 version commences a restart cycle. In either event, fault pin FLTb pulls low to signal a fault condition. Overload between the current limit and the fast-trip threshold is permitted for this period. This shutdown scheme is sometimes called an electronic circuit breaker.

The fast-trip threshold protects the system against a severe overload or a dead short circuit. When the voltage across the sense resistor R_{SENSE} exceeds the 60-mV fast-trip threshold, the GATE pin immediately pulls the internal FET gate to ground with approximately 1 A of current. The fast-trip circuit holds the internal FET off for only a few microseconds, after which the TPS2475x turns back on slowly, allowing the current-limit feedback loop to take over the gate control of the internal FET. Then the hot-swap circuit goes into latch mode (TPS24750) or auto-retry mode (TPS24751). Figure 35 and Figure 36 illustrate the behavior of the system when the current exceeds the fast-trip threshold.

Device Functional Modes (continued)

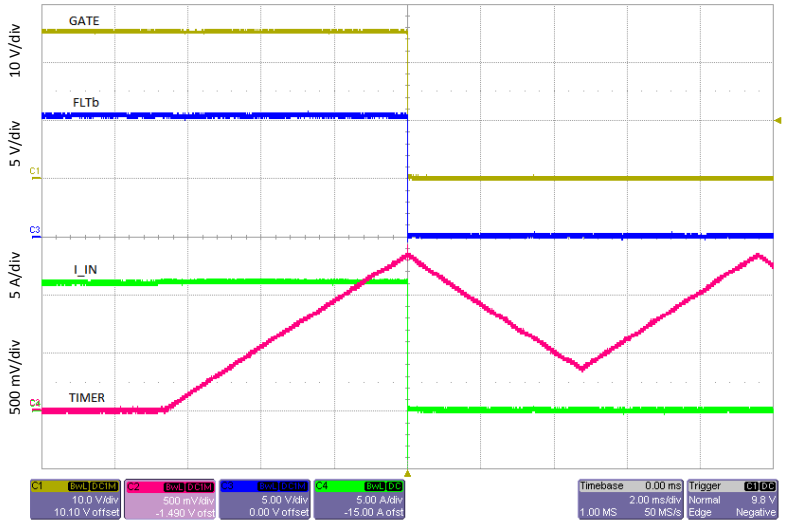


Figure 33. Circuit-Breaker Mode During Overload Condition

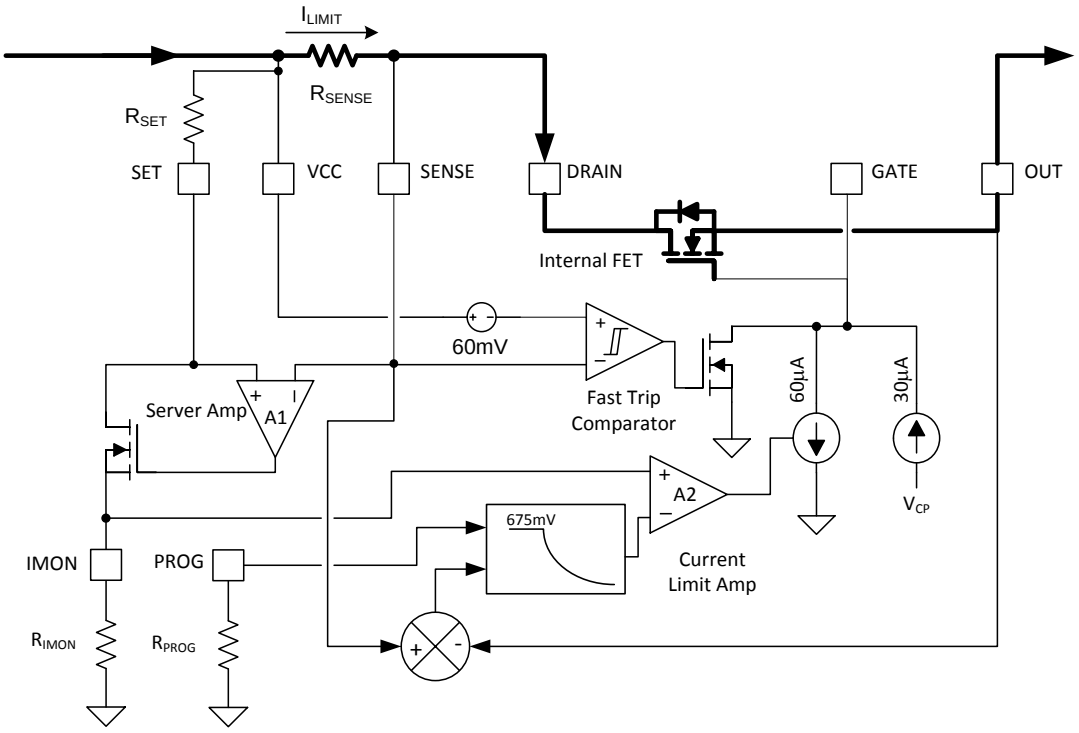


Figure 34. Partial Diagram of the TPS2475x with Selected External Components

Device Functional Modes (continued)

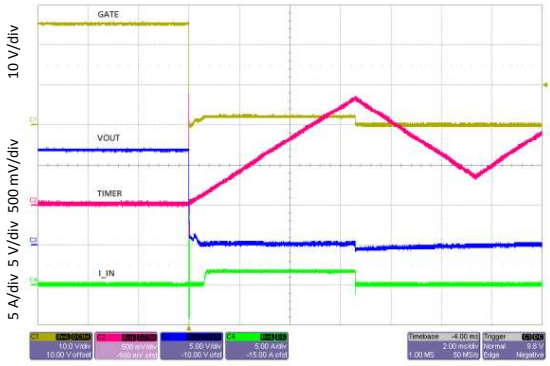


Figure 35. Current Limit During Output-Load Short-Circuit Condition (Overview)

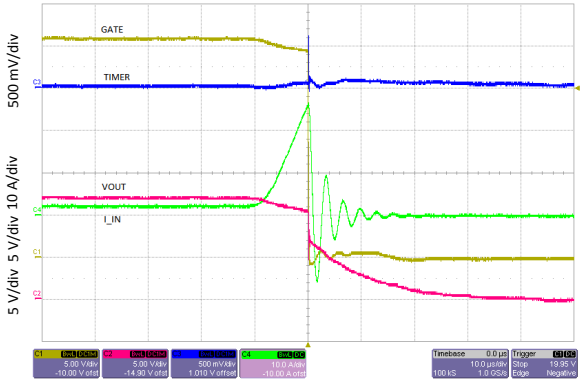


Figure 36. Current Limit During Output-Load Short-Circuit Condition (Onset)

9.4.5 Automatic Restart

In Auto-retry versions (TPS24751), device automatically initiates a restart after a fault has caused it to turnoff the internal FET. Internal control circuits use C_T to count 16 cycles before re-enabling the FET as shown in Figure 37. This sequence repeats if the fault persists. The timer has a 1:1 charge-to-discharge current ratio. For the very first cycle, the TIMER pin starts from 0 V and rises to the upper threshold of 1.35 V and subsequently falls to 0.35 V before restarting. For the following 16 cycles, 0.35 V is used as the lower threshold. This small duty cycle often reduces the average short-circuit power dissipation to levels associated with normal operation and eliminates special thermal considerations for surviving a prolonged output short.

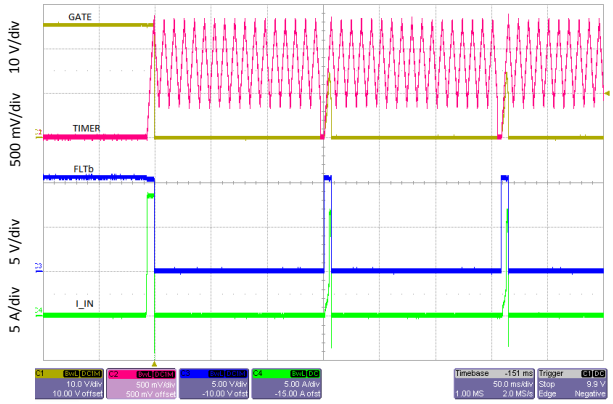


Figure 37. Auto-Restart Cycle Timing

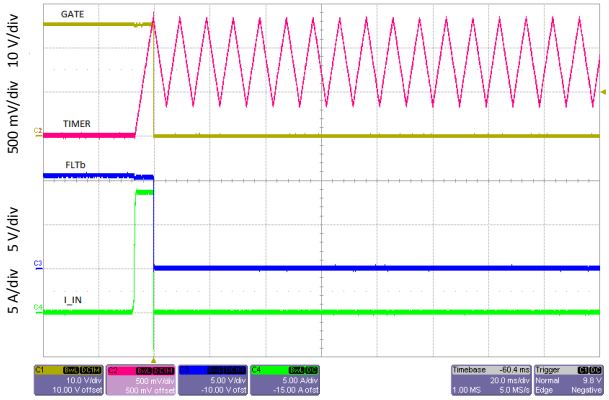


Figure 38. Latch After Overload Fault

Device Functional Modes (continued)

9.4.6 Start-Up with Short on Output

The TPS2475x has ability of detecting the short at the output during start-up and ensure shutdown of the hot-swap circuit/system with fault indication. During start-up, after the initialization process is complete and the GATE is enabled, the device limits the power as explained in the *Action of the Constant-Power Engine* section and the TIMER pin begins to charge the timing capacitor CT with approximately 10 µA constant current source. If the voltage on CT reaches its upper limit threshold of 1.35V, during start-up cycle itself, then the internal FET is turned off and fault pin FLTb is pulled low to signal the fault condition. After this, the hot-swap circuit enters either in latch mode (TPS24750) or auto-retry mode (TPS24751). Figure 39 shows the behavior of the TPS2475x for start-up with short on the output.

This feature help to ensure early detection of fault and quick isolation of the subsystem to ensure stability of the other units connected on the DC bus.

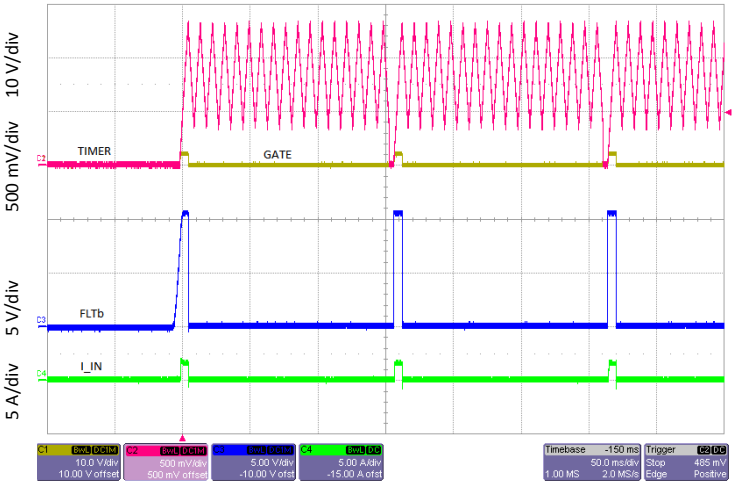


Figure 39. Start-Up with Short on Output

Device Functional Modes (continued)

9.4.7 PGb, FLTb, and Timer Operations

The open-drain PGb output provides a deglitched end-of-inrush indication based on the voltage across internal FET. PGb is useful for preventing a downstream dc/dc converter from starting while its input capacitor C_{OUT} is still charging. PGb goes active-low about 3.4 ms after C_{OUT} is charged. This delay allows the internal FET to fully turnon and any transients in the power circuits to end before the converter starts up. This type of sequencing prevents the downstream converter from demanding full current before the power-limiting engine allows the internal FET to conduct the full current set by the current limit I_{LIM}. Failure to observe this precaution may prevent the system from starting. The pullup resistor shown on the PGb pin in the typical system block diagram application diagram Figure 41 is illustrative only; the actual connection to the converter depends on the application. The PGb pin may indicate that inrush has ended before the MOSFET is fully enhanced, but the downstream capacitor will have been charged to substantially its full operating voltage. After the hot-swap circuit successfully starts up, the PGb pin can return to a high-impedance status whenever the drain-to-source voltage of internal FET exceeds its upper threshold of 340 mV, which presents the downstream converters a warning flag. This flag may occur as a result of overload fault, output short fault, input overvoltage, higher die temperature, or the GATE shutdown by UVLO, EN.

FLTb is an indicator that the allowed fault-timer period during which the load current can exceed the programmed current limit (but not the fast-trip threshold) expires. The fault timer starts when a current of approximately 10 μA begins to flow into the external capacitor C_T, and ends when the voltage of C_T reaches TIMER upper threshold, that is, 1.35 V. FLTb pulls low at the end of the fault timer. Otherwise, FLTb assumes a high-impedance state.

The fault-timer state requires an external capacitor C_T connected between the TIMER pin and GND pin. The duration of the fault timer is the charging time of C_T from 0 V to its upper threshold of 1.35 V. The fault timer begins to count under any of the following three conditions:

1. In the inrush mode, TIMER begins to source current to the timer capacitor, C_T, when device is enabled. TIMER begins to sink current from the timer capacitor, C_T when $V_{(GATE - VCC)}$ exceeds the timer activation voltage (see the *Inrush Operation* section). If $V_{(GATE - VCC)}$ does not reach the timer activation voltage before TIMER reaches 1.35 V, then the TPS2475x disables the internal FET. After the MOSFET turns off, the timer goes into either latch mode (TPS24750) or retry mode (TPS24751).
2. In an overload fault, TIMER begins to source current to the timer capacitor, C_T, when the load current exceeds the programmed current limits. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor, C_T, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into latch mode (TPS24750) or retry mode (TPS24751).
3. In output short-circuit fault, TIMER begins to source current to the timer capacitor, C_T, when the load current exceeds the programmed current limits following a fast-trip shutdown of internal FET. When the timer capacitor voltage reaches its upper threshold of 1.35 V, TIMER begins to sink current from the timer capacitor, C_T, and the GATE pin is pulled to ground. After the fault timer period, TIMER may go into latch mode (TPS24750) or retry mode (TPS24751).

If the fault current drops below the programmed current limit within the fault timer period, V_{TIMER} decreases and the internal pass MOSFET remains enabled.

The behaviors of TIMER are different in the latch mode and retry mode. If the timer capacitor reaches the upper threshold of 1.35 V, then:

- In latch mode(TPS24750), the TIMER pin continues to charge and discharge the attached capacitor periodically until device is disabled by UVLO, EN, or OV, as shown in Figure 38.
- In retry mode(TPS24751), TIMER charges and discharges C_T between the lower threshold of 0.35 V and the upper threshold of 1.35 V for sixteen cycles before the device attempts to re-start. The TIMER pin is pulled to GND at the end of the 16^{th} cycle of charging and discharging and then ramps from 0 V to 1.35 V for the initial half-cycle in which the GATE pin sources current. This periodic pattern is stopped once the overload fault is removed or the TPS2475x is disabled by UVLO, EN or OV.

Device Functional Modes (continued)

9.4.7.1 Overtemperature Shutdown

The TPS2475x includes a built-in overtemperature shutdown circuit designed to disable the gate driver and hence turnoff the internal FET if the die temperature exceeds approximately 140°C. An overtemperature condition also causes the FLTb and PGb pins to go to high-impedance states. Normal operation resumes once the die temperature has fallen approximately 10°C.

9.4.7.2 Start-Up of Hot-Swap Circuit by VCC or EN

The connection and disconnection between a load and the input power bus are controlled by turning on and turning off the internal FET.

The TPS2475x has two ways to turnon the internal FET:

- Increasing V_{VCC} above UVLO upper threshold while EN is already higher than its upper threshold sources current to the gate of internal FET. After an inrush period, the TPS2475x fully turns on internal FET.
- Increasing EN above its upper threshold while V_{VCC} is already higher than the UVLO upper threshold sources current to the gate of internal FET. After an inrush period, the TPS2475x fully turns on internal FET.

The EN pin can be used to start up the TPS2475x at a selected input voltage V_{VCC}.

To isolate the load from the input power bus, the internal FET can be disabled by any of the following conditions: UVLO, EN, load current above the current-limit threshold, hard short at load, OV, or OTSD. Three separate mechanisms disable the internal FET by pulling down the GATE as described below:

1. GATE is pulled down by an 11-mA current source when any of the following occurs.
   - The fault timer expires during an overload current fault (V_{IMON} > 675 mV).
   - V_{EN} is below its falling threshold.
   - V_{VCC} drops below the UVLO threshold.
   - V_{OV} is above its rising threshold.
2. GATE is pulled down by a 1-A current source for 13.5 μs when a hard output short circuit occurs and $V_{(VCC - SENSE)}$ is greater than 60 mV, that is, the fast-trip shutdown threshold. After fast-trip shutdown is complete, an 11-mA sustaining current ensures that the internal FET remains off.
3. GATE is discharged by a 20-kΩ resistor to GND if the chip die temperature exceeds the OTSD rising threshold.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS2475x provide highly integrated load protection for 2.5 V to 18 V applications. The devices integrate a hot swap controller and a power MOSFET in a single package for small form factor applications. These devices protect source, load and internal MOSFET from potentially damaging events in applications such as Servers, Plug-In Modules, RAID systems, Base stations and Fan Control.

The following design procedure can be used to select component values for the device.

Additionally, a spreadsheet design tool *TPS2475x Design Calculator Tool (SLVC545)* is available on web folder.

10.2 Typical Application

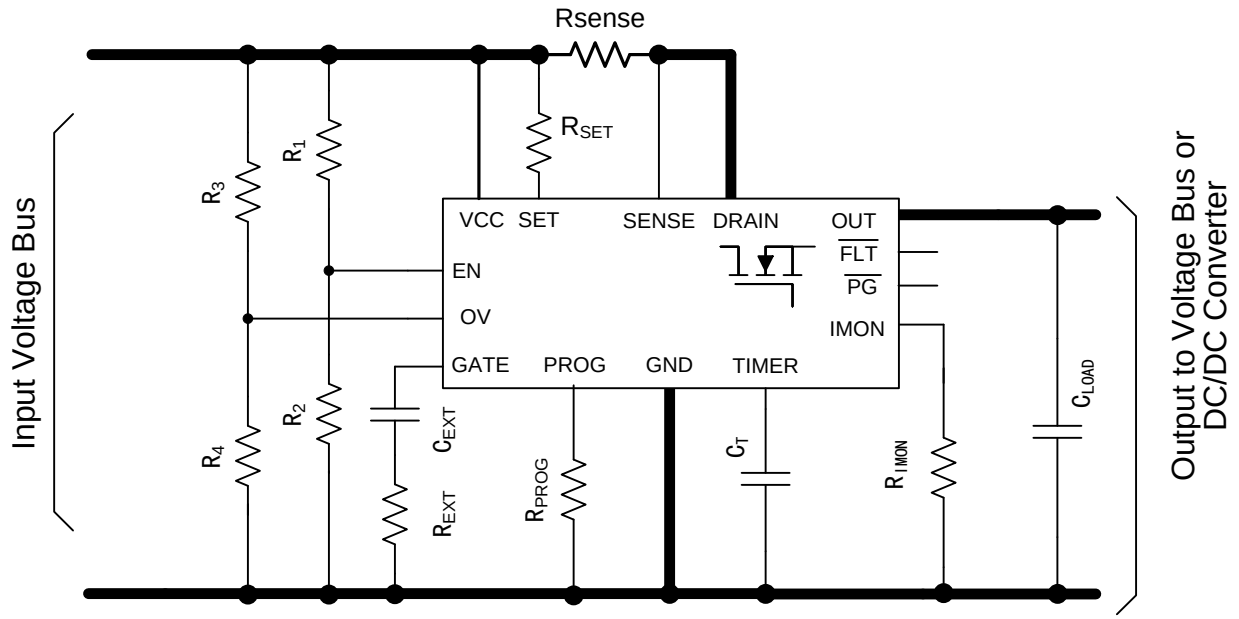


Figure 40. Gate Capacitor (dV/dt) Control Inrush Mode

10.2.1 Design Requirements

For this design example, use the parameters shown in Table 1.

Table 1. Design Parameters

Parameter	Value
Input voltage $V_{(VCC)}$	12 V
Undervoltage lockout set point, V_{UV}	8.4 V
Overvoltage protection set point , V_{OV}	14 V
Load after PG asserted , R_{LOAD}	1.2 Ω
Current limit, I_{LIM}	11 A
Load capacitance , C_{OUT}	470 µF
Maximum ambient temperatures , T_A	60°C

10.2.2 Detailed Design Procedure

10.2.2.1 Power-Limited Start-Up

This design example assumes a 12-V system voltage with an operating tolerance of ±2 V. The rated load current is 10 A. If the current exceeds 11 A, then the device must shut down and then attempt to restart. Ambient temperatures may range from 20°C to 60°C. The load has a minimum input capacitance of 470 µF. The load is turned on only after the PG signal is asserted. Figure 41 shows a simplified system block diagram of the proposed application.

This design procedure seeks to control the junction temperature of device under both static and transient conditions by proper selection of current limit, fault timeout, and power limit. The design procedure assumes the worst case as a unit running at full load and maximum ambient temperature experiences a short circuit event. Adjust this procedure to fit the application and design criteria.

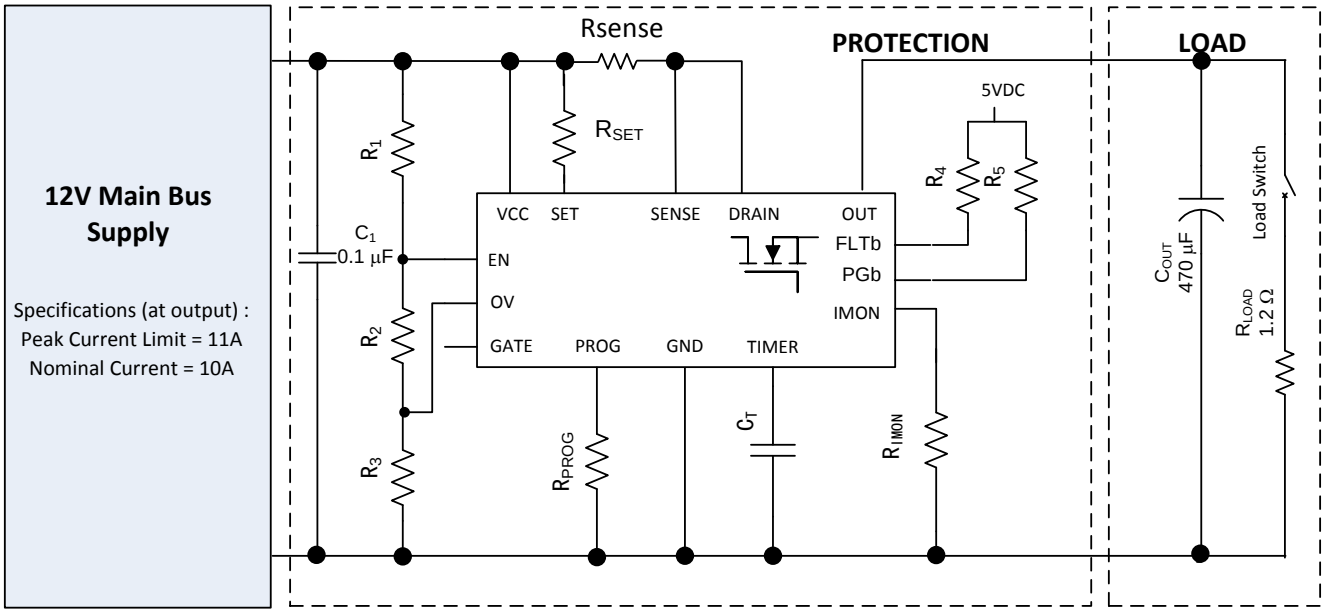


Figure 41. Simplified Block Diagram of the System Constructed in the Design Example

10.2.2.1.1 STEP 1. Choose R_{SENSE}, R_{SET}, and R_{IMON}

The recommended range of the current-limit threshold voltage, $V_{(VCC\ -\ SENSE)}$, extends from 10 mV to 42 mV. Values near the low threshold of 10 mV may be affected by system noise. Values near the upper threshold of 42 mV may be too close to the minimum fast-trip threshold voltage of 52 mV. Values near the middle of this range help minimize both concerns.

To achieve high efficiency, the power dissipation in R_{SENSE} must be kept to a minimum. A R_{SENSE} of 2 mΩ develops a voltage of 22 mV at the specified peak current limit of 11 A, while dissipating only 200 mW at the rated 10-A current. This represents a 0.17% power loss.

For best performance, a current of approximately 0.5 mA (see the *Recommended Operatings Conditions* table) must flow into the SET pin and out of the IMON pin when the TPS2475x is in current limit. The voltage across R_{SET} nominally equals the voltage across R_{SENSE}, or 22 mV. Dividing 22 mV by 0.5 mA gives a recommended value of R_{SET} of 44 Ω. A 51.1-Ω, 1% resistor was chosen. Using Equation 3, the value of R_{IMON} must equal 1568 Ω, or as near as practically possible. A 1.58-kΩ, 1% resistor was chosen. See Equation 5.

$$I_{LIM} = \frac{0.675\ V \times R_{SET}}{R_{IMON} \times R_{SENSE}}$$

therefore,

$$R_{IMON} = \frac{0.675\ V \times 51.1}{11 \times 0.002} = 1567.8 \quad (5)$$

10.2.2.1.2 STEP 2. Choose Power-Limit Value, P_{LIM}, and R_{PROG}

The internal MOSFET dissipates large amounts of power during inrush. The power limit P_{LIM} of the TPS2475x must be set to prevent the internal FET die temperature from exceeding a short-term maximum temperature, $T_{J(MAX)2}$. The short-term $T_{J(MAX)2}$ could be set ≤125°C to have sufficient margin to the internal maximum FET junction temperature. Equation 6 is an expression for calculating P_{LIM}.

$$P_{LIM} \le 0.8 \times \frac{T_{J(MAX)2} - \left[\left(I_{MAX}{}^2 \times R_{DS(on)} \times R_{\theta CA}\right) + T_{A(MAX)}\right]}{R_{\theta JC}}$$

therefore,

$$P_{LIM} \le 0.8 \times \frac{125°C - \left[\left((11\ A)^2 \times 5\ m\Omega \times (33.7°C/W - 1.1°C/W)\right) + 60°C\right]}{1.1°C/W} = 32.93\ W \quad (6)$$

In the above equation, $R_{\theta CA} = R_{\theta JA} - R_{\theta JC}$

Where, $R_{\theta CA}$ is the case-to-ambient thermal resistance ($R_{\theta CA}$ is a strong function of the user defined PCB layout and heat sinking provided on Pad-2 of the device and can vary accordingly), $R_{\theta JA}$ is the junction-to-ambient thermal resistance and $R_{\theta JC}$ is the junction-to-case thermal resistance of the device, (In Equation 6 , the values are used from the TPS2475x *Thermal Information* table), $r_{DS(on)}$ is internal FET on-resistance at the maximum operating temperature, and the factor of 0.8 represents the tolerance of the constant-power engine. For an ambient temperature of 60°C, the calculated maximum P_{LIM} is 33 W. Power limit selected must be lower than value obtained in Equation 6, to have substantial safe margin considering the tolerance of components and extended system temperatures. Power limit (P_{LIM}) of 21 W is considered for this design. From Equation 1, a 64.9-kΩ, 1% resistor is selected for R_{PROG} (see Equation 7).

$$R_{PROG} = \frac{84375 \times R_{SET}}{P_{LIM} \times R_{SENSE} \times R_{IMON}}$$

therefore,

$$R_{PROG} = \frac{84375 \times 51.1}{21 \times 0.002\Omega \times 1580\Omega} = 64.97\ k\Omega \quad (7)$$

Power Limit fold back (P_{LIM-FB}) is the ratio of operating current (I_{LIM}) and minimum power limited (regulated) current (when V_{OUT} = 0V). Degradation of programmed power limit (P_{LIM}) accuracy and start up issues may occur if P_{LIM-FB} is too large. Equation 8 calculates V_{SNS-PL_MIN} (minimum sense voltage during power limit) and P_{LIM-FB}. To ensure reliable operation, verify that P_{LIM-FB} < 12 and V_{SNS-PL_MIN} ≥ 3mV.

$$V_{SNS-PL\_MIN} = \frac{P_{LIM} \times R_{SENSE}}{V_{CC(MAX)}} = \frac{21W \times 2\ m\Omega}{14\ V} = 3\ mV\ (\ge\ 3\ mV)$$

$$P_{LIM-FB} = \frac{I_{LIM} \times V_{CC(MAX)}}{P_{LIM}} = \frac{11\ A \times 14\ V}{21\ W} = 7.33\ (< 12) \quad (8)$$

If the above conditions are not met, please adjust and align R_{SENSE}, P_{LIM} set, and $T_{A(MAX)}$ appropriately to satisfy the above conditions.

10.2.2.1.3 STEP 3. Choose Output Voltage Rising Time, t_{ON}, and Timing Capacitor C_T

The maximum output voltage rise time, t_{ON}, set by timer capacitor C_T must suffice to fully charge the load capacitance C_{OUT} without triggering the fault circuitry. Equation 9 defines t_{ON} for two possible inrush cases. Assuming that only the load capacitance draws current during startup,

$$t_{ON} = \begin{cases} \dfrac{C_{OUT} \times P_{LIM}}{2 \times I^2_{LIM}} + \dfrac{C_{OUT} \times V^2_{VCC(MAX)}}{2 \times P_{LIM}} & \text{if} \quad P_{LIM} < I_{LIM} \times V_{VCC(MAX)} \\ \dfrac{C_{OUT} \times V_{VCC(MAX)}}{I_{LIM}} & \text{if} \quad P_{LIM} > I_{LIM} \times V_{VCC(MAX)} \end{cases}$$

therefore,

$$t_{ON} = \frac{470\ \mu F \times 21\ W}{2 \times (11 \times 11)} + \frac{470\ \mu F \times 14 \times 14}{2 \times 21} = 2.234\ ms \tag{9}$$

The next step is to determine the minimum fault-timer period. In Equation 9, the output rise time is t_{ON}. This is the amount of time it takes to charge the output capacitor up to the final output voltage. However, the fault timer uses the difference between the input voltage and the gate voltage to determine if the TPS2475x is still in inrush limit. The fault timer continues to run until V_{GS} rises 5.8 V (for V_{VCC} = 12 V) above the input voltage. Some additional time must be added to the charge time to account for this additional gate voltage rise. The minimum fault time can be calculated using Equation 10.

$$t_{FLT} = t_{ON} + \frac{Q_{GINT} + Q_{GBLK}}{I_G}$$

therefore,

$$t_{FLT} = t_{ON} + \frac{22\ nC + 17\ nC}{20\ \mu A} = t_{ON} + 1.95\ ms = 4.184\ ms \tag{10}$$

where Q_{GINT} is the Gate charge of the internal FET to reach the 5.8 V gate voltage (see Figure 25), Q_{GBLK} is the Gate charge of blocking FET (for this design, it is considered that CSD17501Q5A SLPS303 blocking FET is used, take this as '0' if blocking FET is not used) and I_{GATE} is the minimum gate sourcing current of the TPS2475x, or 20 µA. Overall, Equation 10 leads to a minimum fault time of 4.184 ms. Considering the tolerances of C_{OUT}, C_T, I_{LIM} , I_{TIMER} and P_{LIM}, the fault timer must be set to a value ≥ 1.4 times of t_{FLT} obtained, to avoid turning off during start-up, but need to be lower than any maximum fault time limit determined by the device SOA curve (see Figure 27).

For this example, we select 6.3 ms (1.5 x T_{FLT}) to allow for variation of system parameters such as temperature, load, component tolerance, and input voltage. As per SOA curve (T_A = 25°C), for approximately 6.5 ms, the power handled by the device is approximately 70 W at 12 V (value obtained from extrapolation). This need to be scaled (derated) by a factor of $(150 - T_{JDCMAX})/(150 - T_A)$, where T_{JDCMAX} is the maximum steady state junction temperature ($T_{JDMAX} = T_{A(MAX)} + I_{LIM}^2 \times R_{(DS)ON} \times R_{\theta JA}$). The scaled power is approximately 34 W. So the power limit of 21 W considered has safe margin of 38% over the derated SOA. This can be depicted through the Figure 42. Also, from Figure 42, from the blue dotted line shown, it can be analyzed that the device at T_A = 25°C, can tolerate 12 V and 10 A for approximately time 1 ms and can take power of 21 W for duration of approximately 70 to 75 ms.

The timing capacitor is calculated in Equation 11 as 46.67 nF. Selecting the next-highest standard value, 47 nF, yields a 6.35 ms fault time.

$$C_T = \frac{10\ \mu A \times t_{FLT}}{1.35}$$

therefore,

$$C_T = \frac{10\ \mu A \times 6.3\ ms}{1.35} = 46.67\ nF \tag{11}$$

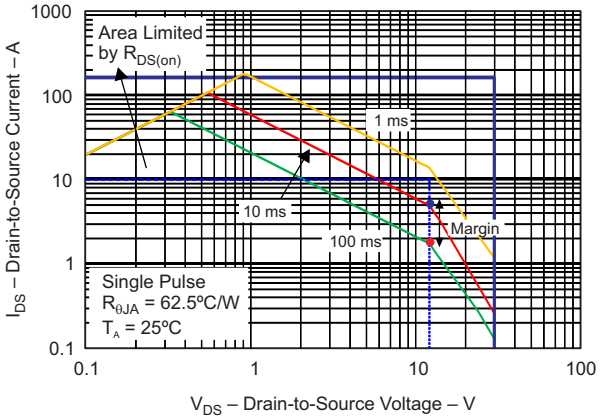


Figure 42. Design Example SOA

10.2.2.1.4 STEP 4. Calculate the Retry-Mode Duty Ratio

In retry mode, the TPS24751 is on for one charging cycle and off for 16 charge-discharge cycles, as can be seen in Figure 37. The first C_T charging cycle is from 0 V to 1.35 V, which gives 6.35 ms. The first C_T discharging cycle is from 1.35 V to 0.35 V, which gives 4.7 ms. Therefore, the total time is 6.35 ms + 33 × 4.7 ms = 161.45 ms. As a result, the retry mode duty ratio is 6.35 ms/161.45 ms = 3.93%. So effective steady state power dissipation in device during continuos short conditions is 4% of P_{LIM}.

10.2.2.1.5 STEP 5. Select R_1, R_2, and R_3 for UV and OV

Next, select the values of the OV and UV resistors, R_1, R_2, and R_3, as shown in the typical system application diagram Figure 41 . From the TPS2475x electrical specifications, $V_{OVTHRESH}$ = 1.35 V and $V_{ENTHRESH}$ = 1.35 V. V_{OV} is the overvoltage trip voltage, which in this case is 14 V. V_{UV} is the undervoltage trip voltage, which for this example equals 8.4 V.

$$V_{OVTHRESH} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{OV} \tag{12}$$

$$V_{ENTHRESH} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{UV} \tag{13}$$

Assume R_3 is 1.5 kΩ and use Equation 12 to solve for (R_1 + R_2). Use Equation 13 and the (R_1 + R_2) from Equation 12 to solve for R_2 and finally for R_1. From Equation 12, (R_1 + R_2) = 14.05 kΩ. From Equation 13, R_2 = 1 kΩ and R_1 = 13.05 kΩ. Scaling all three resistors by a factor of ten to use less supply current for these voltage references and using standard 1% resistor values gives R_1 = 130 kΩ, R_2 = 10 kΩ, and R_3 = 15 kΩ.

10.2.2.1.6 STEP 6. Choose R_4, R_5, and C_1

As per the typical application diagram on the front page, R_4, and R_5 are required only if PGb, and FLTb are used; these resistors serve as pull-ups for the open-drain output drivers. The current sunk by each of these pins must not exceed 2 mA (refer to the *Recommended Operating Conditions* table). C_1 is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise while in the disabled state. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended.

10.2.2.2 Alternative Design Example: Gate Capacitor (dv/dt) Control in Inrush Mode

The TPS2475x can be used in applications that expect a constant inrush current. This current is controlled by a capacitor connected from the GATE terminal to GND. A resistor of 1 kΩ placed in series with this capacitor prevents it from slowing a fast-turnoff event. In this mode of operation, the internal FET operates as a source follower, and the slew rate of the output voltage approximately equals the slew rate of the gate voltage (see Figure 43).

To implement a constant-inrush-current circuit, choose the time to charge, Δt, using Equation 14.

$$\Delta t = \frac{C_{OUT} \times V_{VCC}}{I_{CHG}} \tag{14}$$

where C_{OUT} is the output capacitance, V_{VCC} is the input voltage, and I_{CHG} is the desired charge current. Choose $I_{CHG} < P_{LIM} / V_{VCC}$ to prevent power limiting from affecting the desired current.

To select the gate capacitance use Equation 15. where, I_{GATE} is the nominal gate current and C_{INTRS}, the effective capacitance contributed by the internal FET (approximately 175 pF). In addition, the effect of other capacitances like the capacitance offered by the usage of the Blocking FET (C_{BLK}) and other component capacitances C_{PR} (due to external gate protection diodes, such as Zener diode and board parasitic) to be accounted for arriving at exact value of C_{GATE}. The TIMER capacitor, C_T, must be programmed for timing greater than the total turnon time (t_{ON}), to ensure and avoid fault detection during start-up.

Typical application circuit with Gate Capacitor (dV/dt) Control Inrush Mode is shown in Figure 43. The turnon waveform with C_{GATE} of 4.7 nF and series resistor of 1 kΩ is shown in Figure 44.

$$C_{GATE} = \left(I_{GATE} \times \frac{\Delta t}{V_{VCC}} \right) - C_{INTRS} \tag{15}$$

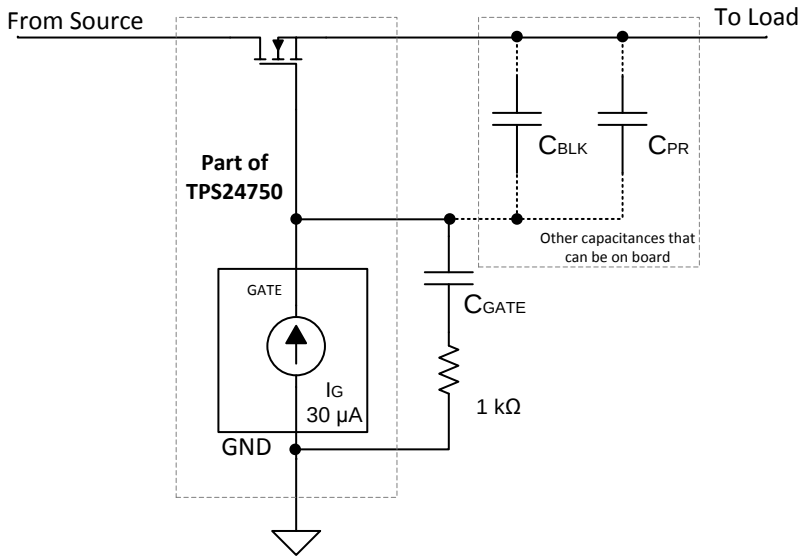


Figure 43. Gate Capacitor (dV/dt) Control Inrush Mode.

10.2.2.3 Additional Design Considerations

10.2.2.3.1 Use of PGb

Use the PGb pin to control and coordinate a downstream dc/dc converter. If this is not done, then a long time delay is needed to allow C_{OUT} to fully charge before the converter starts. An undesirable latch-up condition can be created between the TPS2475x output characteristic and the dc/dc converter input characteristic if the converter starts while C_{OUT} is still charging; using the PGb pin is one way to avoid this.

10.2.2.3.2 Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during a current-limit event. The OUT pin ratings can be satisfied by connecting a diode from OUT to GND. The diode must be selected to control the negative voltage at the full short-circuit current. Schottky diodes are generally recommended for this application.

10.2.2.3.3 Gate Clamp Diode

The TPS2475x has a relatively well-regulated gate voltage of 12 V-15.5 V with a supply voltage V_{VCC} higher than 4 V. For the applications with operating voltage greater than 14 V, a negative gate clamp (of ≤15.5 V) is needed as shown in Figure 47. In addition, a series resistance of several hundred ohms or a series silicon diode is recommended to prevent the output capacitance from discharging through the gate driver to ground. For applications with Blocking FET, a small clamp Zener from gate to OUT is recommended if V_{GS} of external blocking FET is rated below 12 V.

10.2.2.3.4 Bypass Capacitors

It is a good practice to provide low-impedance ceramic capacitor bypassing of the VCC and OUT pins. Values in the range of 10 nF to 1 µF are recommended. Some system topologies are insensitive to the values of these capacitors; however, some are not and require minimization of the value of the bypass capacitor. Input capacitance on a plug-in board may cause a large inrush current as the capacitor charges through the low-impedance power bus when inserted. This stresses the connector contacts and causes a short voltage sag on the input bus. Small amounts of capacitance (that is, 10 nF to 0.1 µF) are often tolerable in these systems.

10.2.2.3.5 Output Short-Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

10.2.3 Application Curves

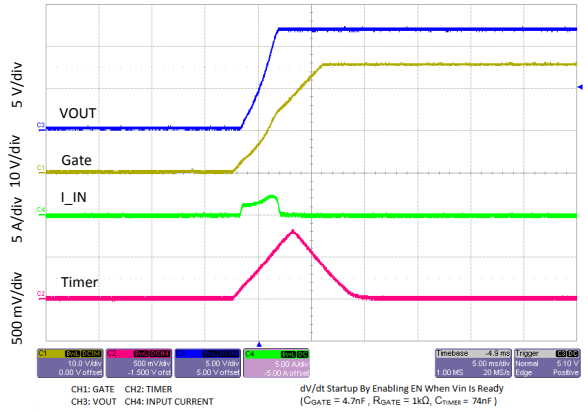


Figure 44. Turnon with Gate Capacitor (dv/dt) Control

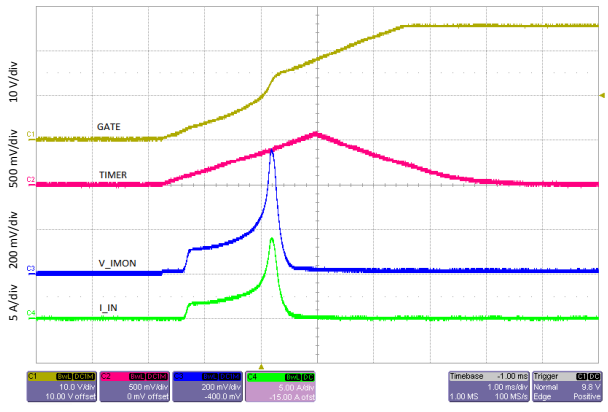


Figure 45. Inrush Mode at Hot-Swap Circuit Insertion

10.3 System Examples

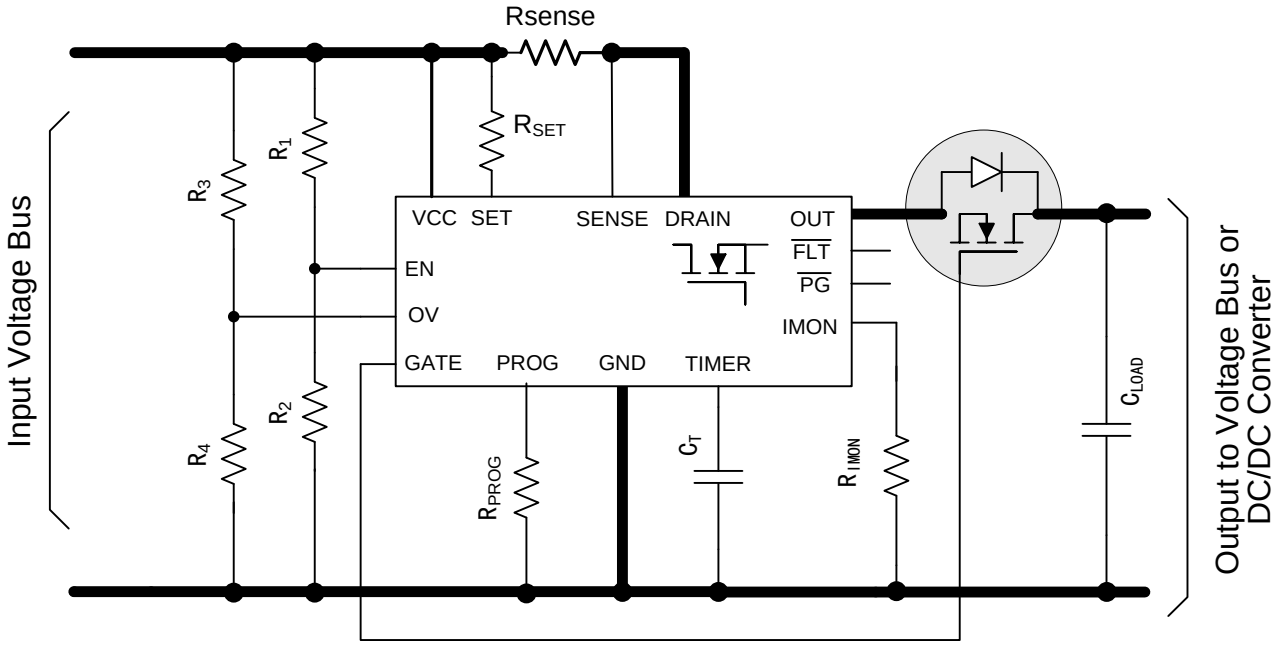


Figure 46. Reverse Blocking Implementation

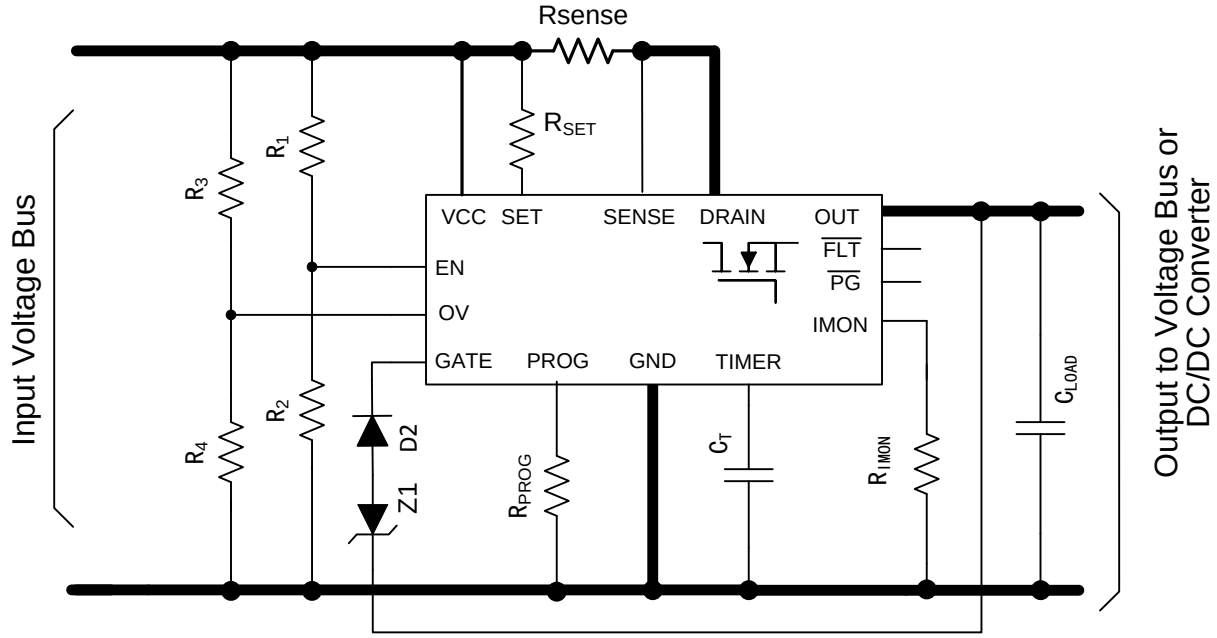


Figure 47. Negative Voltage Gate Protection

System Examples (continued)

The TPS2475x can be configured as a high current load switch with low external part count. The schematic diagram of load switch configuration is shown in Figure 48. The output voltage ramp rate is controlled with RC circuit (R_{gate} and C_{gate}) at the Gate pin of the device. For detailed design process refer to the application note *12-A Integrated Load Switch Using TPS24750/51*.

Due to their robust protection features along with low $R_{DS(on)}$ of 3 mΩ integrated MOSFET and precise current-limiting, the TPS2475x eFuses finds usage in power supply modules for Position Encoder Interfaces in applications such as Servo Drives and Position Control. Refer to the following TI Designs for system usage examples of the TPS2475x in these applications.

Power Supply with Programmable Output Voltage and Protection for Position Encoder Interfaces

Interface to a 5-V BiSS® Position Encoder

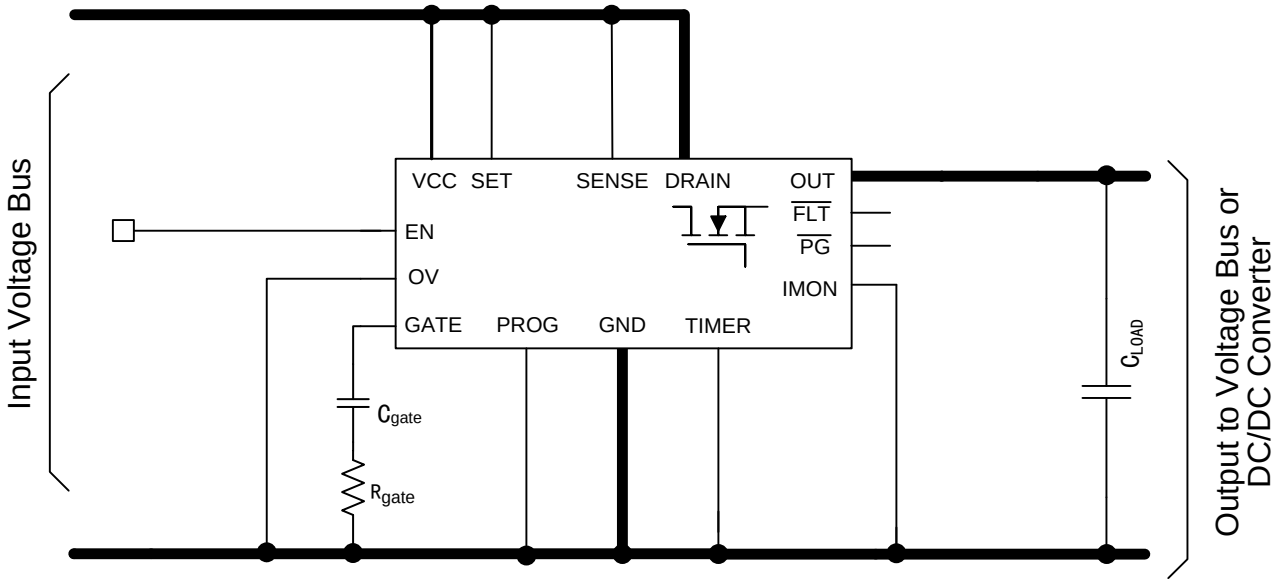


Figure 48. TPS2475x Configured as Simple 12-A Load Switch

11 Power Supply Recommendations

The device is designed for supply voltage range of 2.5 V ≤ $V_{(VCC)}$ ≤ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

11.1 Transient Thermal Impedance

T_A = 25°C (unless otherwise stated)

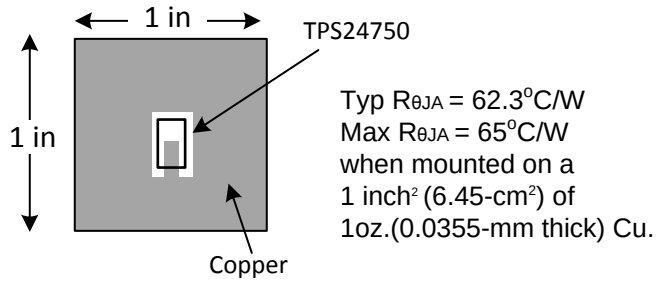


Figure 49. Board Details - Thermal Impedance Characteristic

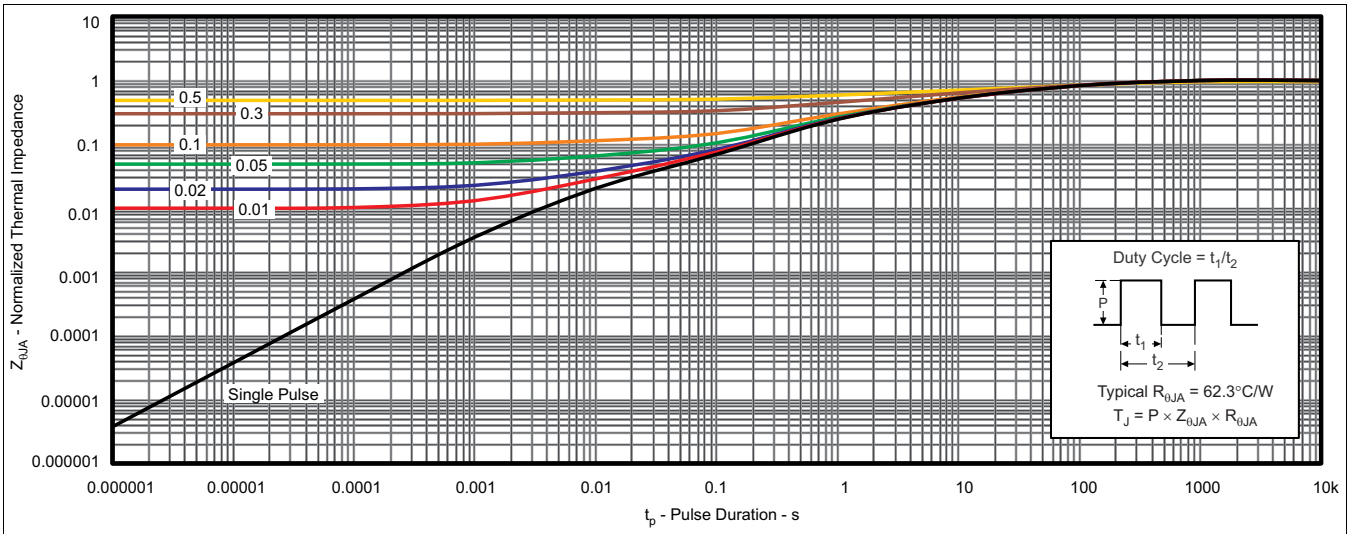


Figure 50. Transient Thermal Impedance with Test Board Details as Shown in Figure 49

12 Layout

12.1 Layout Guidelines

The TPS2475x applications require careful attention to layout to ensure proper performance and to minimize susceptibility to transients and noise. In general, all traces must be as short as possible, but the following list deserves first consideration:

- Decoupling capacitors on VCC pin must have minimal trace lengths to the pin and to GND.
- Traces to SET and SENSE must be short and run side-by-side to maximize common-mode rejection. Kelvin connections must be used at the points of contact with R_{SENSE}. See Figure 51 and Figure 52 for a PCB layout example.
- SET runs must be short on both sides of R_{SET}.
- High current carrying Power path connections must be as short as possible and sized to carry at least twice the full-load current, more if possible.
- Connections to IMON pin must be minimized after the previously described connections have been placed.
- The reference must should be a copper plane or island. Use via holes if necessary for direct connections of components to their appropriate return ground plane or island.
- Thermal Considerations: When properly mounted the PowerPAD package provides significantly greater cooling ability than an ordinary package. To operate at rated power, PowerPAD-2 must be soldered directly to the PC board DRAIN plane directly under the device. The PowerPAD-2 is at the DRAIN potential and can be connected using multiple vias to the inner and bottom layers of the DRAIN. The bottom side of the circuit board is highly recommended to be used for DRAIN plane to increase heat sinking in higher current applications. Refer to Technical Briefs: PowerPAD™ Thermally Enhanced Package, SLMA002) and PowerPAD™ Made Easy, SLMA004) for more information on using this PowerPad package.
- The thermal via land pattern specific to the TPS2475x can be downloaded from the device webpage.
- Protection devices such as snubbers, TVS, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, the protection Schottky diode suggested to address transients due to heavy inductive loads, must be physically close to the OUT pins.

12.2 Layout Example

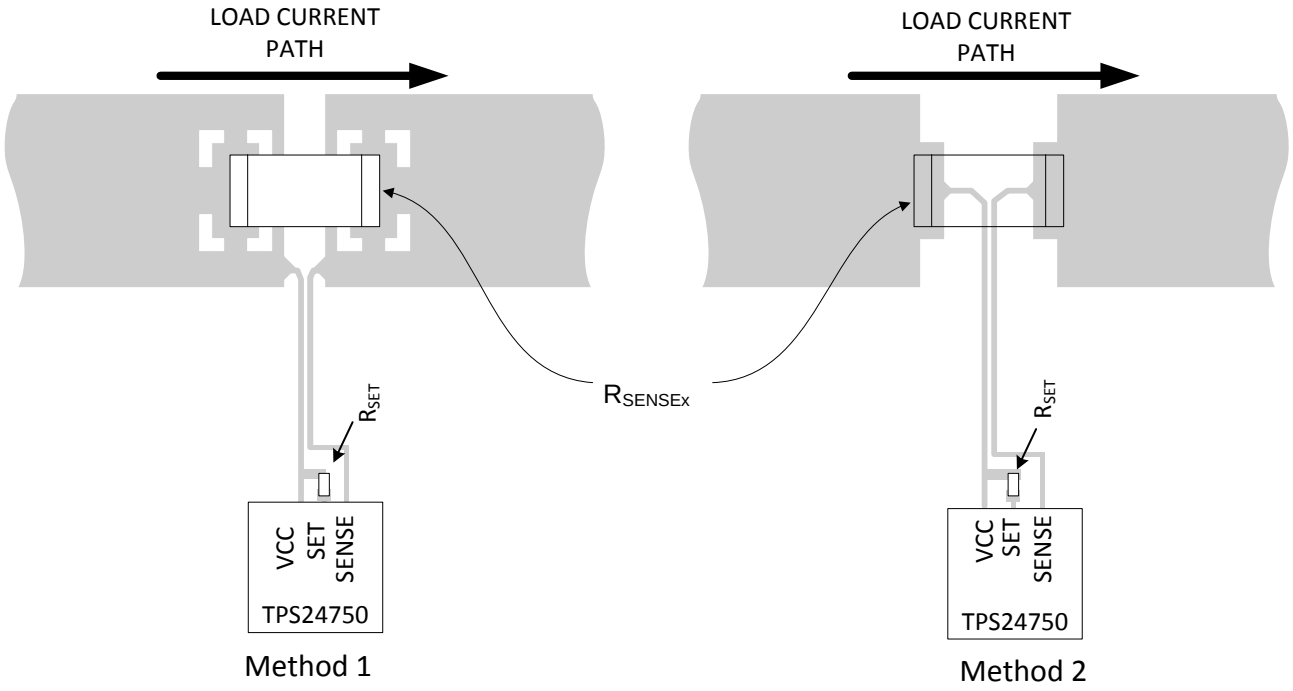
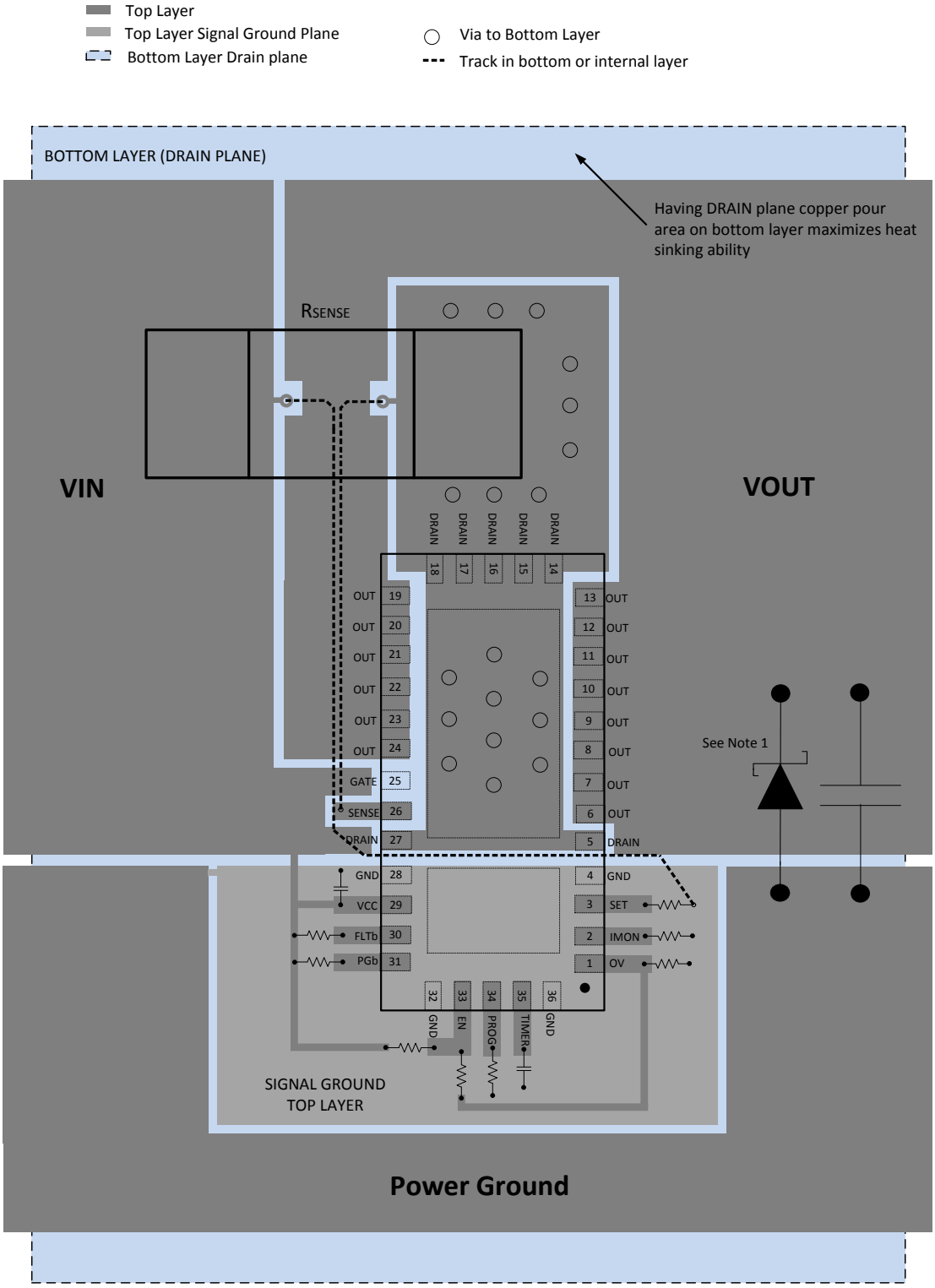


Figure 51. Recommended R_{SENSE} Layout

Layout Example (continued)



(1) Optional: Needed only to suppress the transients caused by inductive load switching.

Figure 52. Layout Example

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- *《PowerPAD™ 耐热增强型封装》（TI 文献编号 SLMA002）*
- 《PowerPAD™ 速成》
- *《适用于位置编码器接口且具有可编程输出电压和保护功能的电源》*
- *《5V BiSS® 位置编码器接口》*
- *《采用 TPS24750/51 的 12A 集成负载开关》*
- *《TPS2475X EVM 用户指南》*

13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
TPS24750	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS24751	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

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13.8 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS24750RUVR	ACTIVE	VQFN	RUV	36	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS24750	Samples
TPS24750RUVT	ACTIVE	VQFN	RUV	36	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS24750	Samples
TPS24751RUVR	ACTIVE	VQFN	RUV	36	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS24751	Samples
TPS24751RUVT	ACTIVE	VQFN	RUV	36	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS24751	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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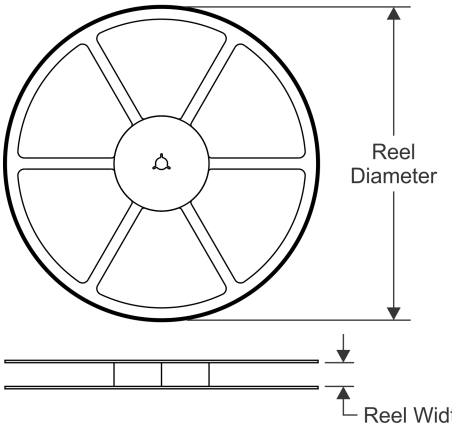
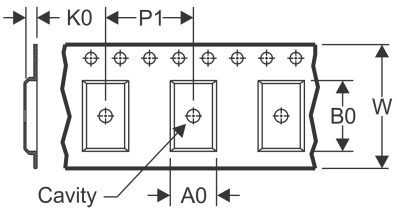
TAPE AND REEL INFORMATION

REEL DIMENSIONS

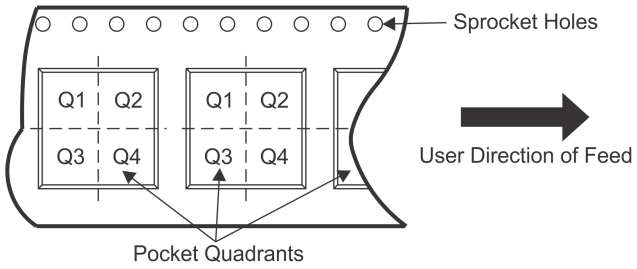


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

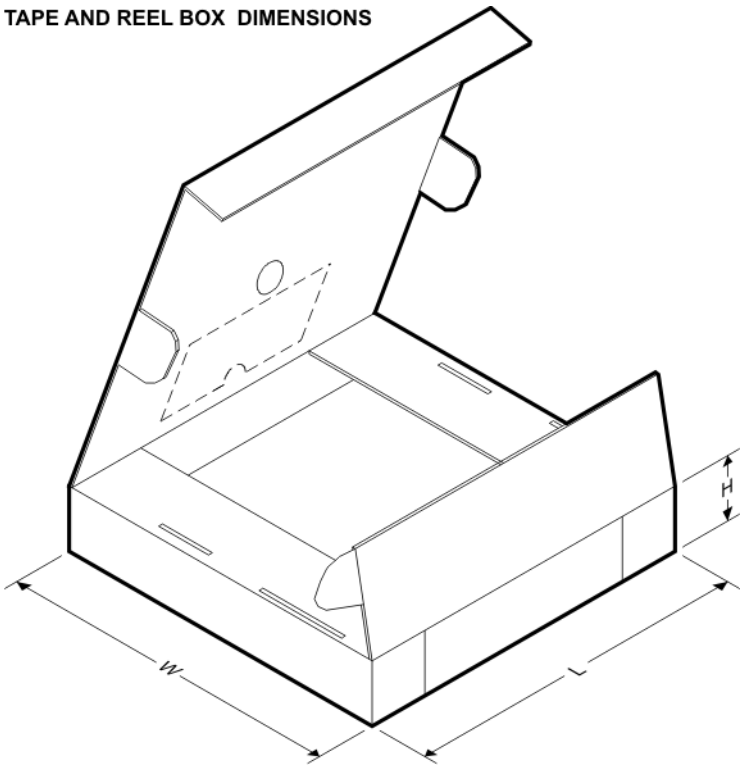
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS24750RUVR	VQFN	RUV	36	3000	330.0	16.4	3.85	7.35	1.2	8.0	16.0	Q1
TPS24750RUVT	VQFN	RUV	36	250	180.0	16.4	3.85	7.35	1.2	8.0	16.0	Q1
TPS24751RUVR	VQFN	RUV	36	3000	330.0	16.4	3.85	7.35	1.2	8.0	16.0	Q1
TPS24751RUVT	VQFN	RUV	36	250	180.0	16.4	3.85	7.35	1.2	8.0	16.0	Q1

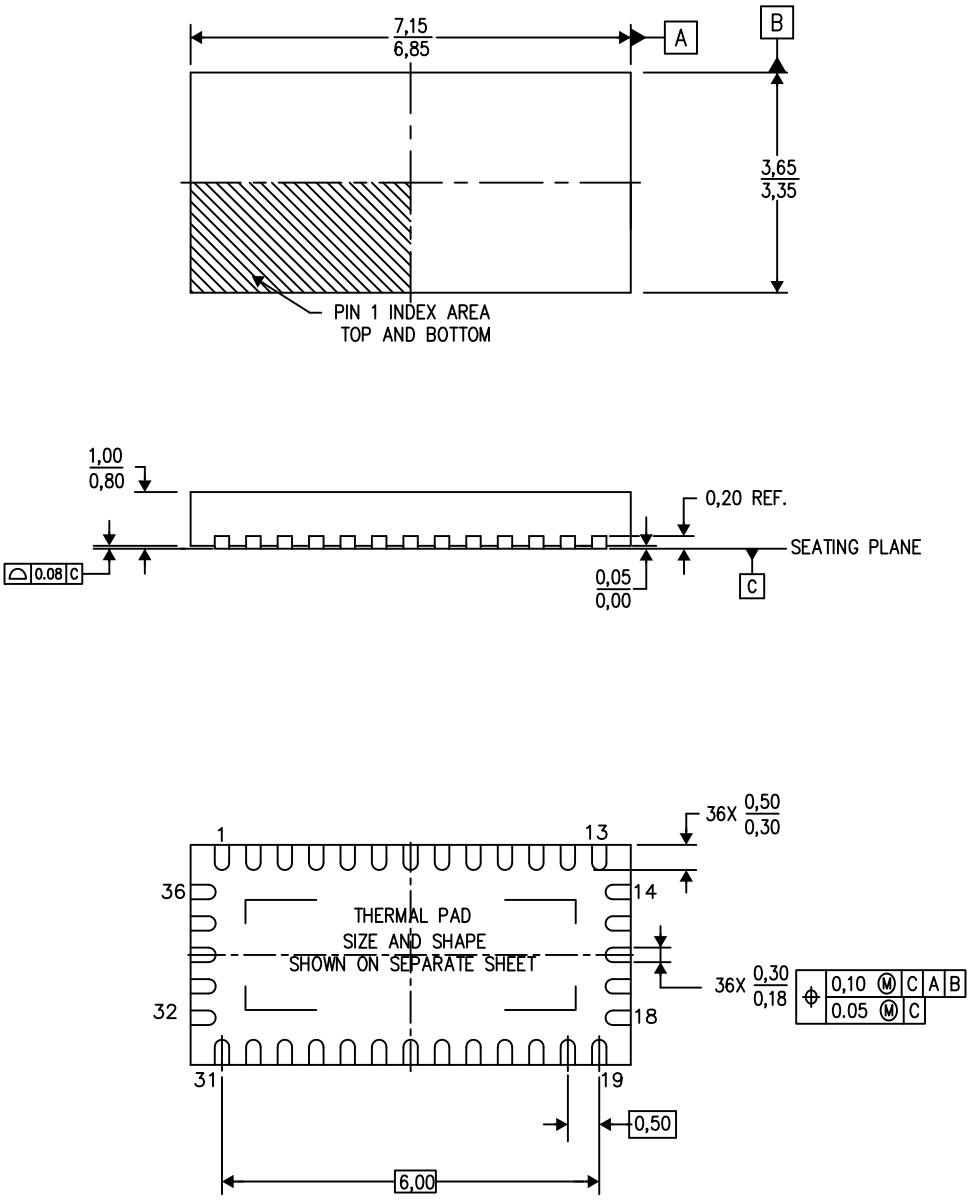
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS24750RUVR	VQFN	RUV	36	3000	367.0	367.0	38.0
TPS24750RUVT	VQFN	RUV	36	250	210.0	185.0	35.0
TPS24751RUVR	VQFN	RUV	36	3000	367.0	367.0	38.0
TPS24751RUVT	VQFN	RUV	36	250	210.0	185.0	35.0

RUV (R–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

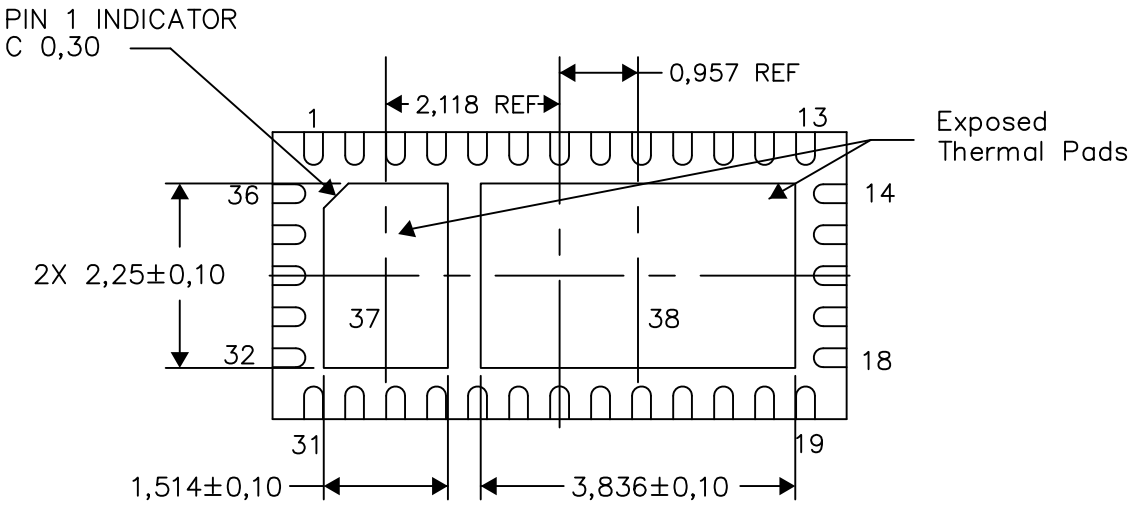
RUV (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



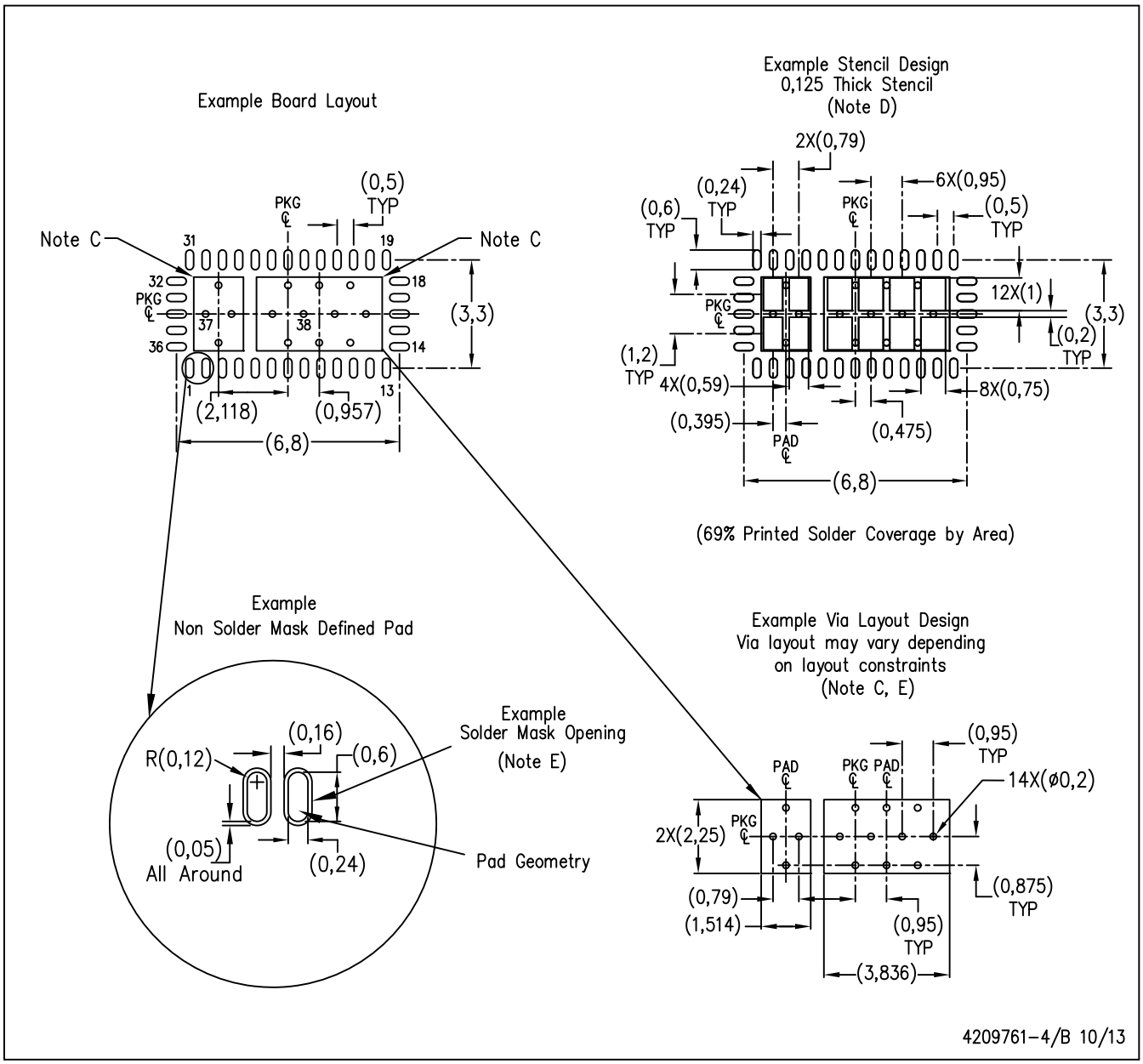
Bottom View

Exposed Thermal Pad Dimensions

4209552–4/E 06/13

NOTE: All linear dimensions are in millimeters

RUV (R–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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