HD3SS213 5.4Gbps DisplayPort 1.2a 2:1 和 1:2 差动开关

1 特性

- 符合 DisplayPort 1.2 电气标准
- 2:1 和 1:2 切换最高支持 5.4Gbps 的数据速率
- 支持 HPD 切换
- 支持 AUX 和 DDC 切换
- –3dB 差动带宽宽达 5.4GHz 以上
- 出色的动态特性（2.7GHz 时）：
  - 串扰 = -50dB
  - 隔离 = -25dB
  - 插入损耗 = -1.5dB
  - 回损 = -13dB
  - 最大位间偏差 = 5ps
- V_{DD} 工作范围：3.3V±10%
- 封装选项：
  - 5mm × 5mm，50 引脚 nFBGA
- 输出使能 (OE) 引脚禁用开关以省电
- HD3SS213 < 10mW（待机功耗 < 30µW 此时，OE = L）

2 应用

- PC 和笔记本电脑
- 平板电脑
- 联网外设和打印机

3 说明

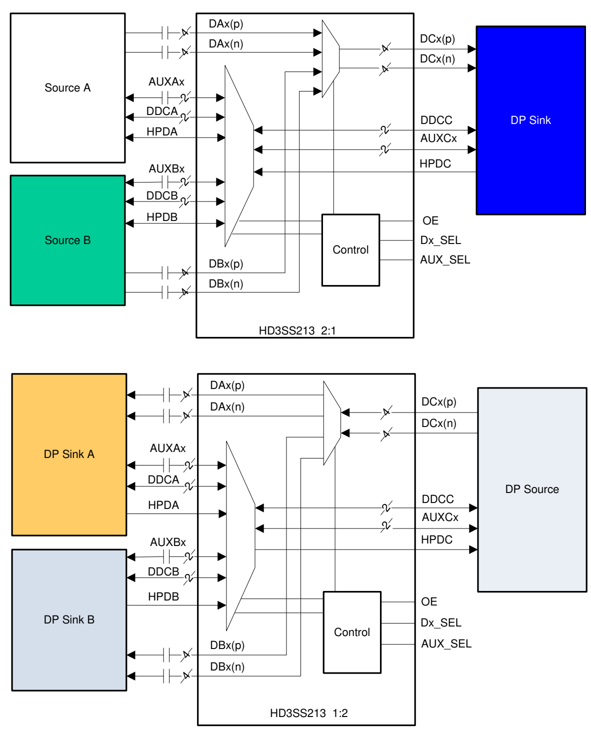
HD3SS213 器件是一款高速无源开关，能够在一个应用中将两个完整 DisplayPort 4 通道端口从两个源之一切换到一个目标位置。它还将一个源切换到两个接收器之一。对于 DisplayPort 应用，HD3SS213 支持 ZEQ 封装中辅助 (AUX)、显示数据通道 (DDC) 和热插拔检测 (HPD) 信号的切换。

一个典型应用是主板，该主板包含两个需要驱动一个 DisplayPort 接收器的 GPU。GPU 由 Dx_SEL 引脚选择。另一个应用是一个源需要在两个接收器之间切换，例如一个侧面连接器和一个扩展坞连接器。此切换操作由 Dx_SEL 和 AUX_SEL 引脚控制。HD3SS213 在 -40°C 至 105°C 的完全工业温度范围内由一个电压为 3.3 V 的单电源供电运行。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
HD3SS213	nFBGA (50)	5.00mm x 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。



HD3SS213 应用方框图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (December 2016) to Revision C (January 2021)	Page
• 注：采用 MicroStar Jr. BGA 封装的器件采用层压 nFBGA 封装进行了重新设计。这种 nFBGA 封装提供了类似于数据表中的电气性能。该封装占用空间也类似于 MicroStar Jr. BGA。将在整个数据表中更新全新封装标识符来代替已停止使用的封装标识符。	1
• 将 u*jr BGA 更改为 nFBGA	1
• Changed ZQE to ZXH	3
• Changed u*jr ZQE to nFBGA ZXH. Updated thermal data	6
• Changed u*jr BGA to nFBGA	10

Changes from Revision A (September 2013) to Revision B (December 2016)	Page
• 添加了*器件信息*表、*ESD 等级*表、*特性说明*部分、*器件功能模式*部分、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分	1
• Added A2 to J4 row in *Pin Functions* table	3

Changes from Revision * (September 2013) to Revision A (September 2013)	Page
• Deleted Ordering Information	3

5 Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9
A	Dx_SEL	VDD		DA0(n)	DA1(n)	DA2(n)		DA3(p)	DA3(n)
B	DC0(n)	DC0(p)	GND	DA0(p)	DA1(p)	DA2(p)	OE	DB0(p)	DB0(n)
C		AUX_SEL						GND	
D	DC1(n)	DC1(p)						DB1(p)	DB1(n)
E	DC2(n)	DC2(p)						DB2(p)	DB2(n)
F	DC3(n)	DC3(p)						DB3(p)	DB3(n)
G		GND						GND	
H	AUXC(n)	AUXC(p)	HPDB	GND	DDCCLK_B	AUXB(p)	GND	DDCCLK_A	AUXA(p)
J	HPDC	HPDA	DDCCLK_C	VDD	DDCDAT_B	AUXB(n)	DDCDAT_C	DDCDAT_A	AUXA(n)

nFBGA 50-Pin ZXH Package Top View

表 5-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION[(2)]
NO.	NAME		
H9, J9	AUXA(p), AUXA(n)	I/O	Port A AUX positive signal Port A AUX negative signal
H6, J6	AUXB(p), AUXB(n)	I/O	Port B AUX positive signal Port B AUX negative signal
H2, H1	AUXC(p), AUXC(n)	I/O	Port C AUX positive signal Port C AUX negative signal
C2	AUX_SEL	I	AUX/DDC selection control pin in conjunction with Dx_SEL Pin

表 5-1. Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION(2)
NO.	NAME		
NA	CADA/B/C	I/O	Port A/B/C cable activity detect
B4, A4	DA0(p), DA0(n)	I/O	Port A, Channel 0, High speed positive signal Port A, Channel 0, High speed negative signal
B5, A5	DA1(p), DA1(n)	I/O	Port A, Channel 1, High speed positive signal Port A, Channel 1, High speed negative signal
B6, A6	DA2(p), DA2(n)	I/O	Port A, Channel 2, High speed positive signal Port A, Channel 2, High speed negative signal
A8, A9	DA3(p), DA3(n)	I/O	Port A, Channel 3, High speed positive signal Port A, Channel 3, High speed negative signal
B8, B9	DB0(p), DB0(n)	I/O	Port B, Channel 0, High speed positive signal Port B, Channel 0, High speed negative signal
D8, D9	DB1(p), DB1(n)	I/O	Port B, Channel 1, High speed positive signal Port B, Channel 1, High speed negative signal
E8, E9	DB2(p), DB2(n)	I/O	Port B, Channel 2, High speed positive signal Port B, Channel 2, High speed negative signal
F8, F9	DB3(p), DB3(n)	I/O	Port B, Channel 3, High speed positive signal Port B, Channel 3, High speed negative signal
B2, B1	DC0(p), DC0(n)	I/O	Port C, Channel 0, High speed positive signal Port C, Channel 0, High speed negative signal
D2, D1	DC1(p), DC1(n)	I/O	Port C, Channel 1, High speed positive signal Port C, Channel 1, High speed negative signal
E2, E1	DC2(p), DC2(n)	I/O	Port C, Channel 2, High speed positive signal Port C, Channel 2, High speed negative signal
F2, F1	DC3(p), DC3(n)	I/O	Port C, Channel 3, High speed positive signal Port C, Channel 3, High speed negative signal
H8, J8	DDCCLK_A, DDCDAT_A	I/O	Port A DDC clock signal Port A DDC data signal
H5, J5	DDCCLK_B, DDCDAT_B	I/O	Port B DDC clock signal Port B DDC data signal
J3, J7	DDCCLK_C, DDCDAT_C	I/O	Port C DDC clock signal Port C DDC data signal
A1	Dx_SEL	I	High speed port selection control pins
B3, C8, G2, G8, H4, H7	GND	S	Ground
J2	HPDA	I/O	Port A hot plug detect
H3	HPDB	I/O	Port B hot plug detect
J1	HPDC	I/O	Port C hot plug detect
B7	OE	I	Output enable: OE = V_{IH}: Normal operation OE = V_{IL}: Standby mode
A2, J4	VDD	S	3.3-V positive power supply voltage

(1) I = Input, O = Output, S = Supply
(2) The high speed data ports incorporate 20-kΩ pulldown resistors that are switched in when a port is not selected and switched out when the port is selected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

		MIN	MAX	UNIT
Supply voltage, V_{DD} [2]		–0.5	4	V
Voltage	Differential I/O	–0.5	4	V
	Control pin	–0.5	V_{DD} + 0.5	
Continuous power dissipation		See 节 6.4		
Operating free-air temperature, T_A		–40	105	°C
Storage temperature, T_{stg}			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted). All temperature limits are specified by design.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		3	3.3	3.6	V
V_{IH}	Input high voltage	Control pins and signal pins (Dx_SEL, AUX_SEL, OE, HPDx)	2		V_{DD}	V
V_{IM}	Input mid level voltage	AUX_SEL pin	$V_{DD}/2$ – 300 mV	$V_{DD}/2$	$V_{DD}/2$ + 300 mV	V
V_{IL}	Input low voltage	Control pins and signal pins (Dx_SEL, AUX_SEL, OE, HPDx)	–0.1		0.8	V
V_{I/O_Diff}	Differential voltage (Dx, AUXx)	Switch I/O differential voltage	0		1.8	V_{PP}
V_{I/O_CM}	Dx switching I/O common-mode voltage	Switch I/O common-mode voltage	0		2	V
	AUXx switching I/O common-mode voltage	Switch I/O common-mode voltage	0		3.6	V
I_{IH}	Input high current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = V_{DD}			1	µA
I_{IM}	Input mid level current (AUX_SEL)	V_{DD} = 3.6V, V_{IN} = $V_{DD}/2$			1	µA
I_{IL}	Input low current (Dx_SEL, AUX_SEL)	V_{DD} = 3.6 V, V_{IN} = GND			1	µA
I_{LK}	Leakage current (Dx_SEL, AUX_SEL)	V_{DD} = 3.3 V, V_I = 2 V, OE = 3.3 V			1	µA
	Leakage current (HPDx)	V_{DD} = 3.3 V, V_I = 2 V, OE = 3.3 V, Dx_SEL = 3.3 V			1	µA
		V_{DD} = 3.3 V, V_I = 2 V, OE = 3.3 V, Dx_SEL = GND			1	

Typical values for all parameters are at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted). All temperature limits are specified by design.

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{off}	Device shut down current	V_{DD} = 3.6 V, OE = GND			2.5	µA
I_{DD}	Supply current	V_{DD} = 3.6 V, Dx_SEL or AUX_SEL = V_{DD} or GND		0.6	1	mA
DA, DB, DC HIGH SPEED SIGNAL PATH						
C_{ON}	Outputs ON capacitance	V_I = 0 V, outputs open, switch ON		1.5		pF
C_{OFF}	Outputs OFF capacitance	V_I = 0 V, outputs open, switch OFF		1		pF
R_{ON}	ON resistance	V_{DD} = 3.3 V, VCM = 0.5 V to 1.5 V, I_O = –40 mA		8	12	Ω
ΔR_{ON}	ON resistance match between pairs of the same channel	V_{DD} = 3.3 V, 0.5 V ≤ V_I ≤ 1.2V, I_O = –40 mA			1.5	Ω
R_{FLAT_ON}	ON resistance flatness, $R_{ON(max)} - R_{ON(min)}$	V_{DD} = 3.3 V, 0.5 V ≤ V_I ≤ 1.2 V		1.3		Ω
AUXx, DDC SIGNAL PATH						
C_{ON}	Outputs ON capacitance	V_I = 0 V, outputs open, switch ON		9		pF
C_{OFF}	Outputs OFF capacitance	V_I = 0 V, outputs open, switch OFF		3		pF
$R_{ON(AUX)}$	ON resistance	V_{DD} = 3.3 V, V_{CM} = 0 V – V_{DD}, I_O = –8 mA		6	10	Ω
$R_{ON(DDC)}$	ON resistance on DDC channel	V_{DD} = 3.3 V, V_{CM} = 0.4 V, I_O = –3 mA		20	30	Ω

6.4 Thermal Information

THERMAL METRIC		HD3SS213 nFBGA (ZXH) 50 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	72.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

6.5 Electrical Characteristics

over recommended operating conditions; R_L and R_{SC} = 50 Ω (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_L	Dx differential return loss	1.35 GHz		–17		dB
		2.7 GHz		–13		
X_{TALK}	Dx differential crosstalk	2.7 GHz		–50		dB
O_{IRR}	Dx differential off-isolation	2.7 GHz		–25		dB
I_L	Dx differential insertion loss	f = 1.35 GHz		–1		dB
		f = 2.7 GHz		–1.5		
	AUX –3-dB bandwidth			360		MHz

(1) For return loss, crosstalk, off-isolation, and insertion loss values, the data was collected on a Rogers material board with minimum length traces on the input and output of the device under test.

6.6 Timing Requirements

over recommended operating conditions; R_L and R_{SC} = 50 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PD}	Switch propagation delay	R_{SC} and R_L = 50 Ω, see 图 6-2			100	ps
T_{on}	Dx_SEL/AUX_SEL-to-switch Ton (Data, AUX and DDC)	R_{SC} and R_L = 50 Ω, see 图 6-1		0.7	1	µs
T_{off}	Dx_SEL/AUX_SEL-to-switch Toff (Data, AUX and DDC)	R_{SC} and R_L = 50 Ω, see 图 6-1		0.7	1	µs
T_{on}	Dx_SEL/AUX_SEL-to-switch Ton (HPD)	R_L = 50 Ω, see 图 6-1		0.7	1	µs
T_{off}	Dx_SEL/AUX_SEL-to-switch Toff (HPD)	R_L = 50 Ω, see 图 6-1		0.7	1	µs
$T_{SK(O)}$	Inter-pair output skew (CH-CH)	R_{SC} and R_L = 1 kΩ, see 图 6-2			50	ps
$T_{SK(b-b)}$	Intra-pair output skew (bit-bit)	R_{SC} and R_L = 1 kΩ, see 图 6-2		1	5	ps

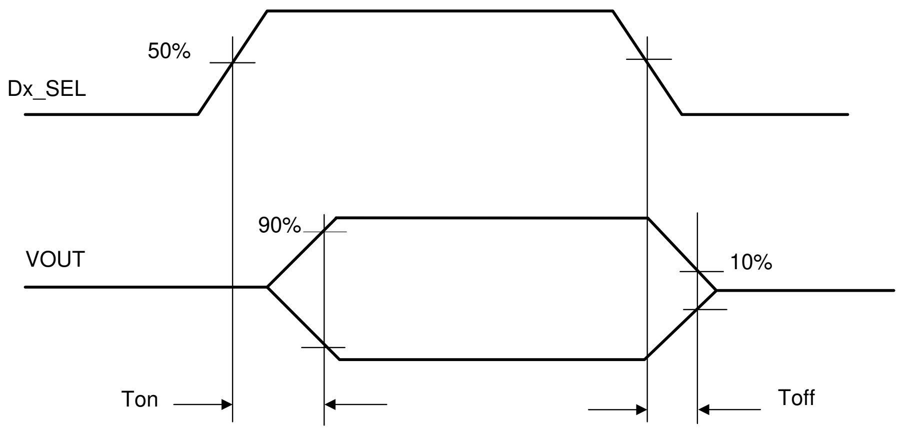


图 6-1. Select to Switch Ton and Toff

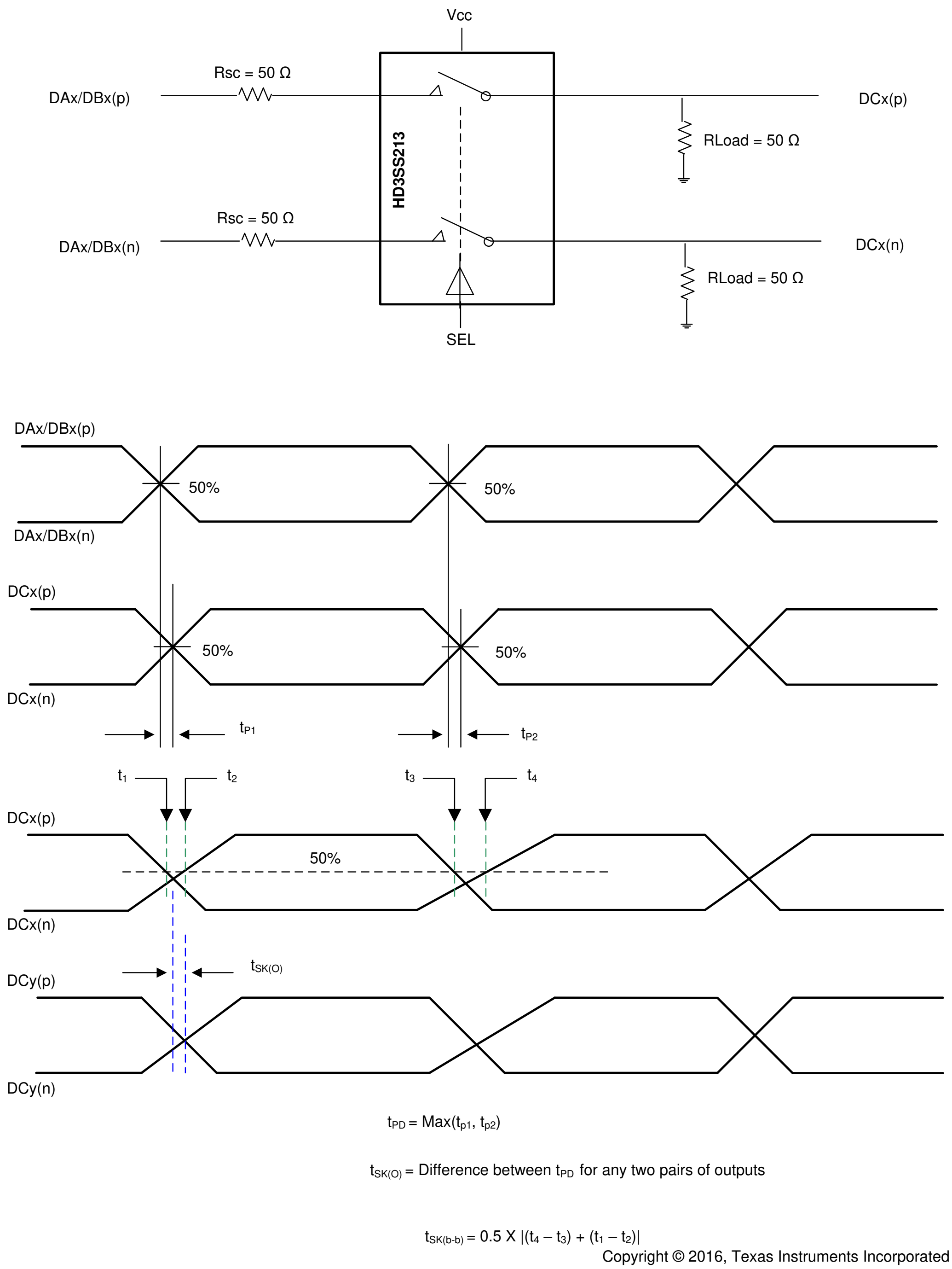


图 6-2. Propagation Delay and Skew

6.7 Typical Characteristics

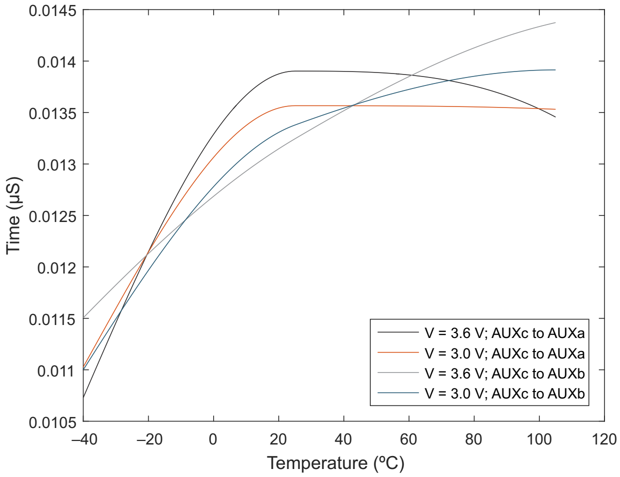


图 6-3. DxSEL to Switch Toff

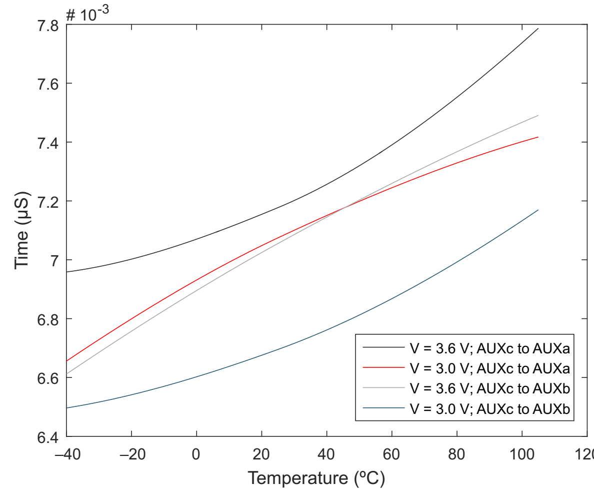


图 6-4. DxSEL to Switch Ton

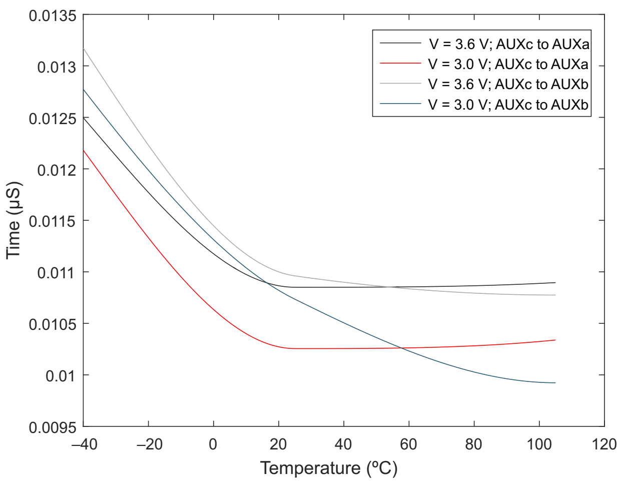


图 6-5. OUTEN to Switch Toff

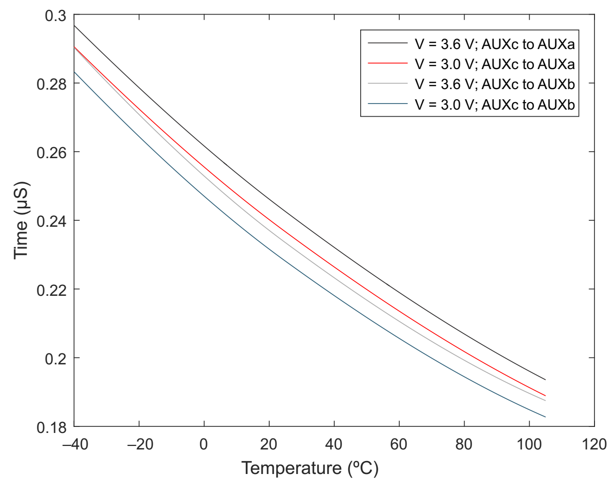


图 6-6. OUTEN to Switch Ton

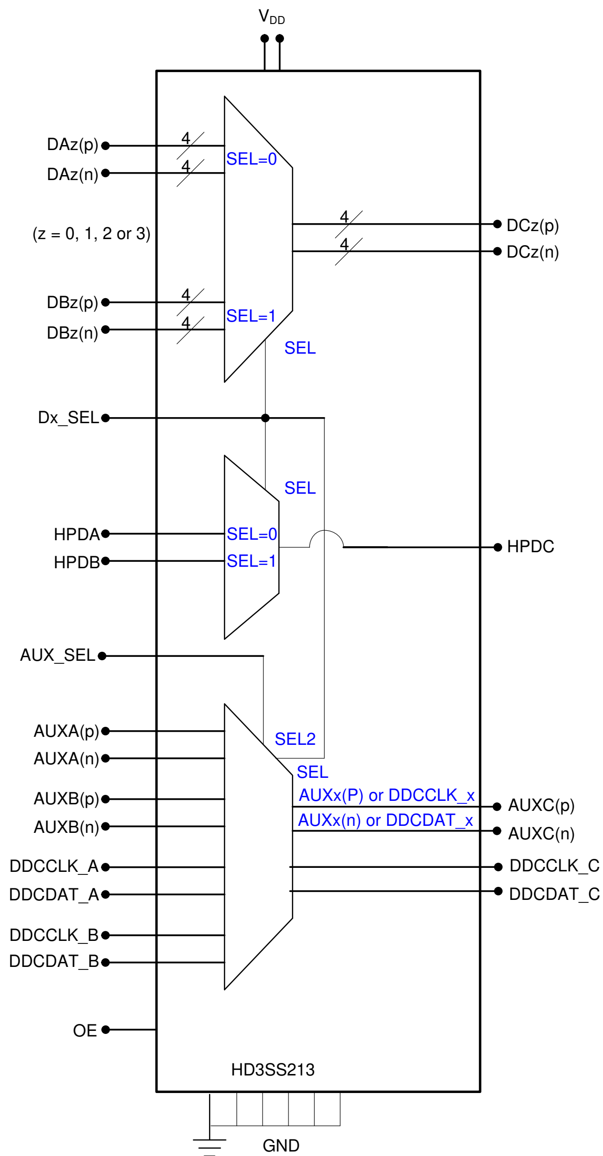
7 Detailed Description

7.1 Overview

The HD3SS213 device is a high-speed passive switch offered in an industry standard 50-pin nFBGA package. The device is specified to operate from a single supply voltage of 3.3 V over the industrial temperature range of –40°C to 105°C. The HD3SS213 is a generic 4-CH high-speed mux/demux type of switch that can be used for routing high-speed signals between two different locations on a circuit board. The HD3SS213 also supports several other high speed data protocols with a differential amplitude of < 1800 mV_{PP} and a common-mode voltage of < 2 V, as with USB 3.0 and DisplayPort 1.2. For display port applications, the HD3SS213 also supports switching of both the auxiliary and hot plug detect signals.

The high speed port selection control inputs of the device, Dx_SEL and AUX_SEL pins can easily be controlled by available GPIO pins within a system.

7.2 Functional Block Diagram



7.3 Feature Description

The HD3SS213 behaves as a two to one or one to two using high bandwidth pass gates (see 节 7.2). The input ports are selected using the AUX_SEL and Dx_SEL pins which are shown in 表 7-1.

表 7-1. AUX/DDC Switch Control Logic

CONTROL LINES		SWITCHED I/O PINS					
AUX_SEL	**Dx_SEL**	**AUXA**	**AUXB**	**AUXC**	**DDCA**	**DDCB**	**DDCC**
L	L	To/From AUXC	Z	To/From AUXA	Z	Z	Z
L	H	Z	To/From AUXC	To/From AUXB	Z	Z	Z
H	L	Z	Z	To/From DDCA	To/From AUXC	Z	Z
H	H	Z	Z	To/From DDCB	Z	To/From AUXC	Z
M	L	To/From AUXC	Z	To/From AUXA	To/From DDCC	Z	To/From DDCA
M	H	Z	To/From AUXC	To/From AUXB	Z	To/From DDCC	To/From DDCB

7.4 Device Functional Modes

The HD3SS213 can be operated in normal operation mode or in shut down mode. In normal operation, the inputs ports of the HD3SS213 are routed to the output ports according to 表 7-1. In standby mode, the HD3SS213 is disabled to enable power savings with a typical current consumption of 2.5 μA. The functional mode is selected through the OE input pin with HIGH for normal operation and LOW for standby.

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

Many interfaces require AC coupling between the source and sink. The 0402 capacitors are the preferred option to provide AC coupling, and the 0603 size capacitors also work. The 0805 size capacitors and C-packs must be avoided. When placing AC coupling capacitors symmetric placement is best. A capacitor value of 0.1 µF is best and the value must be match for the ± signal pair. There are several placement options for the AC coupling capacitors. Because the switch requires a bias voltage, the capacitors must only be placed on one side of the switch. If they are placed on both sides of the switch, a biasing voltage must be provided. A few placement options are shown below.

In 图 8-1, the coupling capacitors are placed on the source pair. In this situation, the switch is biased by the sink.

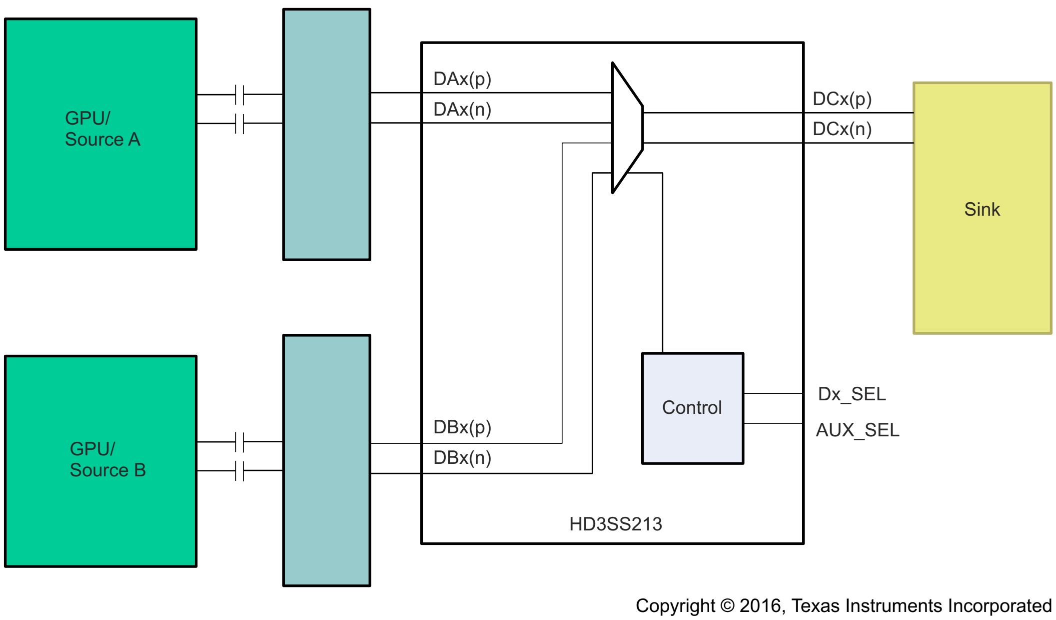


图 8-1. Source Biased by the Sink

In 图 8-2, the coupling capacitors are placed between the switch and Sink. In this situation, the switch is biased by the Source

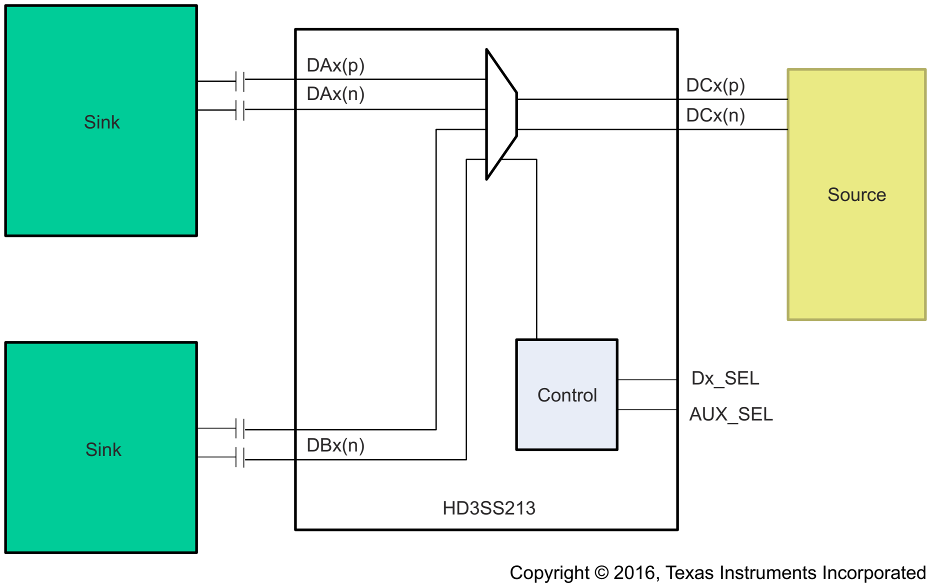


图 8-2. Switch Biased by the Source

8.2 Typical Applications

8.2.1 HD3SS213 AUX Channel in 2:1 Application

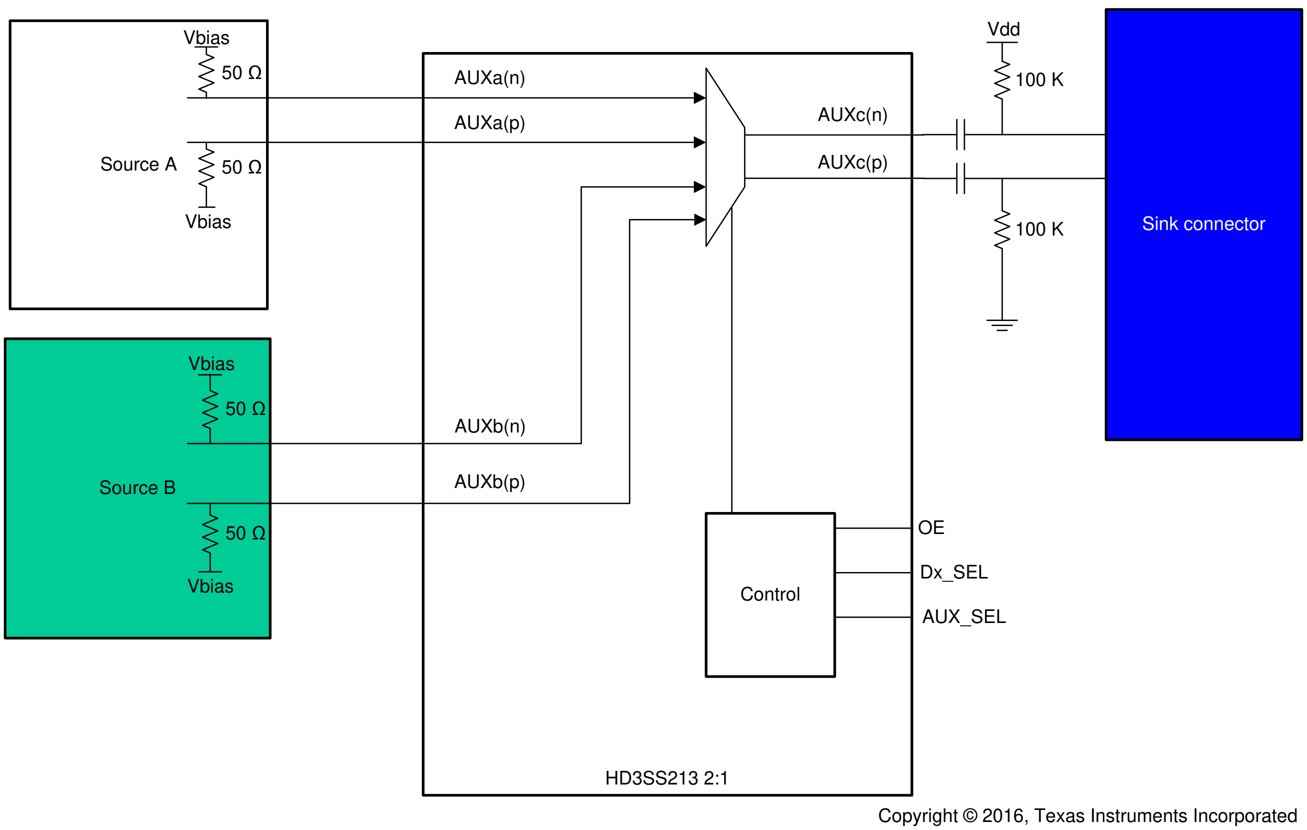


图 8-3. HD3SS213 AUX Channel in 2:1 Application Schematic

8.2.1.1 Design Requirements

表 8-1 lists the design parameters.

表 8-1. Design Parameters

PARAMETERS	VALUE
Input voltage	3.3 V
Decoupling capacitors	0.1 µF
AC capacitors(1)	75 nF to 200 nF AC capacitors

(1) DAx, AUXAx, AUXBx and DBx require AC capacitors. N lines require AC capacitors. Alternate mode signals may or may not require AC capacitors.

8.2.1.2 Detailed Design Procedure

- Connect VDD and GND pins to the power and ground planes of the printed-circuit board with 0.1-µF bypass capacitor
- Use VDD/2 logic level at AUX_SEL pin
- Use 3.3-V TTL/CMOS logic level at Dx_SEL to connect DAx to DCx
- Use GND logic level at Dx_SEL to connect DBx to DCx
- Use controlled-impedance transmission media for all the differential signals
- Ensure the received complimentary signals are with a differential amplitude of <1800 mV_{PP} and a common-mode voltage of <2 V

8.2.1.3 Application Curves

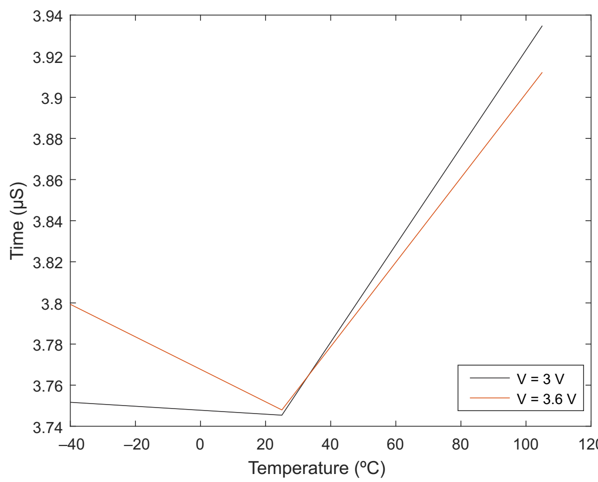


图 8-4. Intra-Pair Skew Ports C to A (µs)

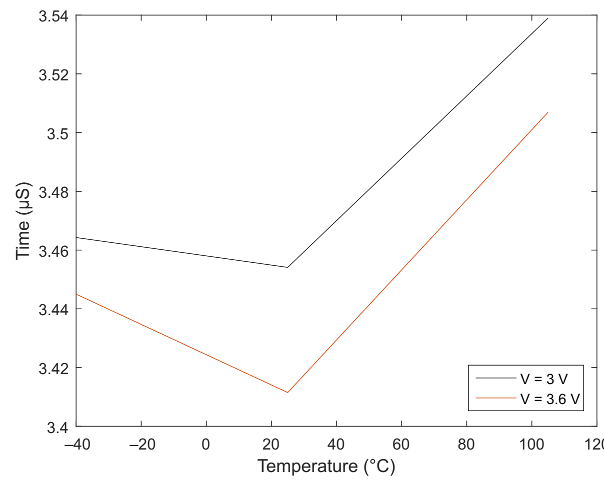


图 8-5. Intra-Pair Skew Ports C to B (µs)

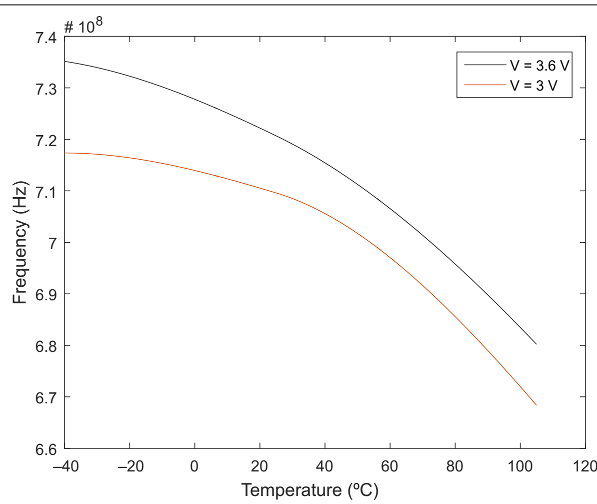


图 8-6. Bandwidth Ports AUXc to AUXa

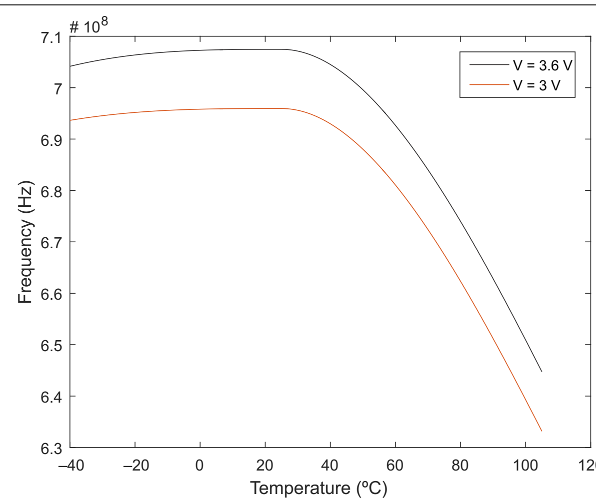


图 8-7. Bandwidth Ports AUXc to AUXb

8.2.2 HD3SS213 AUX Channel in 1:2 Application

AUX channel is controlled by AUX_SEL. This pin configures the switch to route the incoming AUX signal to the outgoing AUX path, when AUX_SEL = 0 the AUXA channel is routed to AUXC, when AUX_SEL = 1 the AUXB channel is routed to AUXC.

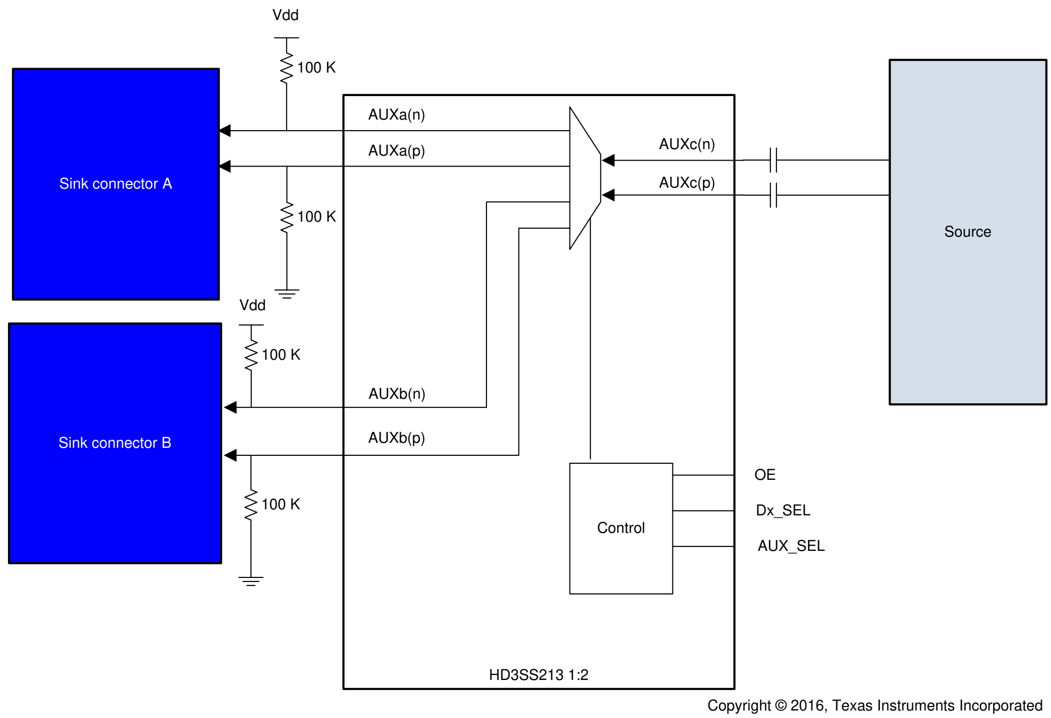


图 8-8. HD3SS213 AUX Channel in 1:2 Application Schematic

Power Supply Recommendations

The HD3SS213 requires 3.3 V power sources. 3.3-V supply (VDD) must have 0.1-µF bypass capacitors to VSS (ground) for proper operation. TI recommends one capacitor for each power terminal. Place the capacitor as close as possible to the terminal on the device and keep trace length to a minimum. Smaller value capacitors like 0.01 µF are also recommended on the supply terminals.

9 Layout

9.1 Layout Guidelines

- Routing the high-speed differential signal traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the DisplayPort connectors to the repeater inputs and from the repeater output to the subsequent receiver circuit.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Decoupling capacitors must be placed next to each power terminal on the HD3SS213. Take care to minimize the stub length of the race connecting the capacitor to the power pin.
- Avoid sharing vias between multiple decoupling capacitors.
- Place vias as close as possible to the decoupling capacitor solder pad.
- Widen VDD and/or GND planes to reduce effect if static and dynamic IR drop.

9.1.1 Differential Traces

Guidelines for routing PCB traces are necessary when trying to maintain signal integrity and lower EMI. Although there seems to be an endless number of precautions, this section provides only a few main recommendations as layout guidance.

1. Reduce intra-pair skew in a differential trace by introducing small meandering corrections at the point of mismatch.
2. Reduce inter-pair skew, caused by component placement and IC pinouts, by making larger meandering correction along the signal path. Use chamfered corners with a length-to-trace width ratio of between 3 and 5. The distance between bends must be 8 to 10 times the trace width
3. Use 45° bends instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45° bends is seen as a smaller discontinuity.
4. When routing around an object, route both trace of a pair in parallel. Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur
5. Place passive components within the signal path, such as source-matching resistors or AC coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b). However, the resulting discontinuity is limited to a far narrower area.
6. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below
7. Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise, they cause the differential impedance to drop below 75 Ω and fail the board during TDR testing.
8. Use the smallest size possible for signal trace vias and DisplayPort connector pads as they have less impact on the 100 Ω differential impedance. Large vias and pads can cause the impedance to drop below 85 Ω.
9. Use solid power and ground planes for 100 Ω impedance control and minimum power noise.
10. For 100 Ω differential impedance use the smallest trace spacing possible, which is usually specified by the PCB vendor.
11. Keep the trace length between the DisplayPort connector and the DisplayPort device as short as possible to minimize attenuation.
12. Use good DisplayPort connectors whose impedances meet the specifications.
13. Place bulk capacitors (for example, 10 μF) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
14. Place smaller 0.1-μF or 0.01-μF capacitors at the device.

9.2 Layout Example

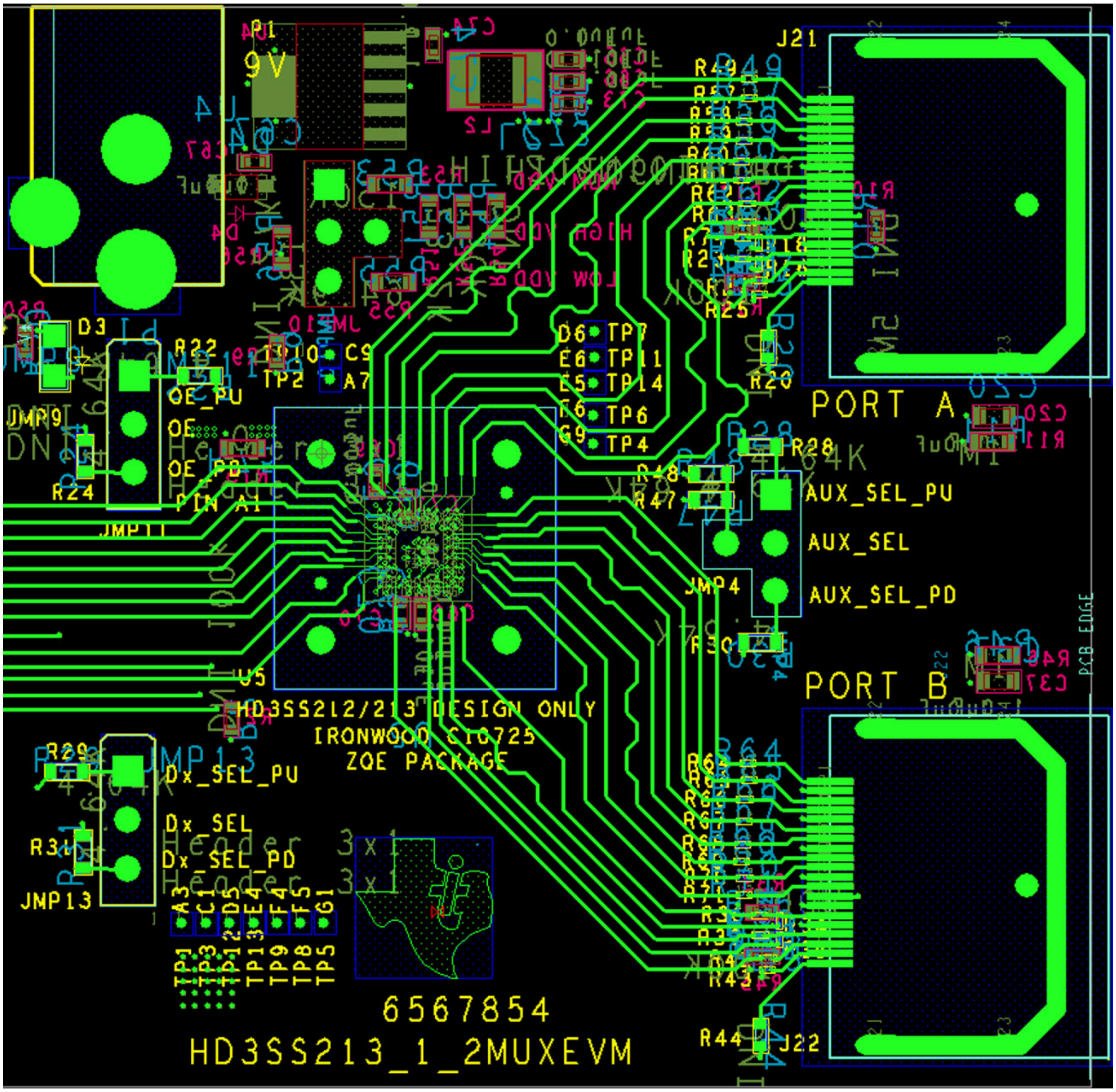


图 9-1. HD3SS213 Layout Example

10 Device and Documentation Support

10.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.3 Trademarks

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10.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS213ZXHR	ACTIVE	NFBGA	ZXH	50	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 105	HD3SS213	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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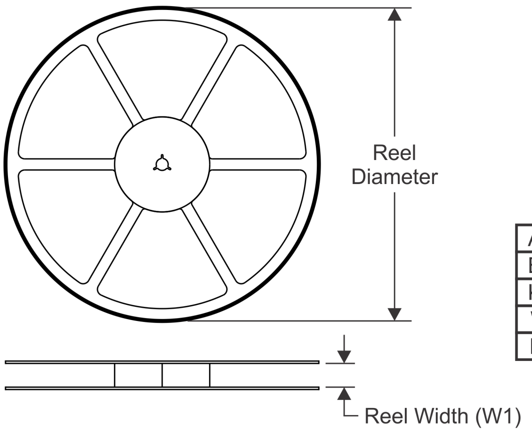
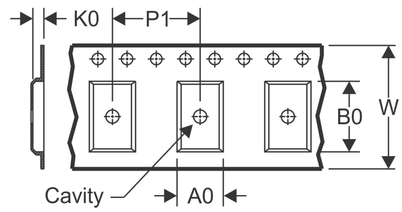
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

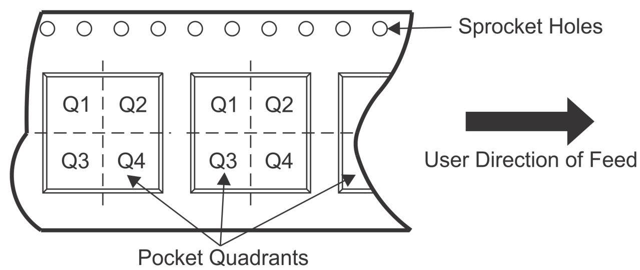


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

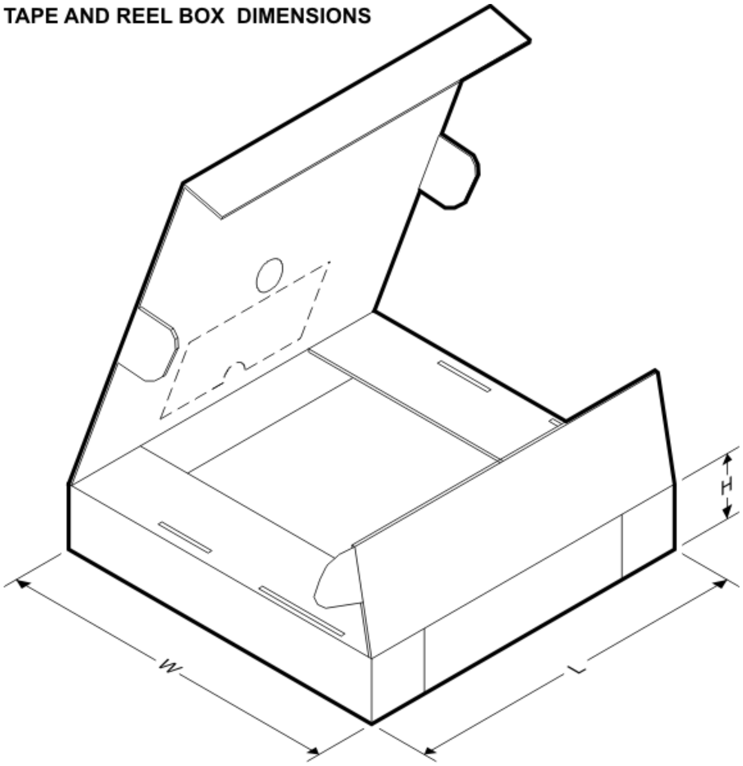
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

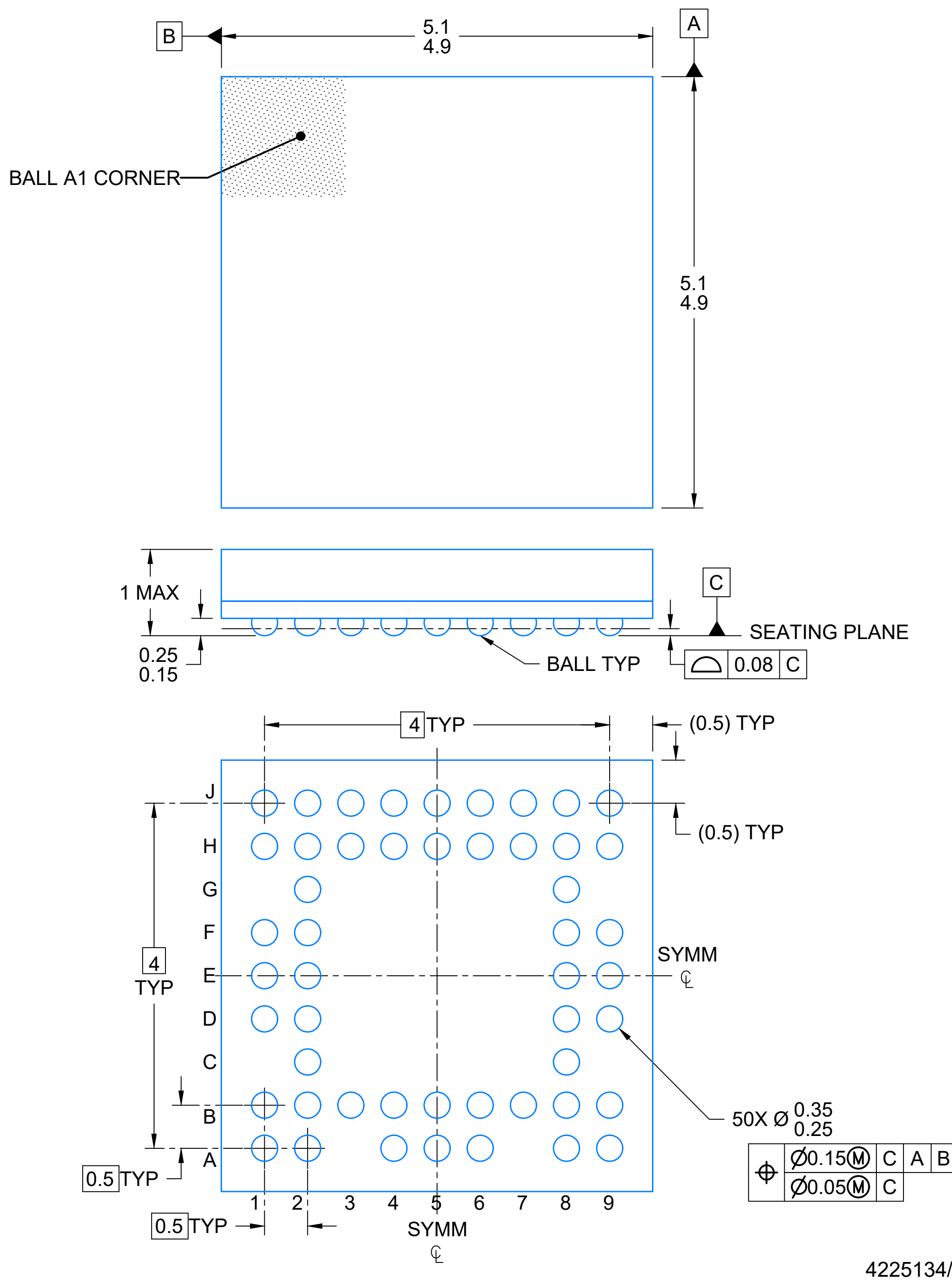
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS213ZXHR	NFBGA	ZXH	50	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS213ZXHR	NFBGA	ZXH	50	2500	336.6	336.6	31.8



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NOTES:

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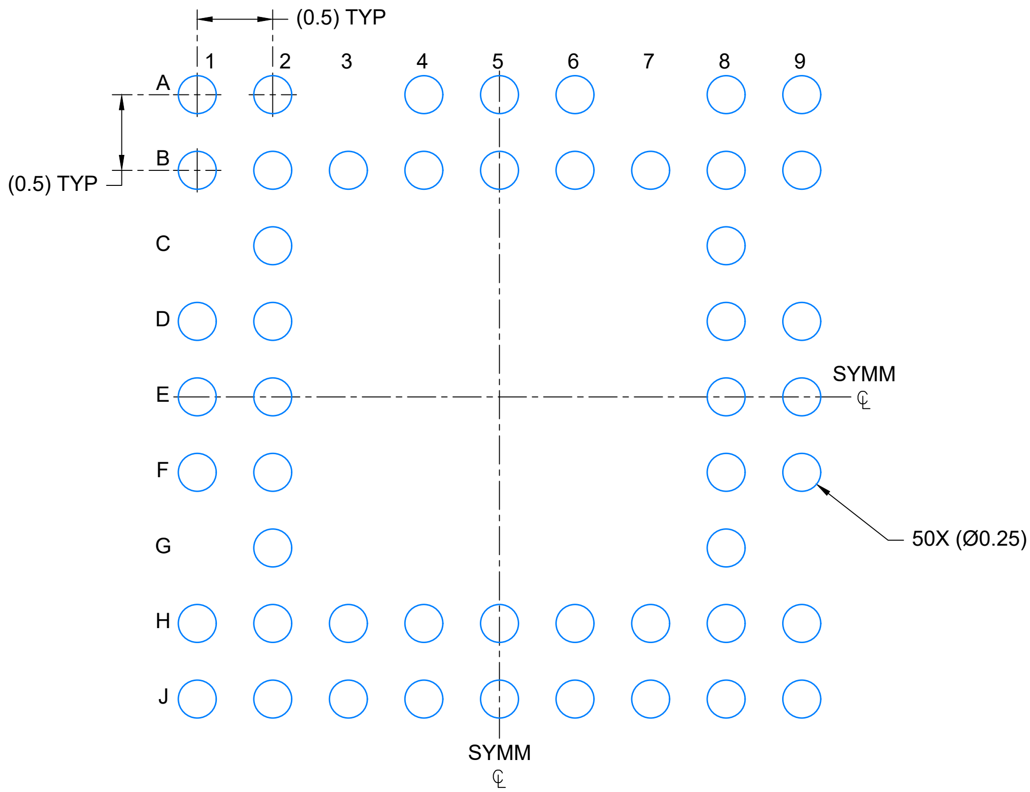
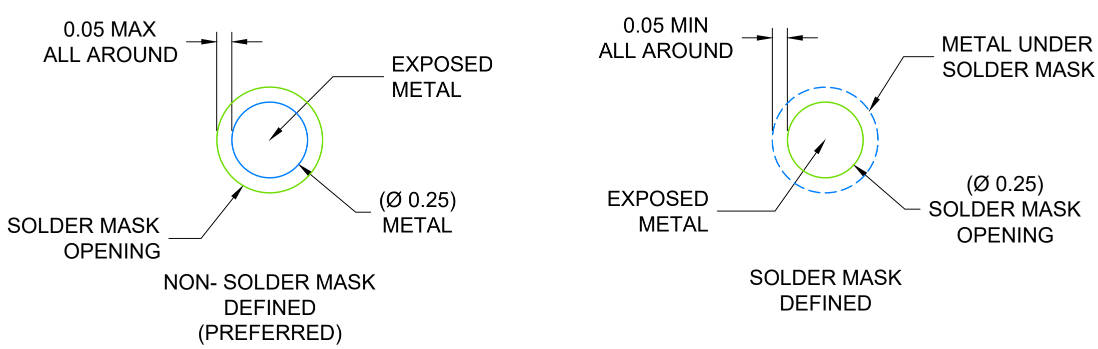
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE: 20X



SOLDER MASK DETAILS
NOT TO SCALE

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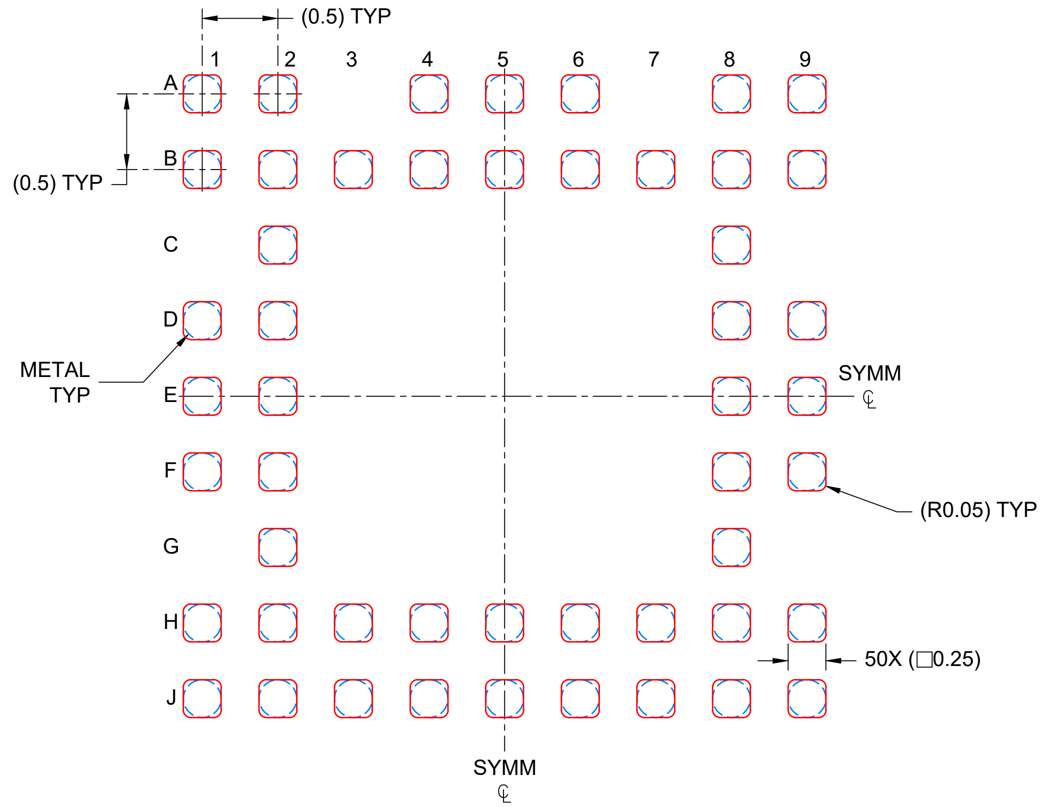
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL
SCALE: 20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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