具有电源正常指示功能的 TPS7B70-Q1 汽车类 300mA 40V 低 I_Q LDO

1 特性

- 符合汽车类应用的 应用
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：–40°C 至 125°C 的环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 器件结温范围：
  –40°C 至 +150°C
- 最大输出电流：300mA
- 4V 至 40V 宽 V_{IN} 输入电压范围，瞬态电压高达 45V
- 3.3V 和 5V 两种固定输出电压
- 最大压降电压：400mV（电流为 300mA）
- 在宽电容（4.7µF 至 500µF）和 ESR（0.001Ω 至 20Ω）范围内，与输出电容器搭配使用时可保持稳定
- 低静态电流 ($I_{(Q)}$)
  - EN 为低电平（关断模式）时 < 4µA
  - 轻负载（VINT 为高电平）时为 19µA（典型值）
- 完全可调的电源正常阈值和电源正常延迟计时
- 针对欠压闭锁 (UVLO) 的低输入电压跟踪功能
- 集成故障保护
  - 过载限流保护
  - 热关断
- 16 引脚 HTSSOP PowerPAD™封装
  - 热阻 ($R_{\theta JA}$)：39.7°C/W

2 应用

- 车身控制模块 (BCM)
- EV 和 HEV 电池管理系统
- 变速器控制单元 (TCU)
- 音响主机
- 电动助力转向 (EPS)

3 说明

TPS7B70-Q1 是一款通过汽车电池供电的 300mA 低压降线性稳压器 (LDO)。该器件在轻负载条件下的静态电流仅有 19µA。因此，TPS7B70-Q1 是用于为微控制器 (MCU) 和控制器局域网 (CAN) 收发器等常开式组件供电的绝佳选择。

TPS7B70-Q1 的输入电压范围扩展到了 40V。该电压可帮助该器件承受瞬态条件，例如负载突降。该器件还具有电源正常 (PG) 引脚，可在输出电压实现稳压后通知系统。要实现必要的操作，您可以调整 PG 阈值电压和延迟。PG 信号的阈值电压通过外部电阻器进行调整。请使用外部电容器来调整延迟。

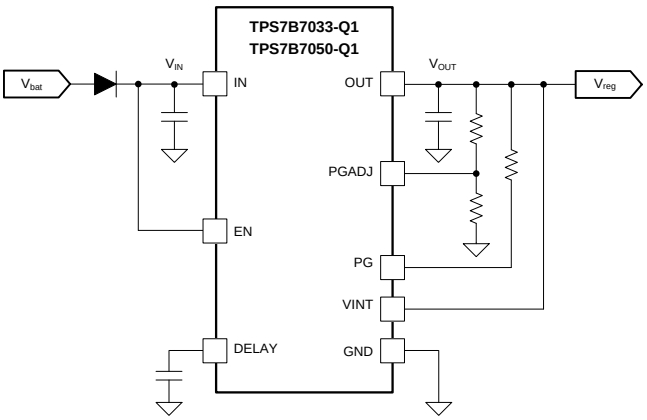
此器件可在 –40°C 至 +125°C 的环境温度下运行，且结温范围为 –40°C 至 +150°C。此外，此器件还采用了热传导封装，即使整个器件散热较多，也能实现持久运行，这是一种典型的脱离电池供电运行的特征。这些特性以及所包含的电流限制和热关断保护使得 TPS7B70-Q1 成为为汽车系统组件供电的绝佳选择。

器件信息(1)

器件编号	输出电压	封装
TPS7B70-Q1	3.3V 或 5V	HTSSOP (16)

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

典型应用



本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

目录

4 修订历史记录

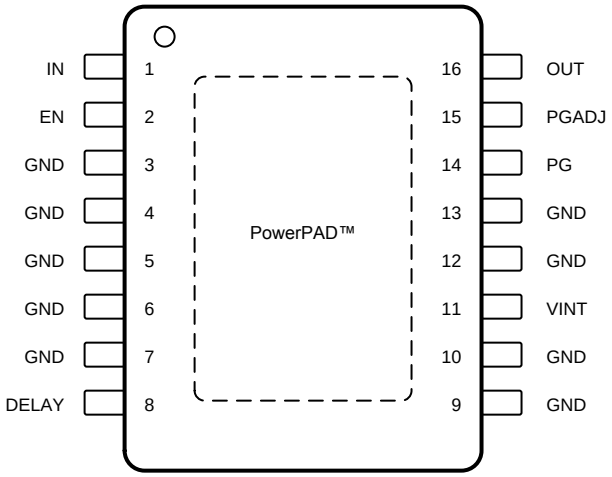
注：之前版本的页码可能与当前版本有所不同。

Changes from Original (August 2018) to Revision A	Page
• 已更改 将器件状态从*高级信息* 更改为*生产数据*	1

Copyright © 2018, Texas Instruments Incorporated

5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With PowerPAD
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DELAY	8	O	Power-good delay adjustment pin. Connect this pin through a capacitor to ground to adjust the power-good delay time.
EN	2	I	Device enable pin. Pull this pin down to low-level voltage to disable the device. Pull this pin up to high-level voltage to enable the device.
GND	3, 4, 5, 6, 7, 9, 10, 12, 13	—	Ground reference
IN	1	I	Device input power supply pin
OUT	16	O	Device 3.3-V or 5-V regulated output-voltage pin
PG	14	O	Power-good pin. Open-drain output pin. Pull this pin up to V_{OUT} or to a reference through a resistor. When the output voltage is not ready, this pin is pulled down to ground.
PGADJ	15	O	Power-good threshold-adjustment pin. Connect a resistor divider between the PGADJ and OUT pins to set the power-good threshold. Connect this pin to ground to set the threshold to 91.6% of output voltage V_{OUT}.
VINT	11	I	Internal voltage rail. Tie this pin above 2 V for lowest I_{GND}.
PowerPAD	—	—	Solder thermal pad to board to improve the thermal performance.

Copyright © 2018, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
	Unregulated input	IN, EN	–0.3	45	V
	Power-good delay-timer output	DELAY	–0.3	7	V
	Regulated output	OUT	–0.3	7	V
	Power-good output voltage	PG	–0.3	7	V
	V-internal	VINT	–0.3	7	V
	Power-good threshold-adjustment voltage	PGADJ	–0.3	7	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 14, 15, and 28)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Unregulated input	IN	4		40	V
	40-V pins	EN	0		V_{IN}	V
	Regulated output	OUT	0		5.5	V
	Power good	PG	0		5.5	V
	Low voltage pins	PGADJ, DELAY	0		5.5	V
I_{OUT}	Output current		0		300	mA
T_A	Ambient temperature		–40		125	°C
T_J	Junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS7B70-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Copyright © 2018, Texas Instruments Incorporated

6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{IN} = 14 V, C_{OUT} ≥ 4.7 µF, and 1 mΩ < ESR < 20 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
$I_{(SLEEP)}$	Input sleep current	EN = off			4.5	µA
$I_{(GND)}$	Input quiescent current	V_{IN} = V_{OUT} + 1 V to 40 V, EN = on, VINT > 2 V, I_{OUT} < 1 mA, –40°C ≤ T_J ≤ 85°C		19	29.6	µA
$V_{(UVLO)}$	Undervoltage lockout, falling	Ramp V_{IN} down until output is turned off			2.6	V
$V_{(UVLO\_HYST)}$	UVLO hysteresis			0.5		V
ENABLE INPUT (EN)						
V_{IL}	Low-level input voltage				0.7	V
V_{IH}	High-level input voltage		2			V
V_{hys}	Hysteresis			150		mV
REGULATED OUTPUT (OUT)						
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 0 mA to 300 mA, –40°C ≤ T_J ≤ 125°C	–2%		2%	
		V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 0 mA to 300 mA	–2.5%		2.5%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 1 mA			10	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	I_{OUT} = 1 mA to 300 mA			20	mV
$V_{(dropout)}$	Dropout voltage (V_{IN} – V_{OUT})(1)(2)	I_{OUT} = 300 mA		300	400	mV
		I_{OUT} = 200 mA		170	325	
$I_{(LIM)}$	Output current limit	V_{OUT} shorted to ground, V_{IN} = 5.6 V	301	680	1000	mA
PSRR	Power-supply ripple rejection(3)	I_{OUT} = 100 mA, C_{OUT} = 10 µF, frequency (f) = 100 Hz		60		dB
		I_{OUT} = 100 mA, C_{OUT} = 10 µF, frequency (f) = 100 kHz		40		
POWER GOOD (PG, PGADJ)						
$V_{OL(PG)}$	PG output, low voltage	I_{OL} = 5 mA, PG pulled low			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	PG pulled to V_{OUT} through a 10-kΩ resistor			1	µA
$V_{(PG\_TH)}$	Default power-good threshold	V_{OUT} powered above the internally set tolerance, PGADJ pin shorted to ground	88.6	91.6	93.6	% of V_{OUT}
$V_{(PG\_HYST)}$	Power-good hysteresis	V_{OUT} falling below the internally set tolerance hysteresis		2		% of V_{OUT}

(1) This test is done with V_{OUT} in regulation, measuring the V_{IN} – V_{OUT} when V_{OUT} drops by 100 mV from the rated output voltage at the specified load.
(2) Dropout is not measured for V_{OUT} = 3.3 V in this test because V_{IN} must be 4 V or greater for proper operation.
(3) Design information—not tested, determined by characterization.

Copyright © 2018, Texas Instruments Incorporated

Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 14 V, C_{OUT} ≥ 4.7 µF, and 1 mΩ < ESR < 20 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGADJ						
$V_{(PGADJ\_TH)}$	Switching voltage for the power-good adjust pin	V_{OUT} is falling	1.067	1.1	1.133	V
POWER-GOOD DELAY						
$I_{(DLY\_CHG)}$	DELAY capacitor charging current		3	5	10	µA
$V_{(DLY\_TH)}$	DELAY pin threshold to release PG high	Voltage at DELAY pin is ramped up	0.95	1	1.05	V
$I_{(DLY\_DIS)}$	DELAY capacitor discharging current	V_{DELAY} = 1 V	0.5			mA
TEMPERATURE						
$T_{(SD)}$	Junction shutdown temperature			175		°C
$T_{(HYST)}$	Hysteresis of thermal shutdown			25		°C

6.6 Switching Characteristics

T_J = –40°C to 150°C, V_I = 14 V, C_O ≥ 4.7 µF, and 1 mΩ < ESR < 20 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-GOOD DELAY (DELAY)						
$t_{(DEGLITCH)}$	Power-good deglitch time			180	250	µs
$t_{(DLY\_FIX)}$	Fixed power-good delay	No capacitor connect at DELAY pin		248	900	µs
$t_{(DLY)}$	Power-good delay	Delay capacitor value: $C_{(DELAY)}$ = 100 nF		20		ms

版权 © 2018, Texas Instruments Incorporated

6.7 Typical Characteristics

T_J = –40ºC to 150ºC, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)

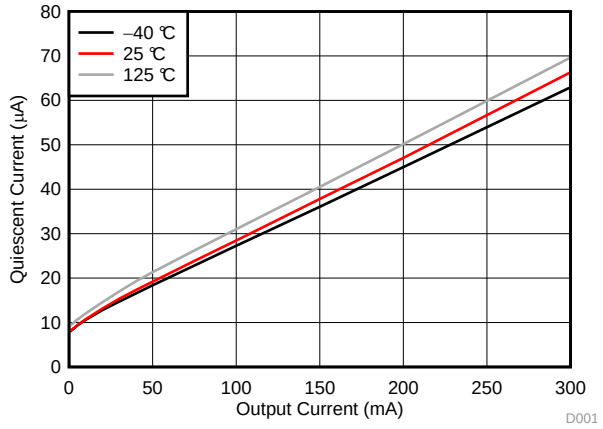


图 1. Ground Current vs Output Current

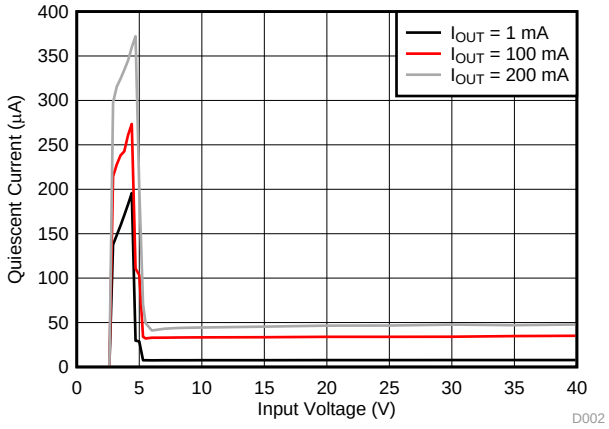
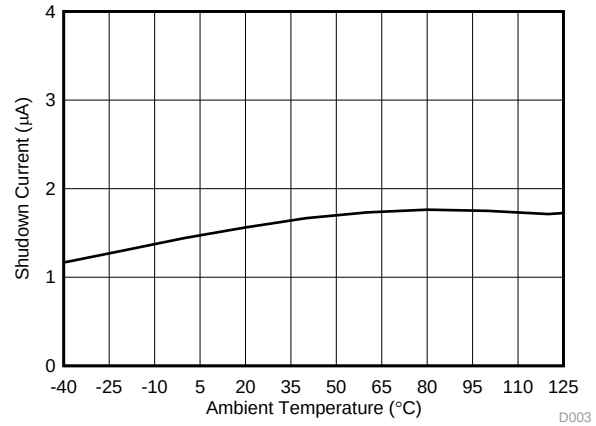


图 2. Ground Current vs Input Voltage



EN = 0 V

图 3. Shutdown Current vs Ambient Temperature

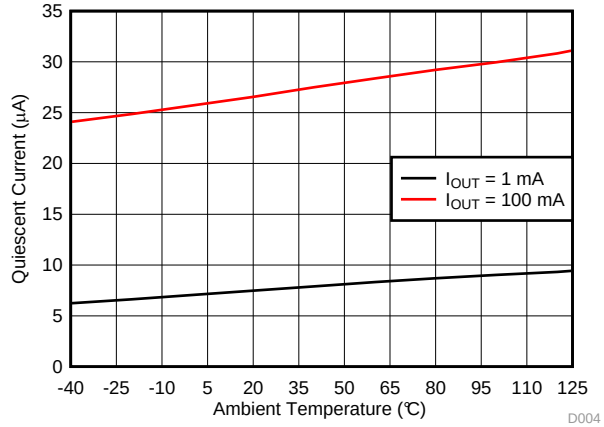


图 4. Ground Current vs Ambient Temperature

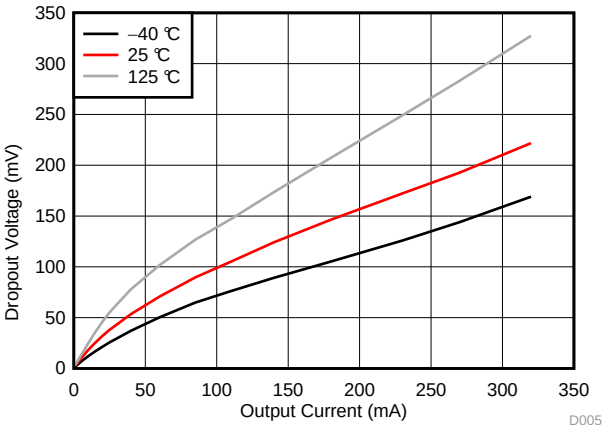
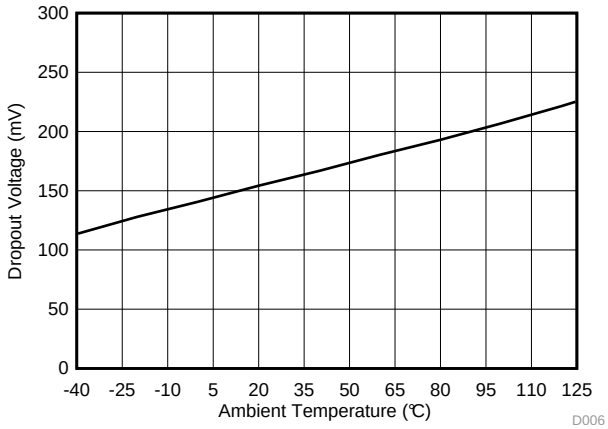


图 5. Dropout Voltage vs Output Current

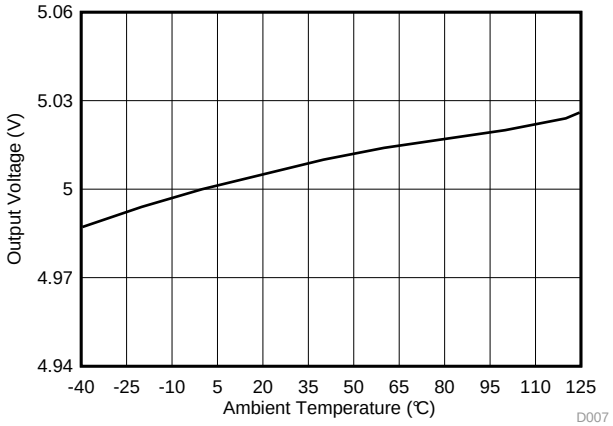


I_{OUT} = 200 mA

图 6. Dropout Voltage vs Ambient Temperature

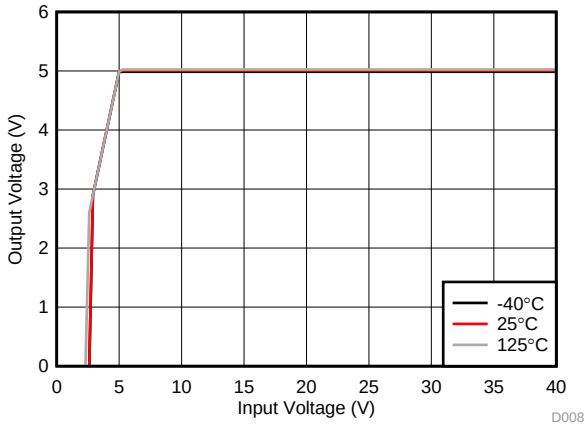
Typical Characteristics (接下页)

T_J = –40ºC to 150ºC, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



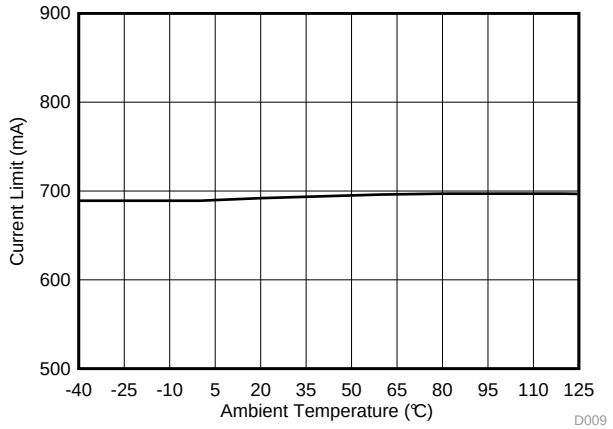
V_{OUT} = 5 V

图 7. Output Voltage vs Ambient Temperature



V_{OUT} = 5 V

图 8. Output Voltage vs Input Voltage



V_{IN} = 5.6 V

图 9. Output Current Limit (I_{LIM}) vs Ambient Temperature

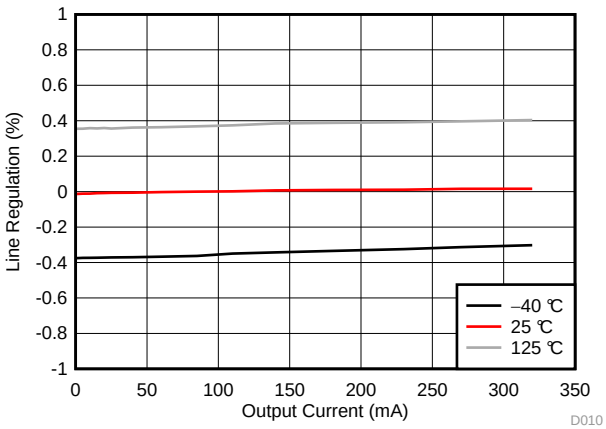


图 10. Load Regulation

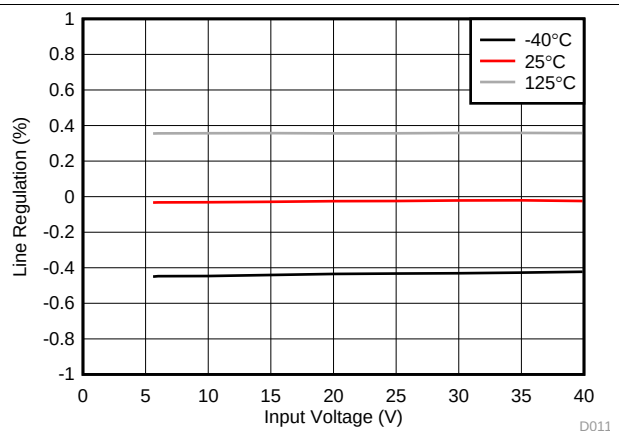
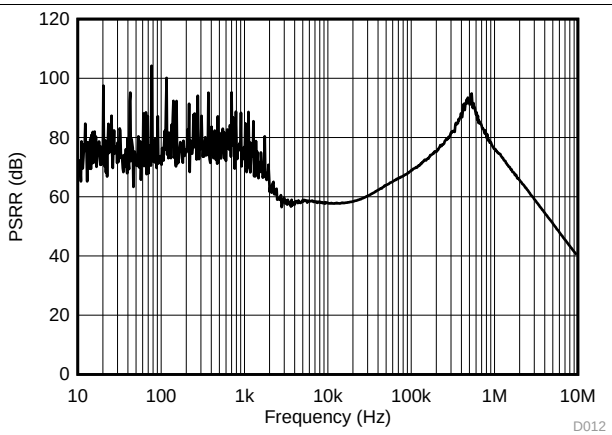


图 11. Line Regulation



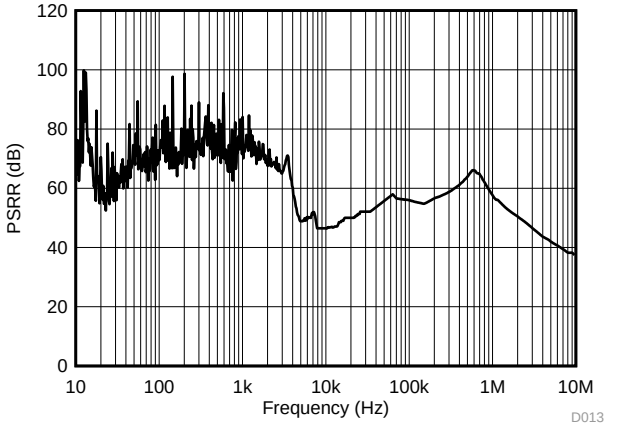
C_{OUT} = 10 µF I_{OUT} = 1 mA T_A = 25°C

图 12. PSRR vs Frequency

版权 © 2018, Texas Instruments Incorporated

Typical Characteristics (接下页)

T_J = –40ºC to 150ºC, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



C_{OUT} = 10 µF I_{OUT} = 100 mA T_A = 25°C

图 13. PSRR vs Frequency

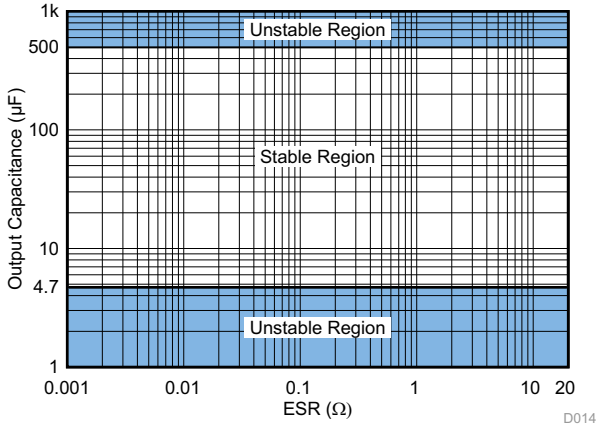
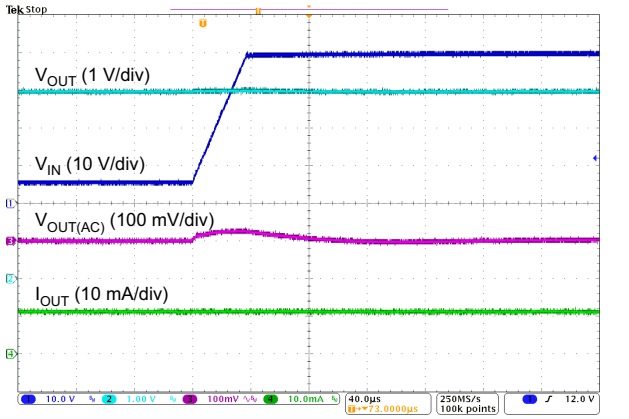
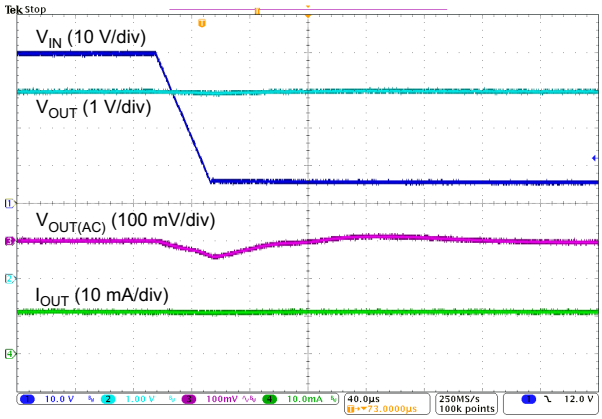


图 14. ESR Stability vs Output Capacitance



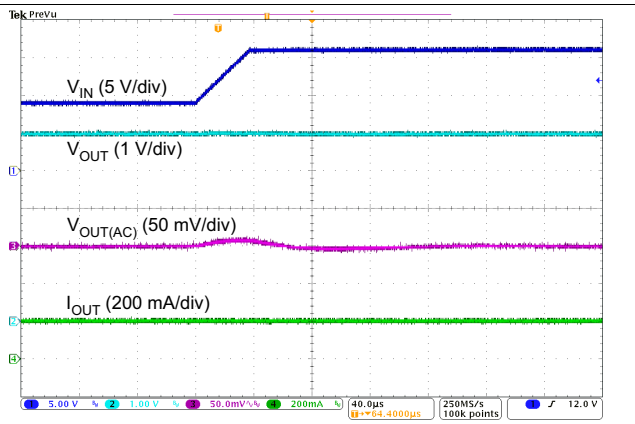
V_{IN} = 6 V to 40 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 1 mA

图 15. Line Transient



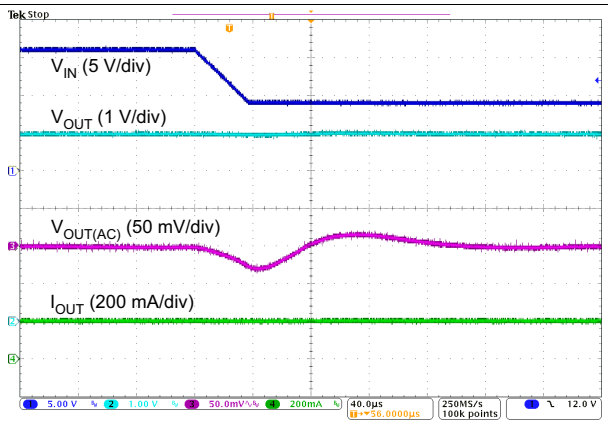
V_{IN} = 40 V to 6 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 1 mA

图 16. Line Transient



V_{IN} = 6 V to 40 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 200 mA

图 17. Line Transient



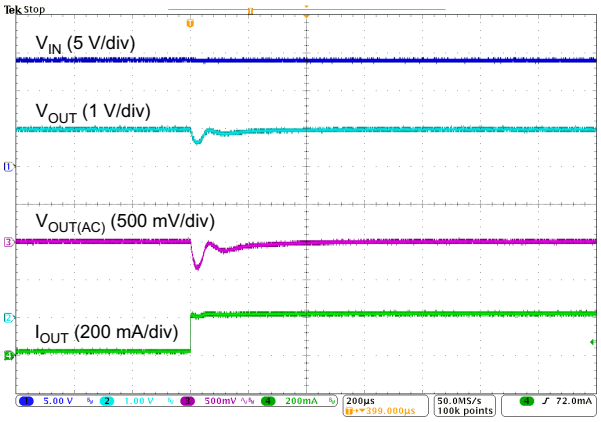
V_{IN} = 40 V to 6 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 200 mA

图 18. Line Transient

版权 © 2018, Texas Instruments Incorporated

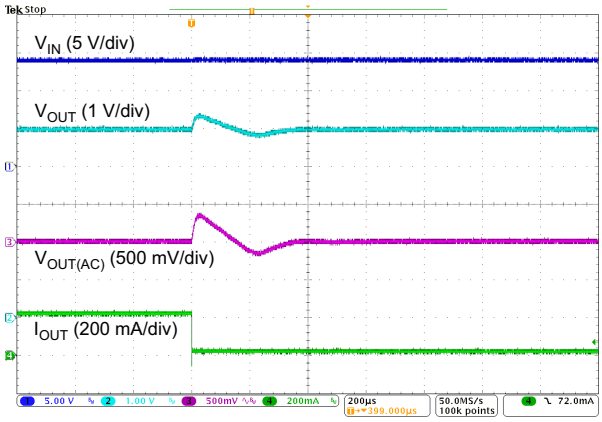
Typical Characteristics (接下页)

T_J = –40ºC to 150ºC, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



V_{OUT} = 5 V C_{OUT} = 10 µF I_{OUT} = 1 mA to 200 mA

图 19. Load Transient



V_{OUT} = 5 V C_{OUT} = 10 µF I_{OUT} = 200 mA to 1 mA

图 20. Load Transient

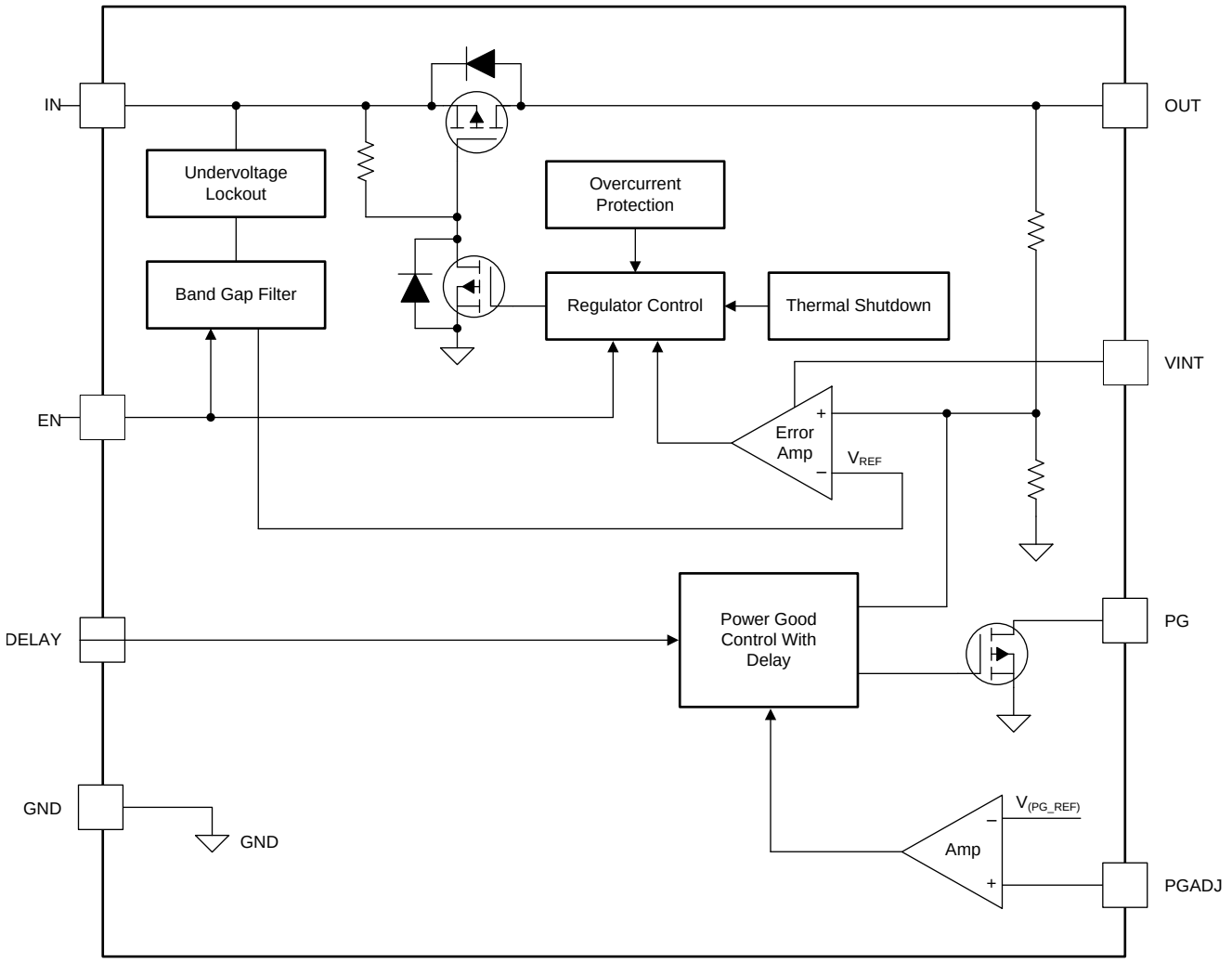
版权 © 2018, Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

The TPS7B70-Q1 is a 300-mA, 40-V monolithic low-dropout linear voltage regulator with adjustable power-good threshold functionality. This voltage regulator consumes only 19-µA quiescent current in light-load applications. Because of the adjustable power-good delay (also called power-on-reset delay) and the adjustable power-good threshold, this device is an excellent choice as a power supply for microprocessors and microcontrollers in automotive applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulator on. Connect this input pin to an external microcontroller or a digital control circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

Feature Description (接下页)

7.3.2 Adjustable Power-Good Threshold (PG, PGADJ)

The PG pin is an open-drain output with an external pullup resistor to the regulated supply, and the PGADJ pin is a power-good threshold adjustment pin. Connecting the PGADJ pin to GND sets the power-good threshold value to the default, $V_{(PG\_TH)}$. When V_{OUT} exceeds the default power-good threshold, the PG output turns high after the power-good delay has expired. When V_{OUT} falls below $V_{(PG\_TH)} - V_{(PG\_HYST)}$, the PG output turns low after a short deglitch time.

The power-good threshold is also adjustable from 1.1 V to 5 V by using an external resistor divider between PGADJ and OUT. 公式 1 calculates the threshold:

$$V_{(PG\_ADJ)\,falling} = V_{(PGADJ\_TH)\,falling} \times \frac{R1+R2}{R2}$$

$$V_{(PG\_ADJ)\,risng} = \left[V_{(PGADJ\_TH)\,falling} + 26\ mV\ (typ) \right] \times \frac{R1+R2}{R2}$$

where:

- $V_{(PG\_ADJ)}$ is the adjustable power-good threshold
- $V_{(PG\_REF)}$ is the internal comparator reference voltage of the PGADJ pin, 1.1 V typical, 2% accuracy specified under all conditions (1)

By setting the power-good threshold $V_{(PG\_ADJ)}$ when V_{OUT} exceeds this threshold, the PG output turns high after the power-good delay has expired. When V_{OUT} falls below $V_{(PG\_ADJ)} - V_{(PG\_HYST)}$, the PG output turns low after a short deglitch time. 图 21 shows a block diagram of this threshold.

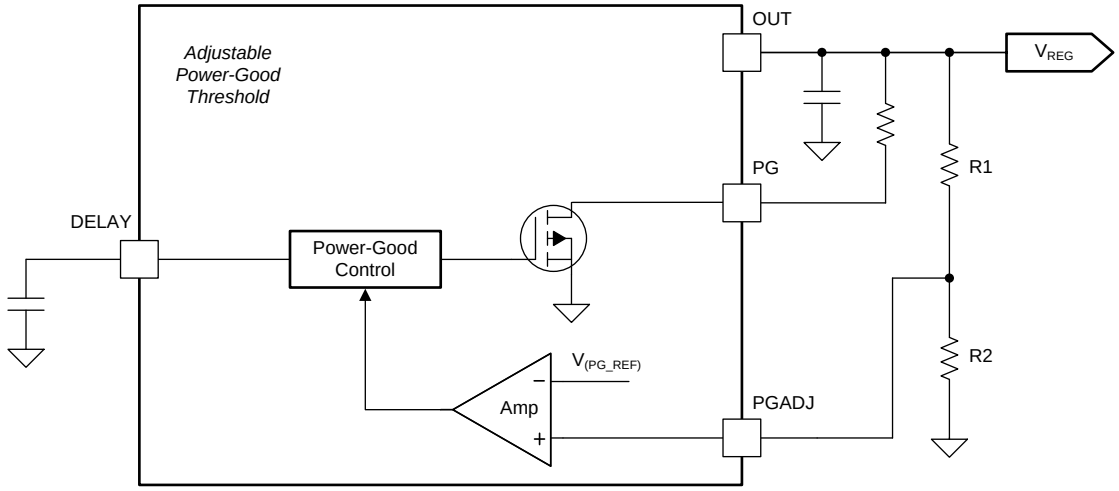


图 21. Adjustable Power-Good Threshold

7.3.3 Adjustable Power-Good Delay Timer (DELAY)

The power-good delay, $t_{(DLY)}$, is the time from when PGADJ is greater than $V_{(PG,REF)}$ until the PG pin goes high. The power-good delay is a function of the value of the external capacitor that is connected to the DELAY pin (C_{DELAY}). Connecting an external capacitor from this pin to GND sets the power-good delay. The constant current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator, and 公式 2 determines the power-good delay. 图 22 illustrates a timing diagram for power-good power-up conditions.

$$t_{(DLY)} = \frac{C_{DELAY} \times 1\ V}{5\ \mu A}$$

where

- $t_{(DLY)}$ is the adjustable power-good delay
- C_{DELAY} is the value of the power-good delay capacitor (2)

版权 © 2018, Texas Instruments Incorporated

Feature Description (接下页)

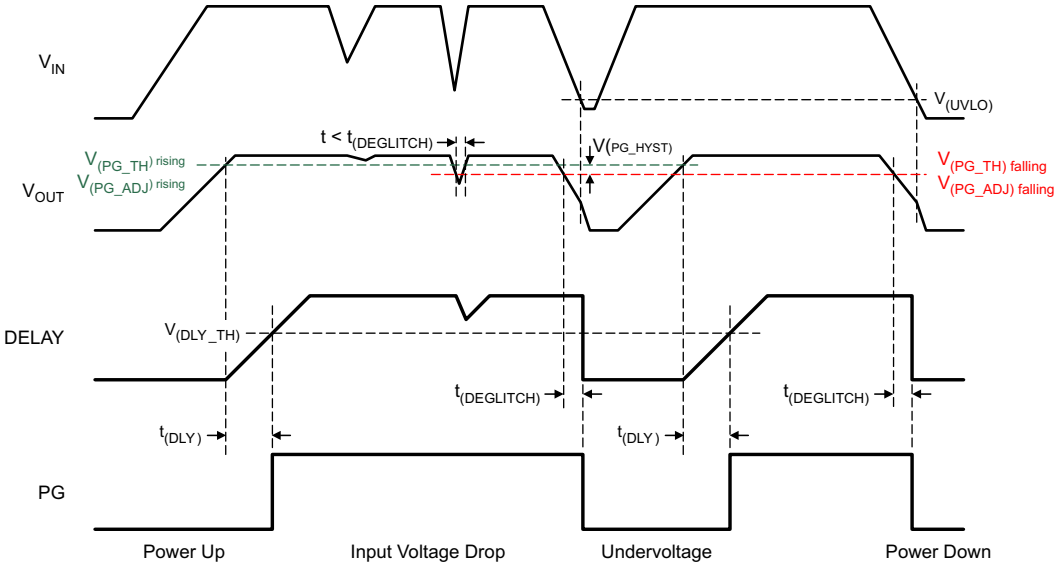


图 22. Power-Up and Conditions for Activation of Power Good

If the DELAY pin is open, the default delay time is $t_{(DLY\_FIX)}$.

7.3.4 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit that shuts down the output if the input voltage falls below an internal UVLO threshold, $V_{(UVLO)}$. The UVLO circuit makes sure that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence after the input voltage rises above the required level.

7.3.5 Current Limit

The TPS7B70-Q1 has current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This feature protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.6 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below $T_{(SD)} – T_{(HYST)}$, the output turns on again.

7.4 Device Functional Modes

7.4.1 Operation With Input Voltage Less Than 4 V

The device normally operates with input voltages above 4 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.6 V. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With Input Voltage Greater Than 4 V

If the input voltage is greater than the output set value plus the device dropout voltage when the input voltage is greater than 4 V, then the output voltage is equal to the set value. Otherwise, the output voltage is equal to the input voltage minus the dropout voltage.

版权 © 2018, Texas Instruments Incorporated

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B70-Q1 is a 300-mA low-dropout linear regulator with ultra-low quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

图 23 shows a typical application circuit for the TPS7B70-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. Use a low-ESR ceramic capacitor with a dielectric of type X7R.

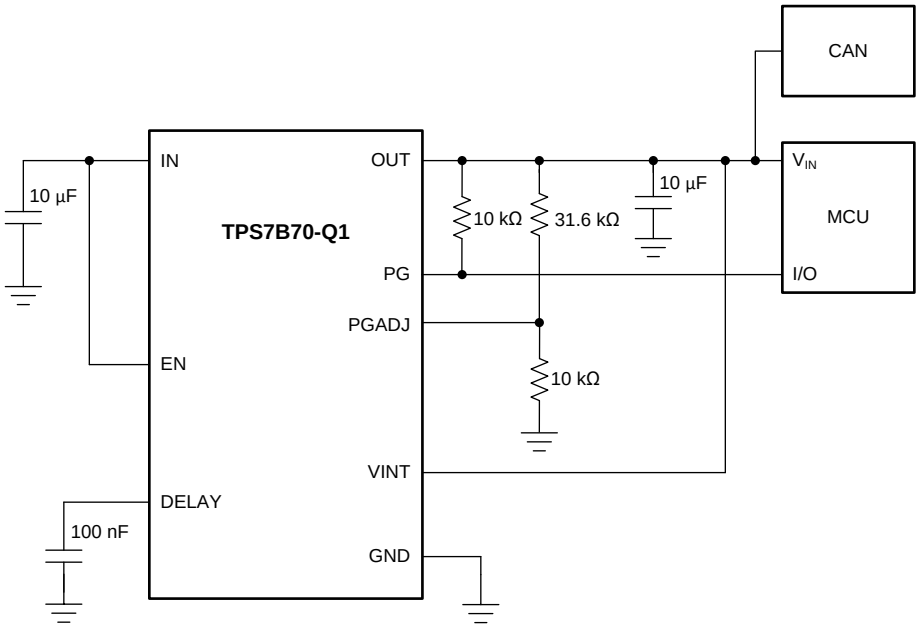


图 23. Supply Power to an MCU

版权 © 2018, Texas Instruments Incorporated

Typical Application (接下页)

8.2.1 Design Requirements

For this design, the TPS7B70-Q1 must be able to supply a CAN transceiver and an MCU from a 12-V automotive battery. To provide good MCU operation, the PG pin must trip when the output is at 95% of the nominal value. The PG pin must have a 20-ms delay in order to avoid shutting down as a result of temporary glitches.

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

A 10-µF capacitor in parallel with a 0.1-µF ceramic bypass capacitor is placed at the input in order to keep the input voltage stable. The input can tolerate transients up to 40 V, so the input capacitors have a 50-V voltage rating.

8.2.2.2 Output Capacitor

For this application, a 10-µF X7R ceramic capacitor is used to provide good output transient performance and good loop stability.

8.2.2.3 Power-Good Threshold

The power-good threshold is set by connecting PGADJ to GND, or by connecting PGADJ to a resistor divider from OUT to GND. The *Adjustable Power-Good Threshold (PG, PGADJ)* section provides the method to setup the power-good threshold. Rearranging 公式 1 yields 公式 3, and solves the values of R1 and R2 that are needed to get the 95% falling threshold. In this design, R2 is a 10-kΩ resistor. Solving 公式 3 for R1 gives a value of 33.18 kΩ. This value is not a standard 1% resistor value, so a 31.6-kΩ resistor is chosen for R1.

$$R1 = R2\left(\frac{V_{(PGADJ)falling}}{V_{(PTGADJ\_TH)falling}}\right) \quad (3)$$

8.2.2.4 Power-Good Delay, $t_{(DLY)}$

Set the power-good delay with an external capacitor (C_{DELAY}) to ground. Calculate the correct capacitance with 公式 2. This application requires a delay of 20 ms, so solve for the correct capacitance required to get this delay. As shown in 公式 4, rearrange 公式 2 to solve for C_{DELAY}.

$$C_{DELAY} = t_{DLY} \times 5\mu A \quad (4)$$

8.2.3 Application Curve

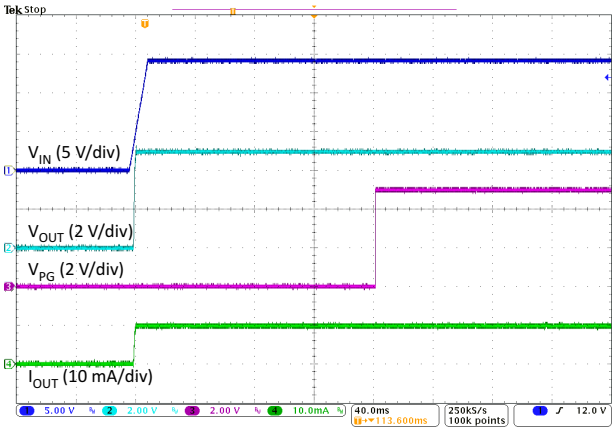


图 24. Power-Up Waveform

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 4 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B70-Q1, add a capacitor with a value of ≥ 10 µF with a 0.1-µF ceramic bypass capacitor in parallel at the input.

10 Layout

10.1 Layout Guidelines

For LDO power supplies, especially high-voltage and high-current supplies, layout is an important step. If the layout is not carefully designed, the regulator cannot deliver enough output current because of thermal limitations. To improve the thermal performance of the device and maximize the current output at high ambient temperature, spread out the thermal pad as much as possible, and put enough thermal vias on the thermal pad. 图 25 shows an example layout.

10.2 Layout Example

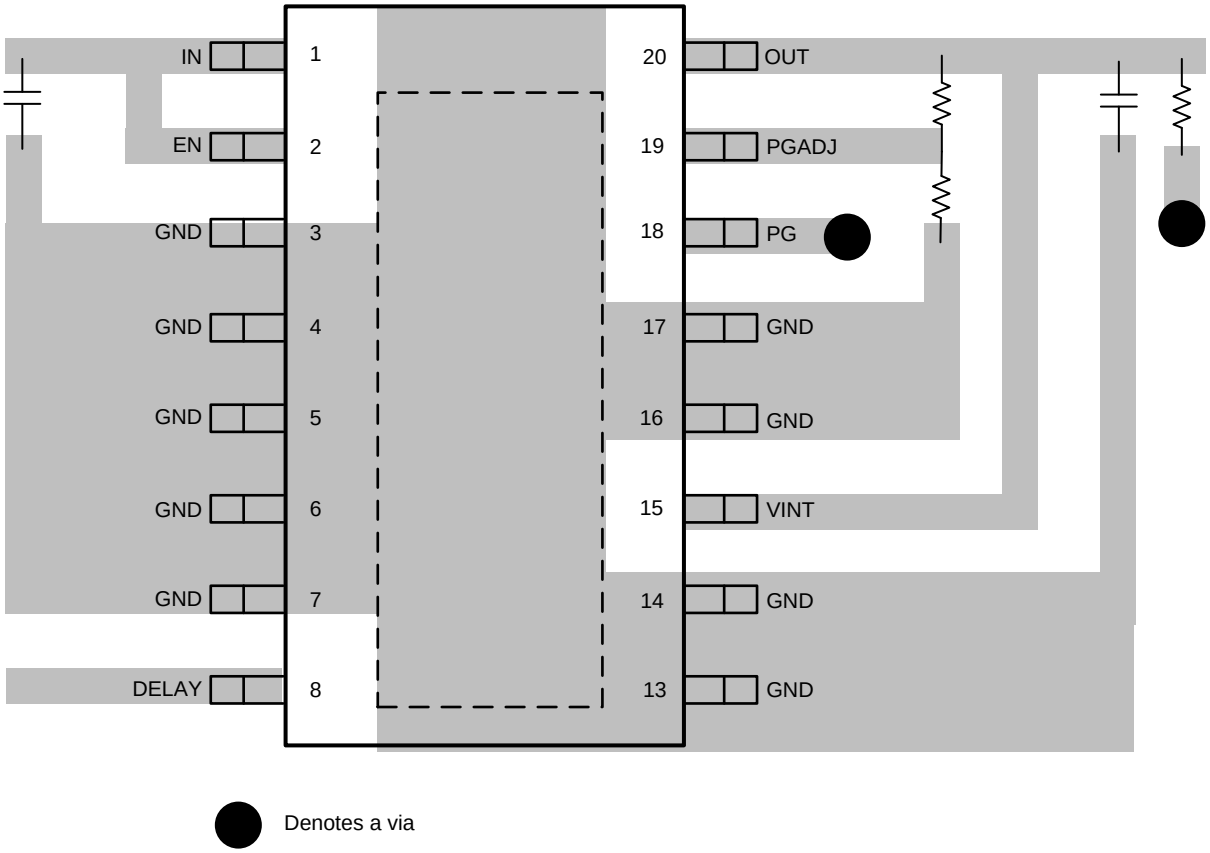


图 25. Layout Example

版权 © 2018, Texas Instruments Incorporated

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

德州仪器 (TI)，*《TPS7B70EVM-008 评估模块》用户指南*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

版权 © 2018, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B7033QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B7033Q	Samples
TPS7B7050QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B7050Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

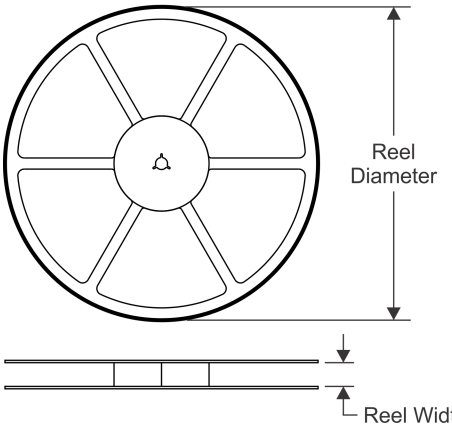
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

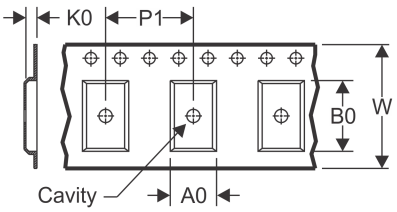
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

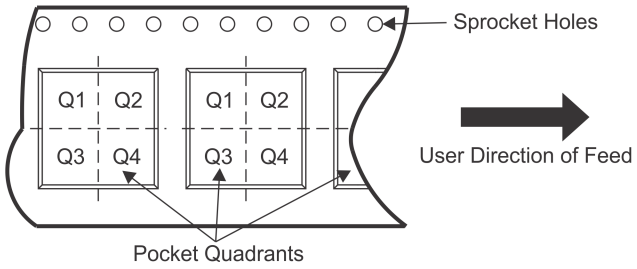


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

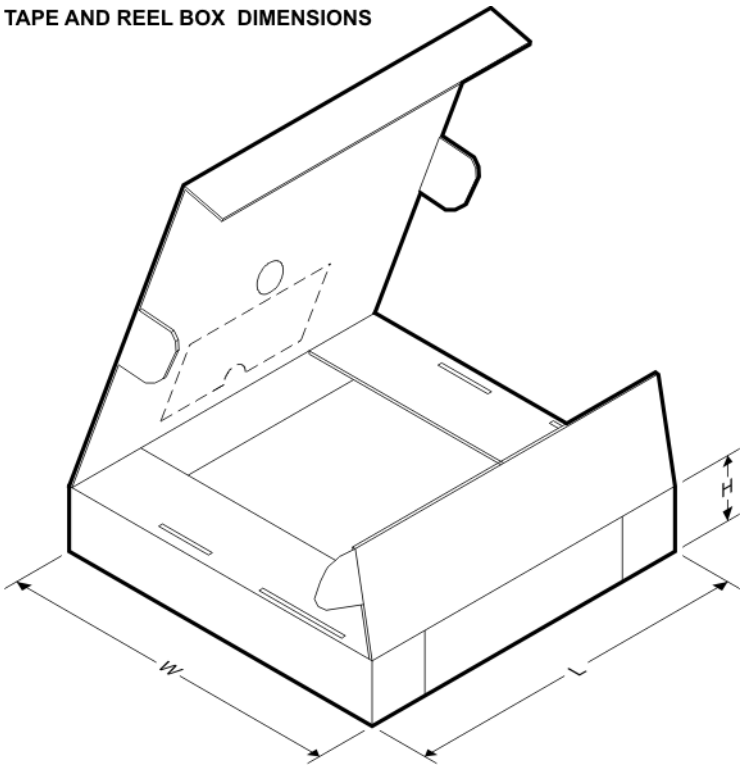
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B7033QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B7050QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

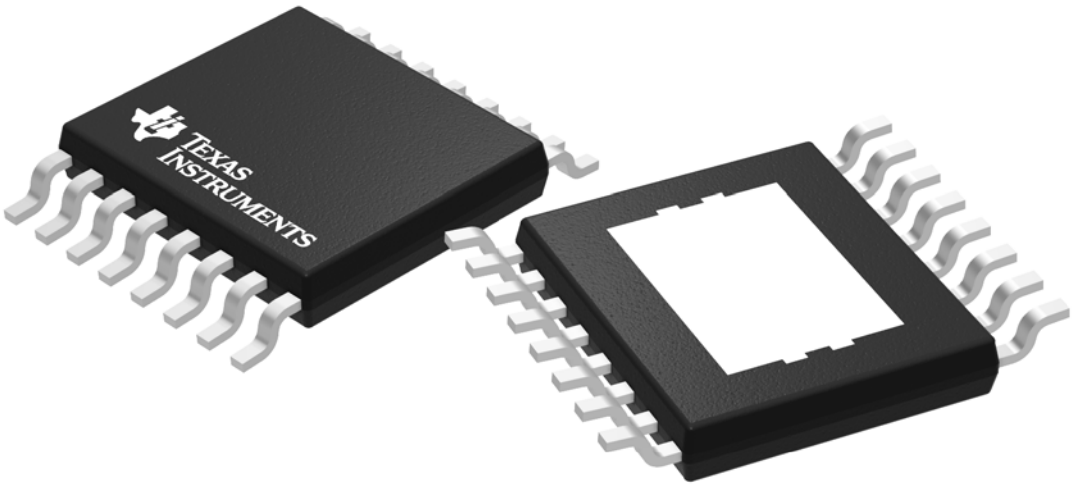


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B7033QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS7B7050QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022，德州仪器 (TI) 公司