

TPS65632 Triple-Output AMOLED Display Power Supply

1 Features

- 2.9-V to 4.5-V Input Voltage Range
- Boost Converter 1 (V_{POS})
 - 4.6-V Output Voltage
 - 0.5% Accuracy (25°C to 85°C)
 - Dedicated Output Sense Pin
 - 300-mA Output Current
- Inverting Buck-Boost Converter (V_{NEG})
 - –1.5-V to –5.4-V Programmable Output Voltage
 - –4-V Default Output Voltage
 - 300-mA Output Current
- Boost Converter 2 (AV_{DD})
 - 5.8-V or 7.7-V Output Voltage
 - 30-mA Output Current
- Excellent Line Transient Regulation
- Short-Circuit Protection
- Thermal Shutdown
- 3-mm x 3-mm, 16-Pin WQFN Package

2 Applications

AMOLED Displays

3 Description

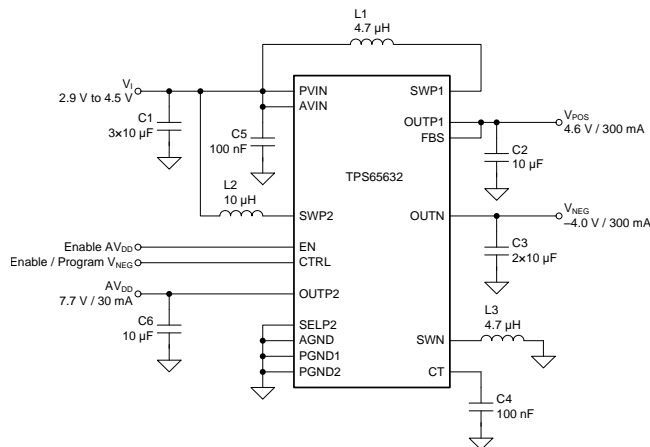
The TPS65632 is designed to drive AMOLED displays (Active Matrix Organic Light Emitting Diode) requiring three supply rails, V_{POS} , V_{NEG} and AV_{DD} . The device integrates a boost converter for V_{POS} , an inverting buck-boost converter for V_{NEG} , and a boost converter for AV_{DD} , all of which are suitable for battery operated products. The digital control pin (CTRL) allows programming the negative output voltage in digital steps. The TPS65632 uses a novel technology enabling excellent line and load regulation.

Device Information⁽¹⁾

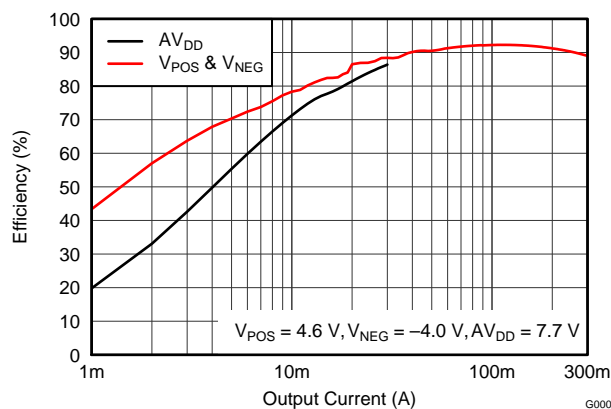
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| TPS65632 | WQFN (16) | 3.00 mm x 3.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Efficiency vs Output Current



G000



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4 Revision History

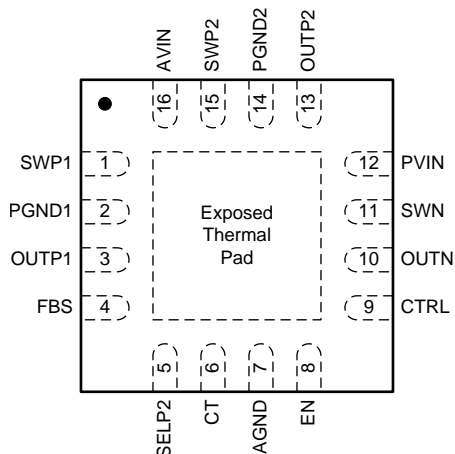
Changes from Original (March 2015) to Revision A

Page

- Changed Load regulation (0.18 TYP) UNIT value in the [Electrical Characteristics](#) From: %/mA To: %/A **6**

5 Pin Configuration and Functions

RTE Package
16-Pin WQFN with Thermal Pad
Top View



Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|---------------------|-----|---------------------|--------------------------------------------------------------------------------------------------------------------------|
| NAME | NO. | | |
| AGND | 7 | GND | Analog ground. |
| AVIN | 16 | PWR | Supply voltage for the device. |
| CT | 6 | I/O | A capacitor connected between this pin and ground sets the transition time for V_{NEG} when programmed to a new value. |
| CTRL | 9 | I | Boost converter 1 (V_{POS}) inverting buck-boost converter (V_{NEG}) enable/program. |
| EN | 8 | I | Boost converter 2 (AV_{DD}) enable. |
| FBS | 4 | I | Boost converter 1 (V_{POS}) sense input. |
| OUTN | 10 | O | Inverting buck-boost converter output (V_{NEG}). |
| OUTP | 3 | O | Boost converter 1 output (V_{POS}). |
| OUTP2 | 13 | O | Boost converter 2 output (AV_{DD}). |
| PGND1 | 2 | GND | Boost converter 1 power ground. |
| PGND2 | 14 | GND | Boost converter 2 power ground. |
| PVIN | 12 | PWR | Inverting buck-boost converter power stage supply voltage. |
| SELP2 | 5 | I | Boost converter 2 output voltage selection pin. $AV_{DD} = 7.7$ V when SELP2 = low and 5.8 V when SELP2 = high. |
| SWN | 11 | I/O | Inverting buck-boost converter switch pin. |
| SWP1 | 1 | I | Boost converter 1 switch pin. |
| SWP2 | 15 | I | Boost converter 2 switch pin. |
| Exposed thermal pad | | — | Connect this pad to AGND, PGND1 and PGND2. |

(1) GND = Ground, PWR = Power, I = Input, O = Output, I/O = Input/Output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------------------------------------|------------------------------|------|-----|------|
| Input supply voltage ⁽²⁾ | SWP1, OUTP1, FBS, PVIN, AVIN | -0.3 | 5 | V |
| | SWP2 | -0.3 | 12 | V |
| | OUTP2 | -0.3 | 8.5 | V |
| | OUTN | -6.0 | 0.3 | V |
| | SWN | -6.5 | 4.8 | V |
| | CTRL, EN, SELP2 | -0.3 | 5.5 | V |
| | CT | -0.3 | 3.6 | V |
| Operating virtual junction, T _J | | -40 | 150 | °C |
| Storage temperature, T _{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) With respect to GND pin.

6.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|------------------------------------------------------------------------------------------|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾ | ±500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|----------------|--------------------------------|-----|-----|-----|------|
| INPUT | | | | | |
| V _I | Input supply voltage range | 2.9 | 3.7 | 4.5 | V |
| T _J | Operating junction temperature | -40 | 85 | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | RTE [WQFN] | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
| | | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 42.9 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 44 | |
| R _{θJB} | Junction-to-board thermal resistance | 14.2 | |
| ψ _{JT} | Junction-to-top characterization parameter | 0.6 | |
| ψ _{JB} | Junction-to-board characterization parameter | 14.1 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 3.3 | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

$V_I = 3.7\text{ V}$, $CTRL = 3.7\text{ V}$, $EN = 3.7\text{ V}$, $V_{POS} = 4.6\text{ V}$, $V_{NEG} = -4.0\text{ V}$, $AV_{DD} = 7.7\text{ V}$, $T_J = -40^\circ\text{C}$ to 85°C , typical values are at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------------------------------------|-------------------------------------------|---------------------------------------------------------------------------|-------|-------|------|------------------|
| SUPPLY CURRENT AND THERMAL PROTECTION | | | | | | |
| V_I | Input voltage range | | 2.9 | 3.7 | 4.5 | V |
| I_{SD} | Shutdown current | $CTRL = GND$, $EN = GND$, sum of current flowing into $AVIN$ and $PVIN$ | | 0.25 | 5 | μA |
| V_{UVLO} | Under-voltage lockout threshold | V_I falling | 1.8 | | 2.1 | V |
| | | V_I rising | 2.1 | | 2.5 | V |
| BOOST CONVERTER 1 (V_{POS}) | | | | | | |
| V_{POS} | Positive output 1 voltage | | | 4.6 | | V |
| | Positive output 1 voltage variation | $25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, No load | -0.5% | | 0.5% | |
| | | $-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, No load | -0.8% | | 0.8% | |
| $r_{DS(on)1A}$ | Switch on-resistance | $I_{(SWP1)} = 200\text{ mA}$ | | 200 | | $\text{m}\Omega$ |
| $r_{DS(on)1B}$ | Rectifier on-resistance | | | 350 | | $\text{m}\Omega$ |
| f_{SW1} | Switching frequency | $I_{POS} = 200\text{ mA}$ | | 1.7 | | MHz |
| I_{SW1} | Switch current limit | Inductor valley current | 0.8 | 1 | 1.4 | A |
| V_{SCP1} | Short-circuit threshold in operation | V_{POS} falling | 3.95 | 4.10 | 4.28 | V |
| t_{SCP1} | Short-circuit detection time in operation | | | 3 | | ms |
| V_T | Output voltage sense threshold | $V_{(OUTP1)} - V_{(FBS)}$ increasing | 200 | 300 | 550 | mV |
| | | $V_{(OUTP1)} - V_{(FBS)}$ decreasing | 100 | 200 | 450 | mV |
| $R_{(FBS)}$ | FBS pin pull-down resistance | | 2 | 4 | 6 | $\text{M}\Omega$ |
| R_{DCHG1} | Discharge resistance | $CTRL = GND$, $I_{(SWP1)} = 1\text{ mA}$ | 10 | 30 | 70 | Ω |
| | Line regulation | $I_{POS} = 200\text{ mA}$ | | 0.01 | | %/V |
| | Load regulation | $1\text{ mA} \leq I_{POS} \leq 300\text{ mA}$ | | 0.007 | | %/A |
| INVERTING BUCK-BOOST CONVERTER (V_{NEG}) | | | | | | |
| V_{NEG} | Output voltage default | | | -4.0 | | V |
| | Output voltage range | | -1.4 | | -5.4 | |
| | Output voltage accuracy | $25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, no load | -50 | | 50 | |
| $-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, no load | | -60 | | 60 | | |
| $r_{DS(on)2A}$ | SWN MOSFET on-resistance | $I_{(SWN)} = 200\text{ mA}$ | | 200 | | $\text{m}\Omega$ |
| $r_{DS(on)2B}$ | SWN MOSFET rectifier on-resistance | | | 300 | | $\text{m}\Omega$ |
| f_{SW2} | SWN Switching frequency | $I_{NEG} = 10\text{ mA}$ | | 1.7 | | MHz |
| I_{SW2} | SWN switch current limit | $V_I = 2.9\text{ V}$ | 1.5 | 2.2 | 3 | A |
| V_{SCP2} | Short circuit threshold in operation | Voltage increase from nominal V_{NEG} | 300 | 500 | 700 | mV |
| | Short circuit threshold in start up | | 180 | 200 | 230 | mV |
| t_{SCP2} | Short circuit detection time in start up | | | 10 | | ms |
| | Short circuit detection time in operation | | | 3 | | ms |
| R_{DCHG2} | Discharge resistance | $CTRL = GND$, $I_{(SWN)} = 1\text{ mA}$ | 130 | 150 | 170 | Ω |
| | Line regulation | $I_{NEG} = 200\text{ mA}$ | | 0.004 | | %/V |
| | Load regulation | | | 0.1 | | %/A |

Electrical Characteristics (continued)

$V_I = 3.7\text{ V}$, $CTRL = 3.7\text{ V}$, $EN = 3.7\text{ V}$, $V_{POS} = 4.6\text{ V}$, $V_{NEG} = -4.0\text{ V}$, $AV_{DD} = 7.7\text{ V}$, $T_J = -40^\circ\text{C}$ to 85°C , typical values are at $T_J = 25^\circ\text{C}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------------------|---------------------------------|--------------------------------------------------------------|-------|------|------|------------------|
| BOOST CONVERTER 2 (AV_{DD}) | | | | | | |
| AV_{DD} | Output voltage | SELP2 = Low | | 7.7 | | V |
| | | SELP2 = High | | 5.8 | | |
| AV_{DD} | Output voltage accuracy | $25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, no load | -1% | | 1% | |
| | | $-30^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, no load | -1.3% | | 1.3% | |
| $r_{DS(on)3A}$ | SWP2 switch on-resistance | $I_{(SWP2)} = 200\text{ mA}$ | | 400 | | m Ω |
| $r_{DS(on)3B}$ | SWP2 rectifier on-resistance | | | 650 | | |
| f_{SW3} | Switching frequency | $I_{AV_{DD}} = 0\text{ mA}$ | | 1.7 | | MHz |
| I_{LIM3} | Switch current limit | Inductor valley current | 0.25 | 0.35 | 0.45 | A |
| R_{DCHG3} | Discharge resistance | $EN = GND$, $I_{(SWP2)} = 1\text{ mA}$ | 10 | 30 | 70 | Ω |
| | Line regulation | $I_{AV_{DD}} = 30\text{ mA}$ | | 0.02 | | %/V |
| | Load regulation | | | 0.18 | | %/A |
| CTRL INTERFACE (CTRL, EN, SELP2) | | | | | | |
| V_{IH} | Logic input high level voltage | | 1.2 | | | V |
| V_{IL} | Logic input low level voltage | | | | 0.4 | V |
| R | Pull-down resistance | | 150 | 400 | 860 | k Ω |
| OTHER | | | | | | |
| R_{CT} | CT pin resistance | | 150 | 300 | 500 | k Ω |
| t_{INIT} | Initialization time | | | 300 | 400 | μs |
| t_{STORE} | Data storage/accept time period | | 30 | | 80 | μs |
| t_{SDN} | Shutdown time period | | 30 | | 80 | μs |
| T_{SD} | Thermal shutdown temperature | Temperature rising | | 145 | | $^\circ\text{C}$ |

6.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|-----------------------|--------------------------------------|-----|-----|-----|---------------|
| CTRL INTERFACE | | | | | |
| t_{LOW} | Low-level pulse duration | 2 | 10 | 25 | μs |
| t_{HIGH} | High-level pulse duration | 2 | 10 | 25 | μs |
| t_{OFF} | Shutdown pulse duration (CTRL = low) | 200 | | | μs |

6.7 Typical Characteristics

$T_J = 25^\circ\text{C}$, $V_I = 3.7\text{ V}$, unless otherwise stated.

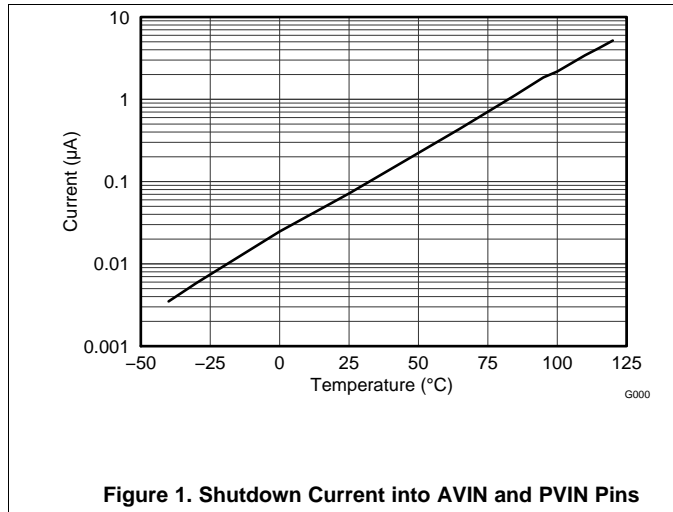


Figure 1. Shutdown Current into AVIN and PVIN Pins

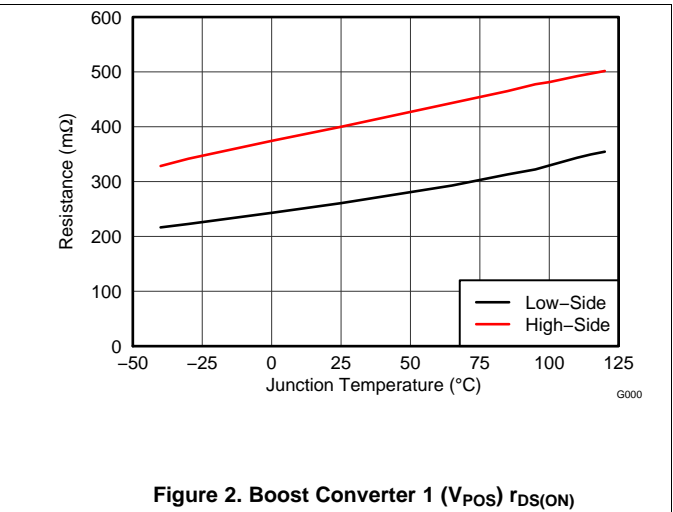


Figure 2. Boost Converter 1 (V_{POS}) $r_{DS(ON)}$

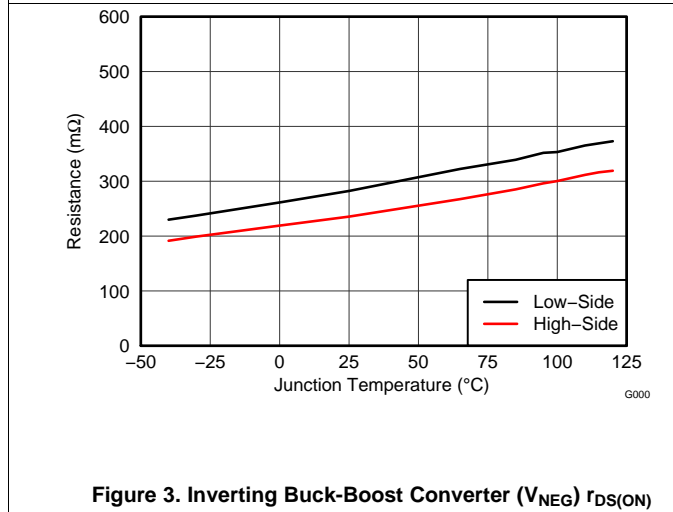


Figure 3. Inverting Buck-Boost Converter (V_{NEG}) $r_{DS(ON)}$

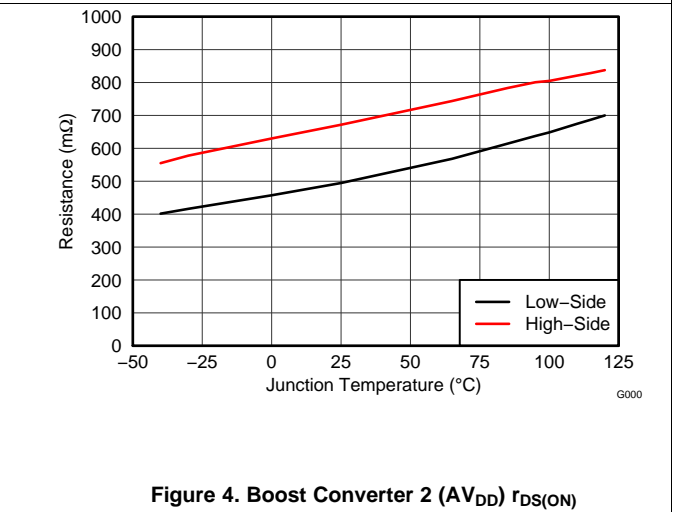


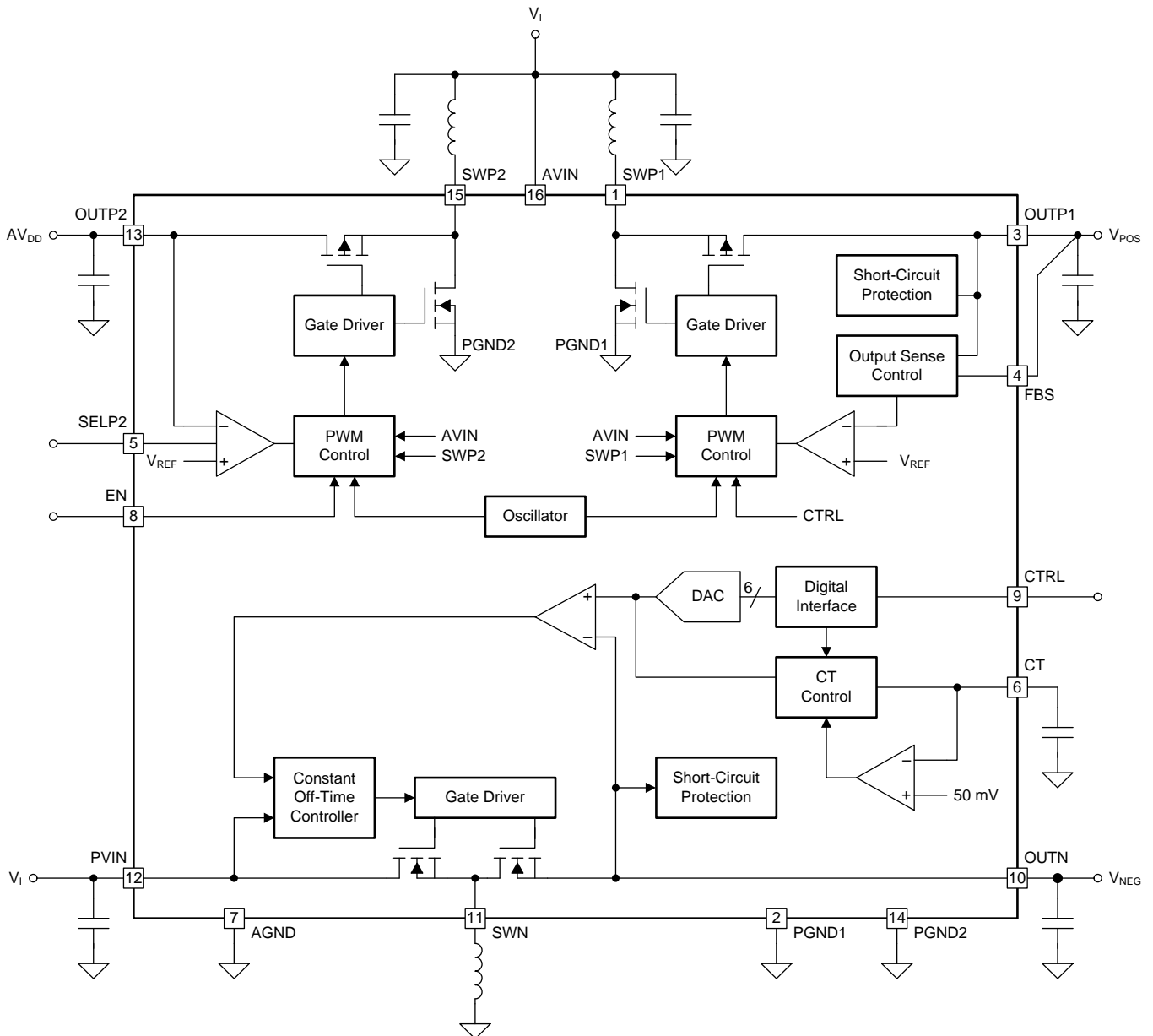
Figure 4. Boost Converter 2 (AV_{DD}) $r_{DS(ON)}$

7 Detailed Description

7.1 Overview

The TPS65632 consists of two boost converters and an inverting buck-boost converter. The V_{POS} output is fixed at 4.6 V and V_{NEG} is programmable via a digital interface in the range of -1.4 V to -5.4 V; the default is -4 V. AV_{DD} can be selected between 7.7 V and 5.8 V, using the SELP2 pin. The transition time of V_{NEG} output is adjustable by the CT pin capacitor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Boost Converter 1 (V_{POS})

Boost converter 1 uses a fixed-frequency current-mode topology. Its output voltage (V_{POS}) is programmed at the factory to 4.6 V and cannot be changed by the user.

For highest output voltage accuracy, connect the output sense pin (FBS) directly to the positive terminal of the main output capacitor. If not used, the FBS pin can be left floating or connected to ground, in which case the boost converter senses the output voltage via the OUTP1 pin.

7.3.1.1 $V_{(POS)}$ Boost Output Sense (FBS Pin)

$V_{(POS)}$ boost has a dedicated output sense pin (FBS). If FBS is floating or connected to ground, $V_{(POS)}$ boost senses the output through OUTP1 pin.

7.3.2 Inverting Buck-Boost Converter (V_{NEG})

The inverting buck-boost converter uses a constant-off-time current-mode topology. The converter's default output voltage (V_{NEG}) is -4.0 V, but it can be programmed from -1.4 V to -5.4 V (see [Programming \$V_{NEG}\$](#)).

7.3.2.1 Programming V_{NEG}

The digital interface allows programming of V_{NEG} in discrete steps. If the output voltage setting function is not required then the CTRL pin can also be used as a standard enable pin. The digital output voltage programming of V_{NEG} is implemented using a simple digital interface with the timing shown in [Figure 5](#).

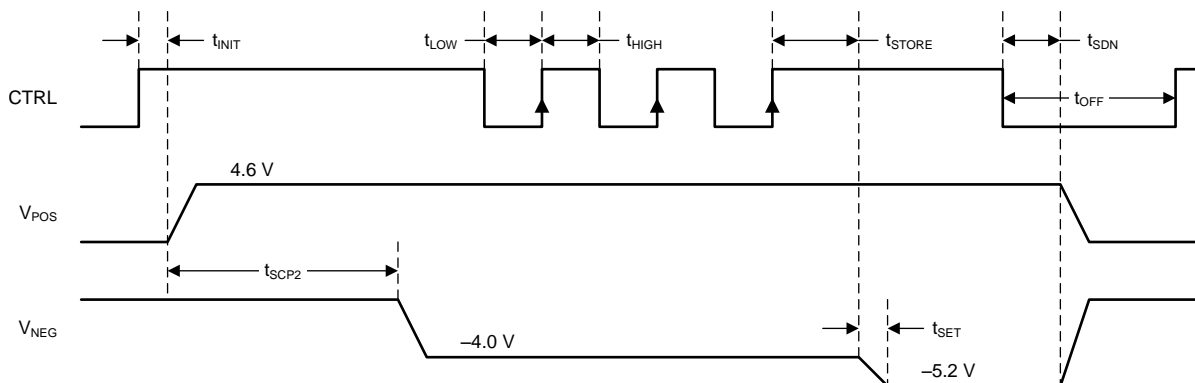


Figure 5. Digital Interface Using CTRL

When CTRL is pulled high the device starts up with its default voltage of -4 V. The device includes a 6-bit DAC that generates the output voltages shown in [Table 1](#). The interface counts the rising edges applied to the CTRL pin once the device is enabled. According to [Table 1](#), V_{NEG} is programmed to -5.2 V since 3 rising edges are detected.

Feature Description (continued)
Table 1.

| Bit / Rising Edges | V _{NEG} | DAC Value | Bit / Rising Edges | V _{NEG} | DAC Value |
|--------------------|------------------|-----------|--------------------|------------------|-----------|
| 0 / no pulse | -4.0 V | 000000 | 21 | -3.4 V | 010101 |
| 1 | -5.4 V | 000001 | 22 | -3.3 V | 010110 |
| 2 | -5.3 V | 000010 | 23 | -3.2 V | 010111 |
| 3 | -5.2 V | 000011 | 24 | -3.1 V | 011000 |
| 4 | -5.1 V | 000100 | 25 | -3.0 V | 011001 |
| 5 | -5.0 V | 000101 | 26 | -2.9 V | 011010 |
| 6 | -4.9 V | 000110 | 27 | -2.8 V | 011011 |
| 7 | -4.8 V | 000111 | 28 | -2.7 V | 011100 |
| 8 | -4.7 V | 001000 | 29 | -2.6 V | 011101 |
| 9 | -4.6 V | 001001 | 30 | -2.5 V | 011110 |
| 10 | -4.5 V | 001010 | 31 | -2.4 V | 011111 |
| 11 | -4.4 V | 001011 | 32 | -2.3 V | 100000 |
| 12 | -4.3 V | 001100 | 33 | -2.2 V | 100001 |
| 13 | -4.2 V | 001101 | 34 | -2.1 V | 100010 |
| 14 | -4.1 V | 001110 | 35 | -2.0 V | 100011 |
| 15 | -4.0 V | 001111 | 36 | -1.9 V | 100100 |
| 16 | -3.9 V | 010000 | 37 | -1.8 V | 100101 |
| 17 | -3.8 V | 010001 | 38 | -1.7 V | 100110 |
| 18 | -3.7 V | 010010 | 39 | -1.6 V | 100111 |
| 19 | -3.6 V | 010011 | 40 | -1.5 V | 101000 |
| 20 | -3.5 V | 010100 | 41 | -1.4 V | 101001 |

7.3.2.2 Controlling V_{NEG} Transition Time

The transition time (t_{SET}) is the time required to move V_{NEG} from one voltage level to the next. Users can control the transition time with a capacitor connected between the CT pin and ground. When the CT pin is left open or connected to ground the transition time is as short as possible. When a capacitor is connected to the CT pin the transition time is determined by the time constant (τ) of the external capacitor ($C_{(CT)}$) and the internal resistance of the CT pin (R_{CT}). The output voltage reaches 70% of its programmed value after 1τ .

An example is given when using 100 nF for $C_{(CT)}$.

$$\tau = 300 \text{ k}\Omega \times 100 \text{ nF} = 30 \text{ ms} \quad (1)$$

The output voltage is at 70% of its final value after 1τ (i.e. 30 ms in this case) and at its final value after approximately 3τ (90 ms in this case).

7.3.3 Boost Converter 2 (AV_{DD})

Boost converter 2 uses a fixed-frequency current-mode topology. The TPS65632 device supports fixed output voltages of 5.8 V and 7.7 V, selected by the SELP2 pin. $AV_{DD} = 7.7 \text{ V}$ when SELP2 is low or left floating, and $AV_{DD} = 5.8 \text{ V}$ when SELP2 is high.

7.3.4 Soft Start and Start-Up Sequence

The devices feature a soft-start function to limit inrush current. Boost converter 2 (AV_{DD}) is enabled when EN goes high. When CTRL goes high, boost converter 1 starts with a reduced switch current limit and 10 ms later the inverting buck-boost converter (V_{NEG}) starts with its default value of -4 V. The typical start-up sequence is shown in [Figure 6](#). The two boost converters operate independently and boost converter 1 (V_{POS}) does not require boost converter 2 (AV_{DD}) to be in regulation in order for it to start..

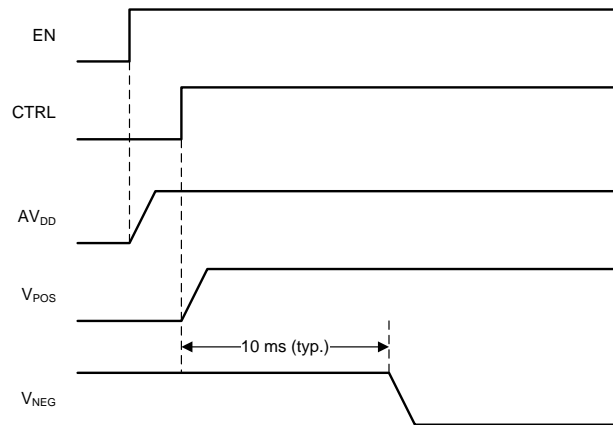


Figure 6. Start-Up Sequence

7.3.5 Enable (CTRL)

The CTRL pin serves two functions: one is to enable and disable the device, and the other is to program the output voltage (V_{NEG}) of the inverting buck-boost converter (see [Programming \$V_{NEG}\$](#)). If the V_{NEG} programming function is not required the CTRL pin can be used as a standard enable pin for the device, which will start up with its default value of -4.0 V on V_{NEG} . The device is enabled when CTRL is pulled high and disabled when CTRL is pulled low.

Note that to ensure proper start up CTRL must be pulled low for a minimum of $200\ \mu\text{s}$ before being pulled high again.

7.3.6 Undervoltage Lockout

The device features an undervoltage lockout function that disables it when the input supply voltage is too low for proper operation.

7.3.7 Short-Circuit Protection

7.3.7.1 Short Circuits During Operation

The device is protected against short circuits of V_{POS} and V_{NEG} to ground and short circuit of these two outputs to each other. During normal operation an error condition is detected if V_{POS} falls below 4.1 V for longer than 3 ms or V_{NEG} is pulled above the programmed nominal output by 500 mV for longer than 3 ms . In either case the device goes into shutdown and the outputs are disconnected from the input. This state is latched, and to resume normal operation, V_I has to cycle below the undervoltage lockout threshold, or CTRL has to toggle LOW and then HIGH.

7.3.7.2 Short Circuits During Start Up

During start up an error condition is detected in the following cases:

- V_{POS} is not in regulation 10 ms after CTRL goes HIGH
- V_{NEG} is higher than threshold level 10 ms after CTRL goes HIGH
- V_{NEG} is not in regulation 20 ms after CTRL goes HIGH

If any of the above conditions is met the device goes into shutdown and the outputs are disconnected from the input. This state is latched, and to resume normal operation V_I has to cycle below the undervoltage threshold, or CTRL has to toggle LOW and HIGH.

7.3.8 Output Discharge During Shut Down

The device discharges outputs during shutdown. [Figure 7](#) shows the discharge control.

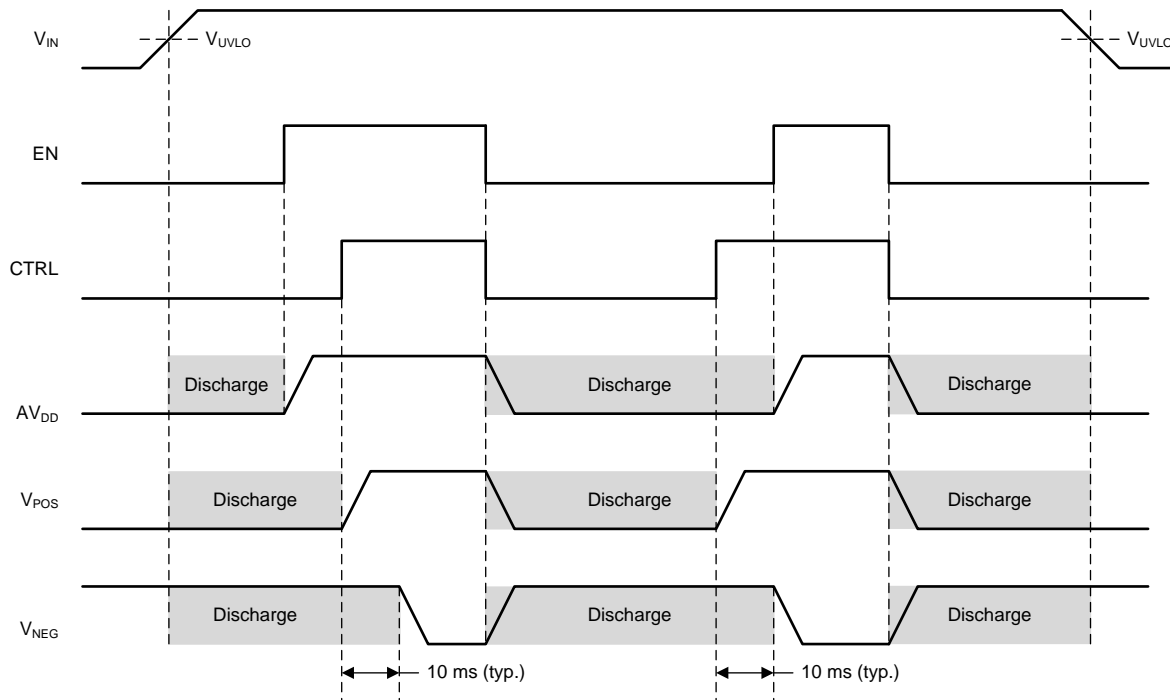


Figure 7. Outputs Discharge During Shut Down

7.3.9 Thermal Shutdown

The TPS65632 device enters thermal shutdown if its junction temperature exceeds 145°C (typical). During thermal shutdown none of the device's functions are available. To resume normal operation V_I has to cycle below the undervoltage threshold, or CTRL has to toggle LOW and then HIGH.

7.4 Device Functional Modes

7.4.1 Operation with $V_I < 2.9\text{ V}$

The recommended minimum input supply voltage for full-performance is 2.9 V. The device continues to operate with input supply voltages below 2.9 V, however, full performance is not guaranteed. The TPS65632 device does not operate with input supply voltages below the UVLO threshold.

7.4.2 Operation with $V_I \approx V_{POS}$ (Diode Mode)

The TPS65632 device features a "diode" mode that enables it to regulate its V_{POS} output even when the input supply voltage is close to V_{POS} (that is, too high for normal boost operation). When operating in diode mode the V_{POS} boost converter's high-side switch is disabled and its body diode used as the rectifier. Note that a minimum load of $\approx 2\text{ mA}$ is required to proper output regulation in diode mode.

7.4.3 Operation with CTRL

When a low-level signal is applied to the CTRL pin the device is disabled and switching is inhibited. When the input supply voltage is above the UVLO threshold and a high-level signal is applied to the CTRL pin the device is enabled and its start-up sequence begins.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65632 device is intended to supply the main analog supplies required by AMOLED displays. V_{POS} is fixed at 4.6 V, but V_{NEG} can be programmed using the CTRL pin to voltages in the range -1.4 V to -5.4 V. The SELP2 pin can be used to set AV_{DD} to either 5.8 V or 7.7 V. The device is highly integrated and requires few external components.

8.2 Typical Application

Figure 8 shows a typical application circuit suitable for supplying AMOLED displays in smartphone applications. The circuit is designed to operate from a single-cell Li-Ion battery and generates a positive output voltage V_{POS} of 4.6 V, a negative output voltage V_{NEG} of -4.0 V, and a positive output voltage AV_{DD} of 5.8 V or 7.7 V. The V_{POS} and V_{NEG} outputs are each capable of supplying up to 300 mA of current, and the AV_{DD} output of up to 30 mA.

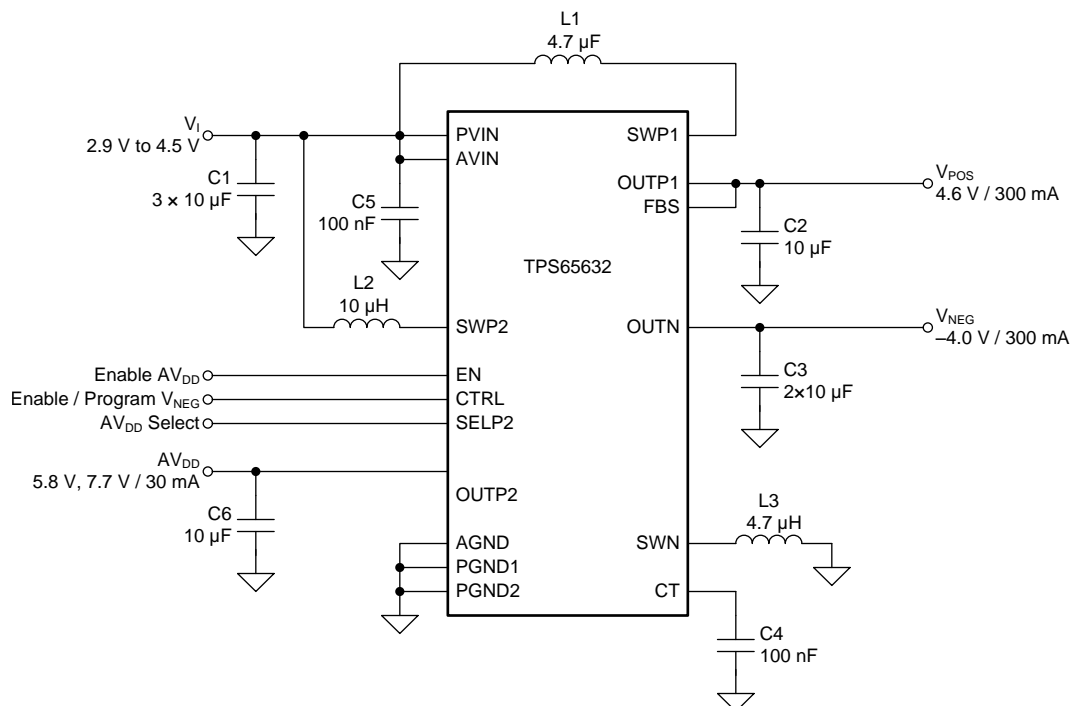


Figure 8. Typical Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters shown in [Table 2](#)

Table 2. Design Parameters

| PARAMETER | VALUE |
|---------------------|------------------------------------------------------------------------------------------------|
| Input voltage range | 2.9 V to 4.5 V |
| Output voltage | $V_{POS} = 4.6\text{ V}$ $V_{NEG} = -4.0\text{ V}$ $AV_{DD} = 7.7\text{ V}$ |
| Current | $I_{(VPOS)} = 300\text{ mA}$ $I_{(VNEG)} = 300\text{ mA}$ $I_{(AVDD)} = 30\text{ mA}$ |
| Switching Frequency | $f_{(SWP1)} = 1.7\text{ MHz}$ $f_{(SWN)} = 1.7\text{ MHz}$ $f_{(SWP2)} = 1.7\text{ MHz}$ |

8.2.2 Detailed Design Procedure

In order to maximize performance, the TPS65632 device has been optimized for use with a relatively narrow range of component values, and customers are strongly recommended to use the application circuits shown in [Figure 8](#) with the components listed in [Table 3](#) and [Table 4](#).

8.2.2.1 Inductor Selection

The V_{POS} and V_{NEG} converters have been optimized for use with 4.7- μH inductors and the AV_{DD} boost converter has been optimized for use with 10- μH inductors. For optimum performance it is recommended that these values be used in all applications. Customers using different inductors than the ones in [Table 3](#) are strongly recommended to characterize circuit performance fully before finalizing their design. Customers should pay particular attention to the inductors' saturation current and ensure it is adequate for their application's worst-case conditions (which may also be during start-up).

Table 3. Inductor Selection

| REFERENCE DESIGNATOR | VALUE | MANUFACTURER | PART NUMBER |
|----------------------|-------------------|--------------|-----------------|
| L1, L3 | 4.7 μH | Coilcraft | XFL4020-4R7ML |
| L2 | 10 μH | Coilmaster | MMPP252012-100N |

8.2.2.2 Capacitor Selection

The recommended capacitor values are shown in [Table 4](#). Applications using less than the recommended capacitance (e.g. to save PCB area) may exhibit increased voltage ripple. In general, the lower the output current, the lower the necessary capacitance. Customers should be aware that ceramic capacitors of the kind typically used with the TPS65632 device exhibit dc bias effects, which means their effective capacitance under normal operating conditions may be significantly lower than their nominal capacitance value. Customers must ensure that the *effective* capacitance is sufficient for their application's performance requirements.

Table 4. Capacitor Selection

| REFERENCE DESIGNATOR | VALUE | MANUFACTURER | PART NUMBER |
|----------------------|-----------------------------|--------------|-------------------|
| C1 | 3 \times 10 μF | Murata | GRM21BR71A106KE51 |
| C2, C6 | 10 μF | Murata | GRM21BR71A106KE51 |
| C3 | 2 \times 10 μF | Murata | GRM21BR71A106KE51 |
| C4, C5 | 100 nF | Murata | GRM155B11A104KA01 |

8.2.3 Application Curves

Unless otherwise stated: $T_A = 25^\circ\text{C}$, $V_I = 3.7\text{ V}$, $V_{\text{POS}} = 4.6\text{ V}$, $V_{\text{NEG}} = -4.0\text{ V}$, $AV_{\text{DD}} = 7.7\text{ V}$; $L1 = L3 = \text{XFL4020-4R7ML}$, and $L2 = \text{MMPP252012-100N}$.

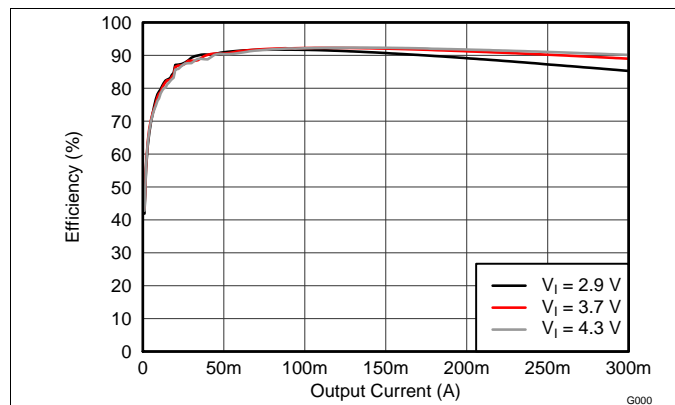


Figure 9. V_{POS} and V_{NEG} Combined Efficiency

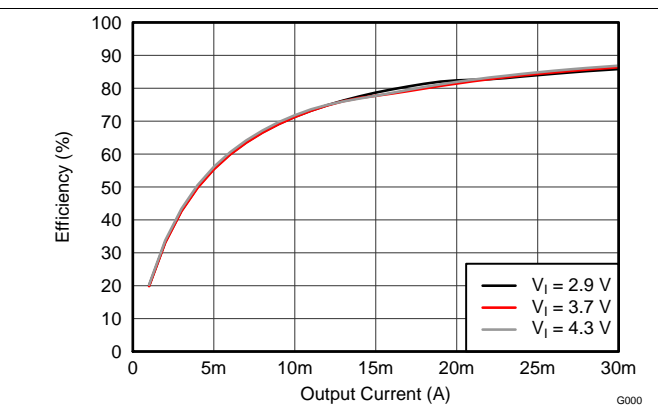


Figure 10. AV_{DD} Efficiency

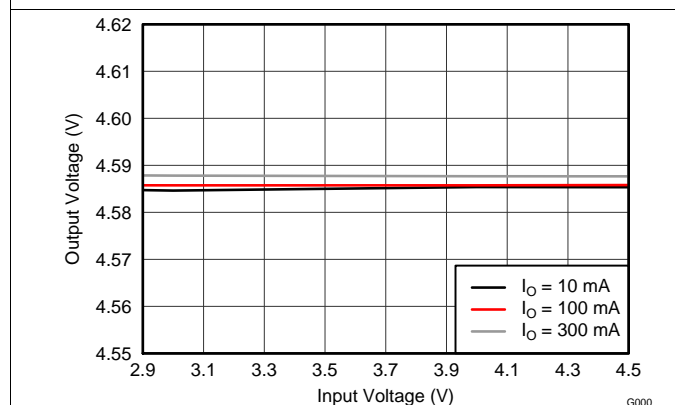


Figure 11. V_{POS} Line Regulation

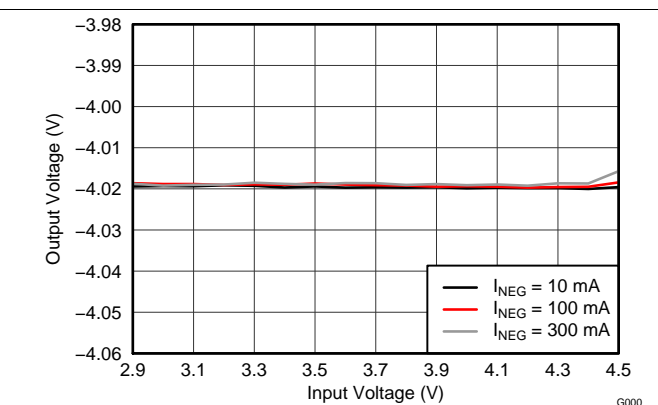


Figure 12. V_{NEG} Line Regulation

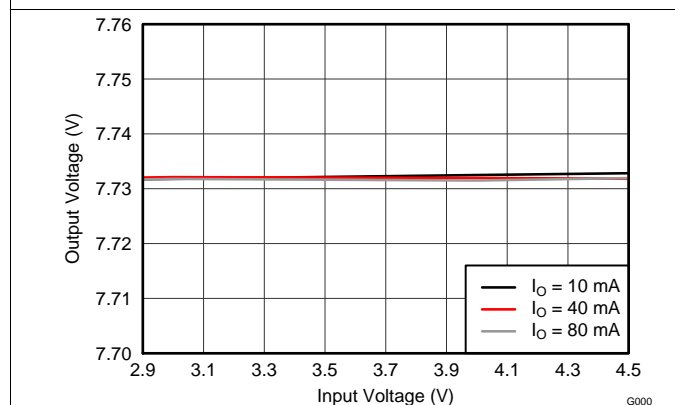


Figure 13. AV_{DD} Line Regulation

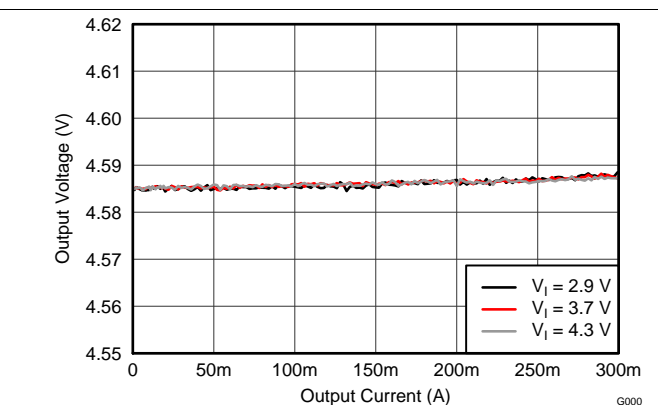


Figure 14. V_{POS} Load Regulation

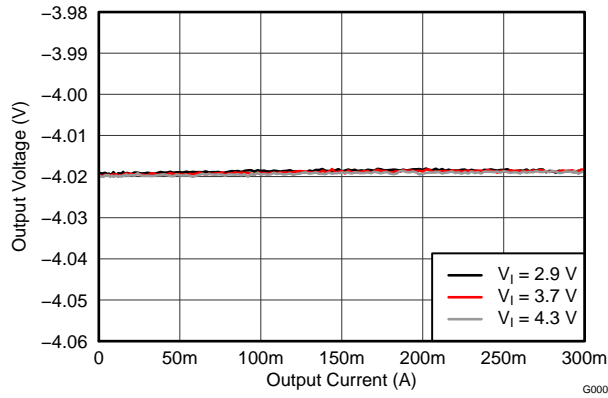


Figure 15. V_{NEG} Load Regulation

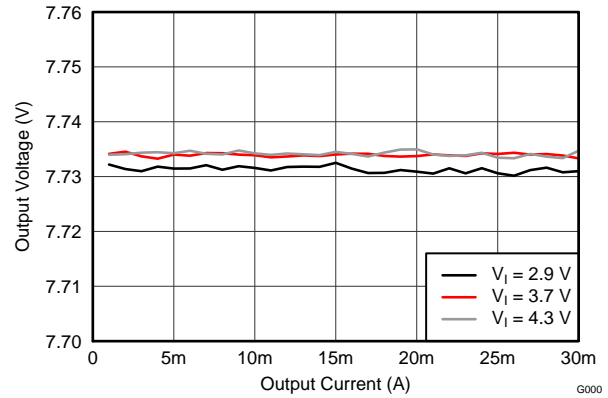


Figure 16. AV_{DD} Load Regulation

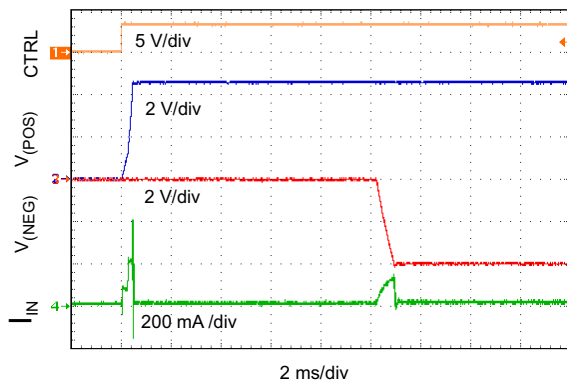


Figure 17. Start-Up: V_{POS} and V_{NEG}

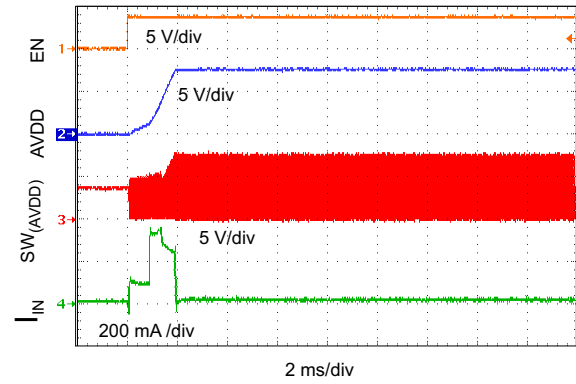


Figure 18. Start-Up: AV_{DD}

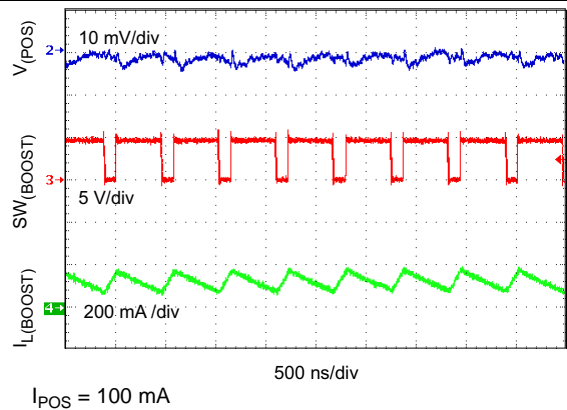


Figure 19. Switch Pin, Inductor Current and Output Voltage Waveforms: V_{POS}

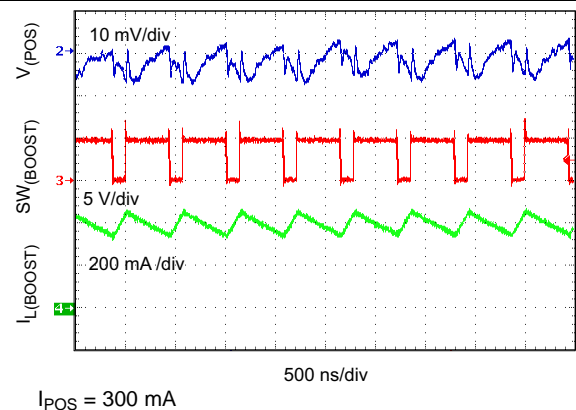


Figure 20. Switch Pin, Inductor Current and Output Voltage Waveforms: V_{POS}

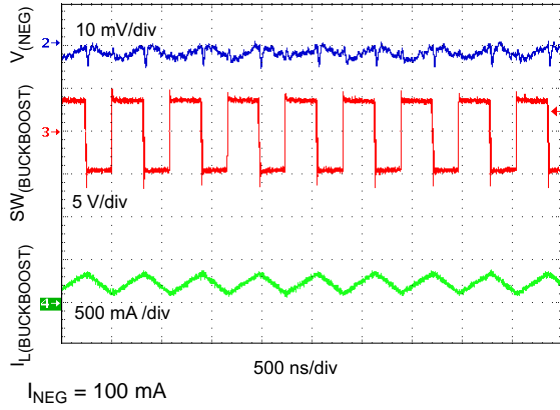


Figure 21. Switch Pin, Inductor Current and Output Voltage Waveforms: V_{NEG}

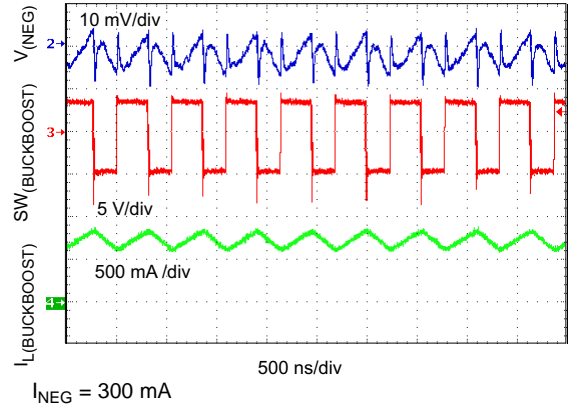


Figure 22. Switch Pin, Inductor Current and Output Voltage Waveforms: V_{NEG}

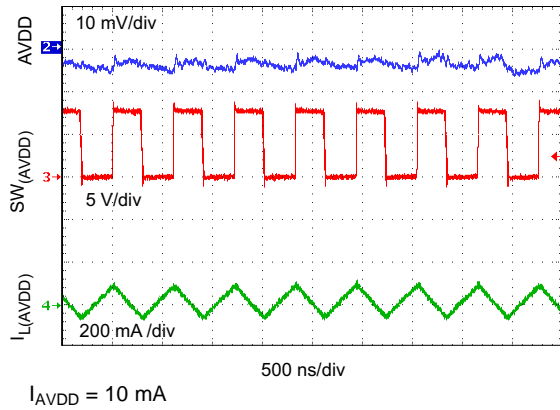


Figure 23. Switch Pin, Inductor Current and Output Voltage Waveforms: AV_{DD}

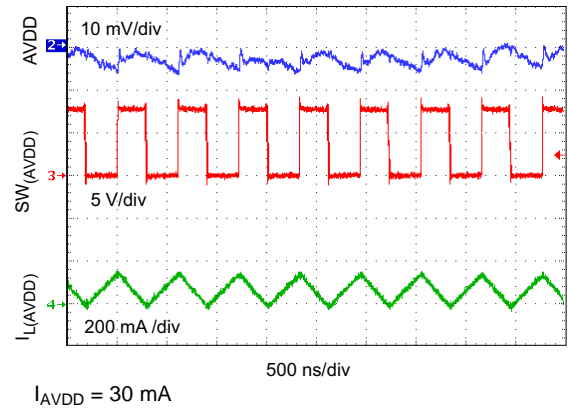


Figure 24. Switch Pin, Inductor Current and Output Voltage Waveforms: AV_{DD}

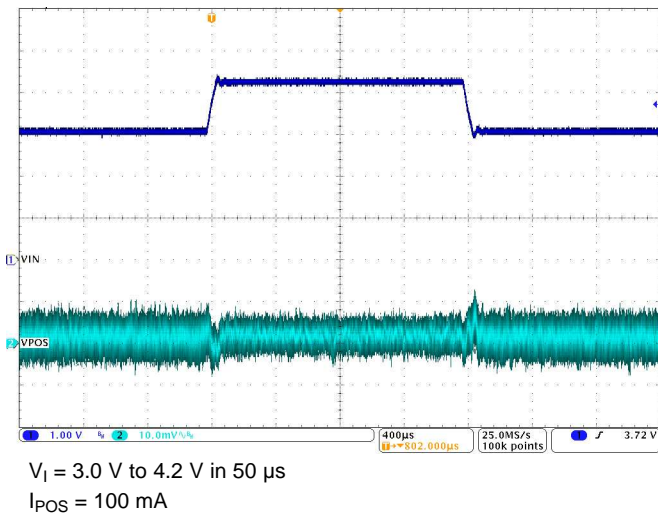


Figure 25. V_{POS} Line Transient Response

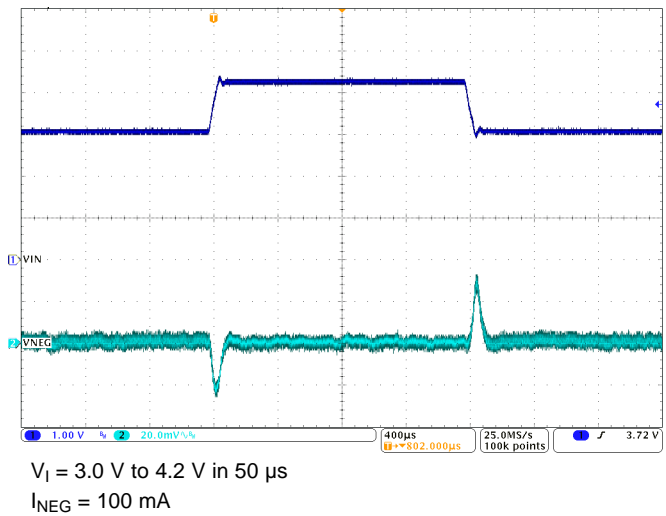
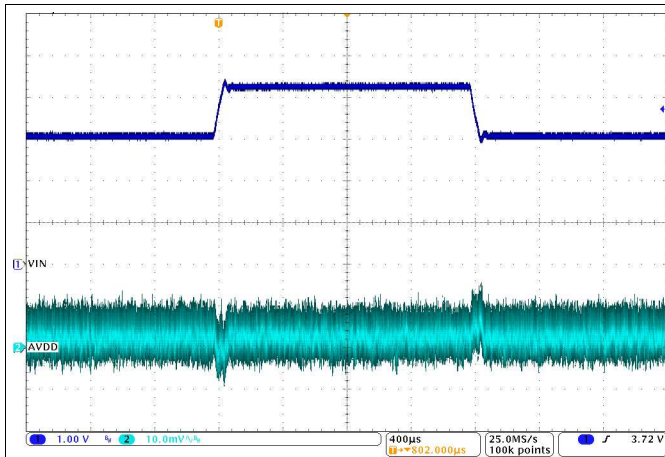
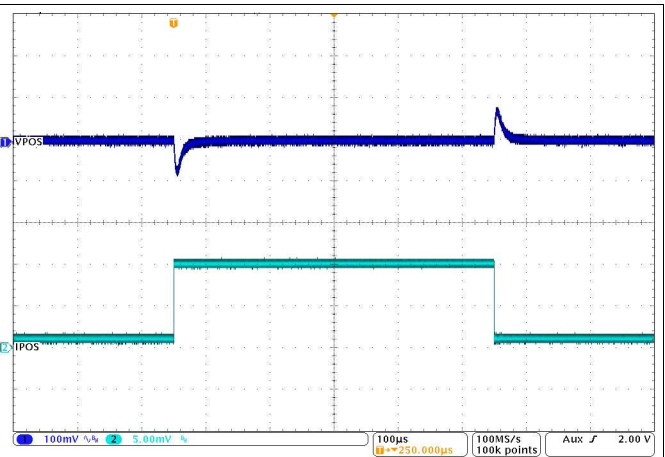


Figure 26. V_{NEG} Line Transient Response



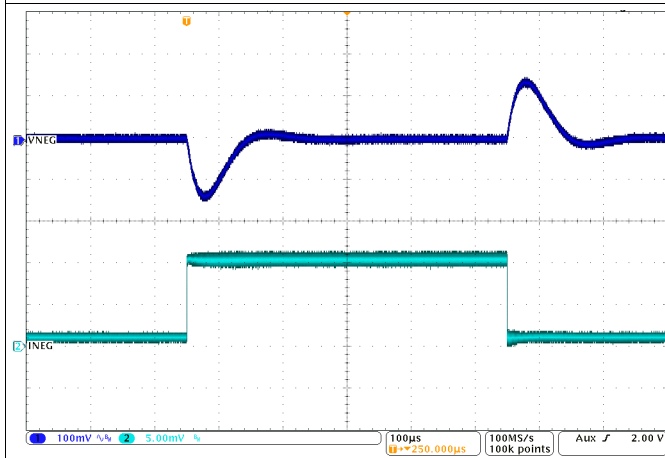
$V_I = 3.0\text{ V to } 4.2\text{ V in } 50\ \mu\text{s}$
 $I_{AVDD} = 30\text{ mA}$

Figure 27. AV_{DD} Line Transient Response



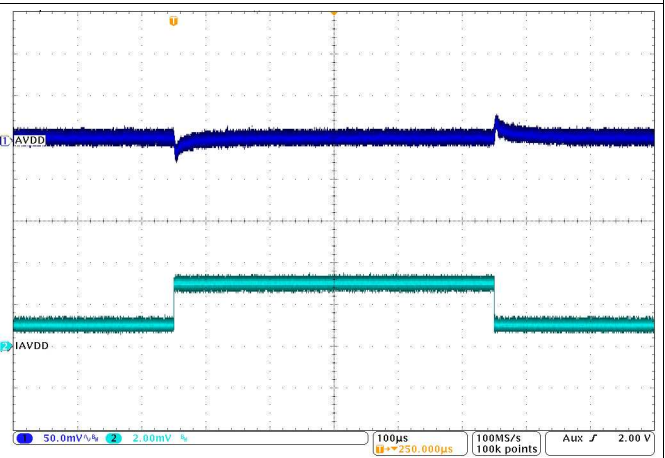
$I_{POS} = 10\text{ mA to } 100\text{ mA in } 100\text{ ns}$

Figure 28. V_{POS} Load Transient Response



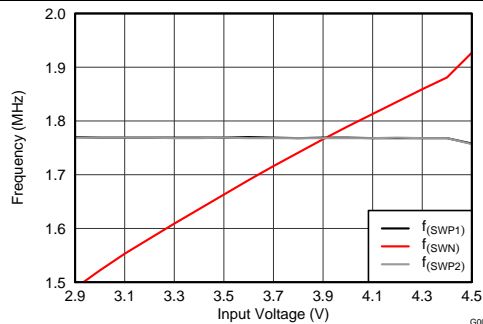
$I_{NEG} = 10\text{ mA to } 100\text{ mA in } 100\text{ ns}$

Figure 29. V_{NEG} Load Transient Response



$I_{AVDD} = 10\text{ mA to } 30\text{ mA in } 100\text{ ns}$

Figure 30. AV_{DD} Load Transient Response



$I_{POS} = 100\text{ mA}$

$I_{NEG} = 100\text{ mA}$

$I_{AVDD} = 30\text{ mA}$

Figure 31. Switching Frequency

9 Power Supply Recommendations

The TPS65632 device is designed to operate with input supply voltages in the range 2.9 V to 4.5 V. If the input supply voltage is located more than a few centimeters away from the device, additional bulk capacitance may be required. The three 10- μ F capacitors shown in [Figure 8](#) are suitable for typical applications.

10 Layout

10.1 Layout Guidelines

- Place the input capacitor on PVIN and the output capacitor on OUTN as close as possible to device. Use short and wide traces to connect the input capacitor on PVIN and the output capacitor on OUTN.
- Place the output capacitor on OUTP1 and OUTP2 as close as possible to device. Use short and wide traces to connect the output capacitor on OUTP1 and OUTP2.
- Connect the ground of CT capacitor with AGND, pin 7, directly.
- Connect input ground and output ground on the same board layer, not through via hole.
- Connect AGND, PGND1 and PGND2 with exposed thermal pad.

10.2 Layout Example

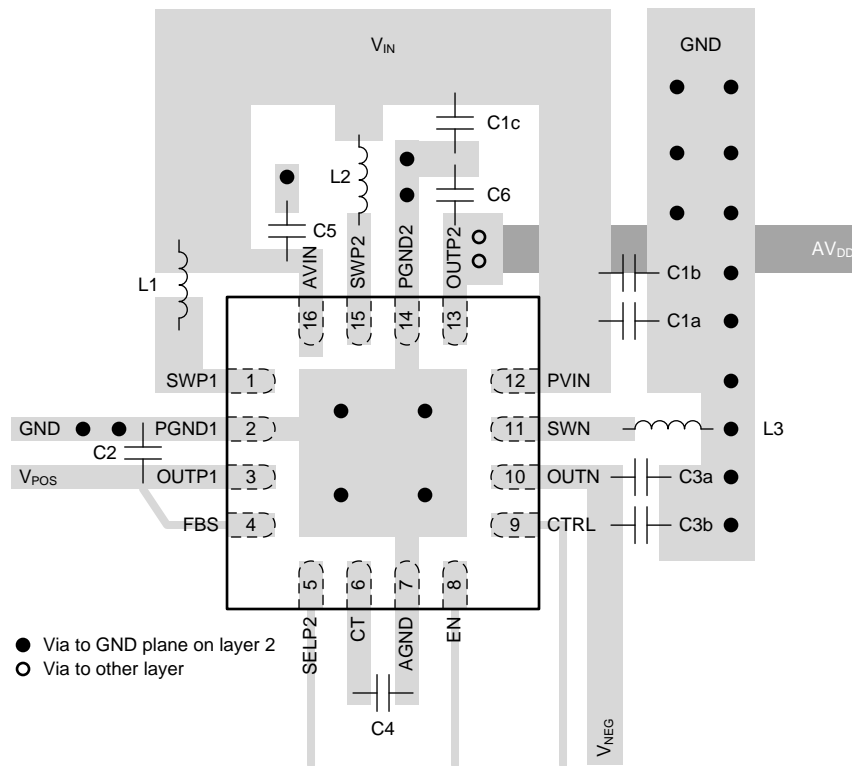


Figure 32. Recommended PCB Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Ordering Information

The following pages include mechanical, packaging, and ordering information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS65632RTER | ACTIVE | WQFN | RTE | 16 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PC6I | Samples |
| TPS65632RTET | ACTIVE | WQFN | RTE | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PC6I | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS65632RTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS65632RTET | WQFN | RTE | 16 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS65632RTER | WQFN | RTE | 16 | 3000 | 335.0 | 335.0 | 25.0 |
| TPS65632RTET | WQFN | RTE | 16 | 250 | 182.0 | 182.0 | 20.0 |

GENERIC PACKAGE VIEW

RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

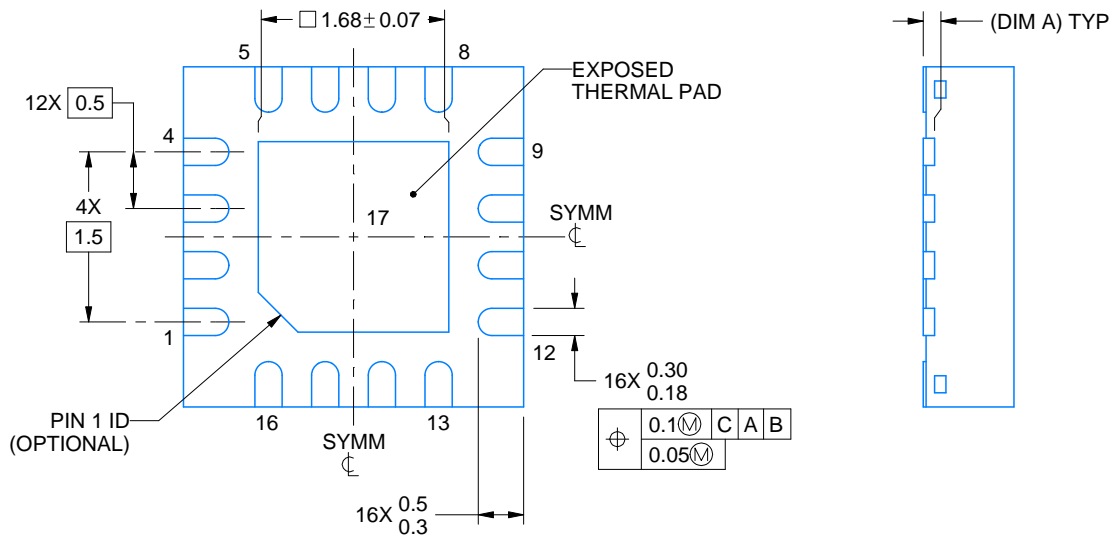
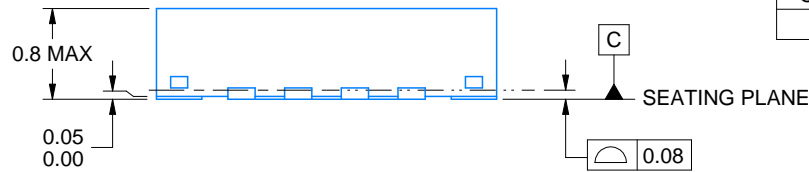
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



| SIDE WALL METAL THICKNESS DIM A | |
|---------------------------------|----------|
| OPTION 1 | OPTION 2 |
| 0.1 | 0.2 |



4219117/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



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NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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