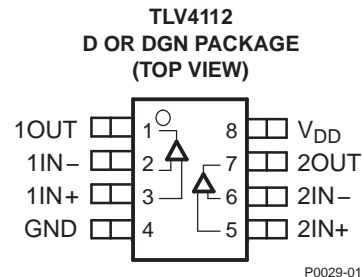


HIGH-OUTPUT-DRIVE OPERATIONAL AMPLIFIERS WITH SHUTDOWN

FEATURES

- **Controlled Baseline**
 - One Assembly Site
 - One Test Site
 - One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree ⁽¹⁾**
- **High Output Drive . . . >300 mA**
- **Rail-To-Rail Output**
- **Unity-Gain Bandwidth . . . 2.7 MHz**
- **Slew Rate . . . 1.5 V/μs**
- **Supply Current . . . 700 μA/Per Channel**
- **Supply Voltage Range . . . 2.5 V to 6 V**
- **Universal Op Amp EVM**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.



DESCRIPTION

The TLV411x single-supply operational amplifiers provide output currents in excess of 300 mA at 5 V. This enables standard pin-out amplifiers to be used as high current buffers or in coil driver applications. The TLV4110 and TLV4113 come with a shutdown feature.

The TLV411x is available in the ultra-small MSOP PowerPAD™ package, which offers the exceptional thermal impedance required for amplifiers delivering high current levels.

All TLV411x devices are offered in SOIC (single and dual) and MSOP PowerPAD (dual).

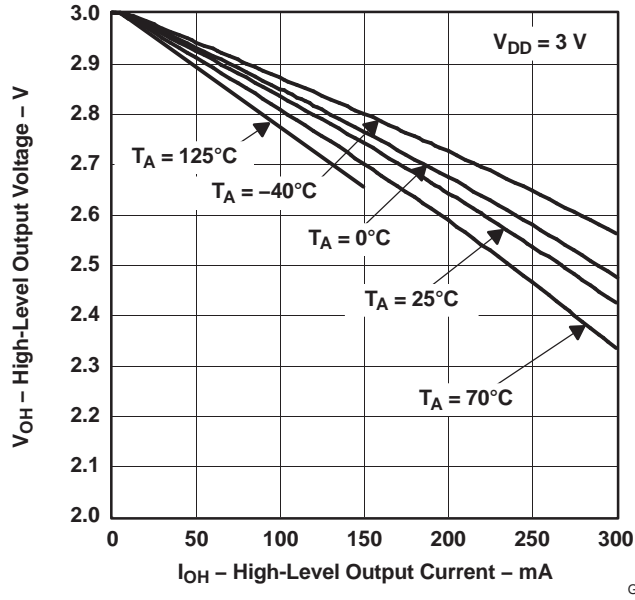
FAMILY PACKAGE TABLE

| DEVICE | NUMBER OF CHANNELS | PACKAGE TYPES | | SHUTDOWN | UNIVERSAL EVM BOARD |
|---------|--------------------|---------------|------|----------|---|
| | | MSOP | SOIC | | |
| TLV4110 | 1 | 8 | 8 | Yes | See the EVM Selection Guide (SLOU060) |
| TLV4111 | 1 | 8 | 8 | – | |
| TLV4112 | 2 | 8 | 8 | – | |
| TLV4113 | 2 | 10 | 14 | Yes | |

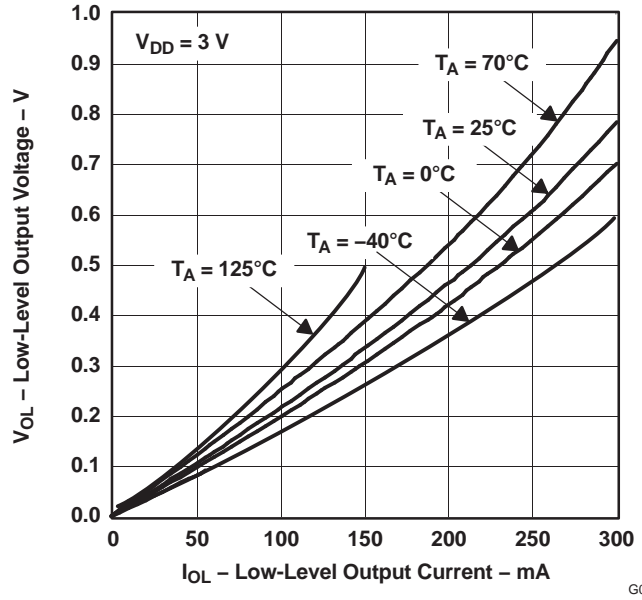


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.
Parts, Microsim PSpice are trademarks of MicroSim Corporation.



G004



G005

TLV4110 AND TLV4111 AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | | |
|----------------|--------------------------------------|------------------------------------|--------|
| | SMALL OUTLINE (D) ^{(1) (2)} | MSOP | |
| | | SMALL OUTLINE (DGN) ⁽¹⁾ | SYMBOL |
| -55°C to 125°C | TLV4110MDREP ⁽³⁾ | TLV4110MDGNREP ⁽³⁾ | BTB |
| | TLV4111MDREP ⁽³⁾ | TLV4111MDGNREP ⁽³⁾ | BTC |

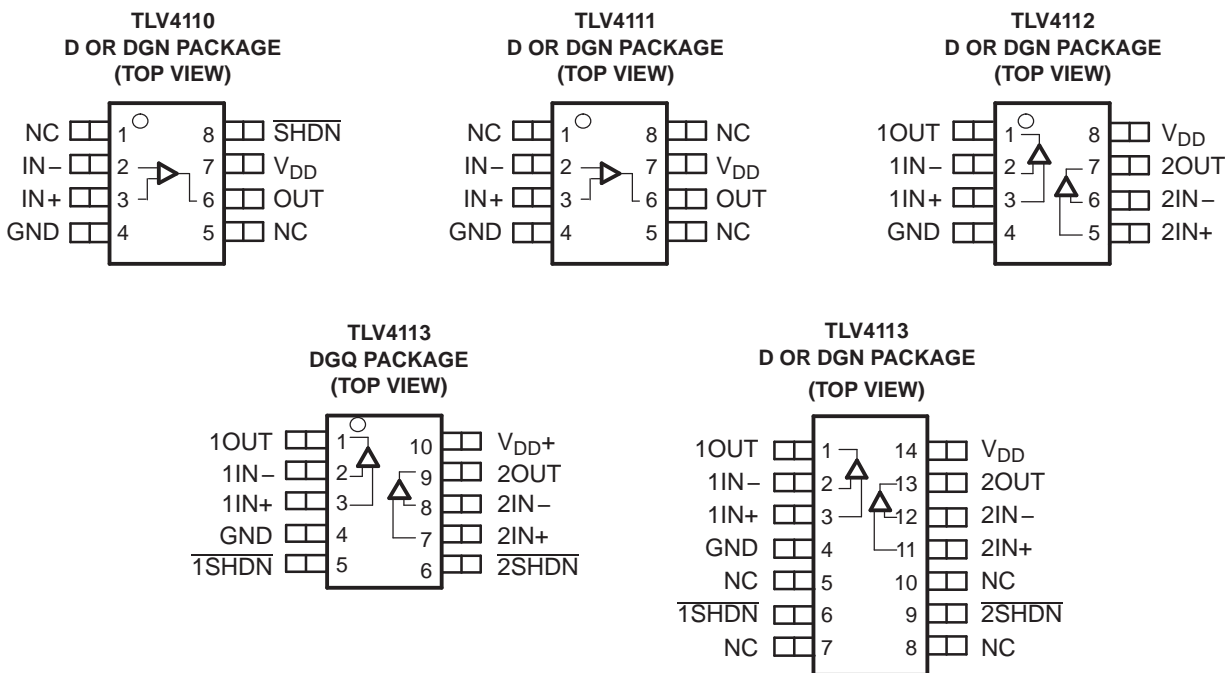
- (1) The R designation indicates package is taped and reeled.
- (2) In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.
- (3) Product preview.

TLV4112 AND TLV4113 AVAILABLE OPTIONS

| T _A | PACKAGED DEVICES | | | | |
|----------------|--------------------------------------|------------------------------------|--------|------------------------------------|--------|
| | SMALL OUTLINE (D) ^{(1) (2)} | MSOP | | | |
| | | SMALL OUTLINE (DGN) ⁽¹⁾ | SYMBOL | SMALL OUTLINE (DGQ) ⁽¹⁾ | SYMBOL |
| -55°C to 125°C | TLV4112MDREP ⁽³⁾ | TLV4112MDGNREP ⁽³⁾ | BTD | – | – |
| | TLV4113MDREP ⁽³⁾ | – | – | TLV4113MDGQREP | BTE |

- (1) The R designation indicates package is taped and reeled.
- (2) In the SOIC package, the maximum RMS output power is thermally limited to 350 mW; 700 mW peaks can be driven, as long as the RMS value is less than 350 mW.
- (3) Product preview.

TLV411X PACKAGE PINOUTS



NC – No internal connection

P0029-02

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | | |
|------------------|---|------------------------|------------------------------|
| V _{DD} | Supply voltage ⁽²⁾ | | 7 V |
| V _{ID} | Differential input voltage | | ±V _{DD} |
| V _I | Input voltage range | | ±V _{DD} |
| I _O | Output current ⁽³⁾ | | 800 mA |
| I _O | Continuous <u>RMS</u> output current (each output of amplifier) | T _J ≤ 105°C | 350 mA |
| | | T _J ≤ 150°C | 110 mA |
| I _O | Peak output current (each output of amplifier) | T _J ≤ 105°C | 500 mA |
| | | T _J ≤ 150°C | 155 mA |
| | Continuous total power dissipation | | See Dissipation Rating Table |
| T _A | Operating free-air temperature range | | –55°C to 125°C |
| T _J | Maximum junction temperature | | 150°C |
| T _{stg} | Storage temperature range | | –65°C to 150°C |
| | Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260°C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to GND.
- (3) To prevent permanent damage, the die temperature must not exceed the maximum junction temperature.

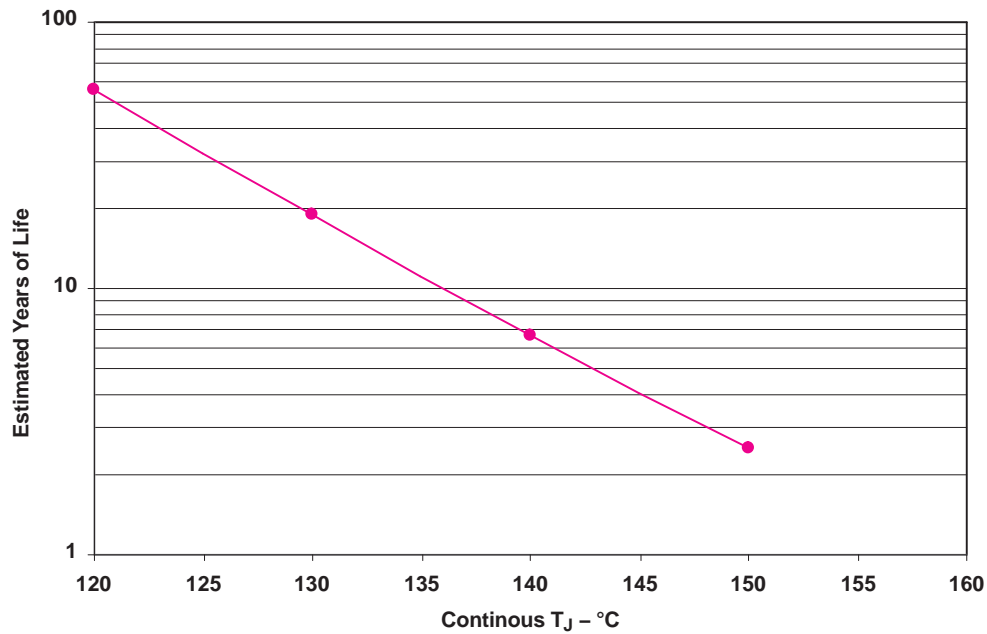


Figure 1. TLV4113MDGQ Wirebond Life

DISSIPATION RATING TABLE

| PACKAGE | θ_{JC} (°C/W) | θ_{JA} (°C/W) | $T_A \leq 25^\circ\text{C}$ POWER RATING | $T_A = 25^\circ\text{C}$ POWER RATING |
|-------------------------|-------------------------|-------------------------|---|--|
| D (8) | 38.3 | 176 | 710 mW | 142 mW |
| D (14) | 26.9 | 122.3 | 1022 mW | 204.4 mW |
| DGN (8) ⁽¹⁾ | 4.7 | 52.7 | 2.37 W | 474.4 mW |
| DGQ (10) ⁽¹⁾ | 4.7 | 52.3 | 2.39 W | 478 mW |

(1) See the Texas Instruments document, *PowerPAD Thermally Enhanced Package Application Report (SLMA002)*, for more information on the PowerPAD package. The thermal data was measured on a PCB layout, based on information in the section entitled *Texas Instruments Recommended Board for PowerPAD*, on page 33 of SLMA002.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|--|---------------------------------|-----------------------|-----------------------|------|
| V _{DD} | Supply voltage | 2.5 | 6 | V |
| V _{ICR} | Common-mode input voltage range | 0 | V _{DD} – 1.5 | V |
| T _A | Operating free-air temperature | –55 | 125 | °C |
| Shutdown turnon/off voltage level ⁽¹⁾ | V(on) | V _{DD} = 3 V | 2.1 | V |
| | | V _{DD} = 5 V | 3.8 | |
| | V(off) | V _{DD} = 3 V | 0.9 | V |
| | | V _{DD} = 5 V | 1.65 | |

(1) Relative to GND

ELECTRICAL CHARACTERISTICS

at recommended operating conditions, V_{DD} = 3 V and 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | T _A ⁽¹⁾ | MIN | TYP | MAX | UNIT |
|------------------------------|---|--|-------------------------------|------------|------|------|-------|
| DC PERFORMANCE | | | | | | | |
| V _{IO} | Input offset voltage | V _{IC} = V _{DD} /2, V _O = V _{DD} /2, R _L = 100 Ω, R _S = 50 Ω | 25°C | 175 | 3500 | | μV |
| | | | Full range | | | 4000 | |
| αV _{IO} | Offset voltage drift | | 25°C | 3 | | | μV/°C |
| CMRR | Common-mode rejection ratio | V _{DD} = 3 V, R _S = 50 Ω, V _{IC} = 0 to 2 V | 25°C | 63 | | | dB |
| | | V _{DD} = 5 V, R _S = 50 Ω, V _{IC} = 0 to 4 V | 25°C | 68 | | | |
| A _{VD} | Large-signal differential voltage amplification | V _{DD} = 3 V | R _L = 100 Ω | 25°C | 78 | 84 | dB |
| | | | | Full range | 67 | | |
| | | | R _L = 10 kΩ | 25°C | 85 | 100 | |
| | | | | Full range | 75 | | |
| | | V _{DD} = 5 V | R _L = 100 Ω | 25°C | 88 | 94 | |
| | | | | Full range | 75 | | |
| | | | R _L = 10 kΩ | 25°C | 90 | 110 | |
| | | | | Full range | 85 | | |
| INPUT CHARACTERISTICS | | | | | | | |
| I _{IO} | Input offset current | | 25°C | 0.3 | 25 | pA | |
| | | | Full range | | 1000 | | |
| I _{IB} | Input bias current | | 25°C | 0.3 | 50 | pA | |
| | | | Full range | | 2000 | | |
| ri(d) | Differential input resistance | | 25°C | 1000 | | | GΩ |
| CIC | Common-mode input capacitance | f = 100 Hz | 25°C | 5 | | | pF |

(1) Full range is –55°C to 125°C.

ELECTRICAL CHARACTERISTICS (continued)

at specified free-air temperature, $V_{DD} = 3\text{ V}$ and 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A^{(1)}$ | MIN | TYP | MAX | UNIT |
|-------------------------------|---|--|---------------------------|-------------|-----------|------|---------------|------|
| OUTPUT CHARACTERISTICS | | | | | | | | |
| V_{OH} | High-level output voltage | $V_{DD} = 3\text{ V},$ $V_{IC} = V_{DD}/2$ | $I_{OH} = -10\text{ mA}$ | 25°C | 2.7 | 2.97 | | V |
| | | | | Full range | 2.6 | | | |
| | | | $I_{OH} = -100\text{ mA}$ | 25°C | 2.6 | 2.73 | | |
| | | | | Full range | 2.5 | | | |
| | | $V_{DD} = 5\text{ V},$ $V_{IC} = V_{DD}/2$ | $I_{OH} = -10\text{ mA}$ | 25°C | 4.7 | 4.96 | | V |
| | | | | Full range | 4.6 | | | |
| | | | $I_{OH} = -100\text{ mA}$ | 25°C | 4.6 | 4.76 | | |
| | | | | Full range | 4.5 | | | |
| V_{OL} | Low-level output voltage | $V_{DD} = 3\text{ V and } 5\text{ V},$ $V_{IC} = V_{DD}/2$ | $I_{OL} = 10\text{ mA}$ | 25°C | | 0.03 | 0.1 | V |
| | | | | Full range | | | 0.2 | |
| | | | $I_{OL} = 100\text{ mA}$ | 25°C | | 0.33 | 0.4 | |
| | | | | Full range | | | 0.55 | |
| I_O | Output current | Measured at 0.5 V from rail | $V_{DD} = 3\text{ V}$ | 25°C | ± 220 | | mA | |
| | | | $V_{DD} = 5\text{ V}$ | | ± 320 | | | |
| I_{OS} | Short-circuit output current | Sourcing | 25°C | 800 | | mA | | |
| | | Sinking | | 800 | | | | |
| POWER SUPPLY | | | | | | | | |
| I_{DD} | Supply current (per channel) | $V_O = V_{DD}/2$ | 25°C | | 700 | 1000 | μA | |
| | | | Full range | | | 1500 | | |
| PSRR | Power supply rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$) | $V_{DD} = 2.7\text{ to } 3.3\text{ V},$ No load $V_{IC} = V_{DD}/2\text{ V}$ | 25°C | 69 | 82 | | dB | |
| | | | Full range | 65 | | | | |
| | | $V_{DD} = 4.5\text{ to } 5.5\text{ V},$ No load $V_{IC} = V_{DD}/2\text{ V}$ | 25°C | 69 | 79 | | dB | |
| | | | Full range | 65 | | | | |

(1) Full range is -55°C to 125°C .

ELECTRICAL CHARACTERISTICS (continued)

 at specified free-air temperature, $V_{DD} = 3\text{ V}$ and 5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | $T_A^{(1)}$ | MIN | TYP | MAX | UNIT |
|-------------------------------------|--|---|------------------------|-------------|-------|------|------------------------|------------------|
| DYNAMIC PERFORMANCE | | | | | | | | |
| GBWP | Gain bandwidth product | $R_L = 100\ \Omega$, $C_L = 10\ \text{pF}$ | | 25°C | 2.7 | | | MHz |
| SR | Slew rate at unity gain | $V_{O(pp)} = 2.5\ \text{V}$, $R_L = 100\ \Omega$, $C_L = 10\ \text{pF}$ | $V_{DD} = 3\ \text{V}$ | 25°C | 0.8 | 1.57 | | V/ μs |
| | | | | Full range | 0.4 | | | |
| | | | $V_{DD} = 5\ \text{V}$ | 25°C | 1 | 1.57 | | |
| | | | | Full range | 0.5 | | | |
| ϕ_M | Phase margin | $R_L = 100\ \Omega$, $C_L = 10\ \text{pF}$ | | 25°C | 66 | | | |
| | Gain margin | $R_L = 100\ \Omega$, $C_L = 10\ \text{pF}$ | | 25°C | 16 | | dB | |
| t_s | Settling time | $V(\text{STEP})_{pp} = 1\ \text{V}$, $A_V = -1$, $C_L = 10\ \text{pF}$, $R_L = 100\ \Omega$ | 0.1% | 25°C | 0.7 | | 1.3 | μs |
| | | | 0.01% | | | | | |
| NOISE/DISTORTION PERFORMANCE | | | | | | | | |
| THD+N | Total harmonic distortion, plus noise | $V_{O(pp)} = V_{DD}/2\ \text{V}$, $R_L = 100\ \Omega$, $f = 100\ \text{Hz}$ | $A_V = 1$ | 25°C | 0.025 | | | |
| | | | $A_V = 10$ | | 0.035 | | | |
| | | | $A_V = 100$ | | 0.15 | | | |
| V_n | Equivalent input noise voltage | $f = 100\ \text{Hz}$ | $f = 10\ \text{Hz}$ | 25°C | 55 | | nV/ $\sqrt{\text{Hz}}$ | |
| | | | | | 10 | | | |
| I_n | Equivalent input noise current | $f = 1\ \text{Hz}$ | | 25°C | 0.31 | | fA/ $\sqrt{\text{Hz}}$ | |
| SHUTDOWN CHARACTERISTICS | | | | | | | | |
| $I_{DD(\text{SHDN})}$ | Supply current in shutdown mode (per channel) (TLV4110, TLV4113) | $\overline{\text{SHDN}} = 0\ \text{V}$ | | 25°C | 3.4 | 10 | μA | |
| | | | | Full range | 15 | | | |
| $t_{(\text{ON})}$ | Amplifier turnon time ⁽²⁾ | $R_L = 100\ \Omega$ | | 25°C | 1 | | μs | |
| $t_{(\text{OFF})}$ | Amplifier turnoff time ⁽²⁾ | | | | 3.3 | | | |

 (1) Full range is -55°C to 125°C .

 (2) Disable time and enable time are defined as the interval between application of the logic signal to $\overline{\text{SHDN}}$ and the point at which the supply current has reached half its final value.

TYPICAL CHARACTERISTICS

Table of Graphs

| | | | FIGURE |
|-----------|--|------------------------------|--------|
| V_{IO} | Input offset voltage | vs Common-mode input voltage | 2, 3 |
| CMRR | Common-mode rejection ratio | vs Frequency | 4 |
| V_{OH} | High-level output voltage | vs High-level output current | 5, 7 |
| V_{OL} | Low-level output voltage | vs Low-level output current | 6, 8 |
| Z_o | Output impedance | vs Frequency | 9 |
| I_{DD} | Supply current | vs Supply voltage | 10 |
| k_{SVR} | Power supply voltage rejection ratio | vs Frequency | 11 |
| A_{VD} | Differential voltage amplification and phase | vs Frequency | 12 |
| | Gain-bandwidth product | vs Supply voltage | 13 |
| SR | Slew rate | vs Supply voltage | 14 |
| | | vs Temperature | 15 |
| | Total harmonic distortion+noise | vs Frequency | 16 |
| V_n | Equivalent input voltage noise | vs Frequency | 17 |
| | Phase margin | vs Capacitive load | 18 |
| | Voltage-follower signal pulse response | | 19, 20 |
| | Inverting large-signal pulse response | | 21 |
| | Small-signal inverting pulse response | | 22 |
| | Crosstalk | vs Frequency | 23 |
| | Shutdown forward and reverse isolation | | 24 |
| | Shutdown supply current | vs Free-air temperature | 25 |
| | Shutdown supply current/output voltage | | 26 |

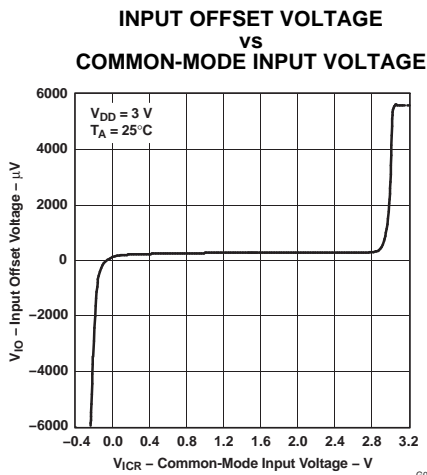


Figure 2.

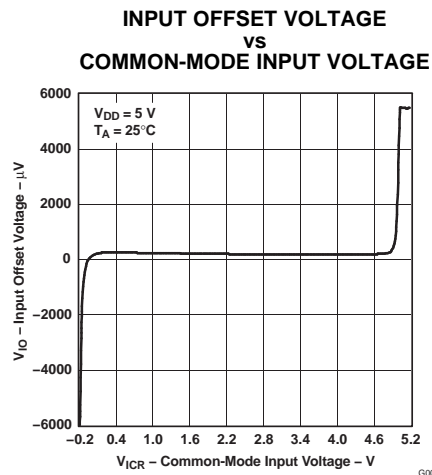


Figure 3.

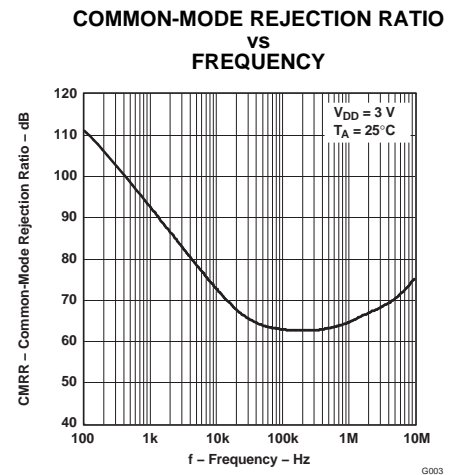


Figure 4.

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

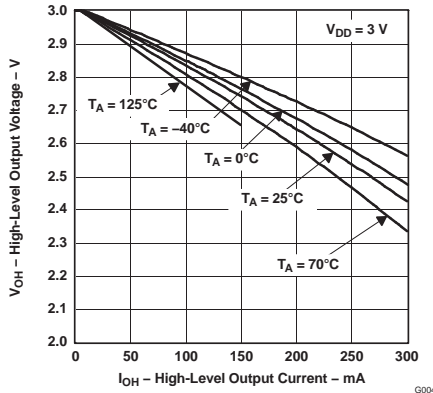


Figure 5.

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

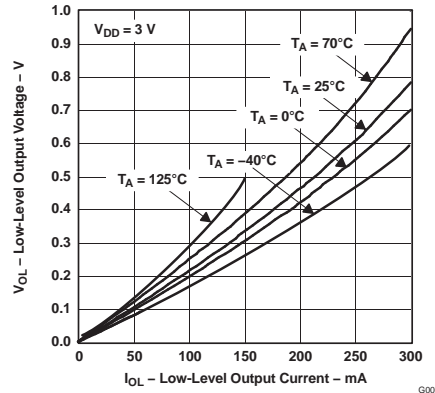


Figure 6.

**HIGH-LEVEL OUTPUT VOLTAGE
VS
HIGH-LEVEL OUTPUT CURRENT**

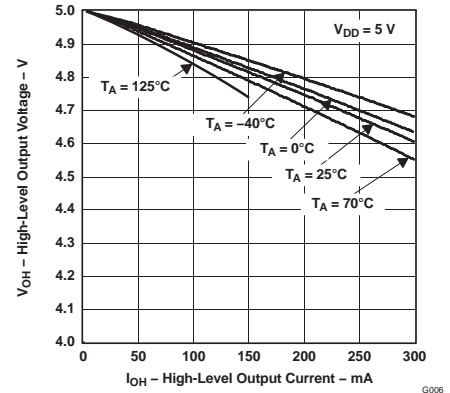


Figure 7.

**LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT**

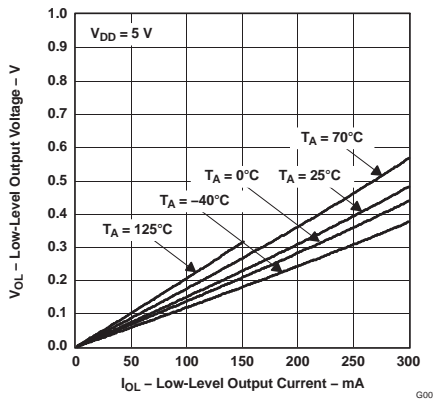


Figure 8.

**OUTPUT IMPEDANCE
VS
FREQUENCY**

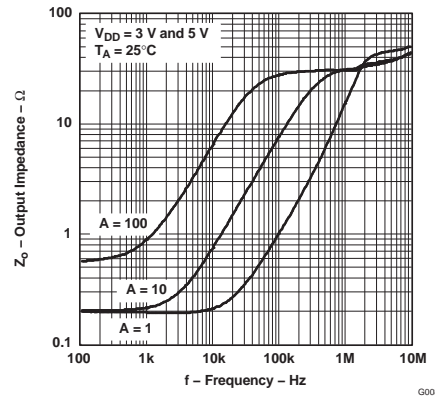


Figure 9.

**SUPPLY CURRENT
VS
SUPPLY VOLTAGE**

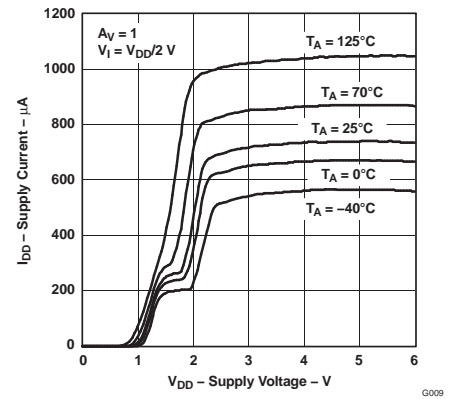


Figure 10.

**POWER-SUPPLY REJECTION
RATIO
VS
FREQUENCY**

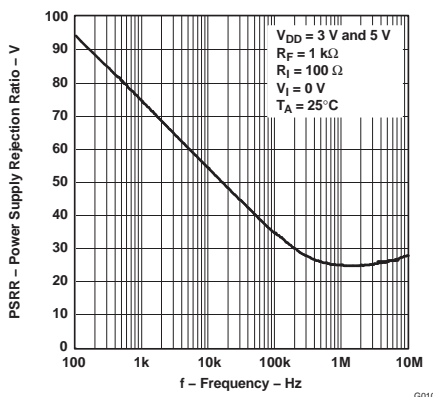


Figure 11.

**DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE
VS
FREQUENCY**

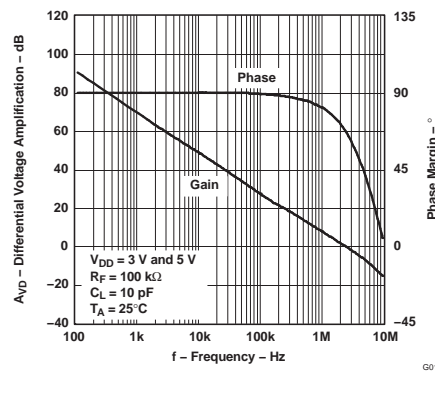


Figure 12.

**GAIN-BANDWIDTH PRODUCT
VS
SUPPLY VOLTAGE**

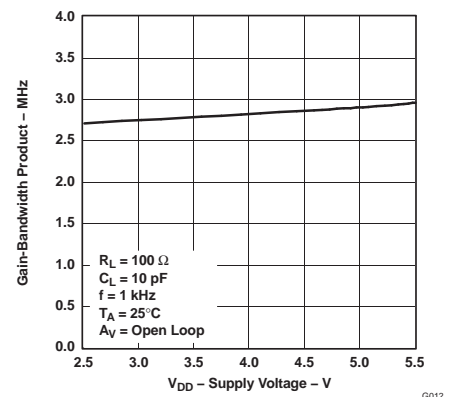


Figure 13.

**SLEW RATE
VS
SUPPLY VOLTAGE**

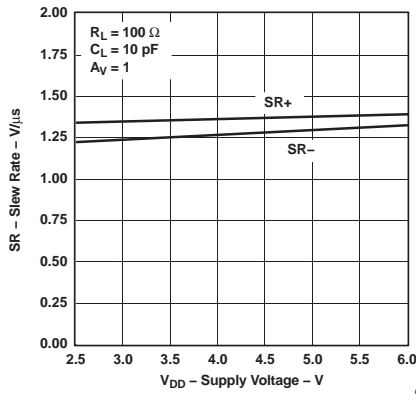


Figure 14.

**SLEW RATE
VS
TEMPERATURE**

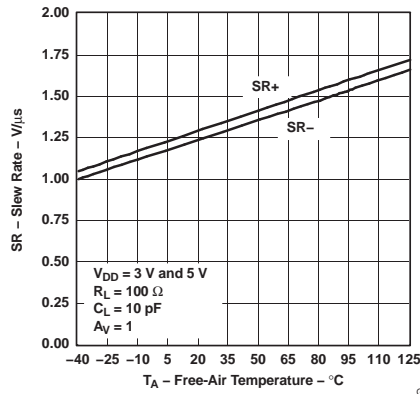


Figure 15.

**TOTAL HARMONIC
DISTORTION+NOISE
VS
FREQUENCY**

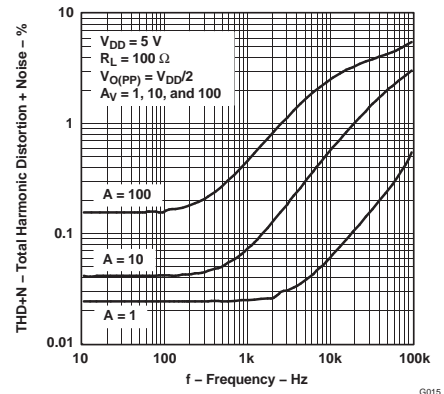


Figure 16.

**EQUIVALENT INPUT VOLTAGE
NOISE
VS
FREQUENCY**

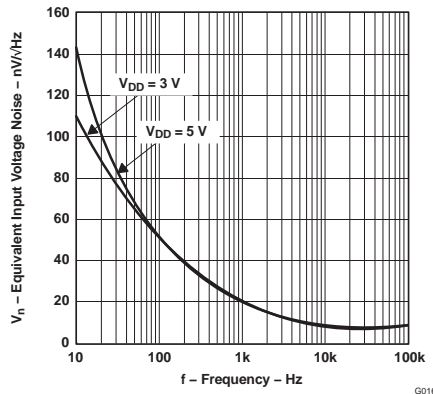


Figure 17.

**PHASE MARGIN
VS
CAPACITIVE LOAD**

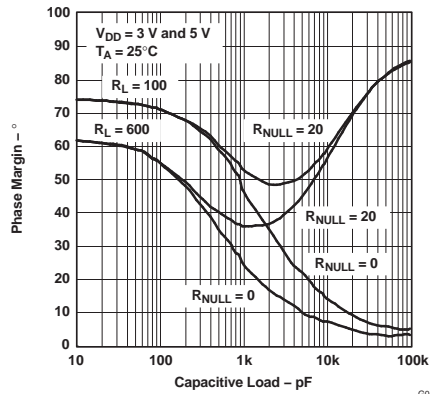


Figure 18.

**VOLTAGE-FOLLOWER
LARGE-SIGNAL PULSE RESPONSE**

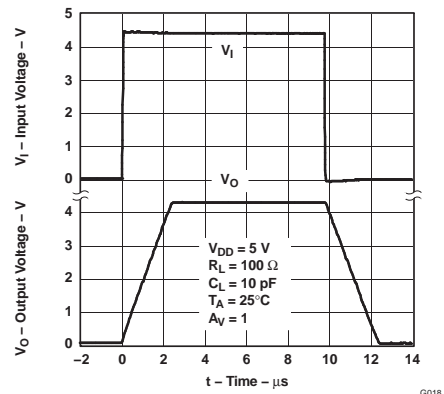


Figure 19.

**VOLTAGE-FOLLOWER
SMALL-SIGNAL PULSE RESPONSE**

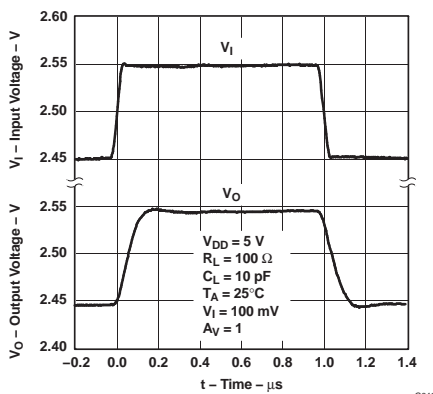


Figure 20.

INVERTING LARGE-SIGNAL PULSE RESPONSE

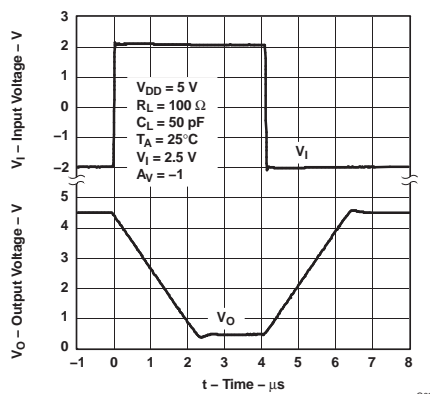


Figure 21.

**SMALL-SIGNAL INVERTING
PULSE RESPONSE**

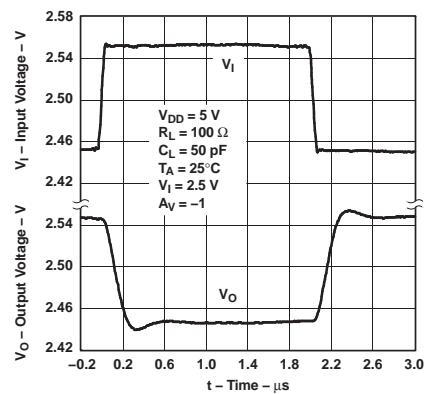


Figure 22.

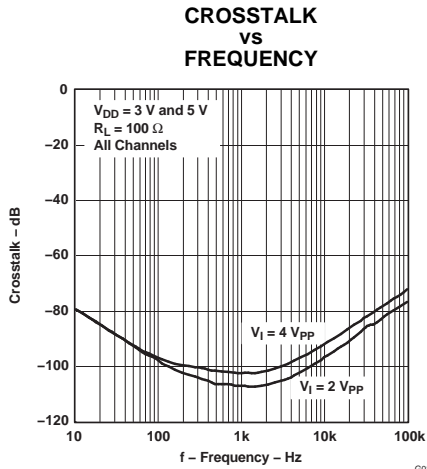


Figure 23.

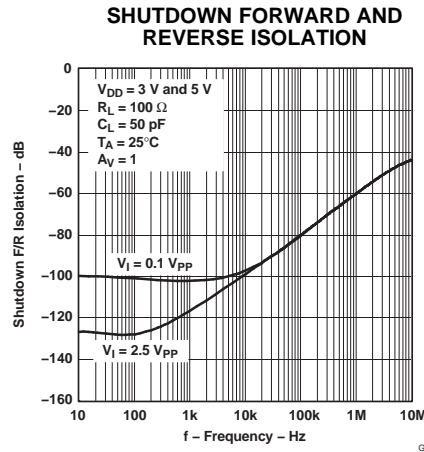


Figure 24.

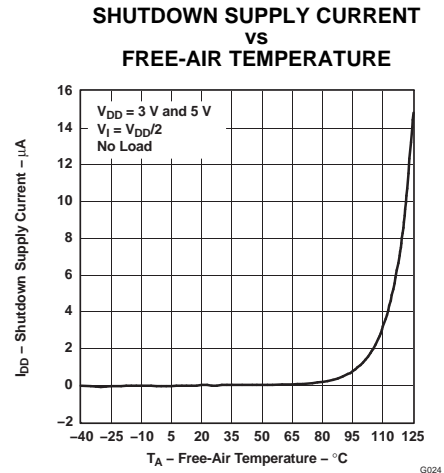


Figure 25.

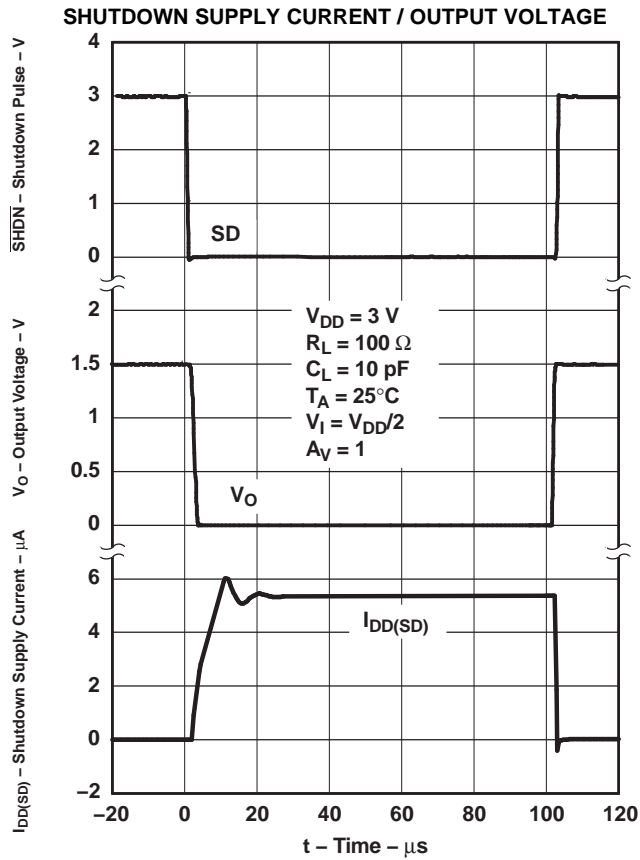


Figure 26.

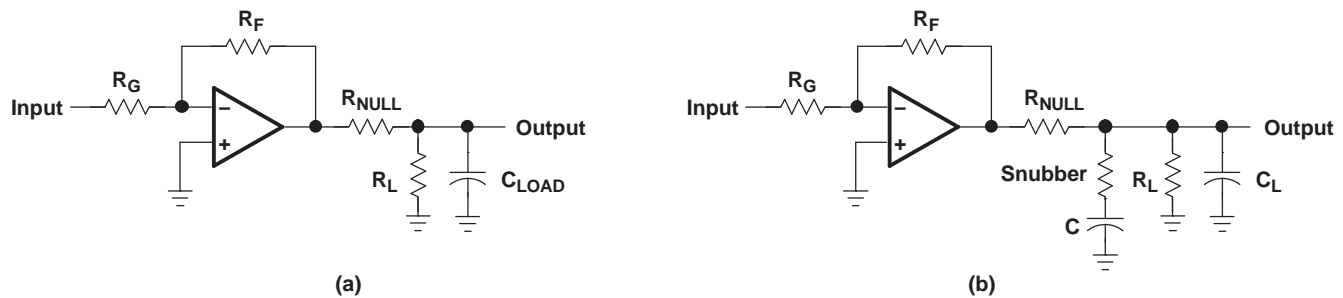
APPLICATION INFORMATION

SHUTDOWN FUNCTION

Two members of the TLV411x family (TLV4110/3) have a shutdown terminal for conserving battery life in portable applications. When the shutdown terminal is tied low, the supply current is reduced to just nano amps per channel, the amplifier is disabled, and the outputs are placed in a high-impedance mode. In order to save power in shutdown mode, an external pullup resistor is required; therefore, to enable the amplifier, the shutdown terminal must be pulled high. When the shutdown terminal is left floating, care should be taken to ensure that parasitic leakage current at the shutdown terminal does not inadvertently place the operational amplifier into shutdown.

DRIVING A CAPACITIVE LOAD

When the amplifier is configured in this manner, capacitive loading directly on the output decreases the device's phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 1 nF, it is recommended that a resistor be placed in series (R_{NULL}) with the output of the amplifier, as shown in Figure 27. A maximum value of 20 Ω is recommended for most applications.

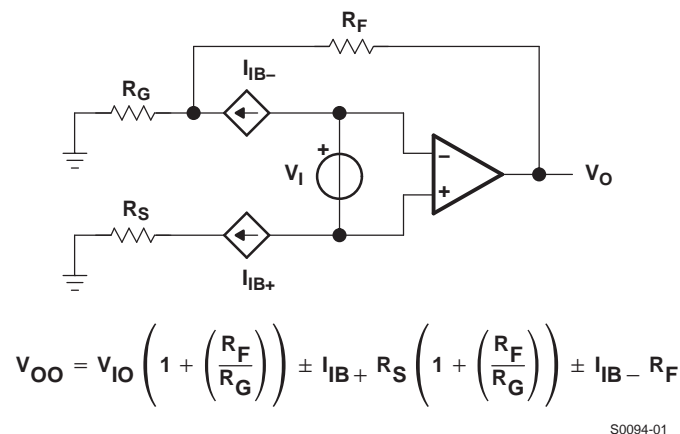


S0048-03

Figure 27. Driving a Capacitive Load

OFFSET VOLTAGE

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage.



S0094-01

Figure 28. Output Offset Voltage Model

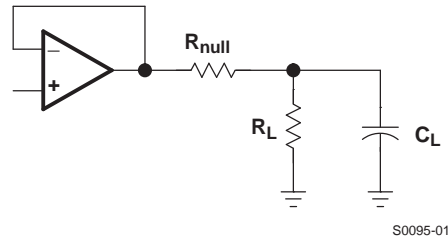


Figure 29.

GENERAL POWER DESIGN CONSIDERATIONS

When driving heavy loads at high junction temperatures there is an increased probability of electromigration affecting the long-term reliability of ICs. Therefore, to avoid this issue:

- The output current must be limited (at these high-junction temperatures).

OR

- The junction temperature must be limited.

The maximum continuous output current at a die temperature 150°C will be 1/3 of the current at 105°C.

The junction temperature will be dependent on the ambient temperature around the IC, thermal impedance from the die to the ambient and power dissipated within the IC.

$$T_J = T_A + \theta_{JA} \times P_{DIS}$$

Where:

P_{DIS} is the IC power dissipation and is equal to the output current multiplied by the voltage dropped across the output of the IC.

θ_{JA} is the thermal impedance between the junction and the ambient temperature of the IC.

T_J is the junction temperature.

T_A is the ambient temperature.

Reducing one or more of these factors results in a reduced die temperature. The 8-pin SOIC (small outline integrated circuit) has a thermal impedance from junction to ambient of 176°C/W. For this reason it is recommended that the maximum power dissipation of the 8-pin SOIC package be limited to 350 mW, with peak dissipation of 700 mW as long as the RMS value is less than 350 mW.

The use of the MSOP PowerPAD™ dramatically reduces the thermal impedance from junction to case. And, with correct mounting, the reduced thermal impedance greatly increases the IC's permissible power dissipation and output current handling capability. For example, the power dissipation of the PowerPAD™ is increased to above 1 W. Sinusoidal and pulse-width modulated output signals also increase the output current capability. The equivalent dc current is proportional to the square-root of the duty cycle:

$$I_{DC(EQ)} = I_{Cont} \times \sqrt{(\text{duty cycle})} \quad (1)$$

| CURRENT DUTY CYCLE AT PEAK RATED CURRENT | EQUIVALENT DC CURRENT AS A PERCENTAGE OF PEAK |
|---|--|
| 100 | 100 |
| 70 | 84 |
| 50 | 71 |

Note that, with an operational amplifier, a duty cycle of 70% often results in the op-amp sourcing current 70% of the time and sinking current 30%; therefore, the equivalent dc current is still 0.84 times the continuous current rating at a particular junction temperature.

GENERAL PowerPAD DESIGN CONSIDERATIONS

The TLV411x is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset lead frame upon which the die is mounted [see [Figure 30\(a\)](#) and [Figure 30\(b\)](#)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see [Figure 30\(c\)](#)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device.

The PowerPAD package represents a breakthrough in combining the small area and ease of assembly of surface mount with the previously awkward mechanical methods of heat sinking.

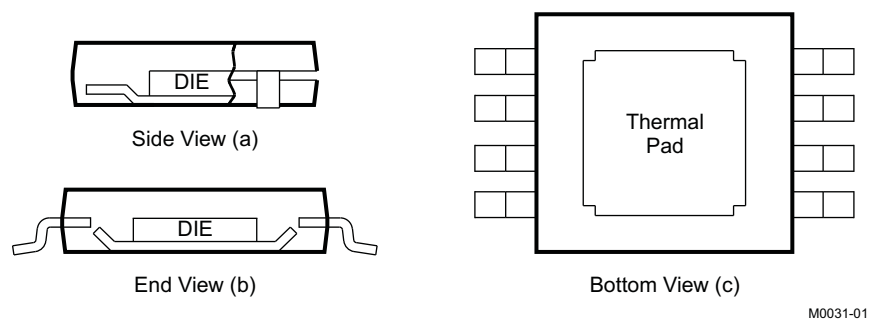
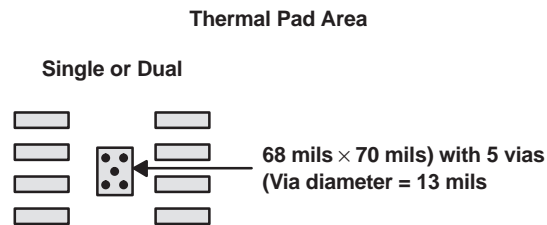


Figure 30. Views of Thermally Enhanced DGN Package

Although there are many ways to properly heatsink the PowerPAD package, the following steps illustrate the recommended approach.

1. Prepare the PCB with a top-side etch pattern, as shown in [Figure 31](#). There should be etch for the leads as well as etch for the thermal pad.
2. Place five holes (dual) or nine holes (quad) in the area of the thermal pad. These holes should be 13 mils in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This helps dissipate the heat generated by the TLV411x IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
4. Connect all holes to the internal ground plane.
5. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal-resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the TLV411x PowerPAD package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes (dual) or nine holes (quad) exposed. The bottom-side solder mask should cover the five or nine holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, the TLV411x IC is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.



M0032-01

Figure 31. PowerPAD PCB Etch and Via Pattern

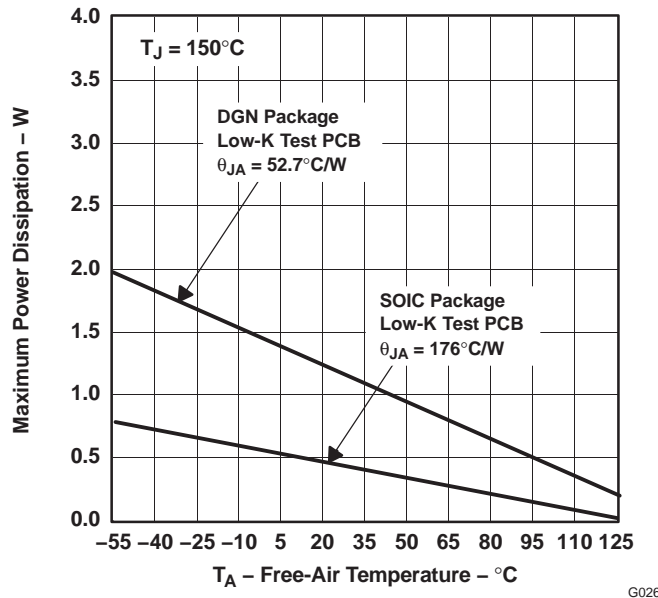
For a given θ_{JA} , the maximum power dissipation is shown in Figure 32 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

Where:

- P_D = Maximum power dissipation of TLV411x IC (watts)
- T_{MAX} = Absolute maximum junction temperature (150°C)
- T_A = Free-ambient air temperature (°C)
- θ_{JA} = $\theta_{JC} + \theta_{CA}$
- θ_{JC} = Thermal coefficient from junction to case
- θ_{CA} = Thermal coefficient from case to ambient air (°C/W)

(2)



NOTE: Results are with no air flow and using JEDEC Standard Low-K test PCB.

Figure 32. Maximum Power Dissipation vs Free-Air Temperature

The next consideration is the package constraints. The two sources of heat within an amplifier are quiescent power and output power. The designer should never forget about the quiescent heat generated within the device, especially multi-amplifier devices. Because these devices have linear output stages (Class A-B), most of the heat dissipation is at low output voltages with high output currents.

The other key factor when dealing with power dissipation is how the devices are mounted on the PCB. The PowerPAD devices are extremely useful for heat dissipation. But, the device should always be soldered to a copper plane to fully use the heat dissipation properties of the PowerPAD. The SOIC package, on the other hand, is highly dependent on how it is mounted on the PCB. As more trace and copper area is placed around the device, θ_{JA} decreases and the heat-dissipation capability increases. The currents and voltages shown in these graphs are for the total package. For the dual or quad amplifier packages, the sum of the RMS output currents and voltages should be used to choose the proper package.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TLV4113MDGQREP | ACTIVE | HVSSOP | DGQ | 10 | 2500 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -55 to 125 | BTE | Samples |
| V62/06646-04ZE | ACTIVE | HVSSOP | DGQ | 10 | 2500 | RoHS & Green | NIPDAUAG | Level-1-260C-UNLIM | -55 to 125 | BTE | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV4113-EP :

- Catalog: [TLV4113](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TLV4113MDGQREP | HVSSOP | DGQ | 10 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TLV4113MDGQREP | HVSSOP | DGQ | 10 | 2500 | 358.0 | 335.0 | 35.0 |

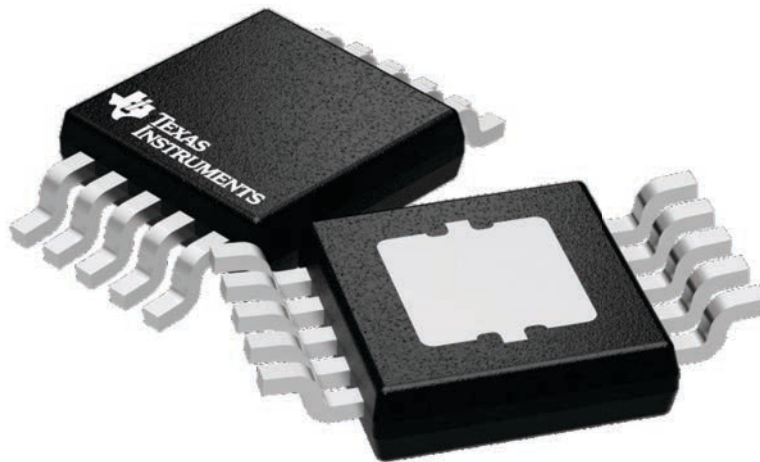
GENERIC PACKAGE VIEW

DGQ 10

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

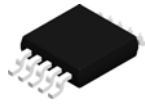
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224775/A

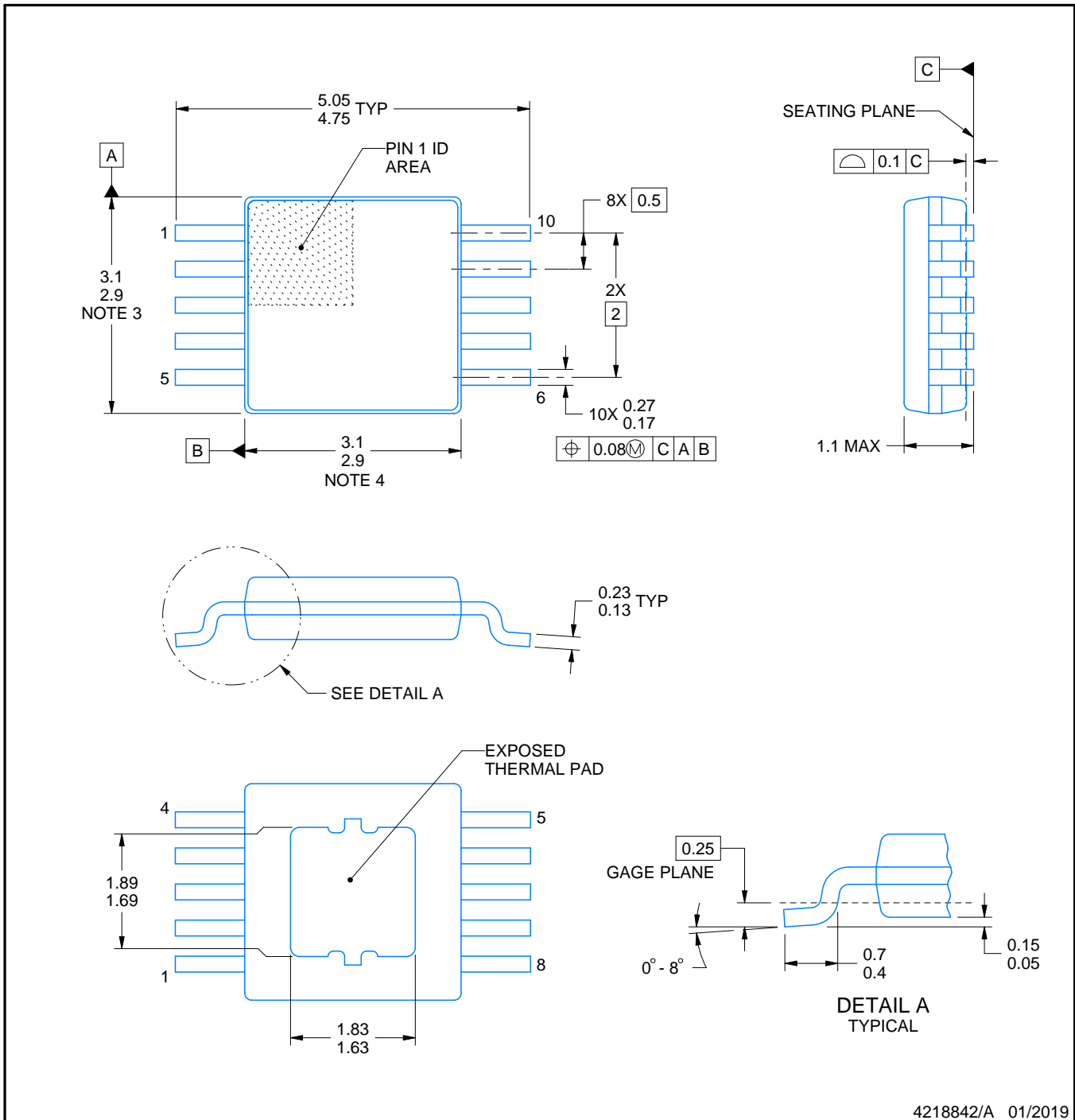
DGQ0010D



PACKAGE OUTLINE

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



4218842/A 01/2019

PowerPAD is a trademark of Texas Instruments.

NOTES:

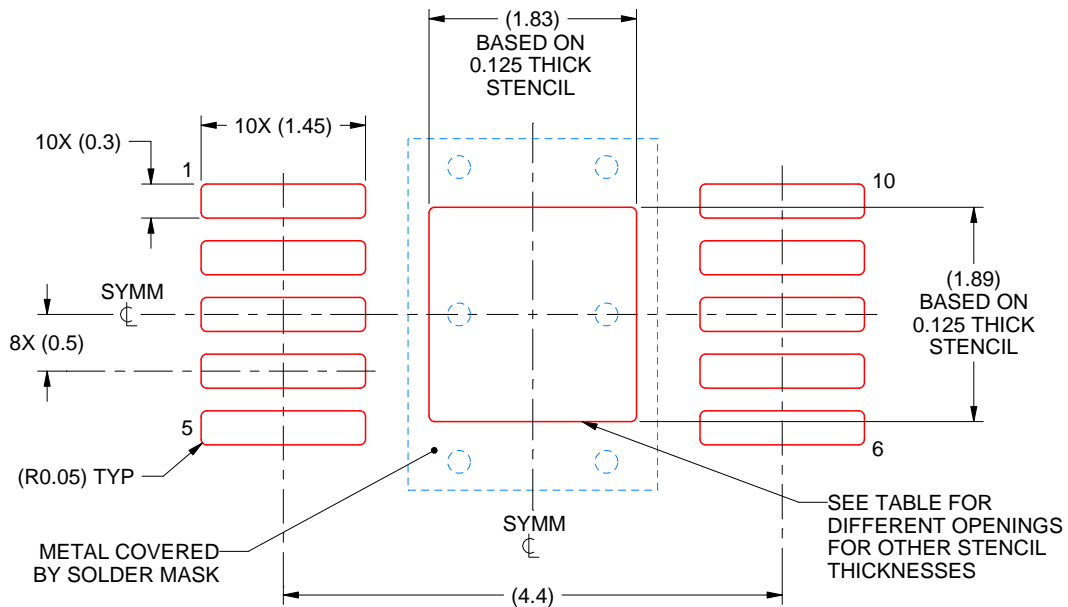
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.

EXAMPLE STENCIL DESIGN

DGQ0010D

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
 EXPOSED PAD
 100% PRINTED SOLDER COVERAGE BY AREA
 SCALE:15X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1 | 2.05 X 2.11 |
| 0.125 | 1.83 X 1.89 (SHOWN) |
| 0.150 | 1.67 X 1.73 |
| 0.175 | 1.55 X 1.60 |

4218842/A 01/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (<https://www.ti.com/legal/termsofsale.html>) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021, Texas Instruments Incorporated