SN74CBTLV3257-EP 低电压 4 位 2 选 1 FET 多路复用器/多路信号分离器

1 特性

- 受控基线
  - 一个组装地点
  - 一个测试地点
  - 一个制造地点
- 更宽泛的工作温度范围 -55°C 至 125°C
- 为制造资源减少 (DMS) 提供增强型支持
- 改进了产品变更通知
- 资质谱系 (1)
- 两个端口间使用 5Ω 开关连接
- 支持在数据 I/O 端口进行轨至轨开关
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体模型 (A114-A)
  - 200V 机器模型 (A115-A)

(1) 组件资质符合 JEDEC 和行业标准，确保在更宽泛的工作温度范围内可靠运行。这包括但不限于高加速应力测试 (HAST) 或偏压 85/85、温度循环、热压器或无偏压 HAST、电迁移、金属间键合寿命和模塑化合物寿命。这些资质测试不能作为在超出额定性能和环境限制的条件下使用此组件的依据。

2 应用

- 支持国防、航天和医疗 应用

3 说明

SN74CBTLV3257 是一款 4 位 2 选 1 高速 FET 多路复用器/多路信号分离器。此开关具有低通态电阻，可以在最短传播延迟情况下建立连接。

选择 (S) 输入控制数据流。当输出使能 ($\overline{OE}$) 输入为高电平时，FET 多路复用器/多路解复用器被禁用。

该器件完全 适用于 I_{off} 为了部分断电的应用。I_{off} 特性可确保在关断时防止损坏电流通过器件回流。该器件可在关断时提供隔离。

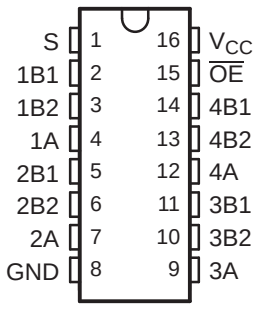
为了确保加电或断电期间的高阻抗状态，$\overline{OE}$ 应通过一个上拉电阻器被连接至 V_{CC}；该电阻器的最小值由驱动器的电流吸入能力来决定。

器件信息(1)

器件型号	等级	封装
CCBTLV3257MPWREP	T_A = -55°C 至 125°C	TSSOP – PW 卷带封装

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

PW PACKAGE
(TOP VIEW)



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2008) to Revision A **Page**

- 已更改 将*可订购信息* 表更改为*器件信息* 表 1
- 已添加 *添加了应用* 部分、*目录*、*修订历史记录* 部分、*器件和文档支持* 部分和*机械、封装和可订购信息* 部分 1

5 Pin Configuration and Functions

Table 1. Function Table

INPUTS		FUNCTION
$\overline{OE}$	S	
L	L	A port = B1 port
L	H	A port = B2 port
H	X	Disconnect

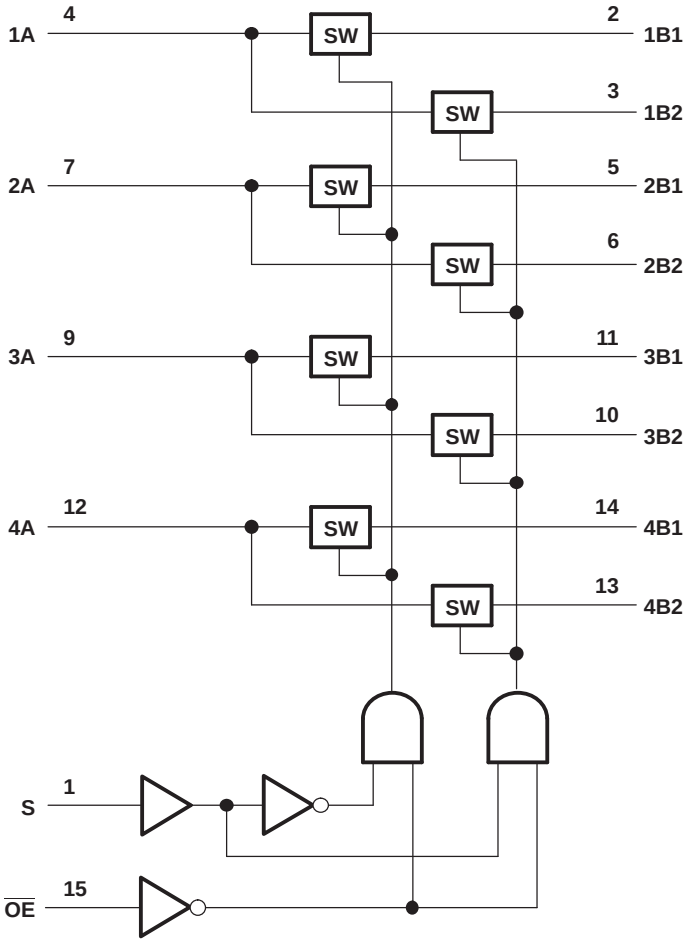


Figure 1. Logic Diagram (Positive Logic)

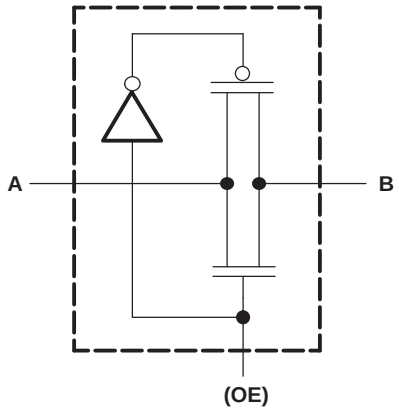


Figure 2. Simplified Schematic, Each FET Switch

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	4.6	V
V_I	Input voltage(2)		–0.5	4.6	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	V_{IO} < 0		–50	mA
θ_{JA}	Package thermal impedance	PW package(3)		108	°C/W
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2.3	3.6	V
V_{IH}	High-level control input voltage	V_{CC} = 2.3 V to 2.7 V	1.7		V
		V_{CC} = 2.7 V to 3.6 V	2		
V_{IL}	Low-level control input voltage	V_{CC} = 2.3 V to 2.7 V		0.7	V
		V_{CC} = 2.7 V to 3.6 V		0.8	
T_A	Operating free-air temperature		–55	125	°C

(1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*.

6.3 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IK}		V_{CC} = 3 V, I_I = –18 mA					–1.2	V
I_I		V_{CC} = 3.6 V, V_I = V_{CC} or GND					±1	μA
I_{off}		V_{CC} = 0, V_I or V_O = 0 to 3.6 V					15	μA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND					10	μA
ΔI_{CC}(2)	Control inputs	V_{CC} = 3.6 V, one input at 3 V, other inputs at V_{CC} or GND					300	μA
C_i	Control inputs	V_I = 3 V or 0				3		pF
$C_{io(OFF)}$	A port	V_O = 3 V or 0, $\overline{OE}$ = V_{CC}				10.5		pF
	B port					5.5		
r_{on}(3)		V_{CC} = 2.3 V, TYP at V_{CC} = 2.5 V	V_I = 0	I_I = 64 mA		5	8	Ω
				I_I = 24 mA		5	8	
			V_I = 1.7 V	I_I = 15 mA		27	40	
		V_{CC} = 3 V	V_I = 0	I_I = 64 mA		5	7	
				I_I = 24 mA		5	7	
			V_I = 2.4 V	I_I = 15 mA		10	15	

(1) All typical values are at V_{CC} = 3.3 V (unless otherwise noted), T_A = 25°C.
(2) This is the increase in supply current for each input that is at the specified voltage level, rather than V_{CC} or GND.
(3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

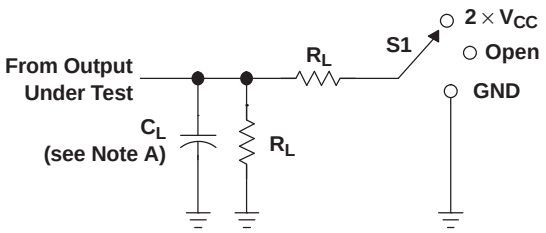
6.4 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	A or B(1)	B or A		0.15		0.25	ns
	S	A or B	1.8	8.1	1.8	7.3	
t_{en}	S	A or B	1.7	7.5	1.7	6.5	ns
t_{dis}	S	A or B	1	6.3	1	6.0	ns
t_{en}	$\overline{OE}$	A or B	1.9	7.1	2	6.2	ns
t_{dis}	$\overline{OE}$	A or B	1	7.0	1.6	6.5	ns

(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

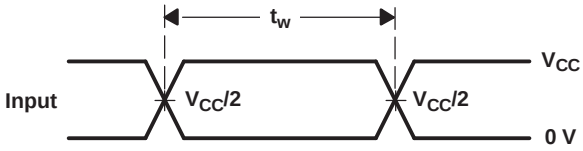
7 Parameter Measurement Information



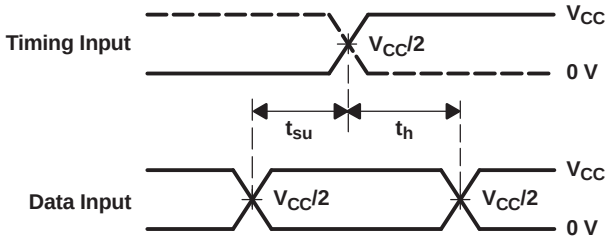
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

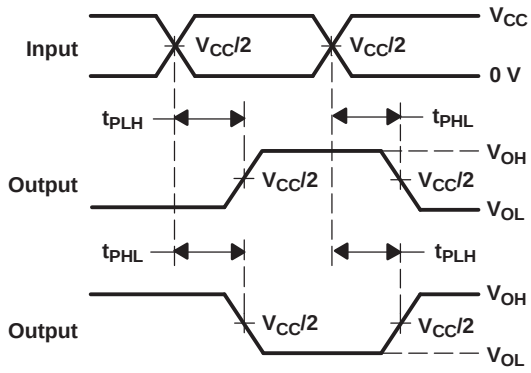
V_{CC}	C_L	R_L	V_Δ
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	50 pF	500 Ω	0.3 V



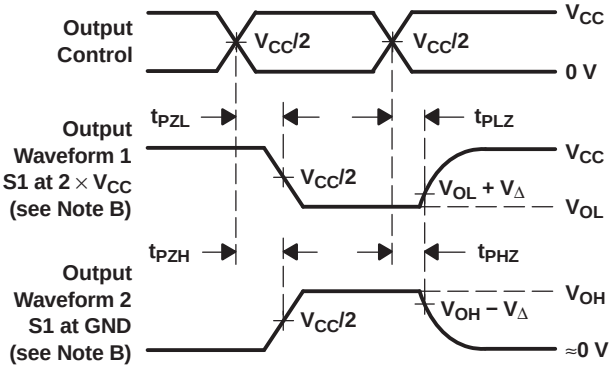
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 器件和文档支持

8.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 社区资源

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

8.3 商标

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8.4 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CCBTLV3257MPWREP	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CL257EP	Samples
V62/08615-01XE	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CL257EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

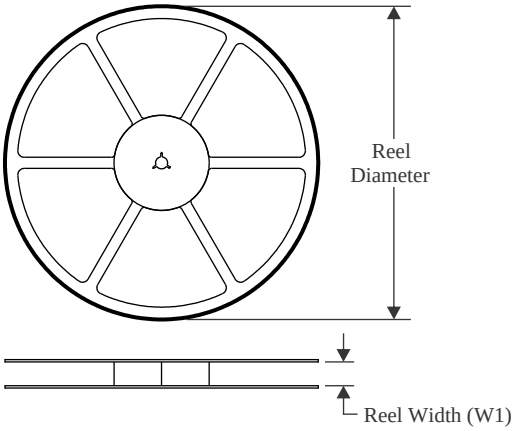
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

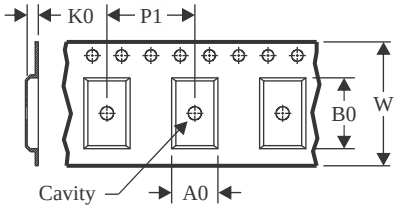
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

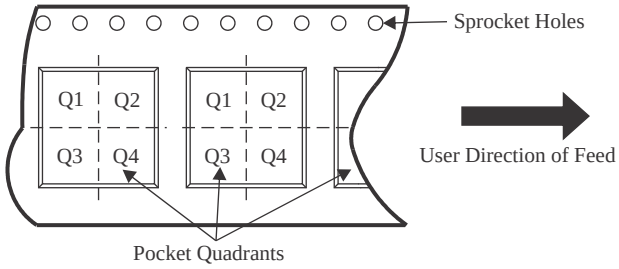


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

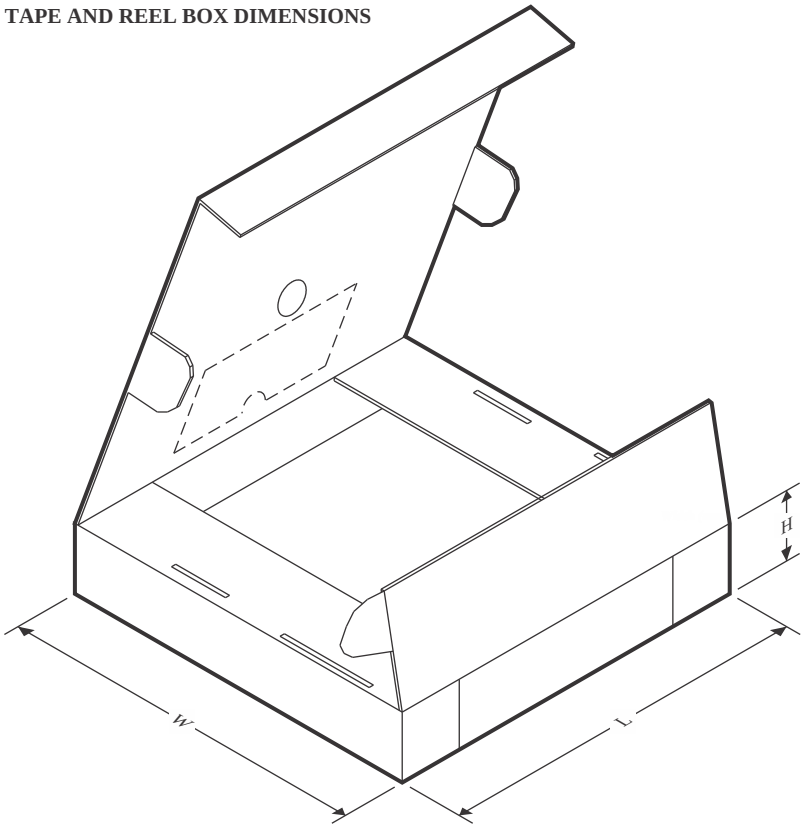
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CCBTLV3257MPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

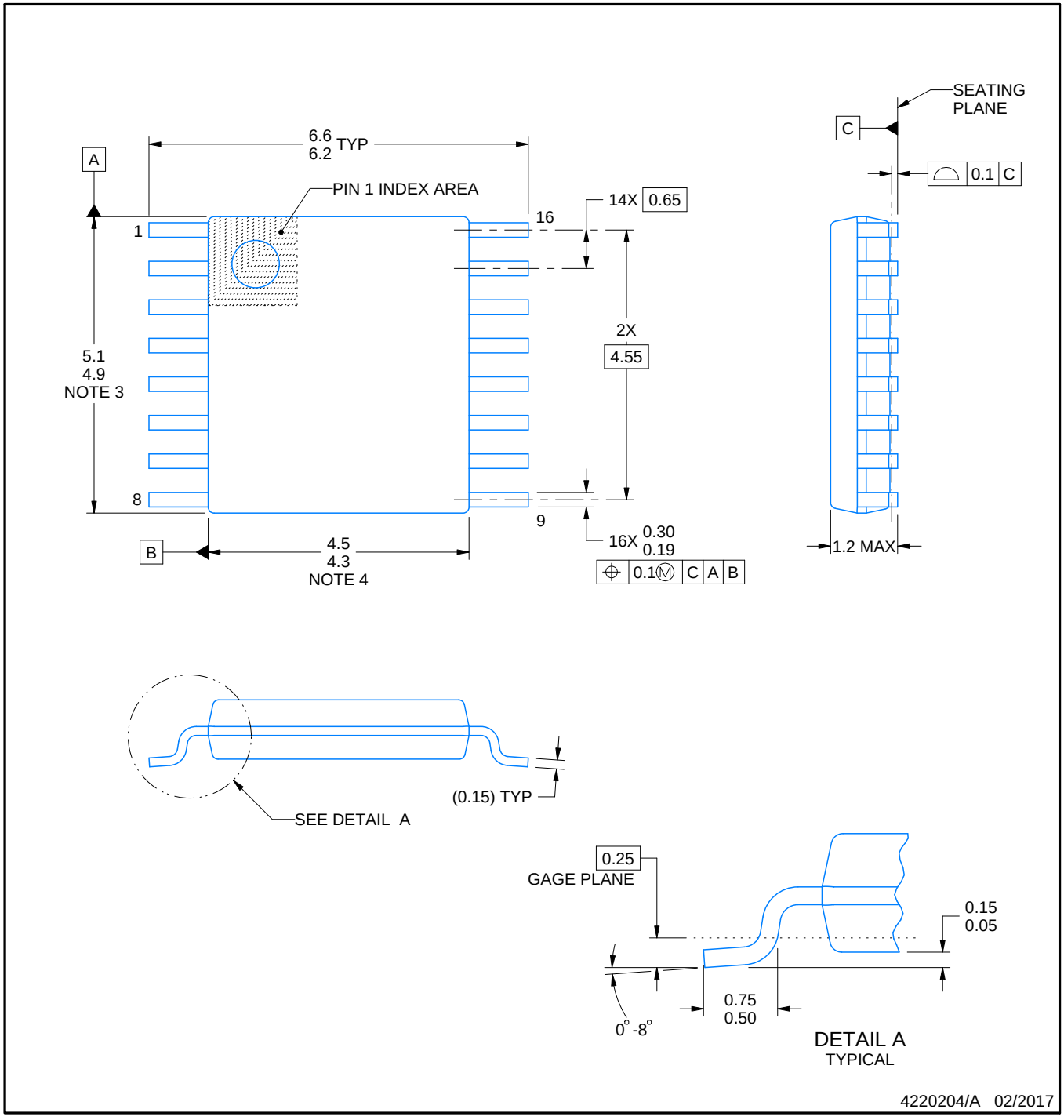
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CCBTLV3257MPWREP	TSSOP	PW	16	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0016A

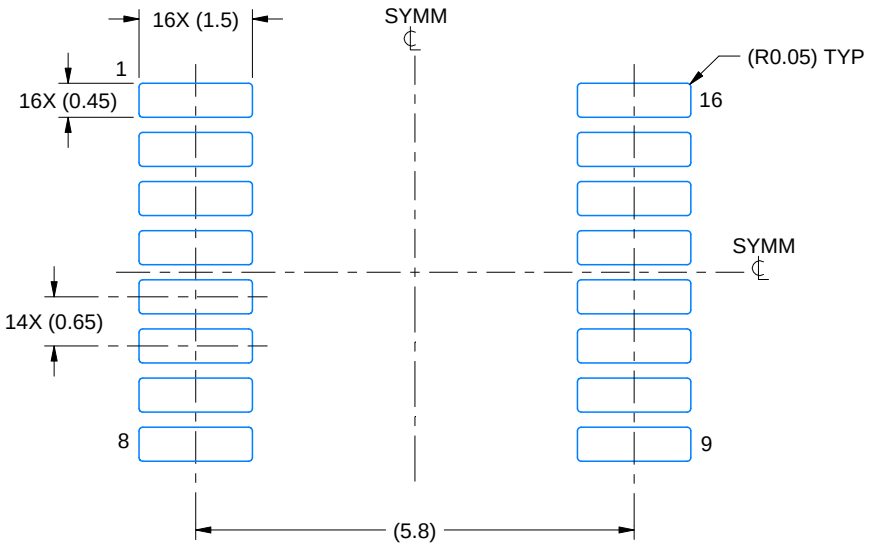
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

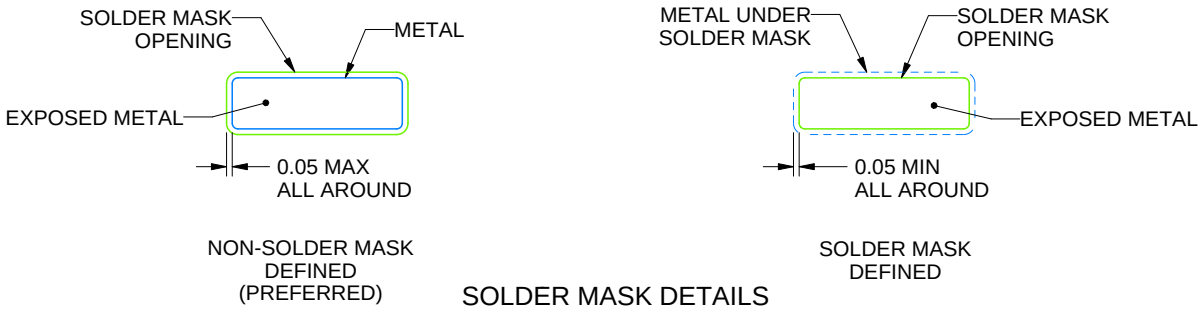


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

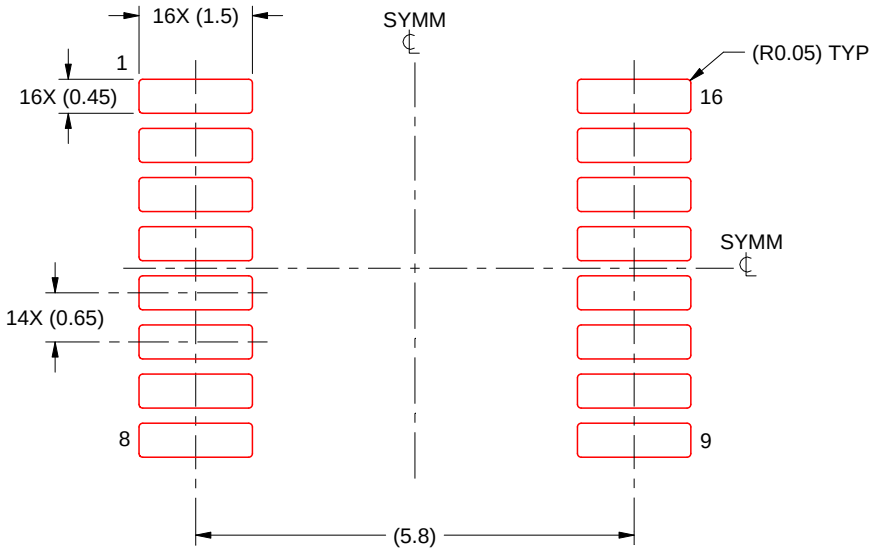


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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