具有 GPIO 的 ADS7066 小型 8 通道 16 位 SAR ADC

1 特性

- 小尺寸解决方案：
  - 1.62mm × 1.62mm WCSP
  - 节省空间、无电容、2.5V 内部基准
- 8 通道，可配置为以下任意组合：
  - 最多 8 个模拟输入、数字输入或数字输出
- 可编程均值滤波器:
  - 用于求平均值的可编程样本大小
  - 利用内部转换求平均值
  - 用于计算平均输出的 20 位分辨率
- 具有通道序列发生器的低泄漏多路复用器：
  - 手动模式
  - 动态模式
  - 自动序列模式
- 出色的交流和直流性能：
  - SNR：86dB，THD：–100dB
  - 可编程均值滤波器提高了 SNR
  - INL：±1LSB，16 位，无丢码
  - 内部校准改善了失调电压和漂移
  - 高采样率、无延迟输出：
    - 250kSPS
- 宽工作电压范围：
  - ADC 输入范围：0V 至 V_{REF} 和 2 x V_{REF}
  - 模拟电源：3V 至 5.5V
  - 数字电源：1.65V 至 5.5V
  - 温度范围：-40°C 至 +125°C
- 增强型 SPI 数字接口：
  - 高速 60MHz SPI 接口
  - 使用 > 4.5MHz SPI 实现最大吞吐量

2 应用

- 光学模块
- 光线路卡
- 多参数患者监视器

3 说明

ADS7066 是一款小型、16 位、8 通道、高精度逐次逼近寄存器 (SAR) 型模数转换器 (ADC)。ADS7066 具有集成的无电容基准和基准缓冲器，无需较多的外部组件，有助于减小整体解决方案尺寸。晶圆级芯片级封装和较少的外部组件使该器件适用于空间受限型 应用。

ADS7066 具有 内置的失调电压校准功能，可在系统的宽工作范围内提高精度。可编程均值滤波器可实现更高的分辨率测量。ADS7066 的八个通道可以单独配置为模拟输入、数字输入或数字输出，以实现更小的系统尺寸，并简化混合信号反馈和数字控制的电路设计。

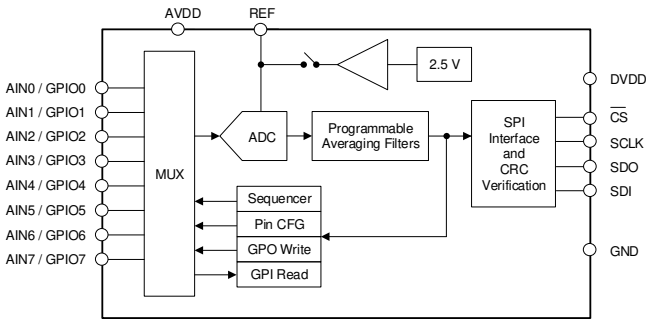
增强型 SPI 支持 ADS7066 以较低的时钟速度实现高吞吐量，从而简化电路板布局并降低系统成本。ADS7066 具有 循环冗余校验 (CRC) 功能，可用于数据读取和写入操作以及上电配置。

器件信息(1)

器件名称	封装	封装尺寸（标称值）
ADS7066	WCSP (16)	1.62mm × 1.62mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

ADS7066 方框图



ADVANCE INFORMATION

目录

ADVANCE INFORMATION

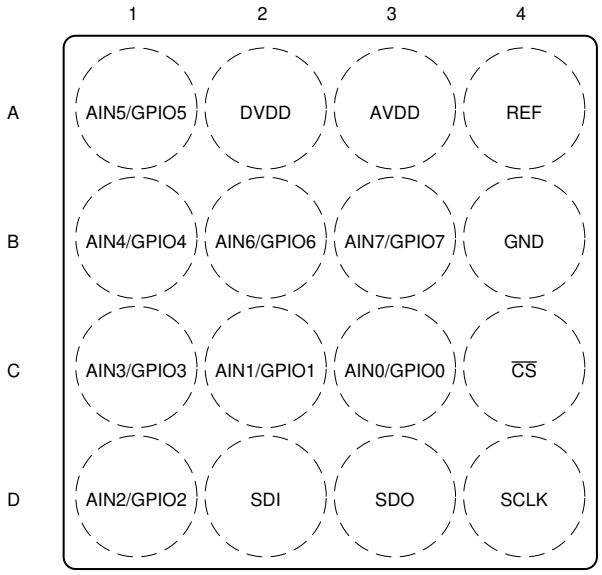
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2020 年 2 月	*	初始发行版。

5 Pin Configuration and Functions

YBH Package
16-Pin WCSP
Top View



Not to scale

Pin Functions

PIN		FUNCTION(1)	DESCRIPTION
NO.	NAME		
A1	AIN5/GPIO5	AI, DI, DO	Channel 5; configurable as either an analog input (default) or general-purpose input/output (GPIO).
A2	DVDD	P	Digital I/O supply voltage. Connect a 1-µF capacitor to GND.
A3	AVDD	P	Analog supply voltage. Connect a 1-µF capacitor to GND.
A4	REF	P	Internal reference buffer output; external reference input. Connect a 1-µF capacitor to GND.
B1	AIN4/GPIO4	AI, DI, DO	Channel 4; configurable as either an analog input (default) or GPIO.
B2	AIN6/GPIO6	AI, DI, DO	Channel 6; configurable as either an analog input (default) or GPIO.
B3	AIN7/GPIO7	AI, DI, DO	Channel 7; configurable as either an analog input (default) or GPIO.
B4	GND	P	Ground for power supply, all analog and digital signals are referred to this pin.
C1	AIN3/GPIO3	AI, DI, DO	Channel 3; configurable as either an analog input (default) or GPIO.
C2	AIN1/GPIO1	AI, DI, DO	Channel 1; configurable as either an analog input (default) or GPIO.
C3	AIN0/GPIO0	AI, DI, DO	Channel 0; configurable as either an analog input (default) or GPIO.
C4	$\overline{CS}$	DI	Chip-select input pin; active low. The device takes control of the data bus when $\overline{CS}$ is low. The SDO pin goes to Hi-Z when $\overline{CS}$ is high.
D1	AIN2/GPIO2	AI, DI, DO	Channel 2; configurable as either an analog input (default) or GPIO.
D2	SDI	DI	Serial data input pin for SPI interface.
D3	SDO	DO	Serial data output pin for SPI interface.
D4	SCLK	DI	Clock input pin for the SPI interface.

(1) AI = analog input, DI = digital input, DO = digital output, P = power supply.

ADVANCE INFORMATION

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
DVDD to GND	–0.3	5.5	V
AVDD to GND	–0.3	5.5	V
AINx/GPIOx(2) to GND	GND – 0.3	AVDD + 0.3	V
REF to GND	GND – 0.3	AVDD + 0.3	V
Digital inputs (CS, SDI, SCLK) to GND	GND – 0.3	5.5	V
Input current to any pin except supply pins(3)	–10	10	mA
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) AINx/GPIOx refers to AIN0/GPIO0, AIN1/GPIO1, AIN2/GPIO2, AIN3/GPIO3, AIN4/GPIO4, AIN5/GPIO5, AIN6/GPIO6, and AIN7/GPIO7 pins.
(3) Pin current must be limited to 10 mA or less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
AVDD	Analog power supply	AVDD to GND	3	3.3	5.5	V
DVDD	Digital power supply	DVDD to GND	1.65	3.3	5.5	V
REFERENCE VOLTAGE						
V_{REF}	Reference voltage to the ADC	Internal reference		2.5		V
		External reference	2.4		AVDD	
V_{IN}	Absolute input voltage	AINx(1) to GND	–0.1		AVDD + 0.1	V
ANALOG INPUTS						
FSR	Full-scale input range	RANGE = 0b	0		V_{REF}	V
		RANGE = 1b	0		2 x V_{REF}	
TEMPERATURE RANGE						
T_A	Ambient temperature		–40	25	125	°C

(1) AINx refers to analog inputs AIN0, AIN1, AIN2, AIN3, AIN4, AIN5, AIN6, and AIN7.

ADVANCE INFORMATION

6.4 Thermal Information

THERMAL METRIC(1)		ADS7066 YBH (WCSP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	80.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	18.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

6.5 Electrical Characteristics

at AVDD = 3 V to 5.5 V, DVDD = 1.65 V to 5.5 V, V_{REF} = 2.5 V (internal), and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = -40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
C_{IN}	Input capacitance	ADC and MUX capacitance		30		pF
DC PERFORMANCE						
	Resolution	No missing codes		16		Bits
DNL	Differential nonlinearity		–0.75	±0.5	0.75	LSB
INL	Integral nonlinearity		–4	±1	4	LSB
$V_{(OS)}$	Input offset error(1)		-32	±8	32	LSB
dV_{OS}/dT	Input offset thermal drift			±1		ppm/°C
	Offset error match		–1	0.5	1	LSB
G_E	Gain error(2)		–0.05	±0.02	0.05	%FSR
dG_E/dT	Gain error thermal drift			±1		ppm/°C
	Gain error match		–0.005	±0.001	0.005	%FSR
AC PERFORMANCE						
SINAD	Signal-to-noise + distortion ratio	f_{IN} = 2 kHz	84.7	86		dB
SNR	Signal-to-noise ratio	f_{IN} = 2 kHz	85	86		dB
SFDR	Spurious-free dynamic range	f_{IN} = 2 kHz		105		dB
	Isolation crosstalk	f_{IN} = 10 kHz		–110		dB
REFERENCE						
C_{REF}	Decoupling capacitor at REF pin		1		10	µF
DIGITAL INPUTS						
V_{IL}	Input low logic level	For $\overline{CS}$, SCLK and SDI pins	–0.3		0.3 DVDD	V
		For $GPIO_X$(3) pins	–0.3		0.3 AVDD	
V_{IH}	Input high logic level	For $\overline{CS}$, SCLK and SDI pins	0.7 DVDD		DVDD	V
		For $GPIO_X$ pins	0.7 AVDD		AVDD	
DIGITAL OUTPUTS						
	Output format	Straight binary				
V_{OL}	Output low logic level	For SDO pin, I_{OL} = 500 µA sink	0		0.2 DVDD	V
		For $GPIO_X$(3) pins, I_{OL} = 500 µA sink	0		0.2 AVDD	
V_{OH}	Output high logic level	For SDO pin, I_{OH} = 500 µA source	0.8 DVDD		DVDD	V
		For $GPIO_X$(3) pins, I_{OH} = 500 µA source	0.8 AVDD		AVDD	
POWER SUPPLY						
I_{AVDD}	Analog supply current	AVDD = 3.3 V, external reference		0.7	1	mA
		AVDD = 3.3 V, internal reference		1.2	1.6	mA
		No conversion, external reference		250		µA
		No conversion, internal reference		800		µA

(1) Post offset calibration.
(2) This specification is measured with respect to voltage at REF pin.
(3) $GPIO_X$ refers to GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, and GPIO7 pins.

ADVANCE INFORMATION

6.6 Timing Requirements

at AVDD = 3 V to 5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

		MIN	MAX	UNIT
CONVERSION CYCLE				
f_{CYCLE}	Sampling frequency		250	kSPS
t_{CYCLE}	ADC cycle-time period	$1/f_{CYCLE}$		s
t_{QUIET}	Quiet acquisition time	20		ns
t_{WH_CSZ}	Pulse duration: $\overline{CS}$ high	60		ns
t_{WL_CSZ}	Pulse duration: $\overline{CS}$ low	210		ns
SPI INTERFACE TIMINGS				
f_{CLK}	Maximum SCLK frequency		60	MHz
t_{CLK}	Minimum SCLK time period	16.67		ns
t_{PH_CK}	SCLK high time	0.45	0.55	t_{CLK}
t_{PL_CK}	SCLK low time	0.45	0.55	t_{CLK}
t_{SU_CSCK}	Setup time: $\overline{CS}$ falling to the first SCLK capture edge	15		ns
t_{SU_CKDI}	Setup time: SDI data valid to the SCLK capture edge	0.5		ns
t_{HT_CKDI}	Hold time: SCLK capture edge to data valid on SDI	1.6		ns
t_{D_CKCS}	Delay time: last SCLK falling to $\overline{CS}$ rising	0.5		ns

6.7 Switching Characteristics

at AVDD = 3 V to 5.5 V, DVDD = 1.65 V to 5.5 V, and maximum throughput (unless otherwise noted); minimum and maximum values at T_A = –40°C to +125°C; typical values at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
CONVERSION CYCLE					
t_{CONV}	ADC conversion time			3200	ns
t_{ACQ}	Acquisition time		800		ns
RESET					
t_{PU}	Power-up time for device	AVDD ≥ 3 V		5	ms
t_{RST}	Delay time; RST bit = 1b to device reset complete(1)			5	ms
SPI INTERFACE TIMINGS					
t_{DEN_CSDO}	Delay time: $\overline{CS}$ falling to data enable			22	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising to SDO going Hi-Z			50	ns
t_{D_CKDO}	Delay time: SCLK launch edge to (next) data valid on SDO			16	ns

(1) RST bit is automatically reset to 0b after t_{RST}.

ADVANCE INFORMATION

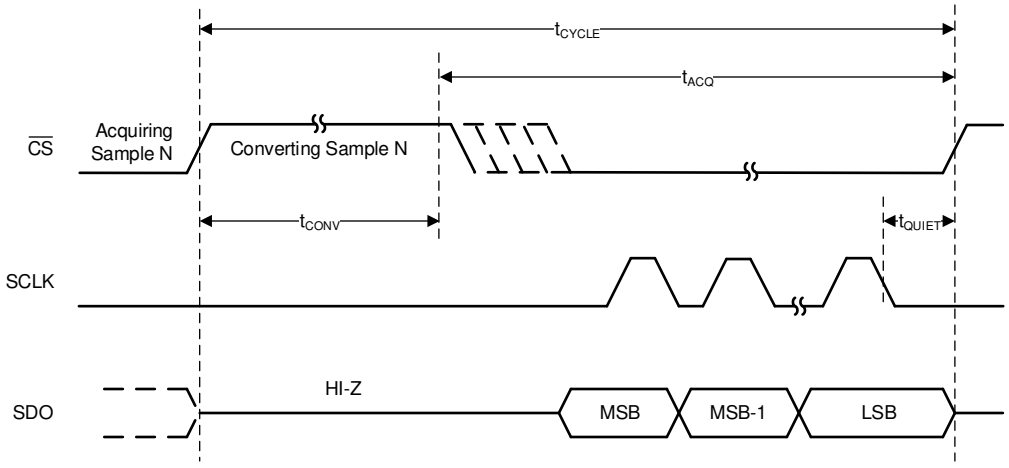


图 1. Conversion Cycle Timing

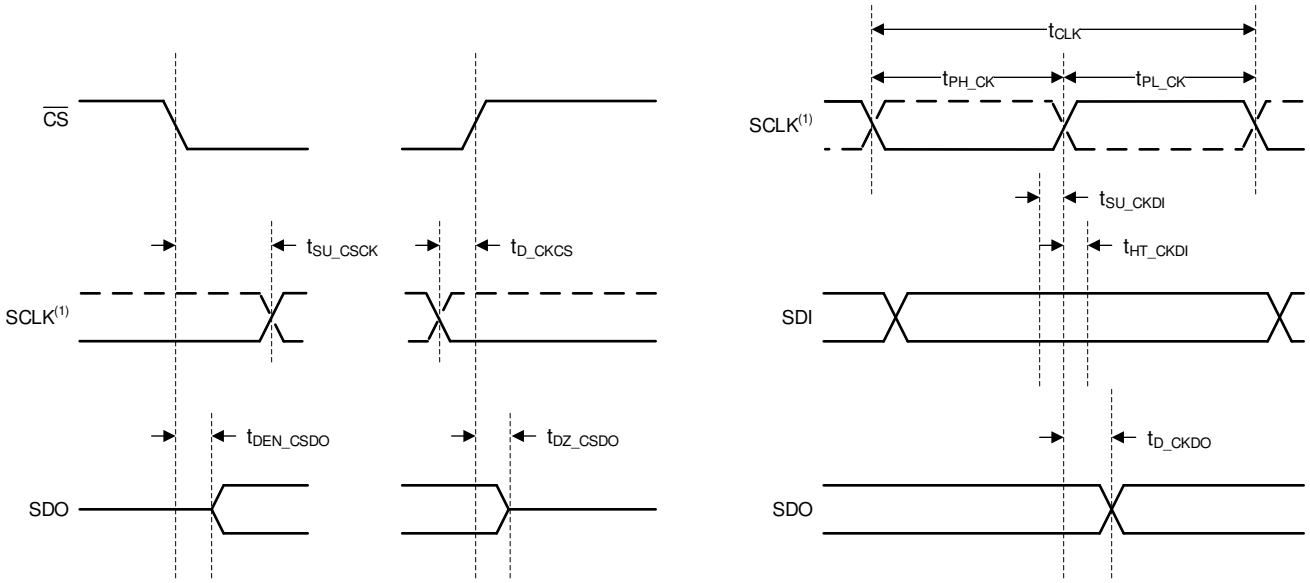


图 2. SPI Interface Timing

ADVANCE INFORMATION

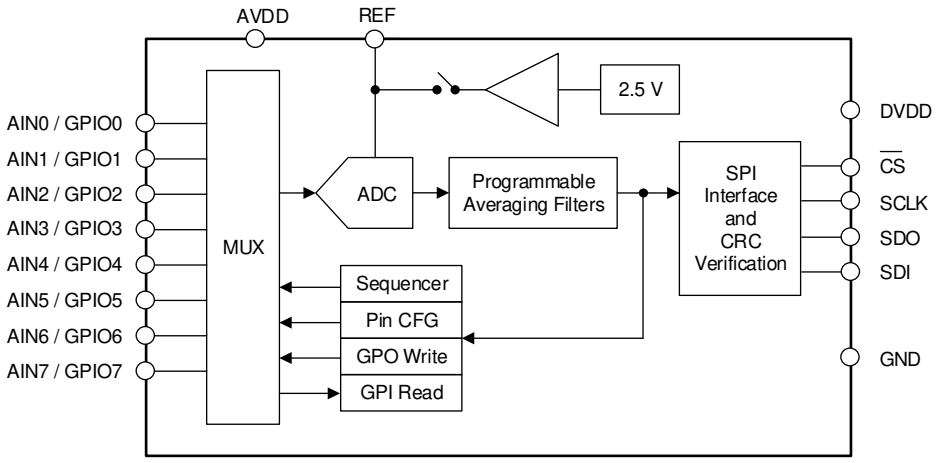
7 Detailed Description

7.1 Overview

The ADS7066 is a 16-bit, successive approximation register (SAR) analog-to-digital converter (ADC) with an analog multiplexer. This device integrates a reference, reference buffer, low-dropout regulator (LDO), and features high performance at full throughput and low-power consumption.

The ADS7066 supports unipolar, single-ended analog input signals. The internal reference generates a low-drift, buffered, 2.5-V reference output. The device uses an internal clock to perform conversions. At the end of the conversion process, the device enters an acquisition phase.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input and Multiplexer

The eight channels of the multiplexer can be independently configured as ADC inputs or general-purpose inputs/outputs (GPIOs). As shown in 图 3, each input pin has ESD protection diodes to AVDD and GND. On power-up or after device reset, all eight channels of the multiplexer are configured as analog inputs.

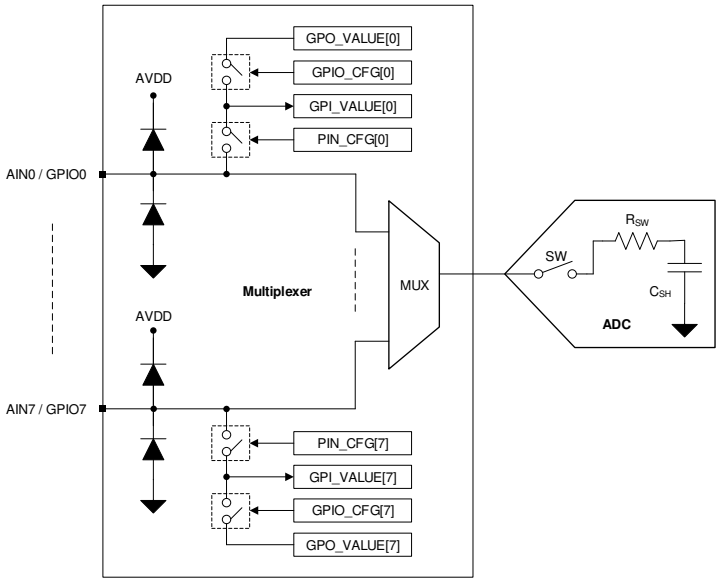


图 3. Analog Inputs, GPIOs, and ADC Connections

ADVANCE INFORMATION

Feature Description (接下页)

图 3 illustrates an equivalent circuit for the pins configured as analog inputs. The ADC sampling switch is represented by an ideal switch (SW) in series with a resistor (R_{SW}, typically 150 Ω) and a sampling capacitor (C_{SH}, typically 30 pF). During acquisition, the SW switch is closed to allow the signal on the selected analog input channel to charge the internal sampling capacitor. During conversion, the SW switch is opened to disconnect the analog input channel from the sampling capacitor.

The multiplexer channels can be configured as GPIOs in the PIN_CFG register. On power-up, all channels of the multiplexer are configured as analog inputs. The direction of a GPIO, input or output, can be set in the GPIO_CFG register. The logic level of channels configured as digital inputs can be read from the GPI_VALUE register. The digital outputs can be accessed by writing to the GPO_VALUE register. The digital outputs can be configured as open-drain or push-pull in the GPO_DRIVE_CFG register.

7.3.2 Reference

The ADS7066 has a precision, low-drift voltage reference internal to the device.

7.3.2.1 Internal Reference

The device features an internal reference source with a nominal output value of 2.5 V. On power-up, the internal reference is disabled by default. To enable the internal reference, set EN_REF = 1b in the GENERAL_CFG register. A minimum 0.1-µF decoupling capacitor is recommended to be placed between the REF and GND pins. The capacitor must be placed as close to the REF pin as possible. The REF pin has ESD protection diodes connected to the AVDD and GND pins.

7.3.2.2 External Reference

An external reference voltage source can be connected to the REF pin with an appropriate decoupling capacitor placed between the REF and GND pins. Best SNR is achieved with a 5-V external reference because the internal reference is limited to 2.5 V. For improved thermal drift performance, a reference from the REF60xx family (REF6025, REF6030, REF6033, REF6041, REF6045, and REF6050) is recommended.

7.3.3 ADC Transfer Function

The ADC output is in straight binary format. The full-scale input range (FSR) of the ADC is determined by the RANGE bit. On power-up, the FSR is 0 V to V_{REF}. When using the 2 x V_{REF} mode (RANGE = 1b), the ADC can measure analog inputs up to two times the voltage reference. 公式 1 can be used to compute the ADC resolution:

$$1\ LSB = FSR / 2^N \quad (1)$$

where:

- FSR = Full-scale input range of the ADC
- N = 16

ADVANCE INFORMATION

Feature Description (接下页)

图 4 and 表 1 show the ideal transfer characteristics for this device.

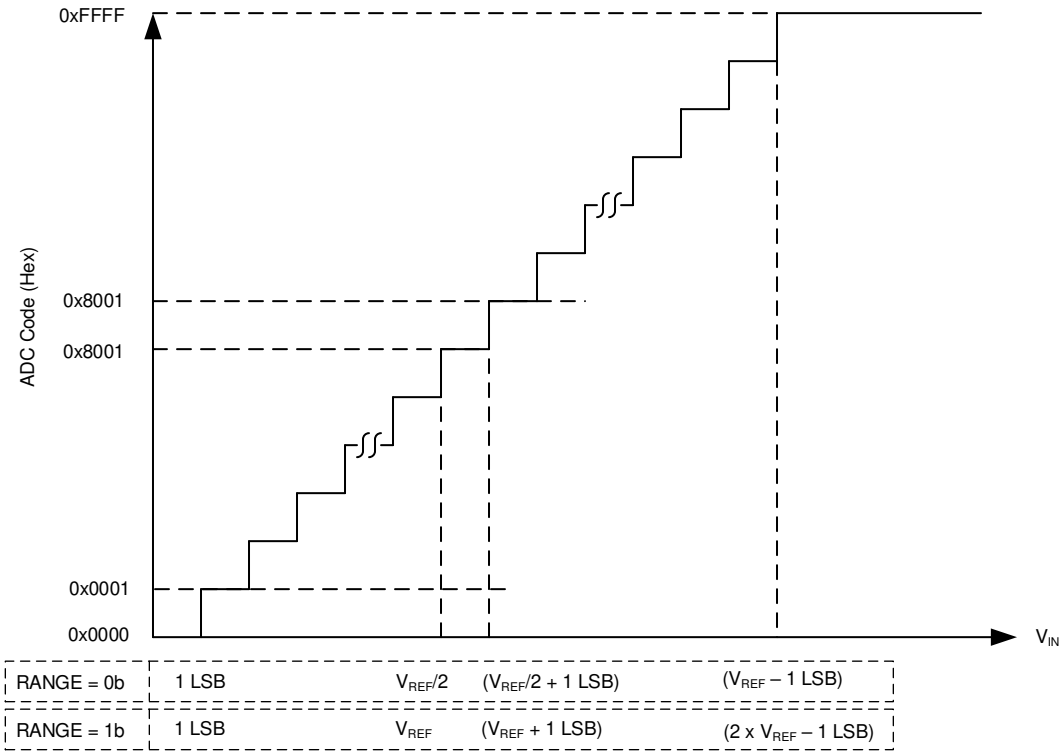


图 4. Ideal Transfer Characteristics

表 1. Transfer Characteristics

INPUT VOLTAGE		CODE	IDEAL OUTPUT CODE
RANGE = 0b	RANGE = 1b		
≤1 LSB	≤1 LSB	Zero	0000
1 LSB to 2 LSBs	1 LSB to 2 LSBs	Zero + 1	0001
(V_{REF} / 2) to (V_{REF} / 2) + 1 LSB	V_{REF} to V_{REF} + 1 LSB	Mid-scale code	8000
(V_{REF} / 2) + 1 LSB to (V_{REF} / 2) + 2 LSBs	V_{REF} + 1 LSB to V_{REF} + 2 LSBs	Mid-scale code + 1	8001
≥ V_{REF} – 1 LSB	≥ 2 x V_{REF} – 1 LSB	Full-scale code	FFFF

ADVANCE INFORMATION

7.3.4 ADC Offset Calibration

The variation in ADC offset error because of changes in temperature or reference voltage can be calibrated by setting the CAL bit in the GENERAL_CFG register. The CAL bit is reset to 0 after calibration. The host can poll the CAL bit to check the ADC offset calibration completion status.

7.3.5 Programmable Averaging Filters

The ADS7066 features a programmable averaging filter that can be used to average analog input samples to output a higher resolution measurement. The averaging filter can be enabled by programming the OSR[2:0] bits in the OSR_CFG register to the averaging factor desired. The averaging configuration is common to all analog input channels. As shown in 图 5, the output of the averaging filter is 20 bits long. In manual mode and auto-sequence mode of conversion, only the first conversion for the selected analog input channel must be initiated by the host, as shown in 图 5; any remaining conversions are generated internally. The time required to complete the averaging operation is determined by the sampling speed and number of samples to be averaged. After completion, the averaged 20-bit result, as shown in 图 5, can be read-out.

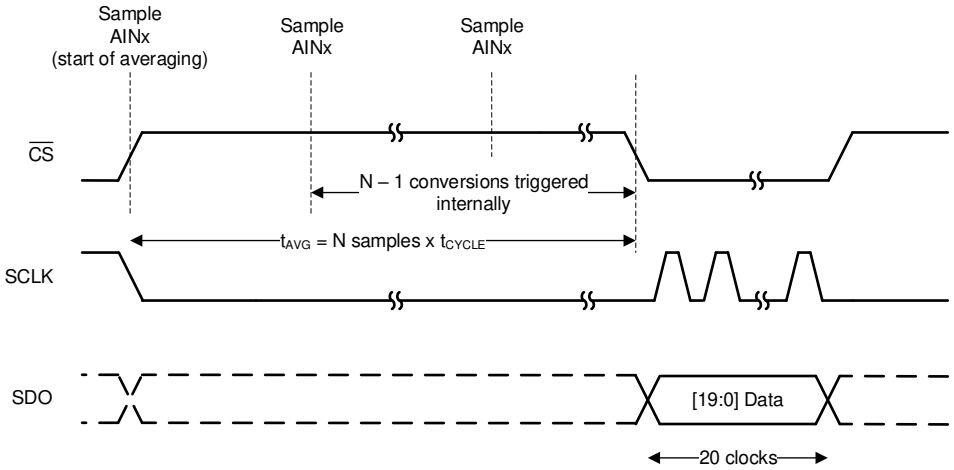


图 5. Averaging Example

In autonomous mode of operation, samples from analog input channels that are enabled in the AUTO_SEQ_CH_SEL register are averaged sequentially.

7.3.6 CRC on Data Interface

The cyclic redundancy check (CRC) is an error checking code that detects communication errors to and from the host. CRC is the division remainder of the data payload bytes by a fixed polynomial. The data payload is two or three bytes, depending on the output data format; see the *Output Data Format* section for details on output data format. The CRC mode is optional and is enabled by the CRC_EN bit in the GENERAL_CFG register.

The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-ATM (HEC): $X^8 + X^2 + X^1 + 1$. The nine binary polynomial coefficients are: 100000111. The CRC calculation is preset with *1* data values.

The host must compute and append the appropriate CRC to the command string in the same SPI frame (see the *Register Read/Write Operation* section). The ADC repeats the CRC calculation and compares the calculation to the received CRC. If the host and repeated ADC CRC values match, the command executes. If the operation is conversion data or register data read, the ADC responds with a second CRC that is computed over the requested data payload bytes. The response data payload is one, two, or three bytes depending on the data operation.

If the host CRC and repeated CRC values do not match, the command does not execute and the error condition can be detected, as listed in 表 2, by either status flags or by a register read.

表 2. Configuring Notifications when CRC Error is Detected

CRC ERROR NOTIFICATION	CONFIGURATION	DESCRIPTION
Status flags	APPEND_STATUS = 10b	4-bit status flags, containing the CRCERR_IN bit appended to the ADC data; see the *Output Data Format* section for details.
Register read	—	Read the CRCERR_IN bit to check if a CRC error was detected.

Further register writes are disabled until the CRCERR_IN bit is cleared by writing 1b to this bit. ADC conversion data and register data can continue to be read before clearing the CRCERR_IN bit.

7.3.7 Oscillator and Timing Control

The device uses an internal oscillator for conversion. When using the averaging module, the host initiates the first conversion and subsequent conversions are generated internally by the device. When the device generates the start of a conversion, the sampling rate can be controlled as described in 表 3 by the OSC_SEL and CLK_DIV[3:0] register fields.

表 3. Configuring the Sampling Rate for Internal Conversion Start Control

CLK_DIV[3:0]	OSC_SEL = 0		OSC_SEL = 1	
	SAMPLING FREQUENCY, f_{CYCLE} (kSPS)	CYCLE TIME, t_{CYCLE} (µs)	SAMPLING FREQUENCY, f_{CYCLE} (kSPS)	CYCLE TIME, t_{CYCLE} (µs)
0000b	Reserved. Do not use.	1	31.25	32
0001b	Reserved. Do not use.	1.5	20.83	48
0010b	Reserved. Do not use.	2	15.63	64
0011b	Reserved. Do not use.	3	10.42	96
0100b	250	4	7.81	128
0101b	166.7	6	5.21	192
0110b	125	8	3.91	256
0111b	83	12	2.60	384
1000b	62.5	16	1.95	512
1001b	41.7	24	1.3	768
1010b	31.3	32	0.98	1024
1011b	20.8	48	0.65	1536
1100b	15.6	64	0.49	2048
1101b	10.4	96	0.33	3072

The conversion time of the device, given by t_{CONV} in the *Switching Characteristics* table, is independent of the OSC_SEL and CLK_DIV[3:0] configuration.

ADVANCE INFORMATION

7.3.8 Diagnostic Modes

The ADS7066 features a programmable test voltage generation circuit that can be used for ADC diagnostics.

7.3.8.1 Bit-Walk Test Mode

To enable write access to the configuration registers for diagnostics, write 0x96 in the DIAGNOSTICS_KEY register. To enable bit-walk test mode, configure BITWALK_EN = 1b. In the bit-walk test mode (see 图 3), the sampling switch (SW) remains open and the test voltage is applied on the sampling capacitor (C_{SH}) during the acquisition phase of the ADC. In diagnostic mode, the conversion process of the ADC remains the same as when not in diagnostic mode. The ADC starts the conversion phase on the rising edge of $\overline{CS}$ and outputs the code corresponding to the sampled test voltage. The output code of the ADC is expected to be proportional to the test voltage, as shown in 公式 2, after adjusting for DC errors (such as INL, gain error, offset error, and thermal drift of offset and gain errors).

$$\text{Output code} = \left(\frac{\text{Test voltage}}{V_{REF}} \times 2^{16}\right) \pm \text{TUE} \quad (2)$$

where

- TUE = Total unadjusted error, given by the root sum square of the offset error, gain error, and INL

The test voltage is generated by a DAC configured by the BIT_SAMPLE_MSB and BIT_SAMPLE_LSB registers. Because the test voltage is derived from the ADC reference, as given by 公式 3, this diagnostic mode is not sensitive to variations in reference voltage.

$$\text{Test voltage} = \frac{V_{REF}}{\text{BIT\_SAMPLE}[15:0]} \pm \text{TUE} \quad (3)$$

To resume conversion of the ADC input signal, configure BITWALK_EN = 0b.

7.3.8.2 Fixed Voltage Test Mode

For diagnostics, the ADS7066 features a fixed 1.8 V (typical) test voltage which can be internally connected to AIN6. To connect AIN6 to the internal test voltage, set VTEST_EN = 1b. When using the fixed voltage test mode, AIN6 pin must be left floating and should not be connected to any external circuit.

If bit-walk test mode is enabled (that is, BITWALK_EN = 1b), enabling the fixed voltage test mode will connect AIN6 to the test voltage but the conversion result would be according to bit-walk test mode configuration.

7.3.9 Output Data Format

图 6 illustrates that the output data payload consists of a combination of the conversion result, data bits from averaging filters, status flags, and channel ID. The conversion result is MSB aligned. If averaging is enabled, the output data from the ADC are 20 bits long, otherwise the data are 16 bits long. Optionally, the 4-bit channel ID or status flags can be appended at the end of the output data by configuring the APPEND_STATUS[1:0] fields.

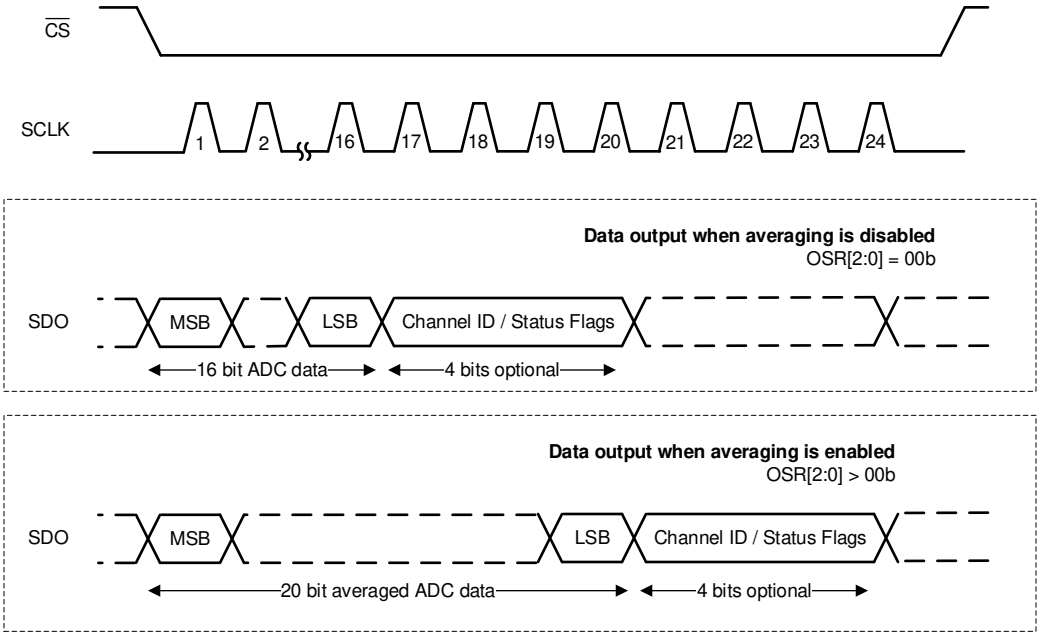


图 6. SPI Frames for Reading Data

7.3.9.1 Status Flags

Status flags can be appended to the ADC output by setting APPEND_STATUS = 10b. The status flag is appended only to frames where ADC data are being read. Status flags are not appended to register read data or when FIX_PAT = 1b. The 4-bit status flag field is constructed as follows:

Status flag[3:0] = { 1, VTEST_MODE, CRCERR_IN, DIAG_MODE }

where:

- VTEST_MODE: This flag is set if the current data frame corresponds to fixed voltage test mode (see the *Fixed Voltage Test Mode* section).
- CRCERR_IN: This flag indicates the status of the CRC verification of data received from the digital interface. This flag is the same as the CRCERR_IN bit in the SYSTEM_STATUS register.
- DIAG_MODE: This flag is set if the current data frame corresponds to the bit-walk test mode (see the *Bit-Walk Test Mode* section).

7.3.9.2 Output CRC (Device to Host)

A CRC byte can be appended to the output data by configuring CRC_EN to 1b. When the CRC module is enabled, the host must use 32-bit frames for SPI communication. The device outputs the data payload followed by the CRC byte computed over the data payload. Additional 0s can be appended by the ADC after the CRC byte to complete the 32-bit SPI frame (see 表 4). The host must compute the CRC corresponding to the data payload and match the computed CRC with the CRC received from the device. The additional 0s appended by the device after the CRC byte must be excluded by the host for computing the CRC.

7.3.9.3 Input CRC (Host to Device)

When the CRC module is enabled, the host must always communicate with the ADC using 32-bit SPI frames comprised of a 24-bit data payload and an 8-bit CRC byte. The host must calculate the CRC byte to be appended based on a 24-bit payload. The ADC computes a CRC over the 24-bit data payload and matches the computed CRC with the CRC received from the host.

The ADS7066 supports daisy-chain mode; see the *Daisy-Chain Mode* section for more details. The serial input data (SDI) are shifted on the serial data output (SDO) after 24 SCLKs. If the output data payload is less than 24 bits long, additional 0s are output until the 24th SCLK. Daisy-chain mode is not supported when the CRC module is enabled.

ADVANCE INFORMATION

表 4. Output Data Frames

CRC_EN	OSR[2:0]	APPEND_STATUS[1:0]	OUTPUT DATA FRAME	DAISY-CHAIN MODE
CRC module disabled (CRC_EN = 0)	No averaging	No flags (00b or 11b)	{Conversion result [15:0], 8'b0}	Supported
		Channel ID (01b)	{Conversion result [15:0], CHID[3:0], 4'b0}	Supported
		Status flags (10b)	{Conversion result [15:0], status flags[3:0], 4'b0}	Supported
	Averaging enabled	No flags (00b or 11b)	{Conversion result [19:0], 4'b0}	Supported
		Channel ID (01b)	{Conversion result [19:0], CHID[3:0]}	Supported
		Status flags (10b)	{Conversion result [19:0], status flags[3:0]}	Supported
CRC module enabled (CRC_EN = 1)	No averaging	No flags (00b or 11b)	{Conversion result [15:0], CRC[7:0], 8'b0}	Supported
		Channel ID (01b)	{Conversion result [15:0], CHID[3:0], 4'b0, CRC[7:0]}	Not supported
		Status flags (10b)	{Conversion result [15:0], status flags[3:0], 4'b0, CRC[7:0]}	Not supported
	Averaging enabled	No flags (00b or 11b)	{Conversion result [19:0], 4'b0, CRC[7:0]}	Not supported
		Channel ID (01b)	{Conversion result [19:0], CHID[3:0], CRC[7:0]}	Not supported
		Status flags (10b)	{Conversion result [19:0], status flags[3:0], CRC[7:0]}	Not supported

7.3.10 Device Programming

7.3.10.1 Enhanced-SPI Interface

The device features an enhanced-SPI interface that allows the host controller to operate at slower SCLK speeds and still achieve full throughput. As described in 表 5, the host controller can use any of the four SPI-compatible protocols (SPI-00, SPI-01, SPI-10, or SPI-11) to access the device.

表 5. SPI Protocols for Configuring the Device

PROTOCOL	SCLK POLARITY (At the $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	CPOL_CPHA[1:0]	DIAGRAM
SPI-00	Low	Rising	00b	图 7
SPI-01	Low	Falling	01b	图 8
SPI-10	High	Falling	10b	图 7
SPI-11	High	Rising	11b	图 8

On power-up, the device defaults to the SPI-00 protocol for data read and data write operations. To select a different SPI-compatible protocol, program the CPOL_CPHA[1:0] field. This first write operation must adhere to the SPI-00 protocol. Any subsequent data transfer frames must adhere to the newly-selected protocol.

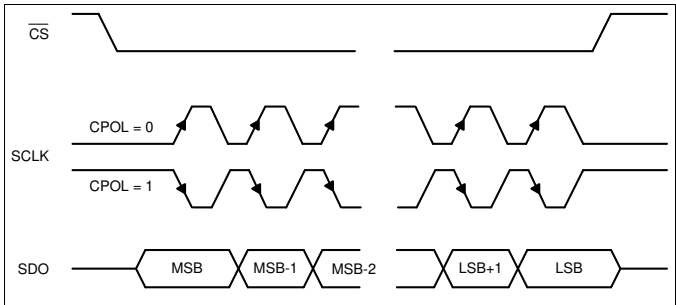


图 7. Standard SPI Timing Protocol (CPHA = 0)

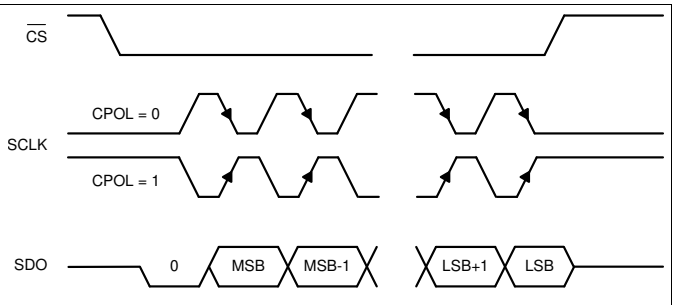


图 8. Standard SPI Timing Protocol (CPHA = 1)

7.3.10.2 Daisy-Chain Mode

The ADS7066 can operate as a single converter or in a system with multiple converters. System designers can take advantage of the simple, high-speed, enhanced-SPI serial interface by cascading converters in a daisy-chain configuration when multiple converters are used. No register configuration is required to enable daisy-chain mode. 图 9 shows a typical connection of three converters in daisy-chain mode.

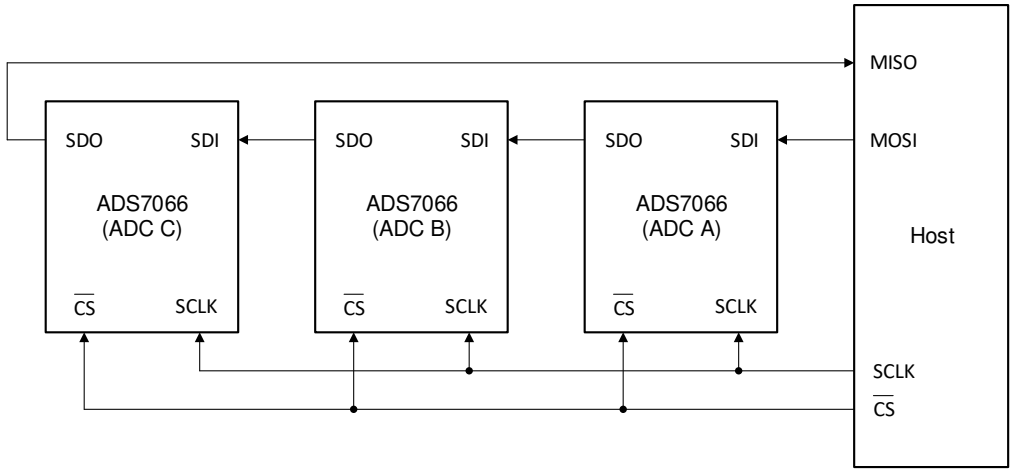


图 9. Multiple Converters Connected Using Daisy-Chain Mode

When the ADS7066 is connected in daisy-chain mode, the serial input data passes through the ADS7066 with a 24-SCLK delay, as long as $\overline{CS}$ is active. 图 10 shows a detailed timing diagram of this mode. In 图 10, the conversion in each converter is performed simultaneously.

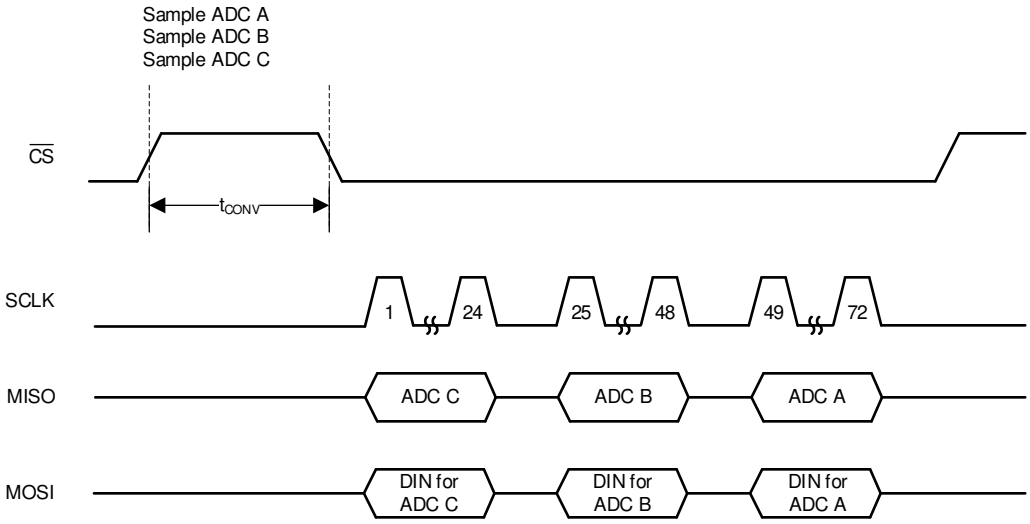


图 10. Simplified Daisy-Chain Mode Timing

The ADS7066 supports daisy-chain mode for output data payloads up to 24 bits long; see the *Output Data Format* section for more details. If either the status flags or channel ID are appended (APPEND_STATUS ≠ 00b) and the CRC module is enabled (CRC_EN = 1b), then the serial input data does not pass through the ADS7066 and daisy-chain mode is disabled.

ADVANCE INFORMATION

7.3.10.3 Register Read/Write Operation

The device supports the commands listed in 表 6 to access the internal configuration registers

表 6. Opcodes for Commands

OPCODE	COMMAND DESCRIPTION
0000 0000b	No operation
0001 0000b	Single register read
0000 1000b	Single register write
0001 1000b	Set bit
0010 0000b	Clear bit

7.3.10.3.1 Register Write

A 24-bit SPI frame is required to write data to configuration registers. The 24-bit data on SDI, as shown in 图 11, consists of an 8-bit write command (0000 1000b), an 8-bit register address, and 8-bit data. The write command is decoded on the $\overline{CS}$ rising edge and the specified register is updated with the 8-bit data specified in the register write operation.

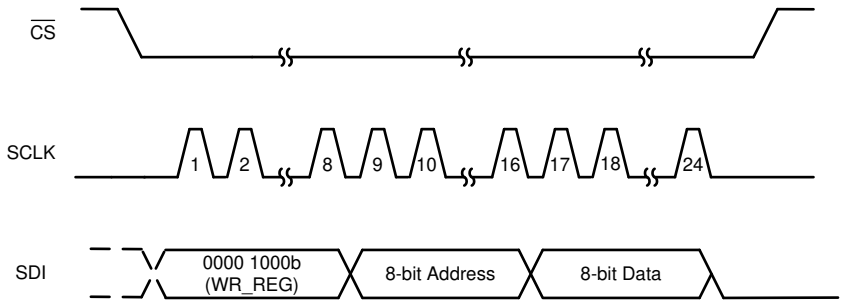


图 11. Register Write Operation

7.3.10.3.2 Register Read

A register read operation consists of two SPI frames: the first SPI frame initiates a register read and the second SPI frame reads data from the register address provided in the first frame. As shown in 图 12, the read command (0001 0000b), the 8-bit register address, and the 8-bit dummy data are sent over the SDI pin during the first 24-bit frame. On the rising edge of $\overline{CS}$, the read command is decoded and the requested register data are available for reading during the next frame. During the second frame, the first eight bits on SDO correspond to the requested register read. During the second frame, SDI can be used to initiate another operation or can be set to 0.

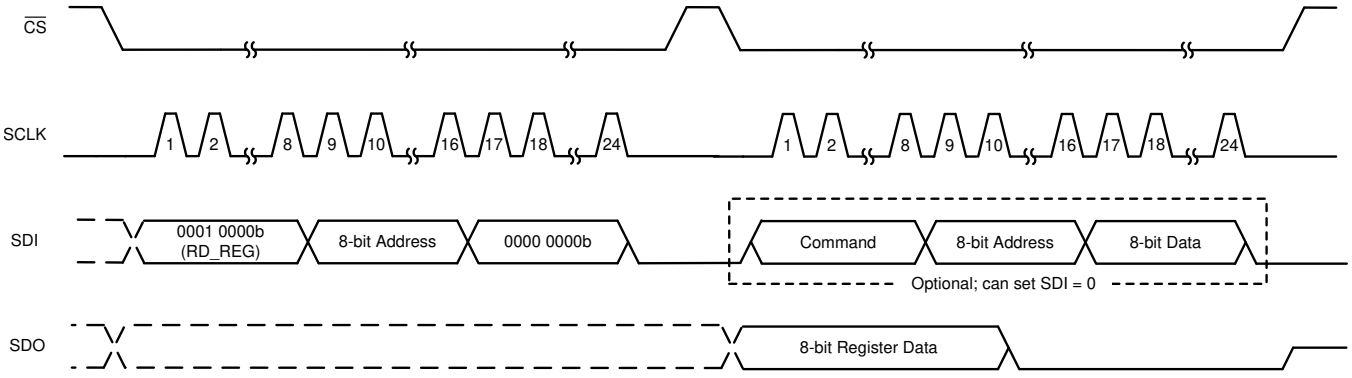


图 12. Register Read Operation

7.3.10.3.2.1 Register Read With CRC

A register read consists of two SPI frames, as described in the *Register Read* section. When the CRC module is enabled during a register read, as shown in 图 13, the device appends an 8-bit output CRC byte along with 8-bit register data. The output CRC is computed by the device on the 8-bit register data.

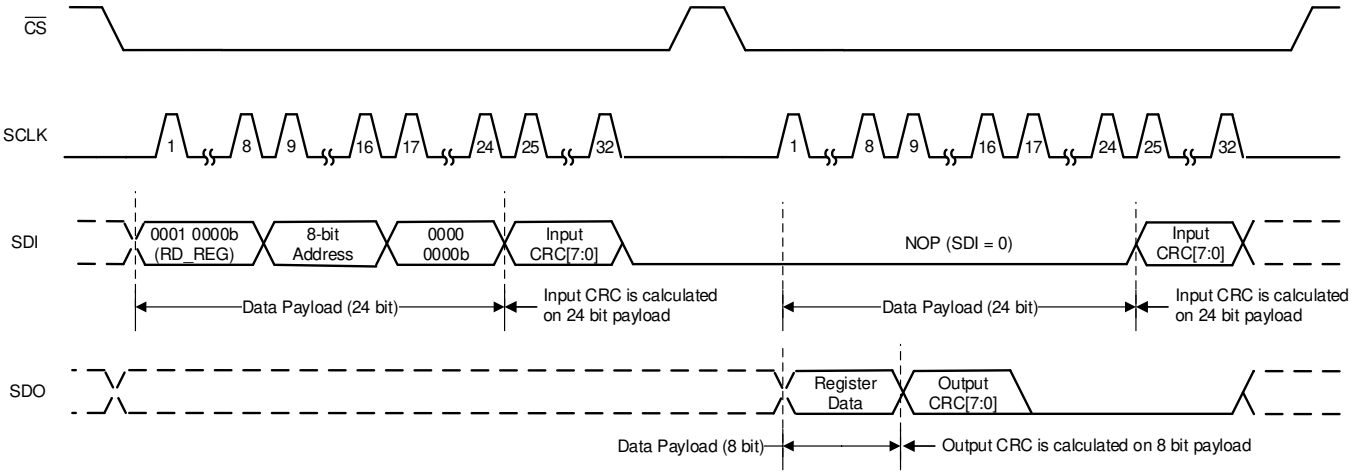


图 13. Register Read With CRC

ADVANCE INFORMATION

7.4 Device Functional Modes

表 7 lists the functional modes supported by the ADS7066.

表 7. Functional Modes

FUNCTIONAL MODE	CONVERSION CONTROL	MUX CONTROL	SEQ_MODE[1:0]
Manual	$\overline{CS}$ rising edge	Register write to MANUAL_CHID	00b
On-the-fly	$\overline{CS}$ rising edge	First 5 bits after $\overline{CS}$ falling edge	10b
Auto-sequence	$\overline{CS}$ rising edge	Channel sequencer	01b

The device powers up in manual mode and can be configured into either of these modes by writing the configuration registers for the desired mode.

7.4.1 Device Power-Up and Reset

On power up, the BOR bit is set indicating a power-cycle or reset event. The device can be reset by setting the RST bit or by recycling the power on the AVDD pin.

7.4.2 Manual Mode

Manual mode allows the external host processor to directly select the analog input channel. 图 14 shows steps for operating the device in manual mode.

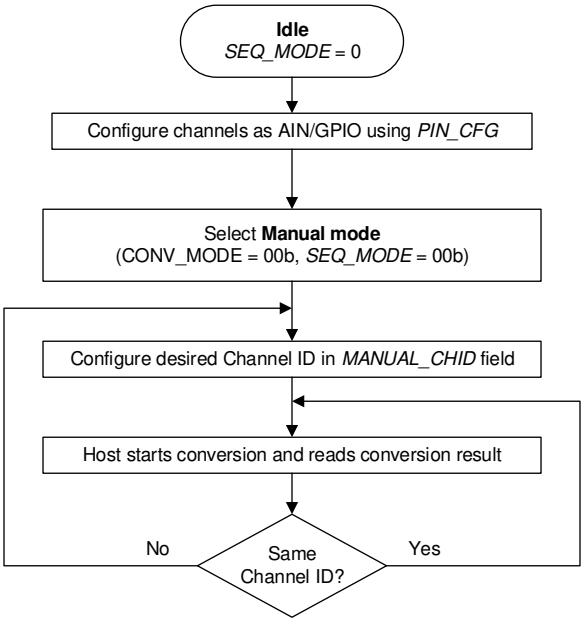


图 14. Device Operation in Manual Mode

In manual mode, the command to switch to a new channel, cycle N in 图 15, is decoded by the device on the $\overline{CS}$ rising edge. The $\overline{CS}$ rising edge is also the start of the conversion signal, and thus the device samples the previously selected MUX channel in cycle N+1. The newly selected analog input channel data are available in cycle N+2. For switching the analog input channel, a register write to the MANUAL_CHID field requires 24 clocks; see the *Register Write* section for more details. After a channel is selected, the number of clocks required for reading the output data depends on the device output data frame size; see the *Output Data Format* section for more details.

ADVANCE INFORMATION

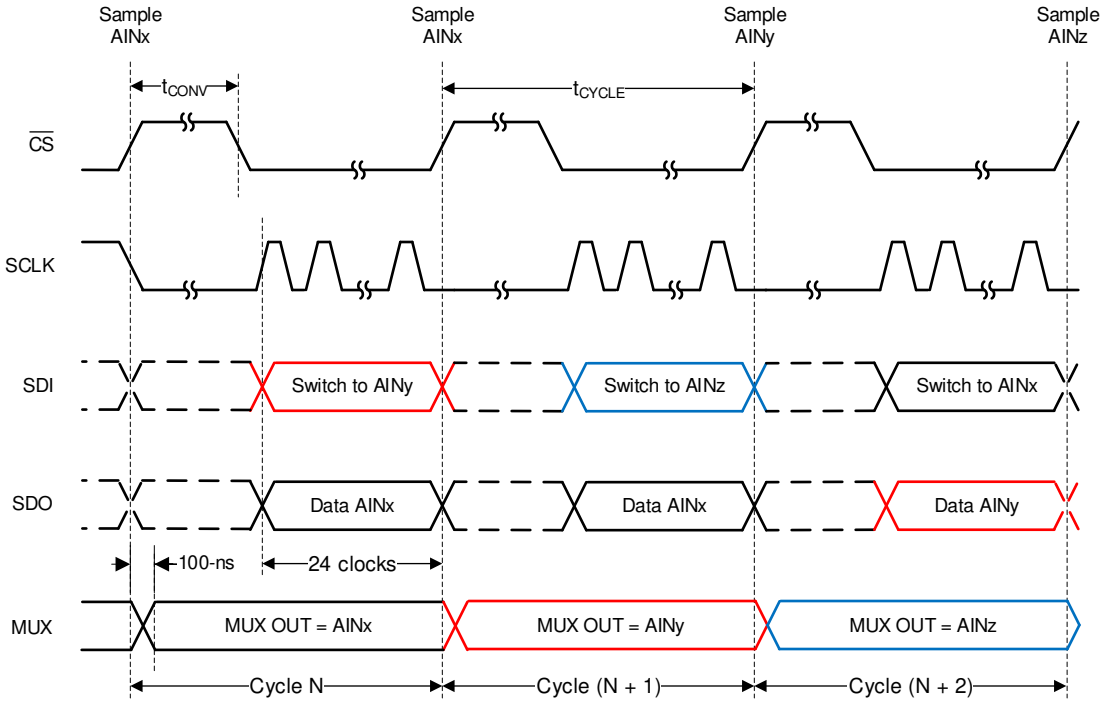


图 15. Starting a Conversion and Reading Data in Manual Mode

7.4.3 On-the-Fly Mode

In the on-the-fly mode of operation, as shown in 图 16, the analog input channel is selected using the first five bits on SDI without waiting for the $\overline{CS}$ rising edge. Thus, the ADC samples the newly selected channel on the $\overline{CS}$ rising edge and there is no latency between the channel selection and the ADC output data. 表 8 lists the channel selection commands for this mode.

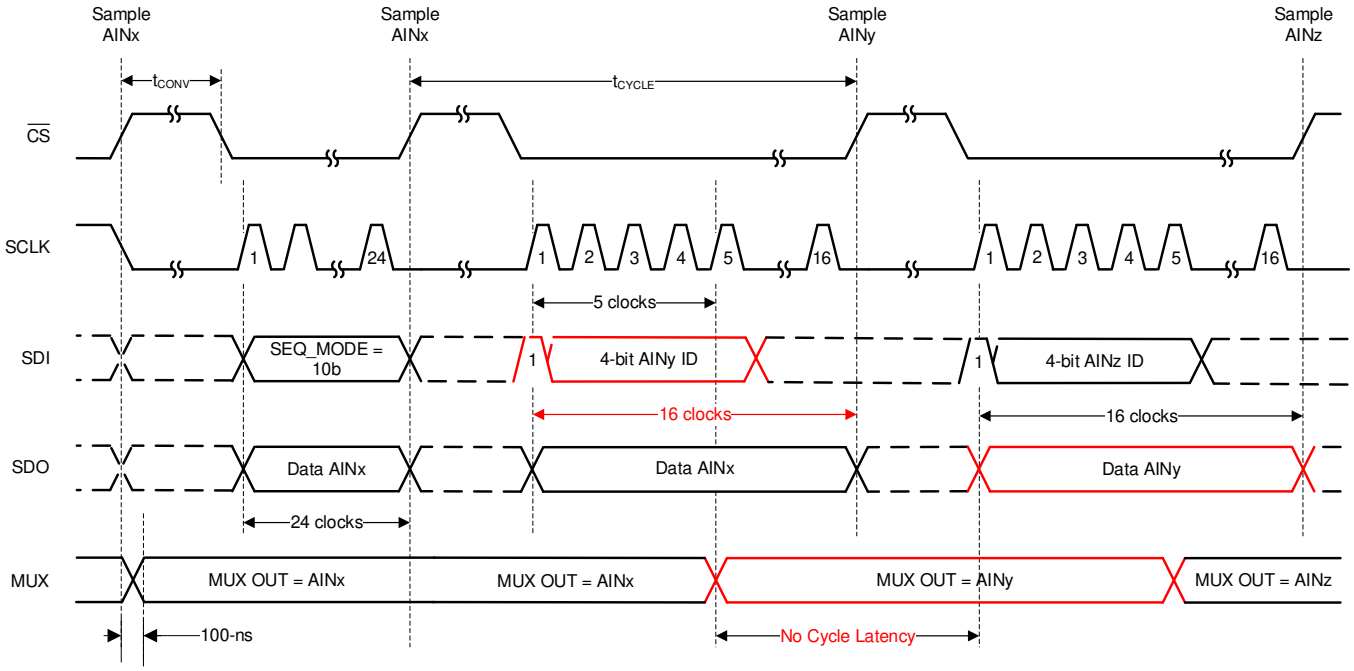


图 16. Starting a Conversion and Reading data in On-the-Fly Mode

ADVANCE INFORMATION

表 8. On-the-Fly Mode Channel Selection Commands

SDI BITS[15:11]	SDI BITS [10:0]	DESCRIPTION
1 0000	Don't care	Select analog input 0
1 0001	Don't care	Select analog input 1
1 0010	Don't care	Select analog input 2
1 0011	Don't care	Select analog input 3
1 0100	Don't care	Select analog input 4
1 0101	Don't care	Select analog input 5
1 0110	Don't care	Select analog input 6
1 0111	Don't care	Select analog input 7
1 1000 to 1 1111	Don't care	Reserved

The number of clocks required for reading the output data depends on the device output data frame size; see the *Output Data Format* section for more details.

7.4.4 Auto-Sequence Mode

In auto-sequence mode, the internal channel sequencer switches the multiplexer to the next analog input channel after every conversion. The desired analog input channels can be configured for sequencing in the AUTO_SEQ_CHSEL register. To enable the channel sequencer, set SEQ_START = 1b. After every conversion, the channel sequencer switches the multiplexer to the next analog input in ascending order. To stop the channel sequencer from selecting channels, set SEQ_START = 0b.

In the example shown in 图 17, AIN2 and AIN6 are enabled for sequencing in the AUTO_SEQ_CHSEL register. The channel sequencer loops through AIN2 and AIN6 and repeats until SEQ_START is set to 0b. The number of clocks required for reading the output data depends on the device output data frame size; see the *Output Data Format* section for more details.

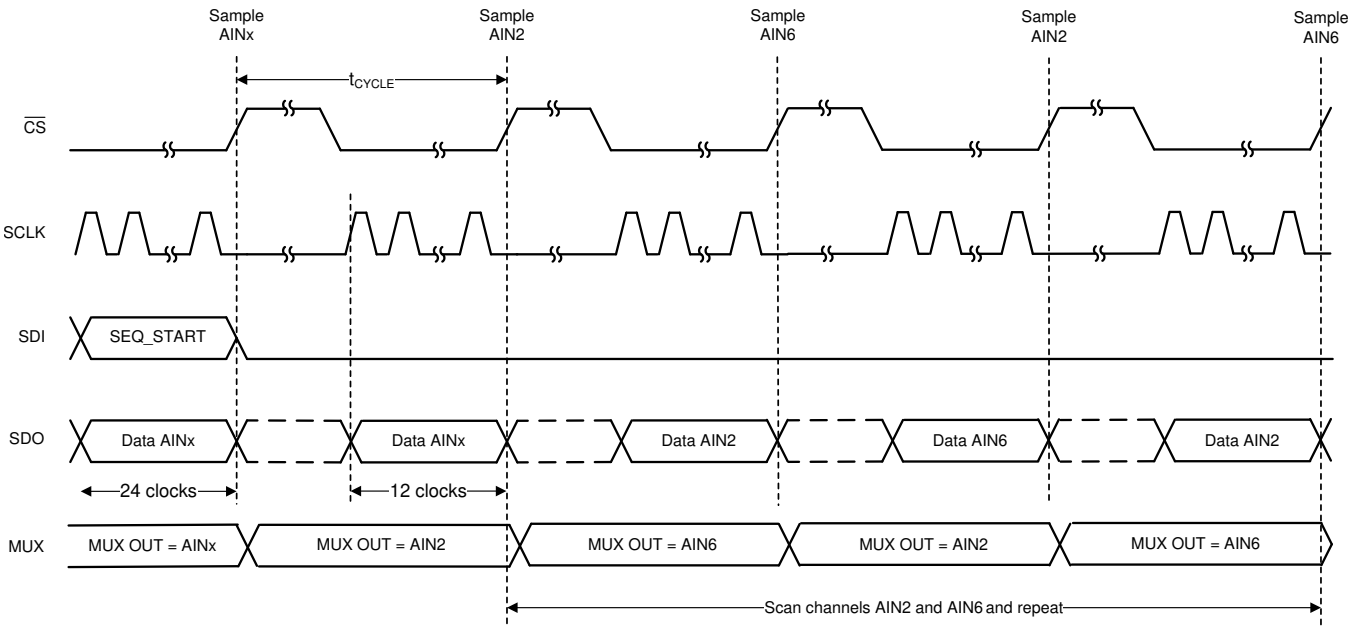


图 17. Starting Conversion and Reading Data in Auto-Sequence Mode

ADVANCE INFORMATION

7.5 ADS7066 Registers

Table 9 lists the ADS7066 registers. All register offset addresses not listed in Table 9 should be considered as reserved locations and the register contents should not be modified.

Table 9. ADS7066 Registers

Address	Acronym	Register Name	Section
0x0	SYSTEM_STATUS		SYSTEM_STATUS Register (Address = 0x0) [reset = 0x81]
0x1	GENERAL_CFG		GENERAL_CFG Register (Address = 0x1) [reset = 0x0]
0x2	DATA_CFG		DATA_CFG Register (Address = 0x2) [reset = 0x0]
0x3	OSR_CFG		OSR_CFG Register (Address = 0x3) [reset = 0x0]
0x4	OPMODE_CFG		OPMODE_CFG Register (Address = 0x4) [reset = 0x0]
0x5	PIN_CFG		PIN_CFG Register (Address = 0x5) [reset = 0x0]
0x7	GPIO_CFG		GPIO_CFG Register (Address = 0x7) [reset = 0x0]
0x9	GPO_DRIVE_CFG		GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]
0xB	GPO_OUTPUT_VALUE		GPO_OUTPUT_VALUE Register (Address = 0xB) [reset = 0x0]
0xD	GPI_VALUE		GPI_VALUE Register (Address = 0xD) [reset = 0x0]
0x10	SEQUENCE_CFG		SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]
0x11	CHANNEL_SEL		CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]
0x12	AUTO_SEQ_CH_SEL		AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]
0xBF	DIAGNOSTICS_KEY		DIAGNOSTICS_KEY Register (Address = 0xBF) [reset = 0x0]
0xC0	DIAGNOSTICS_EN		DIAGNOSTICS_EN Register (Address = 0xC0) [reset = 0x0]
0xC1	BIT_SAMPLE_LSB		BIT_SAMPLE_LSB Register (Address = 0xC1) [reset = 0x0]
0xC2	BIT_SAMPLE_MSB		BIT_SAMPLE_MSB Register (Address = 0xC2) [reset = 0x0]

Complex bit access types are encoded to fit into small table cells. Table 10 shows the codes that are used for access types in this section.

Table 10. ADS7066 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

ADVANCE INFORMATION

7.5.1 SYSTEM_STATUS Register (Address = 0x0) [reset = 0x81]

SYSTEM_STATUS is shown in Figure 18 and described in Table 11.

Return to the Summary Table.

Figure 18. SYSTEM_STATUS Register

7	6	5	4	3	2	1	0
RSVD	SEQ_STATUS	RESERVED			CRCERR_FUSE	CRCERR_IN	BOR
R-1b	R-0b	R-0b			R-0b	R/W-0b	R/W-1b

Table 11. SYSTEM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSVD	R	1b	Reads return 1b.
6	SEQ_STATUS	R	0b	Status of the channel sequencer. 0b = Sequence stopped 1b = Sequence in progress
5-3	RESERVED	R	0b	Reserved. Reads return 0.
2	CRCERR_FUSE	R	0b	Device power-up configuration CRC check status. To re-evaluate this bit, software reset the device or power cycle AVDD. 0b = No problems detected in power-up configuration. 1b = Device configuration not loaded correctly.
1	CRCERR_IN	R/W	0b	Status of CRC check on incoming data. Write 1b to clear this error flag. 0b = No CRC error. 1b = CRC error detected. All register writes, except to addresses 0x00 and 0x01, are blocked.
0	BOR	R/W	1b	Brown out reset indicator. This bit is set if brown out condition occurs or device is power cycled. Write 1b to this bit to clear the flag. 0b = No brown out since last time this bit was cleared. 1b = Brown out condition detected or device power cycled.

7.5.2 GENERAL_CFG Register (Address = 0x1) [reset = 0x0]

GENERAL_CFG is shown in Figure 19 and described in Table 12.

Return to the Summary Table.

Figure 19. GENERAL_CFG Register

7	6	5	4	3	2	1	0
REF_EN	CRC_EN	RESERVED		RANGE	CH_RST	CAL	RST
R/W-0b	R/W-0b	R-0b		R/W-0b	R/W-0b	R/W-0b	W-0b

Table 12. GENERAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	REF_EN	R/W	0b	Enable or disable the internal reference. 0b = Internal reference is powered down. 1b = Internal reference is enabled.
6	CRC_EN	R/W	0b	Enable or disable the CRC on device interface. 0b = CRC module disabled. 1b = CRC appended to data output. CRC check is enabled on incoming data.
5-4	RESERVED	R	0b	Reserved. Reads return 0.

Table 12. GENERAL_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3	RANGE	R/W	0b	Select the input range of the ADC. 0b = Input range of the ADC is 1x VREF 1b = Input range of the ADC is 2x VREF
2	CH_RST	R/W	0b	Force all channels to be analog inputs. 0b = Normal operation 1b = All channels will be set as analog inputs irrespective of configuration in other registers
1	CAL	R/W	0b	Calibrate ADC offset. 0b = Normal operation. 1b = ADC offset is calibrated. After calibration is complete, this bit is set to 0b.
0	RST	W	0b	Software reset all registers to default values. 0b = Normal operation. 1b = Device is reset. After reset is complete, this bit is set to 0b and BOR bit is set to 1b.

7.5.3 DATA_CFG Register (Address = 0x2) [reset = 0x0]

DATA_CFG is shown in Figure 20 and described in Table 13.

Return to the Summary Table.

Figure 20. DATA_CFG Register

7	6	5	4	3	2	1	0
FIX_PAT	RESERVED	APPEND_STATUS[1:0]		RESERVED		CPOL_CPHA[1:0]	
R/W-0b	R-0b	R/W-0b		R-0b		R/W-0b	

Table 13. DATA_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FIX_PAT	R/W	0b	Device outputs fixed data bits which can be helpful for debugging communication with the device. 0b = Normal operation. 1b = Device outputs fixed code 0xA5A5 repeatitively when reading ADC data.
6	RESERVED	R	0b	Reserved. Reads return 0b.
5-4	APPEND_STATUS[1:0]	R/W	0b	Append 4-bit channel ID or status flags to output data. 0b = Channel ID and status flags are not appended to ADC data. 1b = 4-bit channel ID is appended to ADC data. 10b = 4-bit status flags are appended to ADC data. 11b = Reserved.
3-2	RESERVED	R	0b	Reserved. Reads return 0.
1-0	CPOL_CPHA[1:0]	R/W	0b	This field sets the polarity and phase of SPI communication. 0b = CPOL = 0, CPHA = 0. 1b = CPOL = 0, CPHA = 1. 10b = CPOL = 1, CPHA = 0. 11b = CPOL = 1, CPHA = 1.

7.5.4 OSR_CFG Register (Address = 0x3) [reset = 0x0]

OSR_CFG is shown in Figure 21 and described in Table 14.

Return to the Summary Table.

Figure 21. OSR_CFG Register

7	6	5	4	3	2	1	0
RESERVED					OSR[2:0]		
R-0b					R/W-0b		

Table 14. OSR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0b	Reserved. Reads return 0.
2-0	OSR[2:0]	R/W	0b	Selects the oversampling ratio for ADC conversion result. 0b = No averaging 1b = 2 samples 10b = 4 samples 11b = 8 samples 100b = 16 samples 101b = 32 samples 110b = 64 samples 111b = 128 samples

7.5.5 OPMODE_CFG Register (Address = 0x4) [reset = 0x0]

OPMODE_CFG is shown in Figure 22 and described in Table 15.

Return to the Summary Table.

Figure 22. OPMODE_CFG Register

7	6	5	4	3	2	1	0
RESERVED			OSC_SEL	CLK_DIV[3:0]			
R-0b			R/W-0b	R/W-0b			

Table 15. OPMODE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0.
4	OSC_SEL	R/W	0b	Selects the oscillator for internal timing generation. 0b = High-speed oscillator. 1b = Low-power oscillator.
3-0	CLK_DIV[3:0]	R/W	0b	Sampling speed control when using averaging filters. Refer to section on oscillator and timing control for details.

7.5.6 PIN_CFG Register (Address = 0x5) [reset = 0x0]

PIN_CFG is shown in Figure 23 and described in Table 16.

Return to the Summary Table.

Figure 23. PIN_CFG Register

7	6	5	4	3	2	1	0
PIN_CFG[7:0]							
R/W-0b							

Table 16. PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PIN_CFG[7:0]	R/W	0b	Configure device channels AIN/GPIO [7:0] as analog inputs or GPIOs. 0b = Channel is configured as analog input. 1b = Channel is configured as GPIO.

7.5.7 GPIO_CFG Register (Address = 0x7) [reset = 0x0]

GPIO_CFG is shown in Figure 24 and described in Table 17.

Return to the Summary Table.

Figure 24. GPIO_CFG Register

7	6	5	4	3	2	1	0
GPIO_CFG[7:0]							
R/W-0b							

Table 17. GPIO_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPIO_CFG[7:0]	R/W	0b	Configure GPIO[7:0] as either digital inputs or digital outputs. 0b = GPIO is configured as digital input. 1b = GPIO is configured as digital output.

7.5.8 GPO_DRIVE_CFG Register (Address = 0x9) [reset = 0x0]

GPO_DRIVE_CFG is shown in Figure 25 and described in Table 18.

Return to the Summary Table.

Figure 25. GPO_DRIVE_CFG Register

7	6	5	4	3	2	1	0
GPO_DRIVE_CFG[7:0]							
R/W-0b							

Table 18. GPO_DRIVE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_DRIVE_CFG[7:0]	R/W	0b	Configure digital outputs GPO[7:0] as open-drain or push-pull outputs. 0b = Digital output is open-drain; connect external pullup resistor. 1b = Push-pull driver is used for digital output.

7.5.9 GPO_OUTPUT_VALUE Register (Address = 0xB) [reset = 0x0]

GPO_OUTPUT_VALUE is shown in Figure 26 and described in Table 19.

Return to the Summary Table.

Figure 26. GPO_OUTPUT_VALUE Register

7	6	5	4	3	2	1	0
GPO_OUTPUT_VALUE[7:0]							
R/W-0b							

Table 19. GPO_OUTPUT_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPO_OUTPUT_VALUE[7:0]	R/W	0b	Logic level to be set on digital outputs GPO[7:0]. 0b = Digital output set to logic 0. 1b = Digital output set to logic 1.

7.5.10 GPI_VALUE Register (Address = 0xD) [reset = 0x0]

GPI_VALUE is shown in Figure 27 and described in Table 20.

Return to the Summary Table.

Figure 27. GPI_VALUE Register

7	6	5	4	3	2	1	0
GPI_VALUE[7:0]							
R-0b							

Table 20. GPI_VALUE Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPI_VALUE[7:0]	R	0b	Readback the logic level on GPIO[7:0]. 0b = GPIO is at logic 0. 1b = GPIO is at logic 1.

7.5.11 SEQUENCE_CFG Register (Address = 0x10) [reset = 0x0]

SEQUENCE_CFG is shown in Figure 28 and described in Table 21.

Return to the Summary Table.

Figure 28. SEQUENCE_CFG Register

7	6	5	4	3	2	1	0
RESERVED			SEQ_START	RESERVED		SEQ_MODE[1:0]	
R-0b			R/W-0b	R-0b		R/W-0b	

Table 21. SEQUENCE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0.
4	SEQ_START	R/W	0b	Control for start of channel sequence when using auto sequence mode (SEQ_MODE = 01b). 0b = Stop channel sequencing. 1b = Start channel sequencing in ascending order for channels enabled in AUTO_SEQ_CH_SEL register.
3-2	RESERVED	R	0b	Reserved. Reads return 0.
1-0	SEQ_MODE[1:0]	R/W	0b	Selects the mode of scanning of analog input channels. 0b = Manual sequence mode; channel selected by MANUAL_CHID field. 1b = Auto sequence mode; channel selected by AUTO_SEQ_CHSEL. 10b = On-the-fly sequence mode. 11b = Reserved.

7.5.12 CHANNEL_SEL Register (Address = 0x11) [reset = 0x0]

CHANNEL_SEL is shown in Figure 29 and described in Table 22.

Return to the Summary Table.

Figure 29. CHANNEL_SEL Register

7	6	5	4	3	2	1	0
RESERVED				MANUAL_CHID[3:0]			
R-0b				R/W-0b			

Table 22. CHANNEL_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0b	Reserved. Reads return 0.
3-0	MANUAL_CHID[3:0]	R/W	0b	In manual mode (SEQ_MODE = 00b), this field contains the 4-bit channel ID of the analog input channel for next ADC conversion. For valid ADC data, the selected channel must not be configured as GPIO in PIN_CFG register. 1xxx = Reserved. 0b = AIN0 1b = AIN1 10b = AIN2 11b = AIN3 100b = AIN4 101b = AIN5 110b = AIN6 111b = AIN7 1000b = Reserved.

7.5.13 AUTO_SEQ_CH_SEL Register (Address = 0x12) [reset = 0x0]

AUTO_SEQ_CH_SEL is shown in Figure 30 and described in Table 23.

Return to the Summary Table.

Figure 30. AUTO_SEQ_CH_SEL Register

7	6	5	4	3	2	1	0
AUTO_SEQ_CH_SEL[7:0]							
R/W-0b							

Table 23. AUTO_SEQ_CH_SEL Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	AUTO_SEQ_CH_SEL[7:0]	R/W	0b	Select analog input channels AIN[7:0] in for auto sequencing mode. 0b = Analog input channel is not enabled in scanning sequence. 1b = Analog input channel is enabled in scanning sequence.

7.5.14 DIAGNOSTICS_KEY Register (Address = 0xBF) [reset = 0x0]

DIAGNOSTICS_KEY is shown in Figure 31 and described in Table 24.

Return to the Summary Table.

Figure 31. DIAGNOSTICS_KEY Register

7	6	5	4	3	2	1	0
DIAG_KEY[7:0]							
R/W-0b							

Table 24. DIAGNOSTICS_KEY Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_KEY[7:0]	R/W	0b	Enable write access to diagnostics registers in address locations 0xC0, 0xC1, and 0xC2. Write 0x96 to this register to enable write access to diagnostics registers.

7.5.15 DIAGNOSTICS_EN Register (Address = 0xC0) [reset = 0x0]

DIAGNOSTICS_EN is shown in Figure 32 and described in Table 25.

Return to the Summary Table.

Figure 32. DIAGNOSTICS_EN Register

7	6	5	4	3	2	1	0
RESERVED			VTEST_EN	RESERVED			BITWALK_EN
R-0b			R/W-0b	R-0b			R/W-0b

Table 25. DIAGNOSTICS_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0b	Reserved. Reads return 0.
4	VTEST_EN	R/W	0b	Enable measurement of internal 1.8 V (typical) test voltage using AIN6. When using this mode, AIN6 pin should not be left floating and should not be connected to any external circuit. If BITWALK_EN = 1b, this bit has no effect. 0b = Normal operation. 1b = AIN6 is internally connected to 1.8V (typical) test voltage. AIN6 pin should be floating and should not be connected to any external circuit.
3-1	RESERVED	R	0b	Reserved. Reads return 0.
0	BITWALK_EN	R/W	0b	Enable bit-walk mode of the ADC bit decisions. 0b = Normal operation. 1b = Bit walk mode enabled.

7.5.16 BIT_SAMPLE_LSB Register (Address = 0xC1) [reset = 0x0]

BIT_SAMPLE_LSB is shown in Figure 33 and described in Table 26.

Return to the Summary Table.

Figure 33. BIT_SAMPLE_LSB Register

7	6	5	4	3	2	1	0
BIT_SAMPLE_LSB[7:0]							
R/W-0b							

Table 26. BIT_SAMPLE_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BIT_SAMPLE_LSB[7:0]	R/W	0b	Define the [7:0] bit positions during sampling phase of the ADC. This field has no effet when DIAG_EN = 0.

7.5.17 BIT_SAMPLE_MSB Register (Address = 0xC2) [reset = 0x0]

BIT_SAMPLE_MSB is shown in Figure 34 and described in Table 27.

Return to the Summary Table.

Figure 34. BIT_SAMPLE_MSB Register

7	6	5	4	3	2	1	0
BIT_SAMPLE_MSB[7:0]							
R/W-0b							

Table 27. BIT_SAMPLE_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BIT_SAMPLE_MSB[7:0]	R/W	0b	Define the [15:8] bit positions during sampling phase of the ADC. This field has no effet when DIAG_EN = 0.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The primary circuit required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) is the input driver circuits. This section details some general principles for designing the input driver circuit for the ADS7066.

8.2 Typical Application

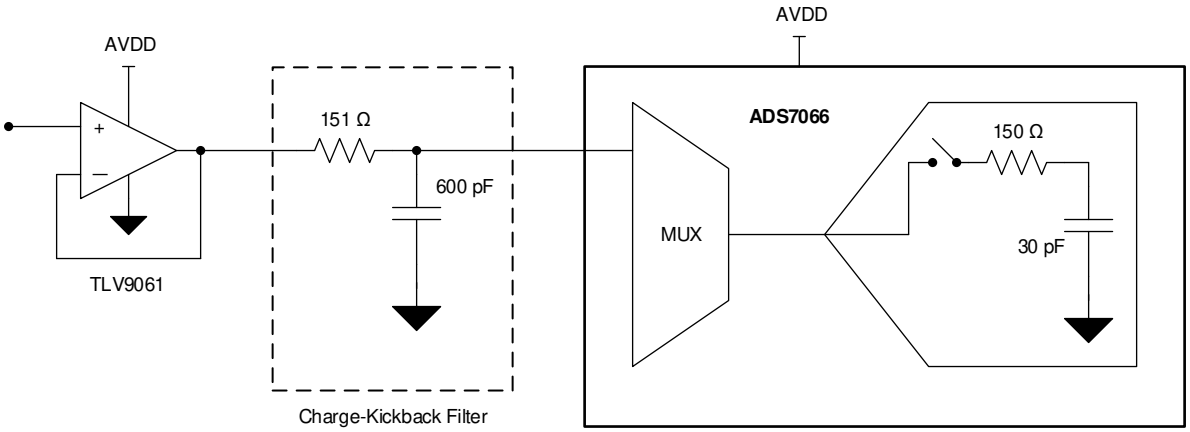


图 35. DAQ Circuit: Single-Supply DAQ

8.2.1 Design Requirements

The goal of this application is to design a single-supply digital acquisition (DAQ) circuit based on the ADS7066 with SNR greater than 80 dB and THD less than –80 dB for input frequencies of 2 kHz at full throughput.

8.2.2 Detailed Design Procedure

The optimal input driver circuit for a high-precision SAR ADC consists of a driving amplifier and a charge-kickback filter (RC filter). The amplifier driving the ADC must have low output impedance and be able to charge the internal sampling capacitor to a 16-bit settling level within the minimum acquisition time. The charge-kickback filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC and helps reduce the wide-band noise contributed by the front-end circuit.

ADVANCE INFORMATION

Typical Application (接下页)

8.2.2.1 Charge-Kickback Filter and ADC Amplifier

As illustrated in 图 35, a filter capacitor (C_{FLT}) is connected from each input pin of the ADC to ground. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. This capacitor must be a COG- or NPO-type. One method for determining the required amplifier bandwidth and the values of the RC charge-kickback filter is provided in this section. This optimization and more details on the math behind the component selection are covered in ADC Precision Labs.

The minimum bandwidth of the amplifier for driving the ADC can be computed using the settling accuracy (0.5 LSB) and settling time (acquisition time) information. 公式 4, 公式 5, 公式 6, and 公式 7 compute the unity-gain bandwidth (UGBW) of the amplifier.

$$LSB = \frac{V_{REF}}{2^N} = \frac{2.5\ V}{2^{16}} = 38.2\ \mu V \tag{4}$$

$$\tau_c = \frac{-t_{ACQ}}{\ln\left(\frac{0.5 \cdot LSB}{100\ mV}\right)} = \frac{-800\ ns}{\ln\left(\frac{0.5 \cdot (38.2\ \mu V)}{100\ mV}\right)} = 93.4\ ns \tag{5}$$

$$\tau_{oa} = \frac{\tau_c}{\sqrt{17}} = \frac{93.4\ ns}{\sqrt{17}} = 22.7\ ns \tag{6}$$

$$UGBW = \frac{1}{2 \cdot \pi \cdot \tau_{oa}} = \frac{1}{2 \cdot \pi \cdot (22.7\ ns)} = 7\ MHz \tag{7}$$

Based on the result of 公式 7, select an amplifier that has more than 7-MHz UGBW. For this example, TLV9061 is used. The OPA320 can be used for improved precision.

The value of C_{filt} is computed in 公式 8 by taking 20 times the internal sample-and-hold capacitance. The factor of 20 is a rule of thumb that is intended to minimize the droop in voltage on the charge-bucket capacitor, C_{filt}, after the start of the acquisition period. The filter resistor, R_{filt}, is computed in 公式 9 using the op-amp time constant and C_{filt}. 公式 10 and 公式 11 compute the minimum and maximum R_{filt} values, respectively.

$$C_{filt} = 20 \cdot C_{SH} = 20 \cdot (30pF) = 600\ pF \tag{8}$$

$$R_{filt} = \frac{4 \cdot \tau_{oa}}{C_{filt}} = \frac{4 \cdot (22.7\ ns)}{600\ pF} = 151\ \Omega \tag{9}$$

$$R_{filtMin} = 0.25 \cdot R_{filt} = 0.25 \cdot (33\Omega) = 37.7\ \Omega \tag{10}$$

$$R_{filtMax} = 2 \cdot R_{filt} = 2 \cdot (33\Omega) = 302.1\ \Omega \tag{11}$$

ADVANCE INFORMATION

9 Power Supply Recommendations

9.1 AVDD and DVDD Supply Recommendations

The ADS7066 has two separate power supplies: AVDD and DVDD. The device operates on AVDD; DVDD is used for the interface circuits. AVDD and DVDD can be independently set to any value within the permissible ranges. 图 36, decouple the AVDD and DVDD pins individually with 1-µF ceramic decoupling capacitors.

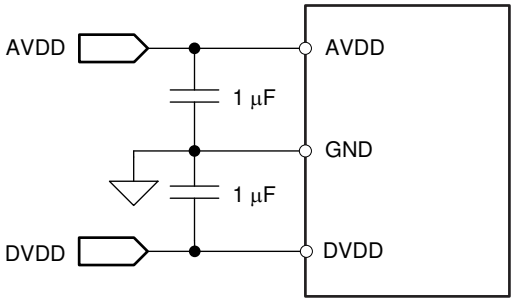


图 36. Power-Supply Decoupling

10 Layout

10.1 Layout Guidelines

图 37 shows a board layout example for the ADS7066. Avoid crossing digital lines with the analog signal path and keep the analog input signals and the reference input signals away from noise sources.

Use 1-µF ceramic bypass capacitors in close proximity to the analog (AVDD) and digital (DVDD) power-supply pins. Avoid placing vias between the AVDD and DVDD pins and the bypass capacitors. Connect all ground pins to the ground plane using short, low-impedance paths.

Place the reference decoupling capacitor (C_{REF}) close to the device REF and GND pins. Avoid placing vias between the REF pin and the bypass capacitors.

The charge-kickback RC filters are placed close to the device. Among ceramic surface-mount capacitors, COG- or NPO-type ceramic capacitors provide the best capacitance precision. The type of dielectric used in COG- or NPO-type ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

10.2 Layout Example

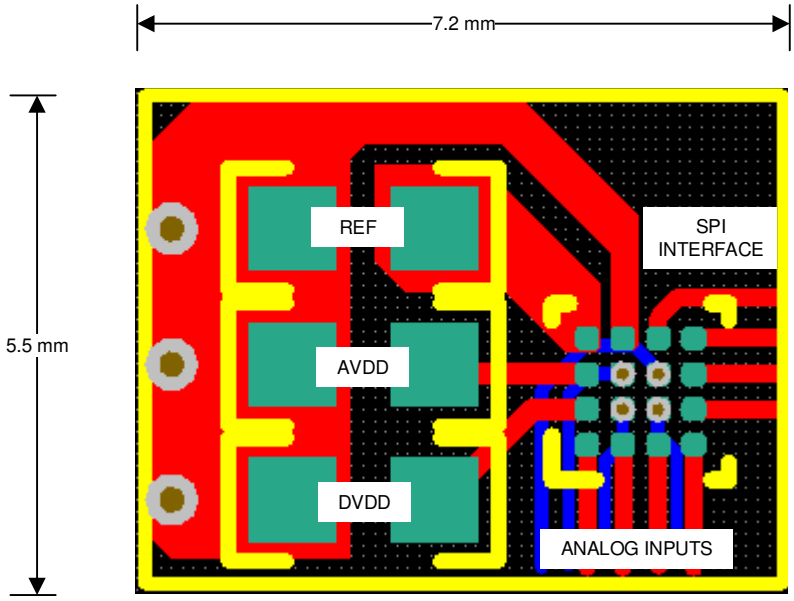


图 37. Example Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

德州仪器 (TI)，ADC 高精度实验室

11.2 文档支持

11.2.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*《具有集成 ADC 驱动器缓冲器的 REF60xx 高精度电压基准》* 数据表
- 德州仪器 (TI)，*《适用于成本敏感型系统的 TLV906xS 10MHz RRIO CMOS 运算放大器》* 数据表
- 德州仪器 (TI)，*《具有关断功能的 OPAx320x 高精度 20MHz、0.9pA、低噪声 RRIO CMOS 运算放大器》* 数据表

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7066IYBHR	ACTIVE	DSBGA	YBH	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ADS7066	Samples
ADS7066IYBHT	ACTIVE	DSBGA	YBH	16	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ADS7066	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

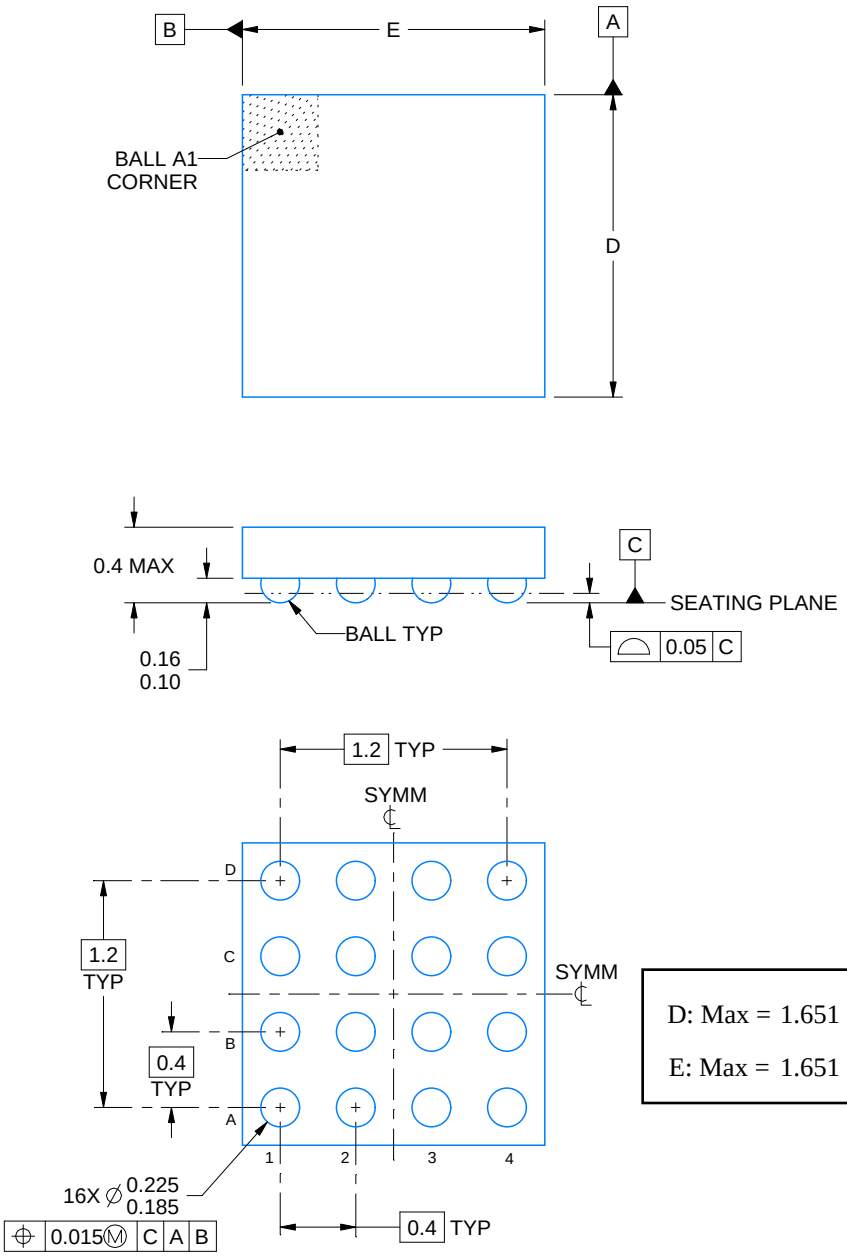
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



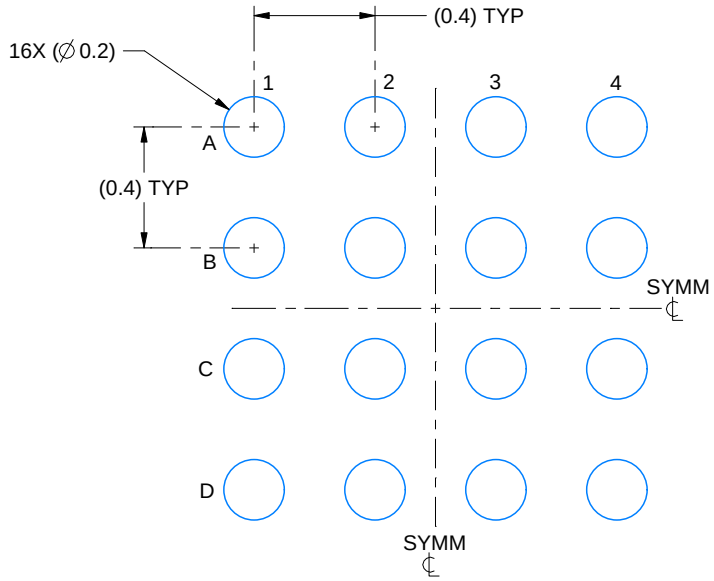
D: Max = 1.651 mm, Min = 1.59 mm

E: Max = 1.651 mm, Min = 1.59 mm

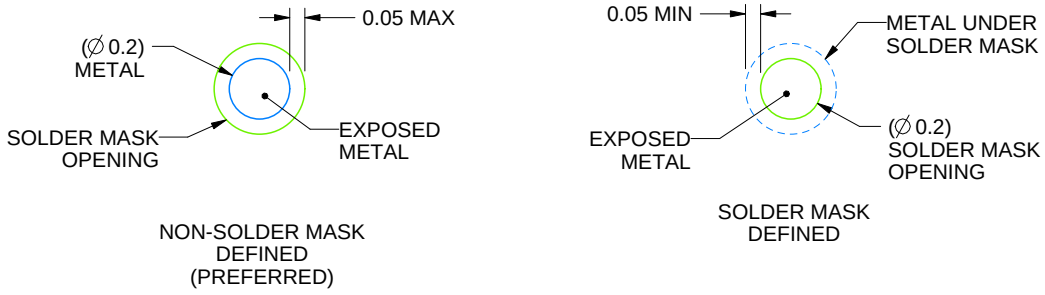
4225022/A 06/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X

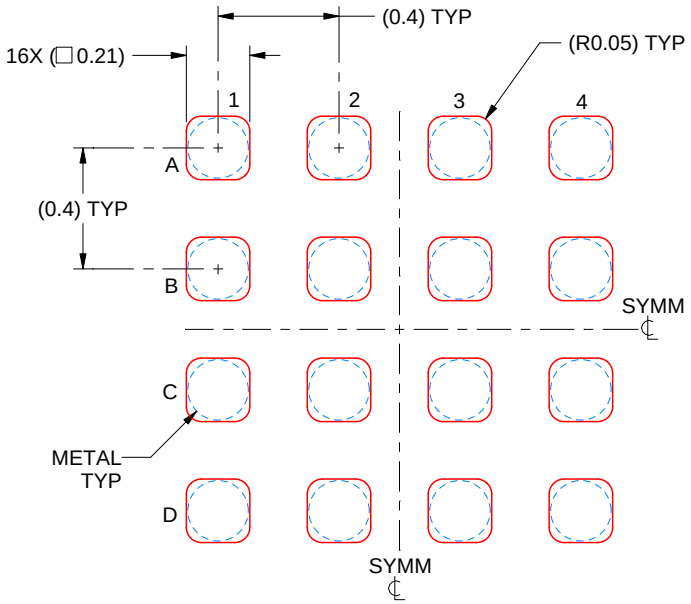


SOLDER MASK DETAILS
NOT TO SCALE

4225022/A 06/2019

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 40X

4225022/A 06/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122