TPS7B67xx-Q1 450mA 高压超低 I_Q 低压降稳压器

1 特性

- 符合汽车类 标准
- 符合 AEC-Q100 标准的下列结果
  - 器件温度等级 1：环境运行温度范围为 -40°C 至 125°C
  - 人体放电模型 (HBM) 静电放电 (ESD) 分类等级 H2
  - 器件 CDM ESD 分类等级 C3B
- 4V 至 40V 宽 V_{IN} 输入电压范围，瞬态电压高达 45V
- 最大输出电流，450mA
- 低静态电流 (I_Q)
  - < 4μA，EN = 低电平（关断模式）
  - 轻负载时典型值为 15μA
- 低 ESR（0.001 至 20Ω）陶瓷输出稳定电容器（$V_O \geq 2.5V$ 时为 10μF 至 500μF，V_O = 1.5V 至 2.5V 时为 22μF 至 500μF）
- 400mA 时的最大压降为 450mV
- 1.5V 至 18V 可调节输出电压
- 低输入电压跟踪至欠压闭锁 (UVLO)
- 集成型加电复位
  - 可编程复位脉冲延迟
  - 漏极开路复位输出
- 集成故障保护
  - 热关断
  - 短路保护功能
- 20 引脚散热薄型小外形尺寸 (HTSSOP) 封装

2 应用

- 汽车
- 信息娱乐系统调谐器电源
- 车身控制模块
- 常开电池 应用
  - 网关 应用
  - 遥控免钥匙进入系统
  - 发动机防盗系统

3 说明

TPS7B6701-Q1、TPS7B6733-Q1 和 TPS7B6750-Q1 器件 (TPS7B67xx-Q1) 为低压降线性稳压器，设计用于输入电压 V_{IN} 高达 40V 的操作。这些器件在轻负载时的静态电流仅为 15μA，显著延长了汽车电池的续航时间，可驱动高达 450mA 的负载。

TPS7B67xx-Q1 系列器件 集成有 短路和过流保护。在加电时执行复位延迟和电源正常信号，以表示输出电压稳定并且在稳压范围内。一个外部电容器设定此延迟。此使能功能使用一个 MCU 的输入输出 (I/O) 端口来激活此器件，以及使器件无效。

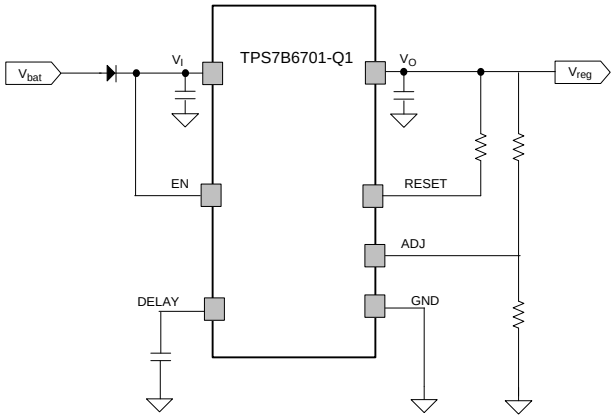
此器件的运行温度范围介于 -40°C 至 125°C 之间。

器件信息(1)

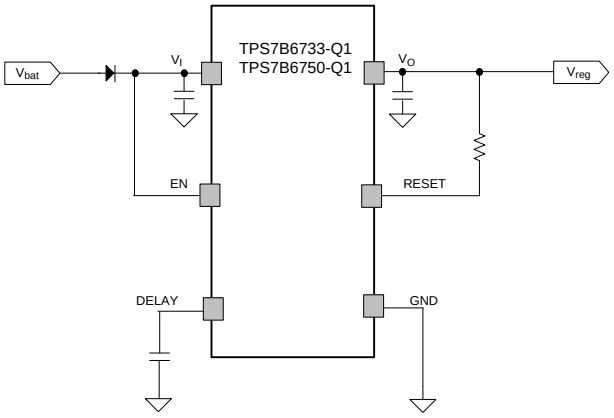
器件型号	封装	封装尺寸（标称值）
TPS7B6701-Q1	HTSSOP (20)	6.50mm x 4.40mm
TPS7B6733-Q1		
TPS7B6750-Q1		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

可调输出选项



固定输出选项



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (December 2014) to Revision D **Page**

- Added *Dropout Recovery* section explaining LDO behavior when exiting dropout ... 17

Changes from Revision B (March 2014) to Revision C **Page**

- 已删除 数据表中的 TPS7B6750A-Q1 和 TPS7B6750B-Q1 器件以及 DDPAK 封装 ... 1
- Changed the word *terminal* to *pin* throughout the data sheet ... 4
- Changed the *Handling Ratings* table to *ESD Ratings* and moved the storage temperature into the *Absolute Maximum Ratings* table. Added corner pin values for CDM ratings. ... 5

Changes from Revision A (November 2013) to Revision B **Page**

- 更新了首页内容，包括以下新增内容：*器件信息*表，器件系列名称更新为文档标题，增加了导航按钮 ... 1
- 已更改 EN = 低电平时的 I_Q 值从 *< 2* 改为 *< 4*（*特性* 列表 ... 1
- 已添加 *内容表* 并且已将 *修订历史记录* 移至第二页 ... 1
- Replaced the *ORDERING INFORMATION* table with the *Device Comparison* Table and deleted the Device and Package columns ... 4
- Added Moved all electrical specifications tables and the *Typical Characteristics* section into the *Specifications* section ... 5
- Changed the max value for DELAY from V_I to 45 V in the *Absolute Maximum Ratings* table. Also added new table note for DELAY ... 5
- Changed the max value for ADJ, RESET from V_O to 22 V in the *Absolute Maximum Ratings* table ... 5
- Changed the value of I_O from 1 mA to 450 mA for the Input voltage test conditions in the *Electrical Characteristics* table . 6
- Added the value for V_I in the test conditions of the Regulated output and the Line regulator parameters in the *Electrical Characteristics* table ... 6
- Moved the timing parameters (TIMING FOR RESET) out of the *Electrical Characteristics* table and into the new *Timing Requirements* table ... 7
- Added the *Overview* section title to the first paragraph of the *Detailed Description* section ... 11

- Updated the *Power-On_Reset (RESET)* section by making the following changes: changed the percentage that V_O exceeds for the reset output to change from 90% to 91.6% (also changed this value in the *Reset Delay Timer (DELAY)* section), removed *The on-chip oscillator presets the delay*, and changed the percentage level to assert the output from 90% to 89.6% 12
- Changed the junction temperature value that disables thermal protection from 170°C to 175°C in the *Thermal Protection* section 14
- Added the *Device Functional Modes* section 14
- Added the *Typical Application* section in the new *Applications and Implementation* section 15
- Added the *Power Supply Recommendations* section 17
- Changed the *LAYOUT INFORMATION* section to the Layout section and added the *Layout Example* section 19
- 已添加 *机械封装和可订购信息* 部分。还添加了*器件和文档支持*部分，目前此部分包含商标部分和 *静电放电警告*。这个部分还包括对 TI 术语表的全新引用 22

Changes from Original (October 2013) to Revision A **Page**

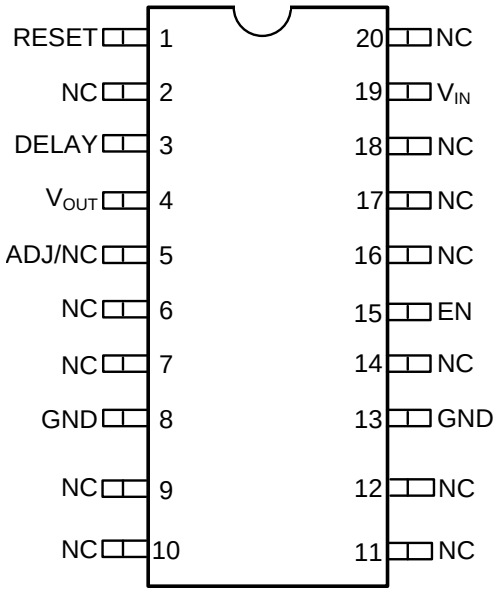
- 已更改 将*特性* 列表的电压监控项目中添加了“独立” 1
- 已添加 车身控制模块到*应用*分类等级 1
- 已更改 *低压跟踪*特性至*使能功能*（*说明部分*） 1
- 已更改 文档状态从 *产品预览* 改为 *生产数据* 1
- 已更改 典型应用电路原理图以显示可调输出和固定输出选项之间的差异 1
- Changed the MIN value for RESET and ADJ in the *RECOMMENDED OPERATING CONDITIONS* table from 0 to 1.5 and removed low voltage parameter for those pins 5
- Added Added board dimensions to the high K profile *THERMAL INFORMATION* table note 5
- Changed test condition for the input voltage to fixed 3.3-V output and added 5-V and two adjustable output conditions 6
- Changed max value for the line regulation parameter from 2 to 10 6
- Changed TYP value for dropout voltage where I_O = 400 mA from 240 to 260 6
- Changed TYP value for dropout voltage where I_O = 200 mA from 160 to 150 6
- Changed Output current-limit typ value to max value for V_{OUT} short to ground 6
- Deleted V_{IN} condition from test condition for PSRR 6
- Added *TYPICAL CHARACTERISTICS* section 8
- Added the *DETAILED DESCRIPTION* section 11
- Added block diagram fro the TPS7B6733-Q1 and TPS7B6750-Q1 11
- Added the *APPLICATION INFORMATION* section 15
- Added the *LAYOUT INFORMATION* section 19

5 Device Comparison

ORDERABLE PART NUMBER	VOLTAGE OPTION (V_{OUT})
TPS7B6701QPWPRQ1	Adjustable 1.5 V to 18 V
TPS7B6733QPWPRQ1	Fixed 3.3 V
TPS7B6750QPWPRQ1	Fixed 5 V

6 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP With PowerPAD™
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	PWP		
ADJ	5	I	Feedback pin. This pin is used with an external resistor divider or the NC pin when in a fixed version.
DELAY	3	O	Reset pulse delay adjustment. Connect this pin through a capacitor to GND.
EN	15	I	Enable pin. When the EN pin becomes lower than threshold, the device enters the stand-by state.
GND	8, 13	G	Ground reference
NC	2, 6, 7, 9, 10, 11, 12, 14, 16, 17, 18, 20	—	Not connected
RESET	1	O	Output ready. This open-drain pin must be connected to V_{OUT} through an external resistor. RESET is pulled down when the output voltage goes below threshold.
V_{IN}	19	P	Input power-supply voltage
V_{OUT}	4	P	Output voltage
PowerPAD™		—	Thermal pad

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Unregulated input range(2)(3)(4)	V_{IN}, EN	–0.3	45	V
Output range	V_{OUT}	–0.3	22	V
	DELAY(2)(3)(5)		45	
	ADJ, RESET		22	
Operating junction temperature (T_J)		–40	150	°C
Storage temperature (T_{stg})		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability
(2) All voltage values are with respect to GND.
(3) Absolute negative voltage on these pins does not go below –0.3 V.
(4) Absolute maximum voltage.
(5) The voltage at the DELAY pin must be lower than the V_{IN} voltage.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)(2)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 10, 11, and 20)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The human body model is a 107-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	Unregulated input range	V_{IN}	4	40	V
	Output range	EN, DELAY	0	40	V
		V_{OUT}, RESET, ADJ	1.5	18	
T_J	Operating junction temperature range		–40	150	°C

7.4 Thermal Information

THERMAL METRIC(1)(2)		TPS7B67xx-Q1 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) The thermal data is based on JEDEC standard high K profile — JESD 51-7. Two signal, two plane, four-layer board with 2-oz copper. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_I = 14 V, 1 mΩ < ESR < 20 Ω, T_J = –40°C to 150°C unless otherwise stated

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (V_{IN})							
V_I	Input voltage	Fixed 3.3-V output, I_O = 0 mA to 450 mA		4		40	V
		Fixed 5-V output, I_O = 0 mA to 450 mA		5.5		40	
		Adjustable output, V_O ≤ 3.5 V, I_O = 0 mA to 450 mA		4		40	
		Adjustable output, V_O ≥ 3.5 V, I_O = 0 mA to 450 mA		V_O + 0.5		40	
I_Q	Quiescent current	V_I = 5.5 V to 40 V (fixed 5 V), 4 V to 40 V (fixed 3.3 V), EN = ON, I_O = 0.2 mA			15	25	µA
		V_I = 4 V to 40 V (adjustable version, V_O = 1.5 V), EN = ON, I_O = 0.2 mA			15	25	
		V_I = 18.5 V to 40 V (adjustable version, V_O = 18 V), EN = ON, I_O = 0.2 mA			25	35	
I_{Sleep}	Input sleep current	NO load current and EN = OFF				4	µA
I_{EN}	EN pin current	EN = 40 V				1	µA
Vbg	Band gap	Reference voltage for ADJ		–2%	1.233	2%	V
V_{INUVLO}	Undervoltage detection	Ramp V_I down until output is turned OFF				2.6	V
$UVLO_{Hys}$	Undervoltage detection hysteresis				1		V
ENABLE INPUT (EN)							
V_{IL}	Logic input low level			0		0.4	V
V_{IH}	Logic input high level			1.7			V
REGULATED OUTPUT (V_{OUT})							
V_O	Regulated output(1)	V_I = V_O + 0.5 V to 40 V and V_I ≥ 4 V, I_O = 0 mA to 450 mA		–2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation	V_I = V_O + 1 V to 40 V and V_I ≥ 4 V, I_O = 100 mA, ΔV_O				10	mV
$\Delta V_{O(\Delta IL)}$	Load regulation	I_O = 1 mA to 450 mA, ΔV_O				10	mV
$V_{dropout}$	Dropout voltage	V_I – V_O, I_O = 400 mA			240	450	mV
		V_I – V_O, I_O = 200 mA			160	300	
I_O	Output current	V_O in regulation		0		450	mA
$I_{Ireg-CL}$	Output current-limit	V_O short to ground		140		360	mA
		V_O = V_O typical × 0.9		470		850	
PSRR	Power-supply ripple rejection(2)	I_L = 100 mA, C_O = 22 µF	Freq = 100 Hz		60		dB
			Freq = 100 kHz		40		
RESET							
V_{OL}	Reset pulled low	I_{OL} = 0.5 mA				0.4	V
I_{OH}	Reset pulled V_{OUT} through 10-kΩ resistor	Leakage current				1	µA
$V_{TH-(POR)}$	Power-on-reset threshold	V_O power-up set tolerance		89.6	91.6	93.6	% of V_{OUT}
V_{hys}	Hysteresis	V_O power-down set tolerance			2		% of V_{OUT}
RESET DELAY							
I_{Chg}	Delay capacitor charging current	R_{delay} = 0 V		6	9.5	14	µA
V_{th}	Threshold to release RESET high				1		V
OPERATING TEMPERATURE RANGE							
T_J	Junction temperature			–40		150	°C
T_{sd}	Junction shutdown temperature				175		°C
T_{hys}	Hysteresis of thermal shutdown				24		°C

(1) External resistor divider variation is not considered.
(2) Design information — not tested, ensured by characterization.

7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
TIMING FOR RESET						
t_{POR}	Power-on reset delay	Where C = delay-capacitor value capacitance, C = 100 nF(1)		10.5		ms
$t_{POR-fixed}$	Power-on reset delay	No capacitor on pin	100	325	550	µs
$t_{Deglitch}$	Reset deglitch time		55	180	420	µs

(1) This information only will NOT be tested in production. The equation is based on:
$(C \times 1) / (9.5 \times 10^{-6}) = t_{Delay}$ (delay time)
Where
- C = delay capacitor value capacitance
- C range = 100 pf to 500 nF

7.7 Typical Characteristics

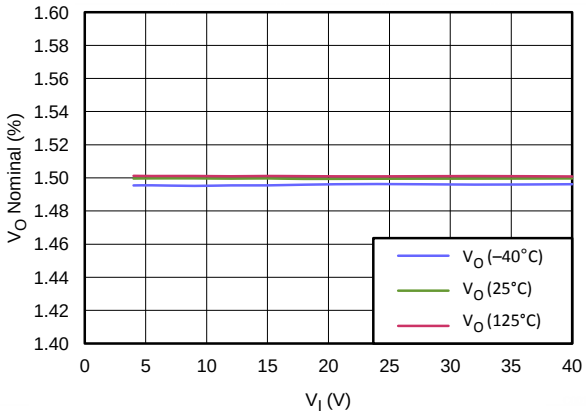


Figure 1. Line Regulation
(V_O = 1.5 V, I_L = 100 mA)

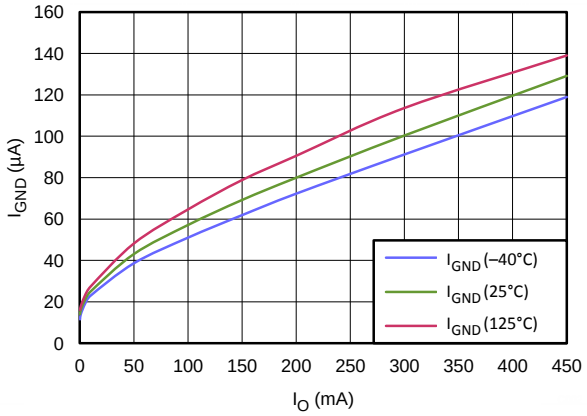


Figure 2. Ground Current vs Output Current
(V_I = 14 V, V_O = 1.5 V)

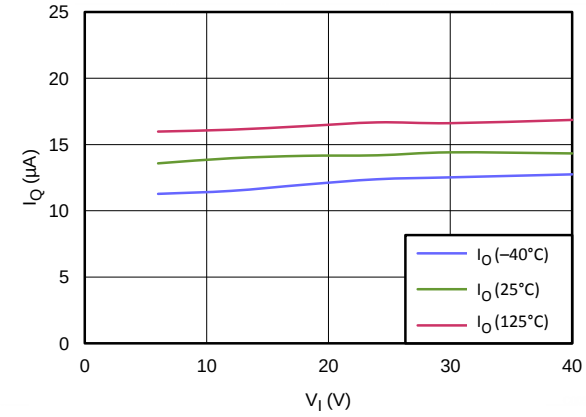


Figure 3. Quiescent Current vs Input Voltage
(V_O = 1.5 V)

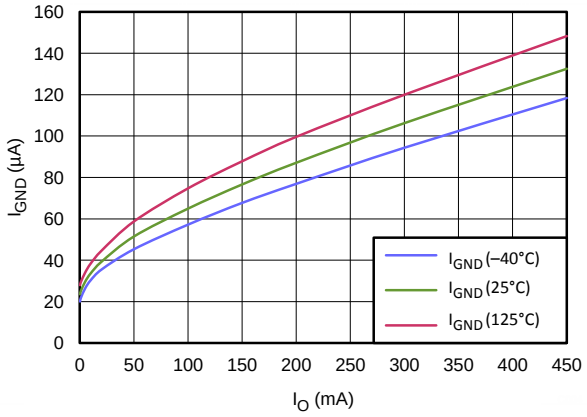


Figure 4. Ground Current vs Output Current
(V_I = 24 V, V_O = 18 V)

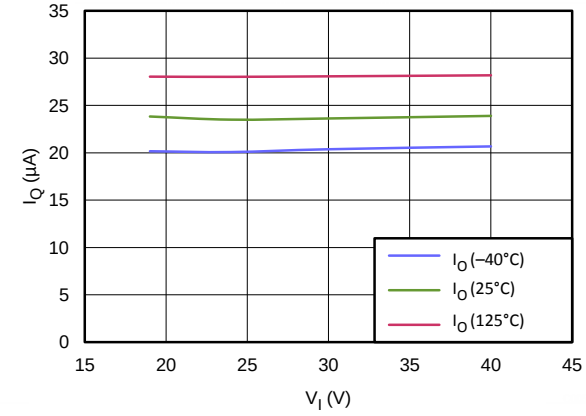


Figure 5. Quiescent Current vs Input Voltage
(V_O = 18 V)

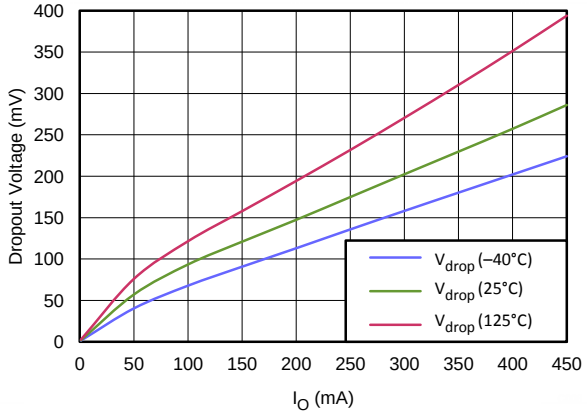


Figure 6. Dropout Voltage vs Output Current

Typical Characteristics (continued)

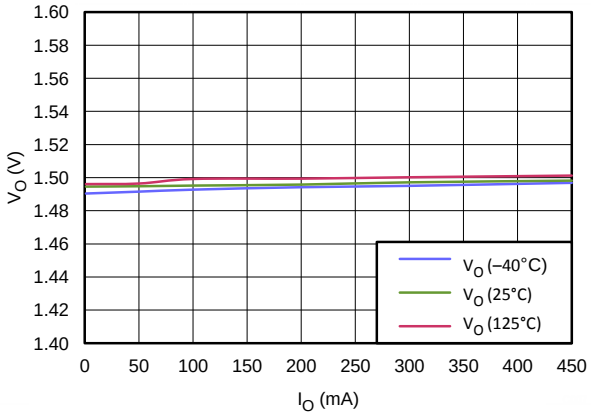


Figure 7. Load Regulation (V_I = 14 V, V_O = 1.5 V)

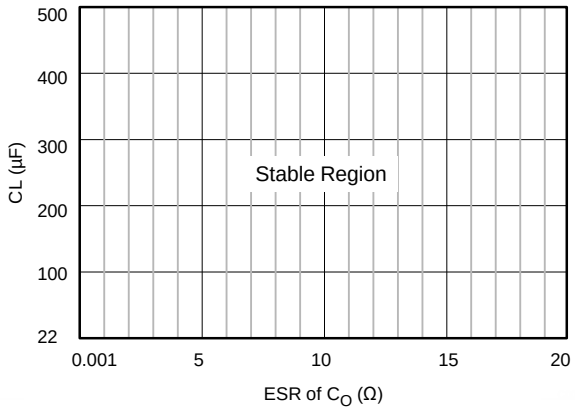


Figure 8. ESR Stability vs Load Capacitance (V_O ≤ 2.5 V)

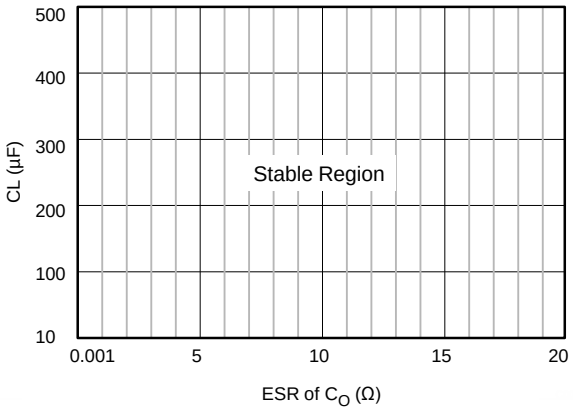


Figure 9. ESR Stability vs Load Capacitance (V_O ≥ 2.5 V)

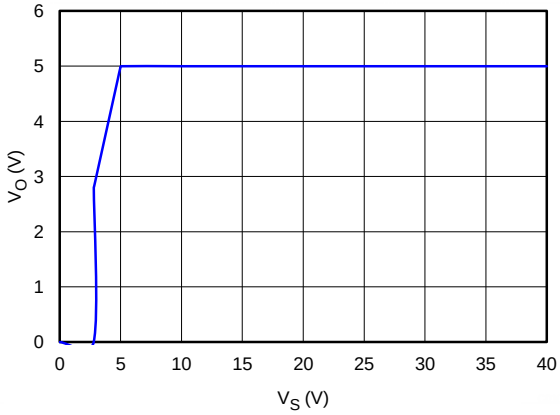


Figure 10. Output Voltage vs Supply Voltage (Fixed 5-V Version, I_L = 0)

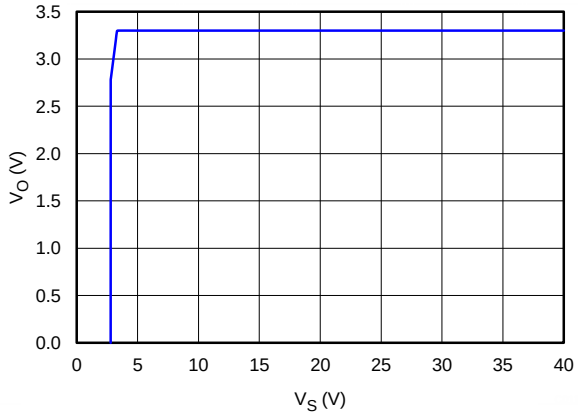


Figure 11. Output Voltage vs Supply Voltage (Fixed 3.3-V Version, I_L = 0)

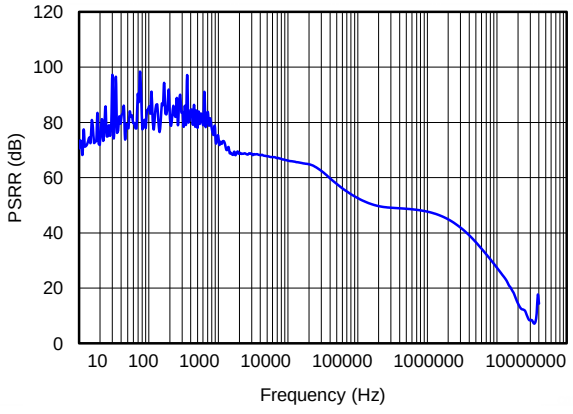


Figure 12. Power-Supply Rejection Ratio vs Frequency (V_I = 14 V, C_O = 47 µF, I_L = 25 mA)

Typical Characteristics (continued)

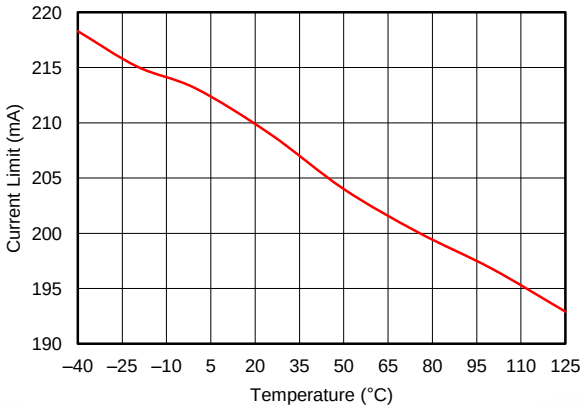


Figure 13. Short to GND Current-Limit vs Temperature

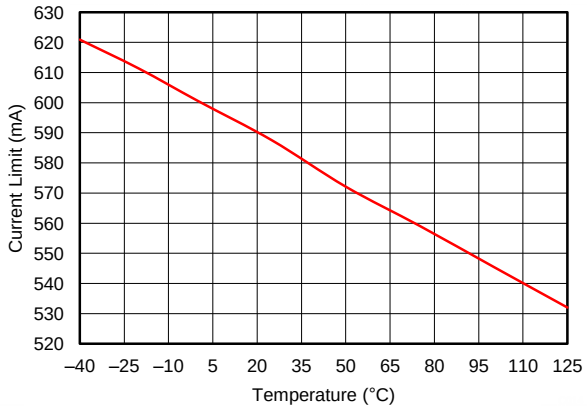


Figure 14. Current-Limit vs Temperature

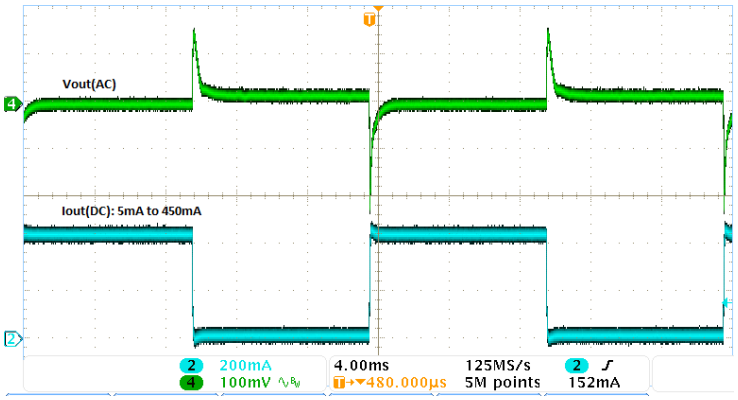


Figure 15. Load Transient
10-µF Ceramic Output Capacitor

8 Detailed Description

8.1 Overview

The TPS7B67xx-Q1 family of devices is an low-dropout linear regulator combined with an enable and reset function. The power-on-reset initializes when the output voltage, V_O, exceeds 91.6% of the target value. The power-on reset delay is a function of the value set by an external capacitor on the DELAY pin before releasing the RST pin high.

8.2 Functional Block Diagrams

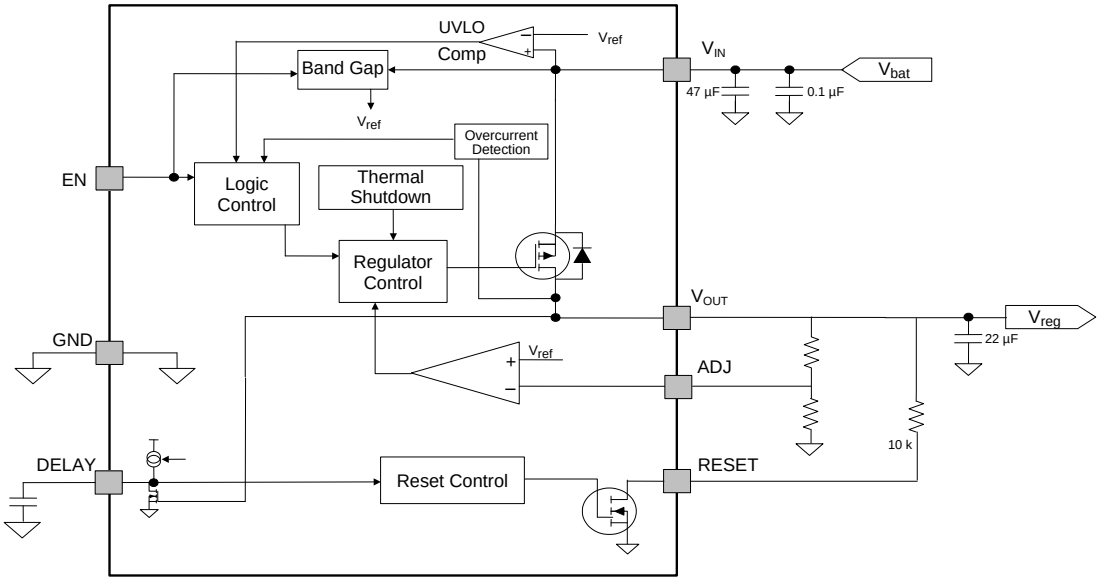


Figure 16. TPS7B6701-Q1 Functional Block Diagram

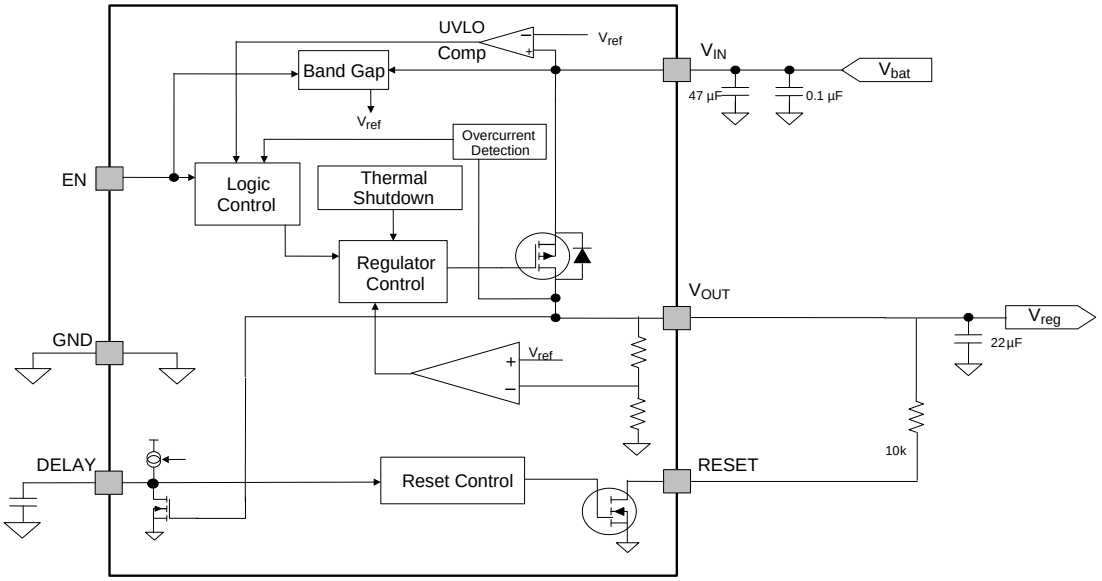


Figure 17. TPS7B6733-Q1 and TPS7B6750-Q1 Functional Block Diagram

8.3 Feature Description

8.3.1 Enable (EN)

The enable pin is a high-voltage-tolerant pin. A high input on EN actives the device and turns on the regulator. For self-bias applications, connect this input to the V_{IN} pin.

8.3.2 Regulated Output (V_{OUT})

The V_{OUT} pin is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control the initial current through the pass element.

In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

8.3.3 Power-On-Reset (RESET)

The power-on-reset is an output with an external pullup resistor to the regulated supply. The reset output remains low until the regulated V_O exceeds approximately 91.6% of the set value and the power-on-reset delay has expired. The regulated output falling below the 89.6% level asserts this output low after a short de-glitch time of approximately 180 µs (typical).

8.3.4 Reset Delay Timer (DELAY)

An external capacitor on this pin sets the timer delay before the reset pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. If this pin is open, the default delay time is 325 µs (typical).

The reset pulse delay time t_d, is defined with the charge time of an external capacitor DELAY (see Equation 1).

$$t_d = \frac{C_{DELAY} \times 1\,V}{9.5\,\mu A} \quad (1)$$

The power-on-reset initializes when V_O exceeds 91.6% of the programmed value. The power-on-reset delay is a function of the value set by an external capacitor on the DELAY pin before the RESET pin is released high.

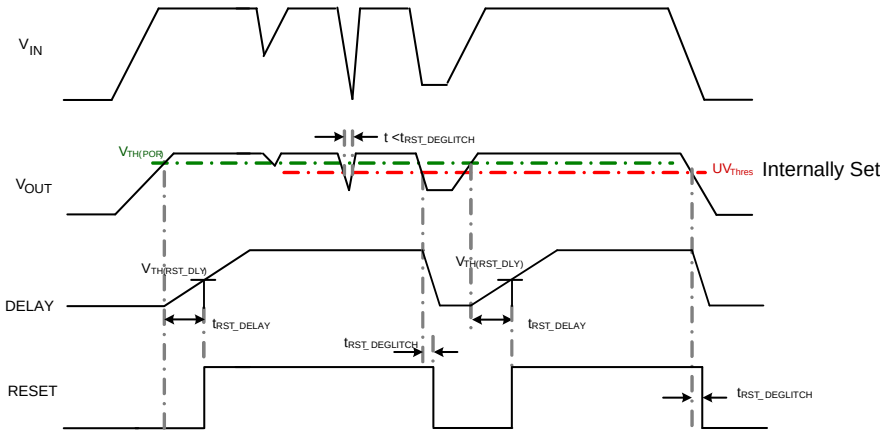


Figure 18. Conditions to Activate RESET

Feature Description (continued)

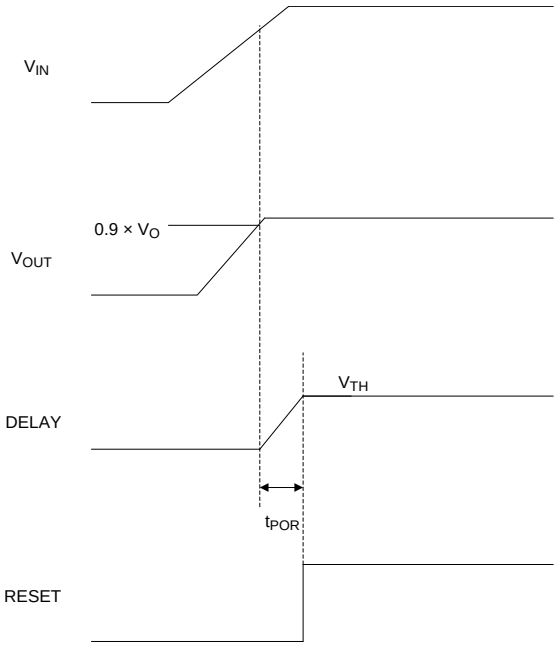


Figure 19. External Programmable-Reset Delay

8.3.5 Adjustable Output Voltage (ADJ for TPS7B6701)

An output voltage between 1.5 V and 18 V can be selected by using the external resistor dividers. Use Equation 2 to calculate the output voltage, where V_{ADJ} = 1.233 V. In order to avoid a large leakage current and to prevent a divider error, the value of (R1 + R2) must between 10 k and 100 kΩ.

$$V_O = V_{ADJ} \times \left(1 + \frac{R2}{R1}\right) \quad (2)$$

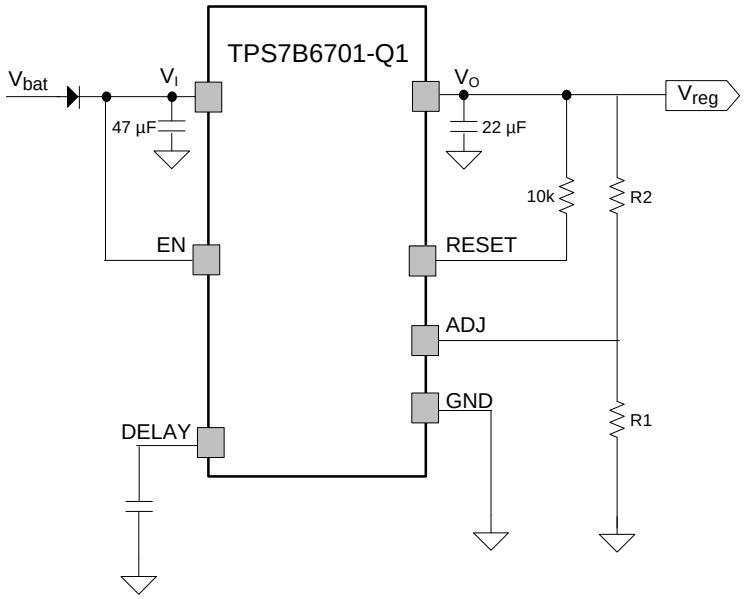


Figure 20. External Feedback Resistor Divider

Feature Description (continued)

8.3.6 Undervoltage Shutdown

The TPS7B67xx-Q1 family of devices has an internally-fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on V_{IN} drops below V_{INUVLO}. This activation ensures the regulator is not latched into an unknown state during low-input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up similar to a typical power-up sequence when the input voltage is above the required levels.

8.3.7 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous standard operation, the junction temperature must not exceed the TSD trip-point. If the junction temperature exceeds the TSD trip-point, the output turns off. When the junction temperature falls below the TSD trip-point minus TSD hysteresis, the output turns on again.

8.3.8 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C which allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The internal protection circuitry of the TPS7B67xx-Q1 device has been designed to protect against overload conditions. The circuitry was not intended to replace proper heat-sinking. Continuously running the TPS7B67xx-Q1 device into thermal shutdown degrades device reliability.

8.4 Device Functional Modes

8.4.1 Operation With V_{IN} < 4 V

The devices operate with input voltages above 4 V. The maximum UVLO voltage is 2.6 V and operates at input voltage above 4 V. The devices can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO voltage, the devices do not operate.

8.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.7 V (maximum), with the EN pin is held above that voltage and the input voltage is above the 4 V, the device becomes active. The enable falling edge is 0.4 V (minimum), with the EN pin is held below that voltage the device is disabled, the IC quiescent current is reduced in this state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 21 and Figure 22 show typical application circuits for the TPS7B6701-Q1 device and the TPS7B6733-Q1 and TPS7B6750-Q1 device respectively. Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps in order to prevent a reset from occurring. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

9.2 Typical Application

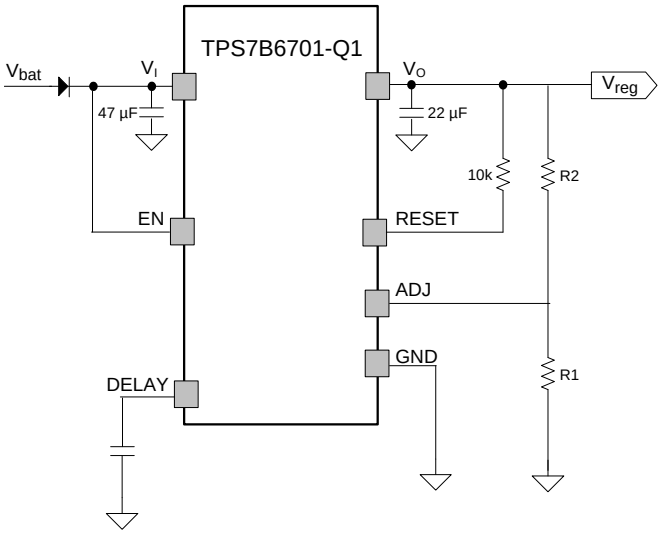


Figure 21. Typical Application Schematic for TPS7B6701-Q1

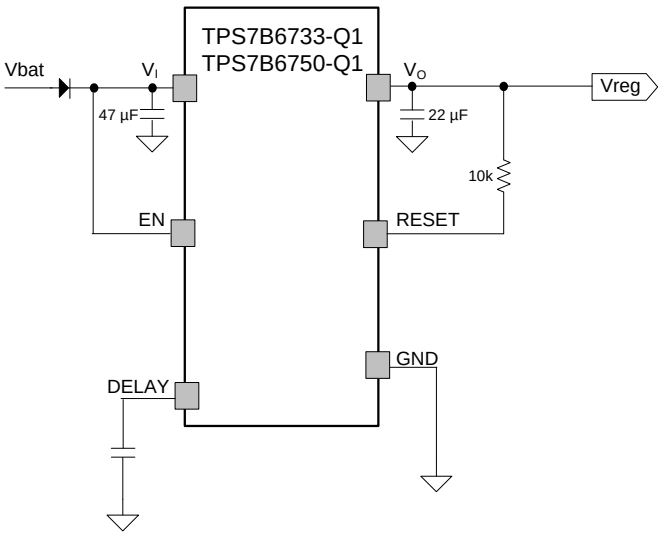


Figure 22. Typical Application Schematic for TPS7B6733-Q1 and TPS7B6750-Q1

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	1.5 V to 18 V
Output current rating	450 mA
Output capacitor range	10 µF to 500 µF
Output capacitor ESR range	1 mΩ to 20 Ω
DELAY capacitor range	100 pF to 500 nF

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Output capacitor
- Power-up reset delay time

9.2.2.1 Power Dissipation and Thermal Considerations

Device power dissipation is calculated with Equation 3.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I \quad (3)$$

where

- P_D = continuous power dissipation
- I_O = output current
- V_I = input voltage
- V_O = output voltage

As $I_Q \ll I_O$, the term $I_Q \times V_I$ in Equation 3 can be ignored.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) with Equation 4.

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (4)$$

where

- $R_{\theta JA}$ = junction-to-ambient air thermal impedance

A rise in junction temperature because of power dissipation can be calculated with Equation 5.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (5)$$

For a given maximum junction temperature (T_{JM}), the maximum ambient air temperature (T_{AM}) at which the device can operate is calculated with Equation 6.

$$T_{AM} = T_{JM} - (R_{\theta JA} \times P_D) \quad (6)$$

9.2.3 Application Curves

Load = 200 mA $C_{IN} = C_{OUT} = 47\ \mu F$

Figure 23. TPS7B6750-Q1 Power-Up Waveform

Load = 200 mA $C_{IN} = C_{OUT} = 47\ \mu F$

Figure 24. TPS7B6750-Q1 Power-Down Waveform

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B67xx-Q1 device, an electrolytic capacitor with a value of 47 µF and a ceramic bypass capacitor are recommended to add at the input.

10.1 Dropout Recovery

All LDOs have some overshoot when recovering from dropout, how much is primarily dependent on the transient response (bandwidth) of the error amplifier. Because of design and system level tradeoffs made when creating the TPS7B67xx-Q1, the error amplifier has a slower transient response than many other LDOs, which is evident in the load transient plot in Figure 15. This slower transient response can cause the output to overshoot significantly when the device is recovering from a dropout condition. A well-regulated power supply eliminates this behavior by keeping the TPS7B67xx-Q1 out of dropout. If the device is placed into dropout and the rising V_{IN} ramp rate is less than 200 mV/ms, the overshoot is limited to 0.5 V; however, faster ramp rates result in more overshoot and may require a zener diode on the output to limit the V_{OUT} overshoot.

10.1.1 LDO Dropout Recovery Explained

When an LDO is in dropout the output voltage is below the accuracy specification. This condition causes the error amplifier to force the gate of the pass transistor such that the pass transistor is fully on and provides the least resistance possible, meaning V_{OUT} tracks V_{IN} as closely as possible. When the input voltage recovers, the error amplifier must force the gate of the pass device to the opposite rail making the pass transistor more resistive. The change in gate voltage takes a finite amount of time, as dictated by the bandwidth of the error amplifier. If V_{IN} rises quickly during that time then V_{OUT} tracks V_{IN} and overshoots above the nominal output voltage. Figure 25 depicts a graphical representation of an LDO recovering from dropout.

The amplitude of the overshoot is determined by both the speed of the V_{IN} ramp and the transient response of the LDO, which determines how long is required for the error amplifier to respond to changes on V_{OUT}. The amount of time required for the overshoot to be discharged is determined by the load current that must drain the excess charge that has accumulated on C_{OUT}.

Dropout Recovery (continued)

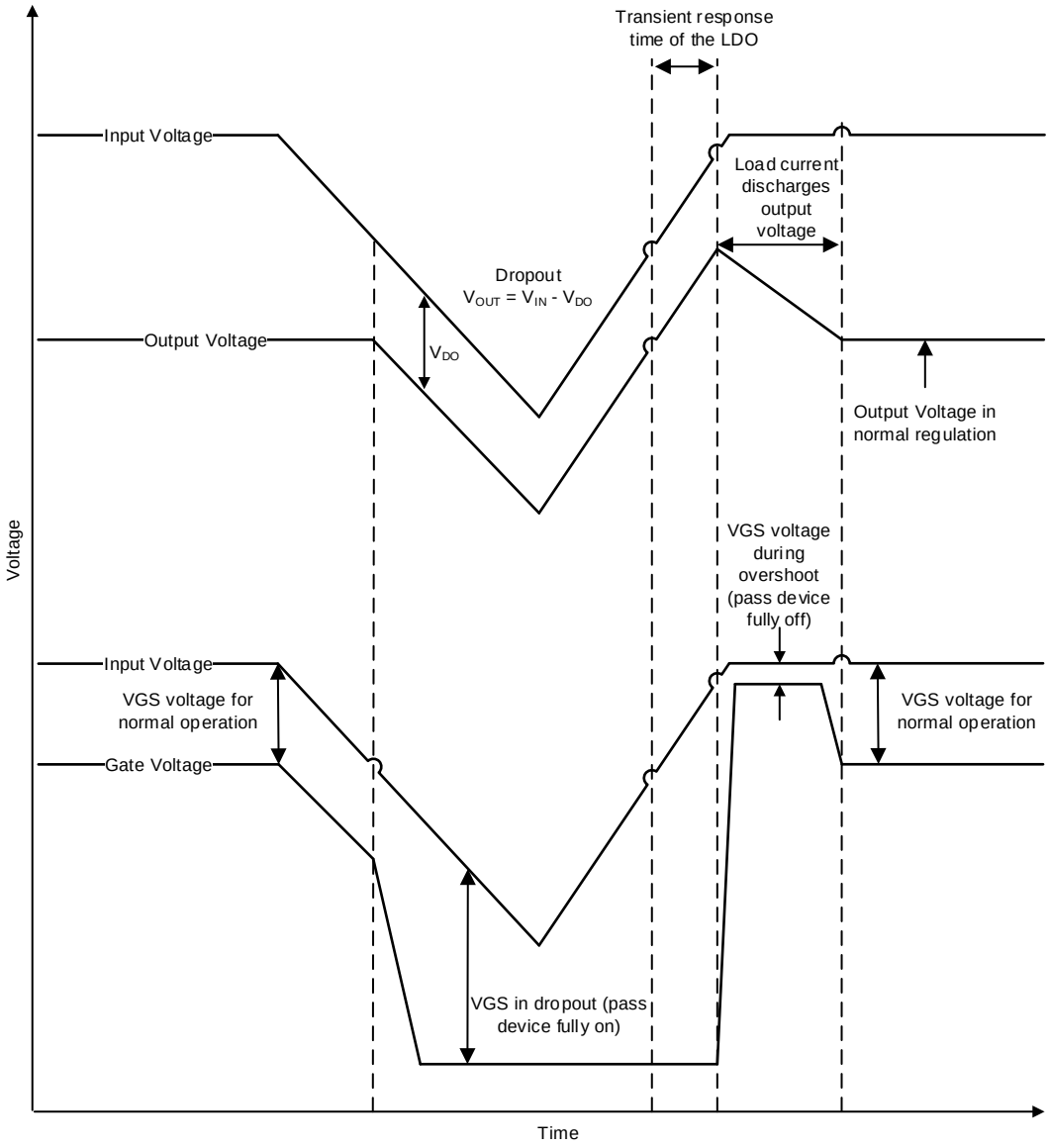


Figure 25. LDO Response Entering and Exiting Dropout

10.1.2 TPS7B67xx-Q1 Dropout During Startup

The TPS7B67xx-Q1 does not overshoot significantly if the LDO is enabled after the input voltage is already above $V_{OUT(NOM)}$ plus V_{DO}. Furthermore, startup performance is not affected as long as the input voltage transitions from $V_{UVLO+(IN)}$ to $V_{OUT(NOM)}$ plus V_{DO} in less than 1 millisecond. Approximately 1 millisecond is required for the TPS7B67xx-Q1 reference voltage to reach its steady state value, so input voltage startup transitions that are less than 1 millisecond do not force the device into dropout. One example that does not overshoot is a 5-V output voltage with full load (full load has the highest dropout), where the input voltage ramps steadily from 0 V to 5.45 V in less than 3 milliseconds. Overshoot does not occur in this case because the input reaches V_{OUT} plus V_{DO} before the reference has come up all the way to its final value, keeping the LDO out of dropout. Figure 26 depicts an example of a startup ramp rate that is just fast enough to keep a device with a 5-V output voltage from going into dropout.

Dropout Recovery (continued)

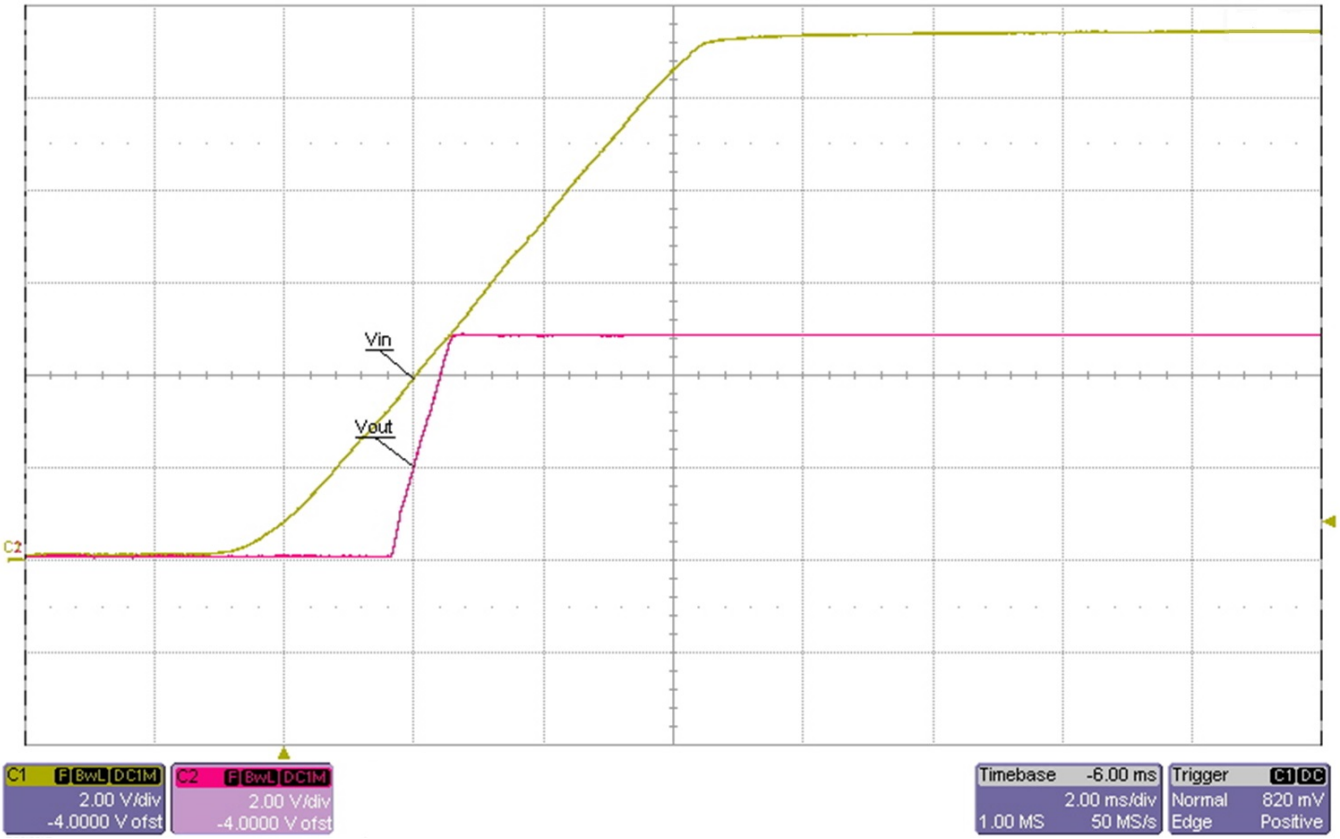


Figure 26. Startup Ramp Speed to Avoid Dropout

11 Layout

11.1 Layout Guidelines

11.1.1 Enhanced Thermal Pad

For the PWP package, TI recommends to layout an enhanced thermal pad on the board in order to realize better thermal impedance; see Figure 27. No extra board size is required and the standard operation is not influenced by this layout.

Layout Guidelines (continued)

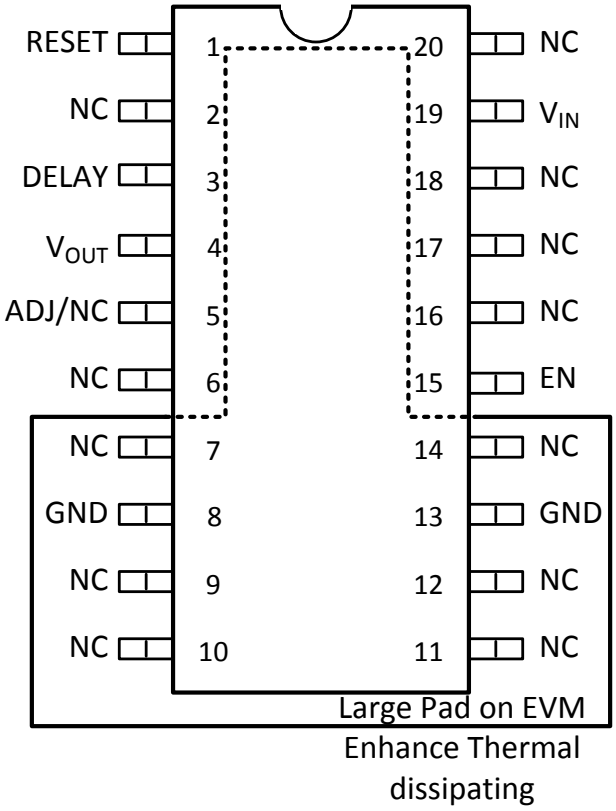


Figure 27. Thermally Enhanced Layout for the PWP Package (TPS7B6701-Q1)

11.1.2 Package Mounting

Solder-pad footprint recommendations for the TPS7B67xx-Q1 devices are available at the end of this data sheet and at www.ti.com.

11.1.3 Board Layout Recommendations to Improve PSRR and Noise Performance

- To improve AC performance such as PSRR, output noise, and transient response, TI recommends to design the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.
- Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close to the device as possible and on the same side of the PCB as the regulator.
- Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.
- If possible, and to ensure the maximum performance listed in this data sheet, use the same layout pattern used for TPS7B67xx-Q1 evaluation board, available at www.ti.com.

Layout Guidelines (continued)

11.1.4 Additional Layout Considerations

Because of the high impedance of the ADJ pin, the regulator is sensitive to parasitic capacitances that can couple undesirable signals from nearby components (especially from logic and digital ICs, such as microcontrollers and microprocessors). These capacitive-coupled signals can produce undesirable output-voltage transients. If undesirable output-voltage transients occur, TI recommends to use a fixed-voltage version of the TPS7B67xx-Q1 devices, or to isolate the ADJ node by flooding the local PCB area with ground-to-plane copper in order to minimize any undesirable signal coupling.

11.2 Layout Example

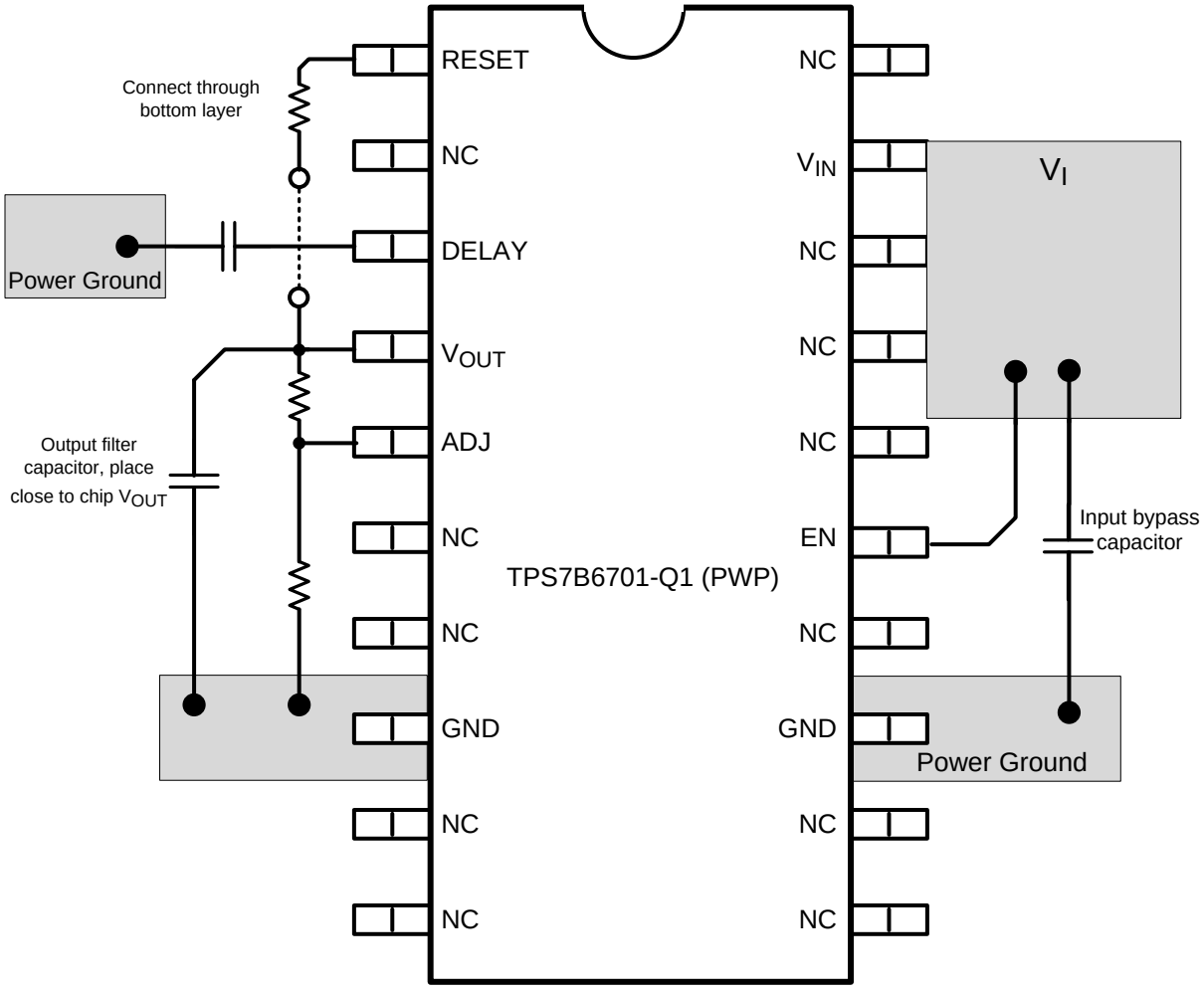


Figure 28. TPS7B6701-Q1 Layout Example

12 器件和文档支持

12.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 2. 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持与社区
TPS7B6701-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS7B6733-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS7B6750-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B6701QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6701	Samples
TPS7B6733QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6733	Samples
TPS7B6750QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6750	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

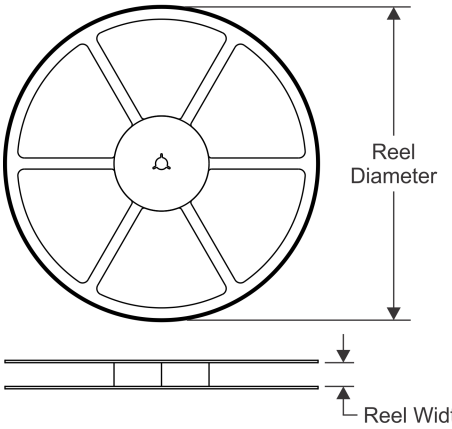
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

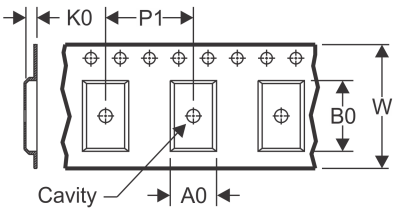
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

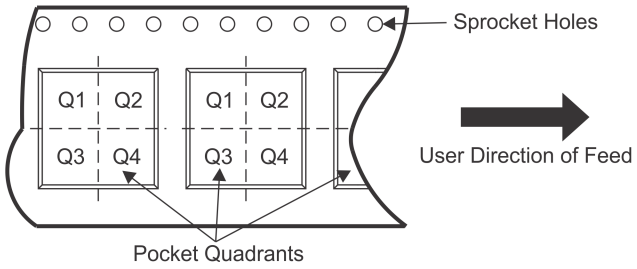


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

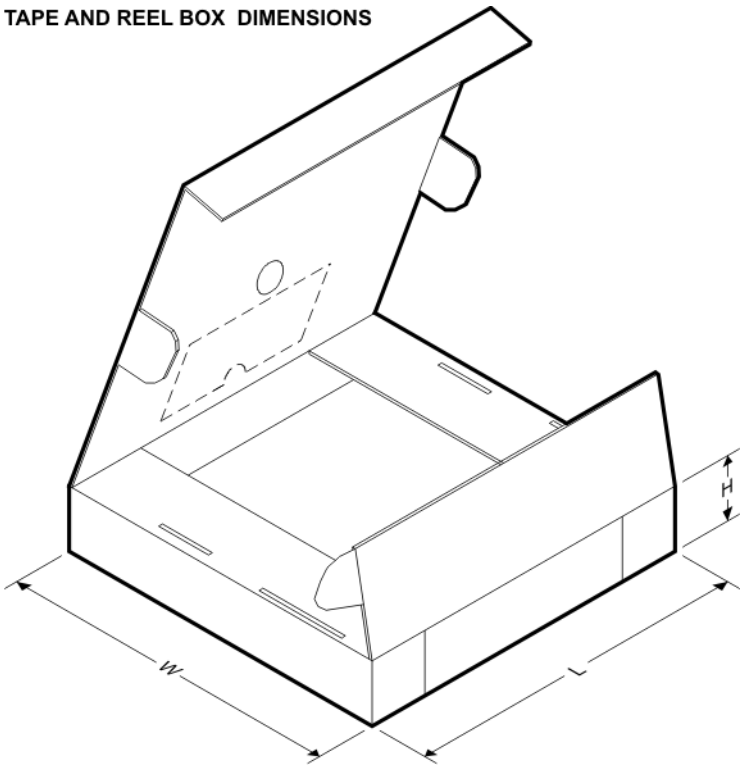
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B6701QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS7B6733QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS7B6750QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

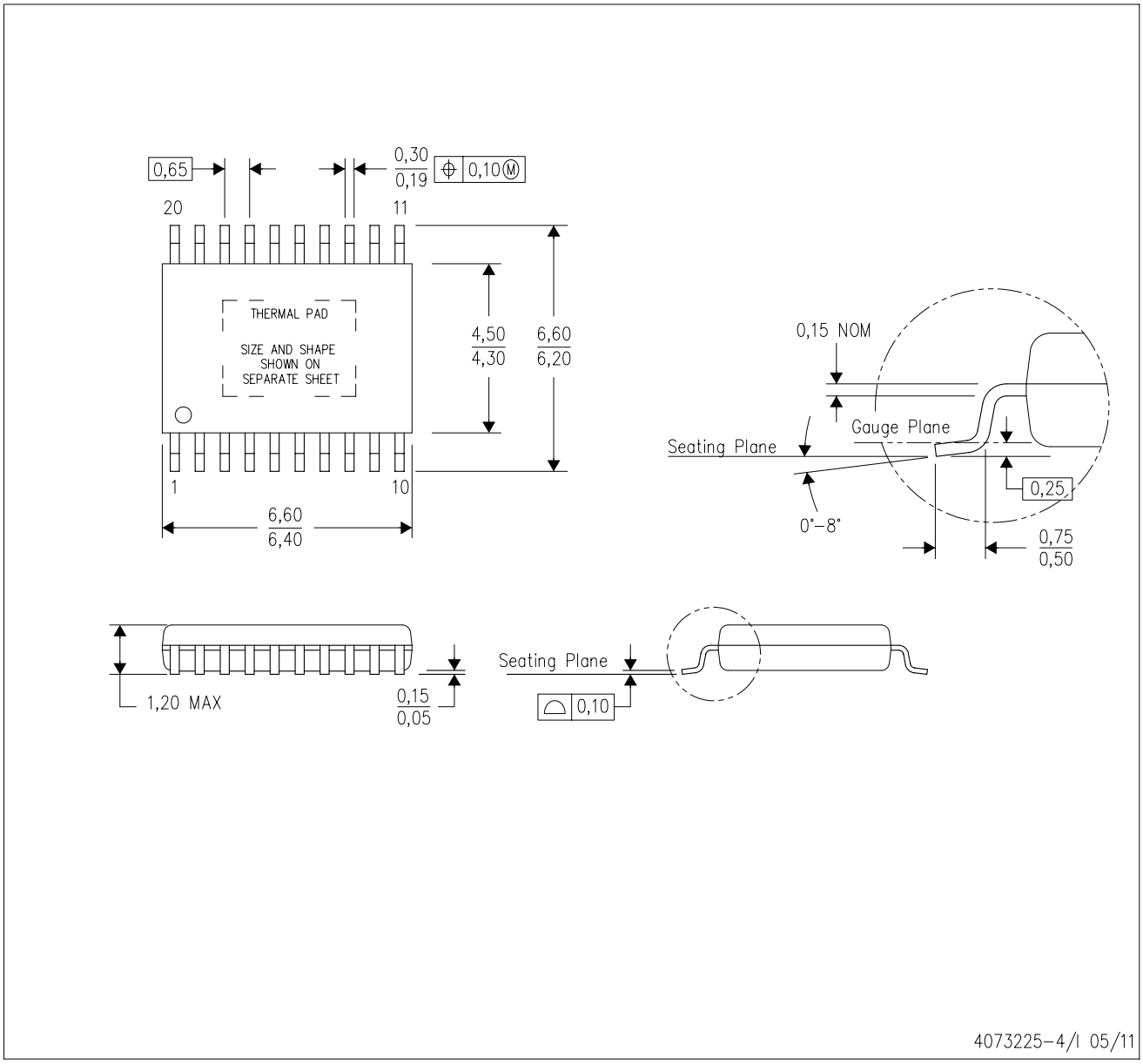
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B6701QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS7B6733QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS7B6750QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

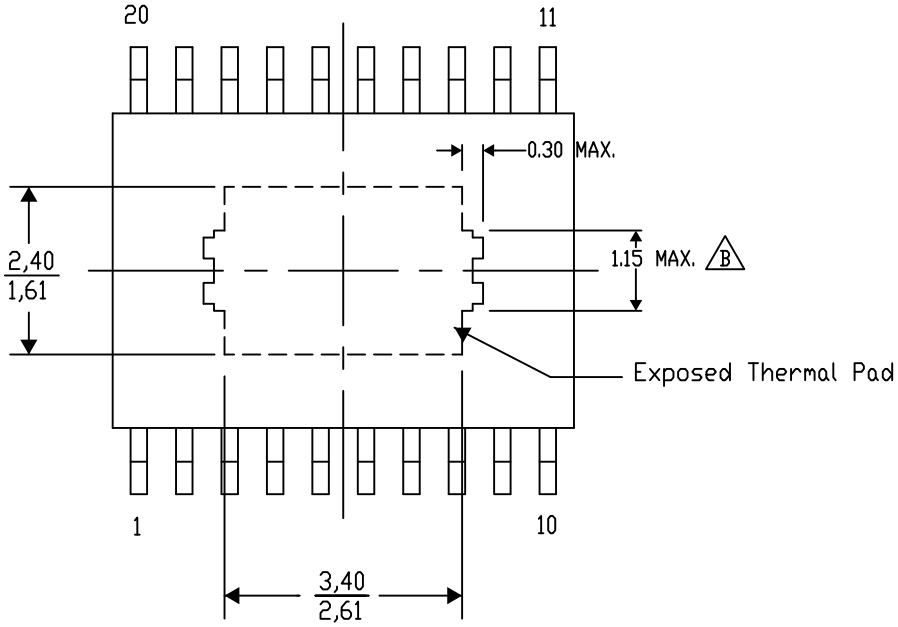
PWP (R–PDSO–G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–15/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B Exposed tie strap features may not be present.

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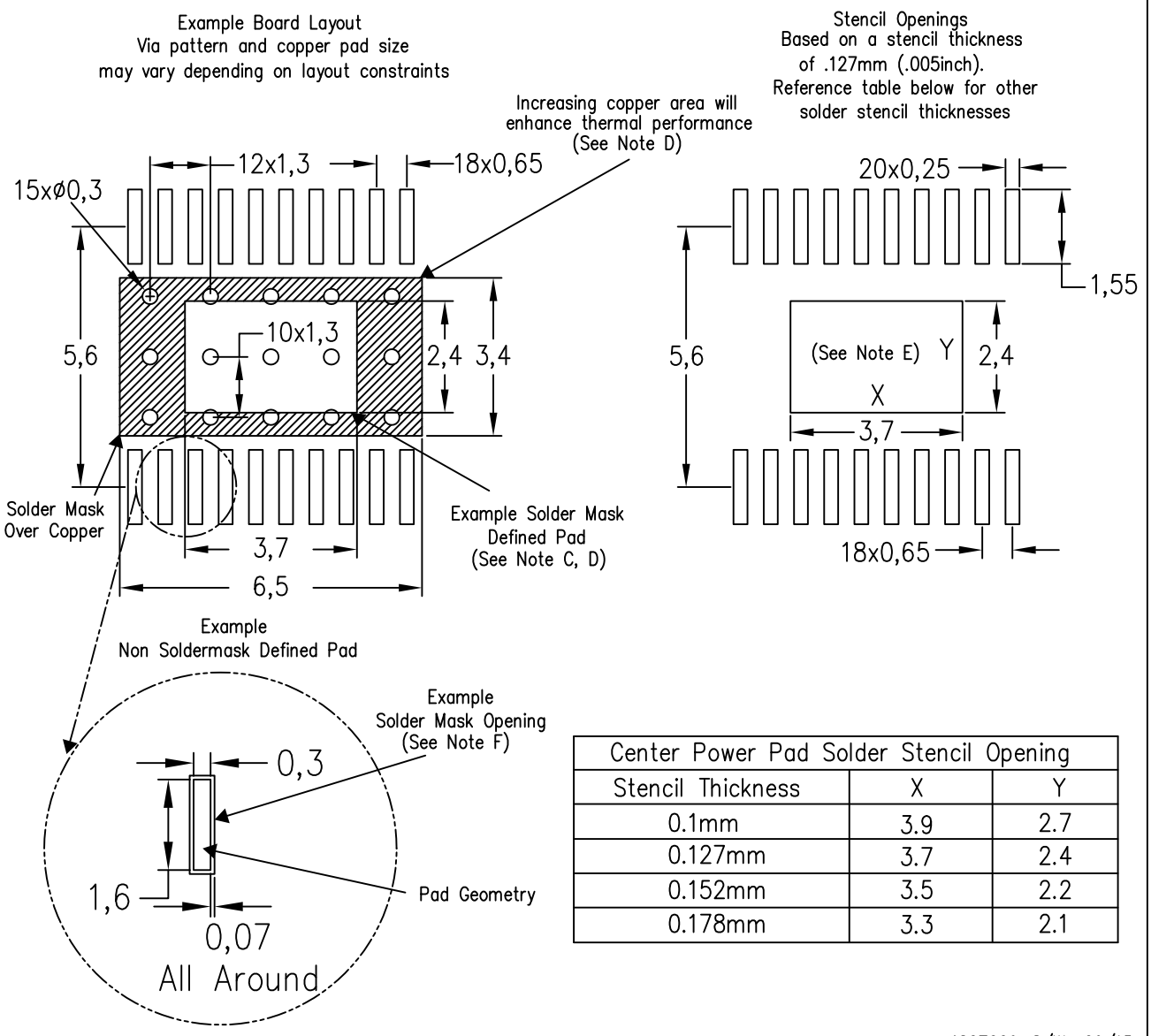
PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122