采用 1.2mm x 1.3mm WCSP 封装的 TPS61253A 3.8MHz、5V/4A 升压转换器

1 特性

- 宽输入电压范围：2.3V 至 5.5V
- 固定输出电压：4.5/4.7/5.0/5.2V
- 集成了两个 FET：35mΩ LS-FET、60mΩ HS-FET
- VOUT = 5V 且 VIN ≥ 3V 时，IOUT 持续 ≥ 1500mA
- 输入静态电流为 42μA
- 开关谷值电流限制为 4A
- 开关频率为 3.8MHz
- 可选择自动 PFM、强制 PWM 和超声波模式
- 支持直通模式
- ±2% 的输出电压精度
- 软启动时间为 600μs
- 间断模式短路保护
- 关断期间负载断开
- 热关断保护
- 总体解决方案尺寸小于 25mm^2
- 利用 TPS61253A 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 智能手机
- 便携式扬声器
- USB 充电端口
- NFC PA 电源
- 锂电池至 5V 电源转换

3 说明

TPS6125xA 器件为电池供电类便携式应用提供了一个电源解决方案。该器件具有 2.3V 至 5.5V 的输入电压，可支持由锂离子电池（具有扩展电压范围）供电的应用。可提供的不同固定输出电压版本包括 4.5V、4.7V、5V 和 5.2V 版本。TPS6125xA 可通过放电后电压低至 3V 的电池提供高达 1500mA 的负载电流。

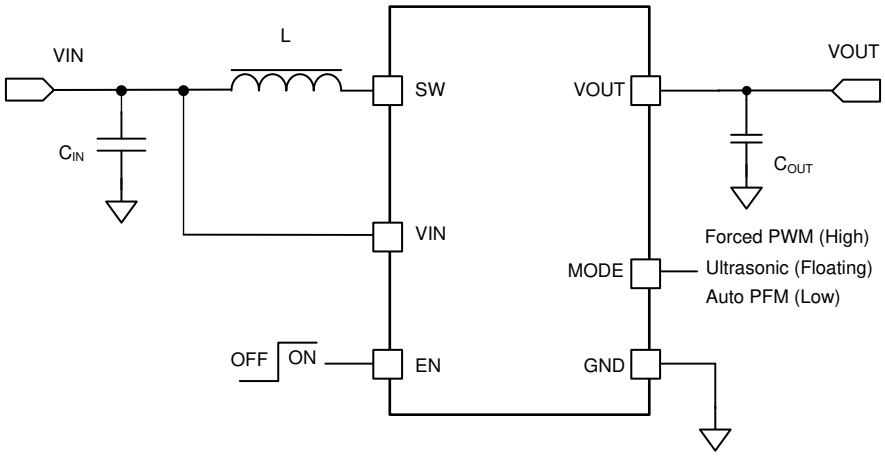
TPS6125xA 的典型工作开关频率为 3.8MHz。TPS6125xA 可灵活地配置为自动 PFM 模式、强制 PWM 模式或超声波模式。自动 PFM 模式可以在轻负载时获得高效率。强制 PWM 工作模式可使开关频率在整个负载范围内保持恒定。超声波模式可在任何负载条件下保持开关频率始终大于 25kHz，从而避免噪声。

TPS6125xA 具有 600μs 的内置软启动时间，从而能够避免启动时的浪涌电流。当输出短接时，该器件将进入间断模式，并可在短接结束后自动恢复。在关断期间，负载与输入端完全断开，消耗的电流最高为 1.3μA。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS61253A	DSBGA (9)	1.2mm × 1.3mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



半桥配置

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (November 2020) to Revision D (January 2021) — **Page**

- Adding HS FET to the functional block diagram 12

Changes from Revision B (October 2020) to Revision C (November 2020) — **Page**

- 从页眉中删除了 TPS612532A 1
- 添加了器件信息表 1

Changes from Revision A (December 2017) to Revision B (October 2020) — **Page**

- 向 TPS6125x 数据表添加了 TPS612532A 1
- 更新了整个文档的表、图和交叉参考的编号格式。 1
- Updated *Device Comparison Table* 3
- Changed TPS612531A to TPS612532A in Output Voltage 6

Changes from Revision * (March 2017) to Revision A (December 2017) — **Page**

- Changed from 5.1 V to 5.2 V in the Specific Features column of the *Device Comparison Table* for TPS612592A 3

5 Device Comparison

PART NUMBER	OUTPUT VOLTAGE	SW VALLEY CURRENT LIMIT (TYP.)	DC START-UP CURRENT LIMT (TYP.)	SPECIFIC FEATURES
TPS61253A	5 V	4 A	1.5 A	Supports output 5 V, up to 1500 mA
TPS612532A	5 V	4 A	1.5 A	Supports output 5 V, up to 1500 mA with output discharge function
TPS61254A(1)	4.5 V	2.5 A	0.75 A	Supports output 4.5 V, up to 1000 mA
TPS61255A(1)	4.7 V	4 A	1.5 A	Supports output 4.5 V, up to 1500 mA
TPS612561A(1)	5 V	2.5 A	0.75 A	Supports output 5 V, up to 1000 mA
TPS61258A(1)	4.5 V	4 A	1.5 A	Supports output 4.5 V, up to 1500 mA
TPS612592A(1)	5.2 V	4 A	0.75 A	Supports output 5.2 V, up to 1500 mA
TPS612531A(1)	5 V	4 A	1.5 A	Supports output 5 V, up to 1500 mA with PFM/PWM mode only

(1) Preview. Contact TI factory for more information.

6 Pin Configuration and Functions

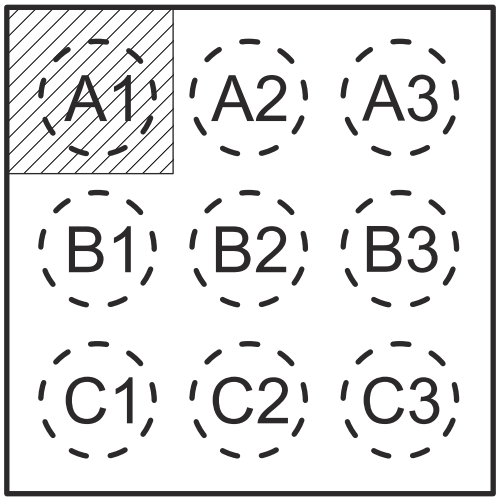


图 6-1. 9-Pin DSBGA YFF Package (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	B3	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin high enables the device. There is an internal resistor pulled to GND.
GND	C1, C2	–	Ground pin
MODE	C3	–	Operation mode selection pin Mode = Low, the device works in the Auto PFM mode with good light load efficiency. Mode = High, the device is in the forced PWM mode, keep the switching frequency be constant crossing the whole load range. Mode = Floating, the device works in the ultrasonic mode; it keeps the switching frequency larger than 25 kHz to avoid the acoustic frequency toward no load condition.
SW	B1, B2	I/O	The switch pin of the converter. It is connected to the drain of the internal low-side power FET and the source of the internal high-side power FET.
VIN	A3	I	Power supply input
VOUT	A1, A2	O	Boost converter output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals	Voltage at VIN, EN, MODE, VOUT	–0.3	6	V
	Voltage at SW	–0.3	7	V
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

Over operating free-air temperature range unless otherwise noted.

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.3		5.5	V
L	Effective inductance	0.33		1.3	µH
C_{OUT}	Effective output capacitance	3.5	5	30	µF
T_J	Operating junction temperature	–40		125	ºC

7.4 Thermal Information

THERMAL METRIC(1)		TPS6125xA YFF (DSBGA) 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 2.3 V to 4.85 V , V_{OUT} = 5 V , T_J = –40°C to 125°C ; Typical values are at V_{IN} = 3.6 V , T_J = 25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN_UVLO}	Input voltage under voltage lockout (UVLO) threshold	V_{IN} rising		2.2	2.3	V
		V_{IN} falling		2.1	2.2	V
I_Q	Quiescent current into VIN pin	V_{IN} = 3.6 V, V_{OUT} = 5 V , EN = V_{IN} Device not switching		42	50	µA
	Quiescent current into VOUT pin	V_{IN} = 3.6 V, V_{OUT} = 5 V , EN = V_{IN} Device not switching		6.6	12	µA
I_{SD}	Shutdown current	EN = GND , V_{IN} = 2.3 V to 5.5 V, –40 °C ≤ T_J ≤ 85°C		0.05	1.3	µA
OUTPUT VOLTAGE						
V_{OUT}	PWM Operation	2.3 V ≤ V_{IN} ≤ 4.85V, I_{OUT} = 0mA, PWM operation. Open Loop	4.9	5	5.1	V
	PFM Operation	Auto PFM Mode		100.8		%V_{OUT}
	Ultrasonic Operation	Ultrasonic Mode		101.6		%V_{OUT}
R_{DIS}	output discharge resistor	V_{OUT} = 5 V, TPS612532A		350		Ω
POWER SWITCHES						
R_{DSON}	Low-side FET on resistance			35	55	mΩ
	High-side FET on resistance			60	80	mΩ
CURRENT LIMIT						
I_{LIM_SW}	Switching valley current limit at Auto PFM / Ultrasonic Mode	TPS61253A	3.4	4	4.6	A
	Switching valley current limit at Forced PWM Mode	TPS61253A	3.35	3.95	4.55	A
I_{LIM_DC}	DC startup current limit	TPS61253A	1	1.5		A
EN AND MODE LOGIC						
V_{EN_H}	EN logic high threshold				1.2	V
V_{EN_L}	EN logic low threshold		0.4			V
R_{EN}	EN pull-down resistor			930		kΩ
V_{MODE_H}	Mode logic high threshold				1.2	V
V_{MODE_L}	Mode logic low threshold		0.4			V
V_{MODE_F}	Mode pin floating voltage		0.75	0.8	0.85	V
I_{MODE_UP}	Pull up current			1		µA
I_{MODE_DOWN}	Pull down current			1		µA
PROTECTION						
T_{SD_R}	Thermal shutdown rising threshold			150		ºC
T_{SD_HYS}	Thermal protection hysteresis			20		ºC

7.6 Timing Requirements

V_{IN} = 2.3 V to 4.85 V , V_{OUT} = 5 V , T_J = –40 °C to 125 °C ; Typical values are at V_{IN} = 3.6 V , T_J = 25 °C, unless otherwise noted.

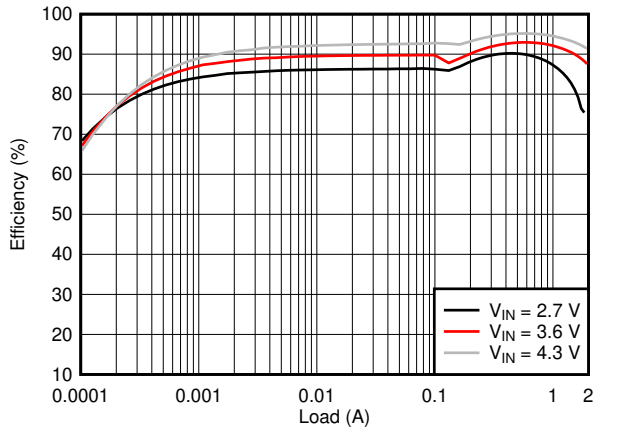
			MIN	NOM	MAX	UNIT
HICCUP OFF TIME						
t_{HCP_ON}	Hiccup on time	V_{IN} = 3.6 V, V_{OUT} = 5 V		1000		µs
t_{HCP_OFF}	Waiting time for the restart	V_{IN} = 3.6 V, V_{OUT} = 5 V		20		ms
START UP TIME						
t_{EN_DELAY}	Startup delay time	Time from EN high to start switching, No load		70		µs
t_{SS}	Soft start time	Time from EN high to V_{OUT}, No load		600		µs

7.7 Switching Characteristics

V_{IN} = 2.3 V to 4.85 V , V_{OUT} = 5 V , T_J = –40 °C to 125 °C ; Typical values are at V_{IN} = 3.6 V , T_J = 25 °C, unless otherwise noted.

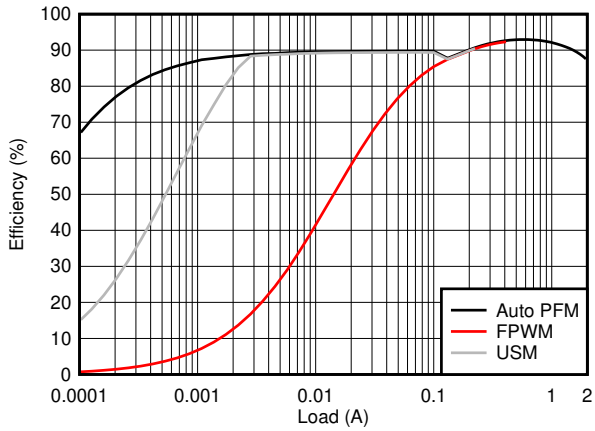
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SW}	Switching frequency, PWM mode	V_{IN} = 3.6 V, V_{OUT} = 5 V		3800		kHz
	Switching frequency, Ultrasonic mode	V_{IN} = 3.6 V, V_{OUT} = 5 V	25			kHz

7.8 Typical Characteristics



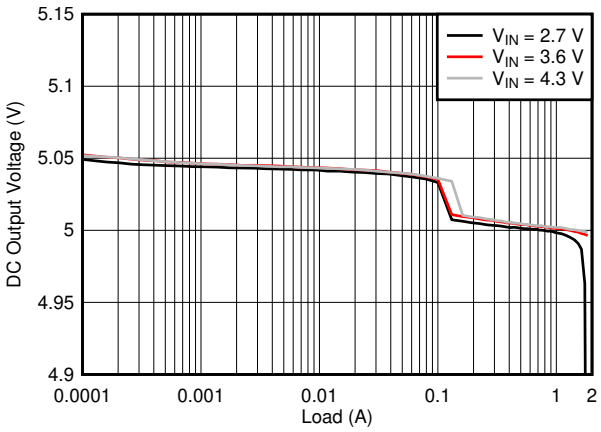
V_{OUT} = 5 V L = 0.56 µH Auto PFM Mode

图 7-1. Efficiency vs Load



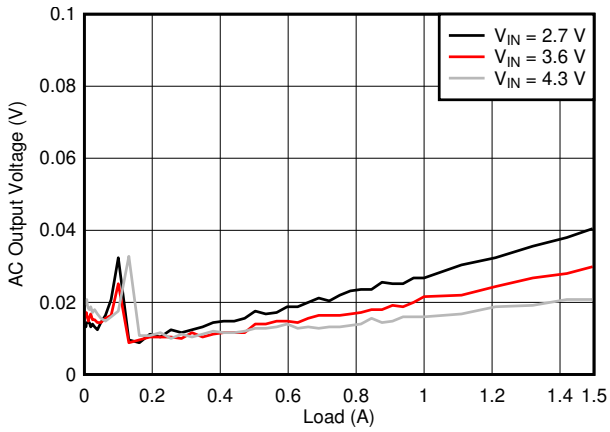
V_{OUT} = 5 V L = 0.56 µH V_{IN} = 3.6 V

图 7-2. Efficiency vs Load



V_{OUT} = 5 V L = 0.56 µH

图 7-3. DC Output Voltage vs Load



V_{OUT} = 5 V L = 0.56 µH Auto PFM Mode

图 7-4. AC Output Voltage vs Load

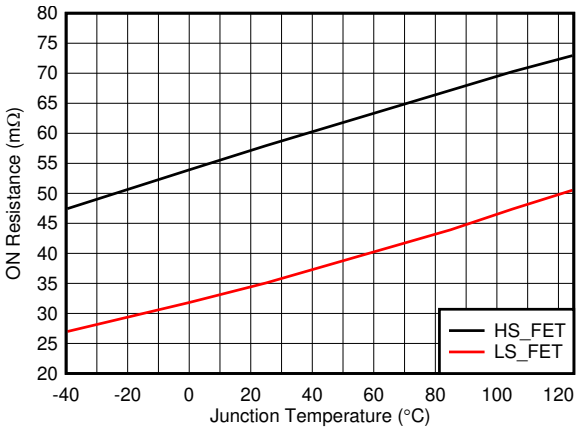


图 7-5. $RDS_{(ON)}$ vs Temperature

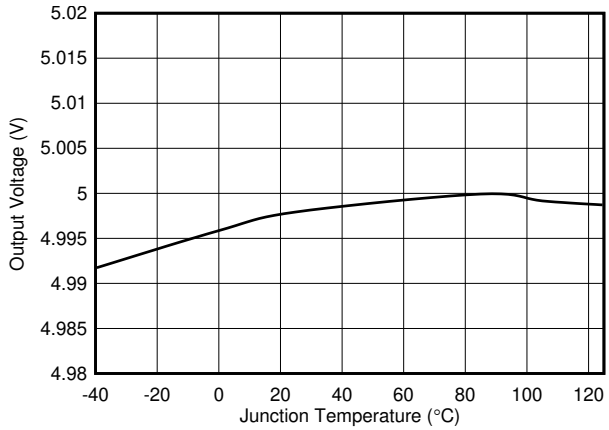


图 7-6. V_{OUT} vs Temperature

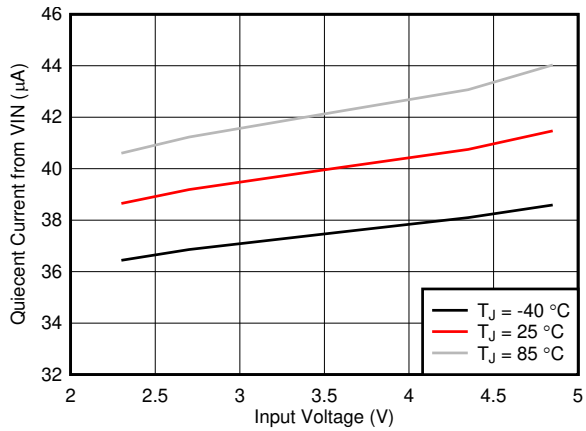


图 7-7. Quiescent Current (from VIN) vs Input Voltage

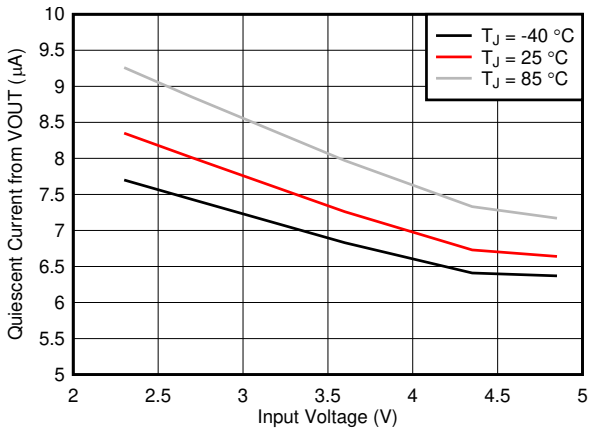


图 7-8. Quiescent Current (from VOUT) vs Input Voltage

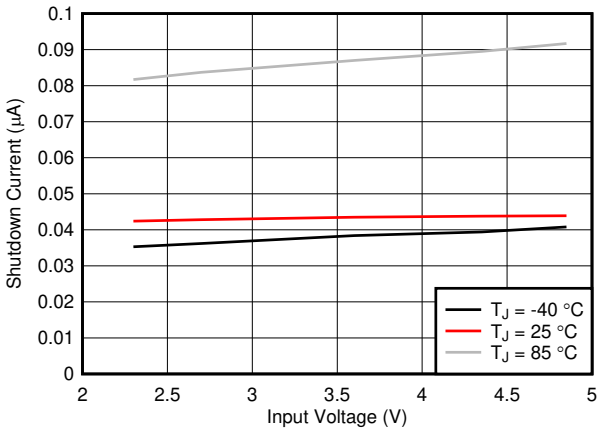


图 7-9. Shutdown Current vs Input Voltage

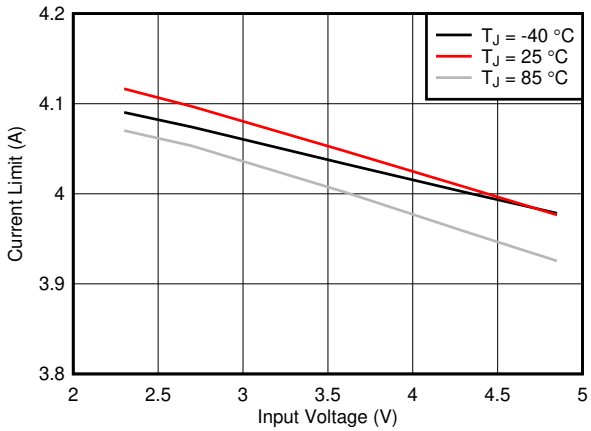


图 7-10. Current Limit (Auto PFM) vs Input Voltage

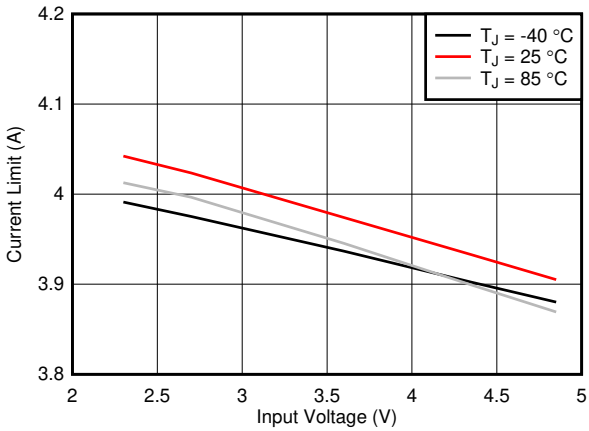


图 7-11. Current Limit (Forced PWM) vs Input Voltage

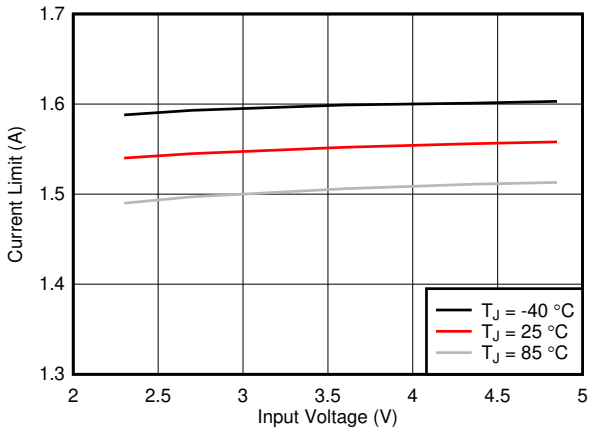


图 7-12. DC Startup Current Limit vs Input Voltage

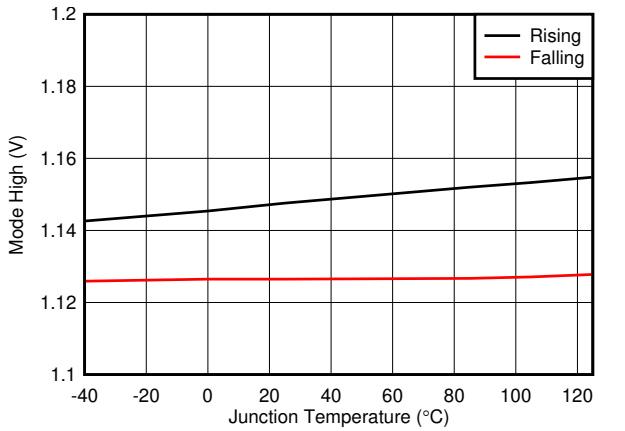


图 7-13. Mode High Rising / Falling vs Temperature

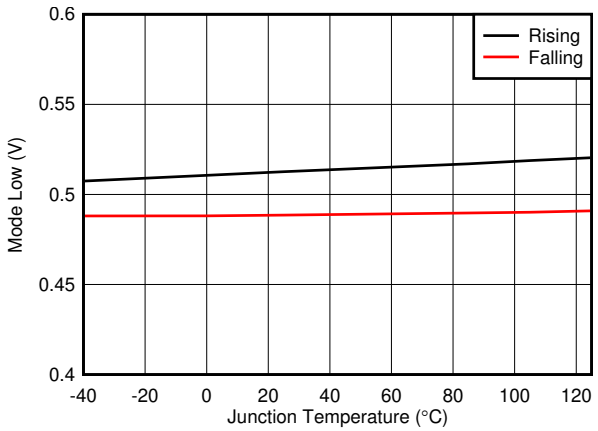


图 7-14. Mode Low Rising / Falling vs Temperature

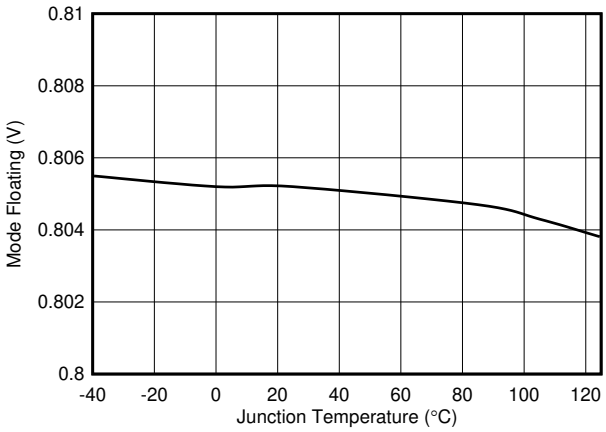


图 7-15. Mode Floating vs Temperature

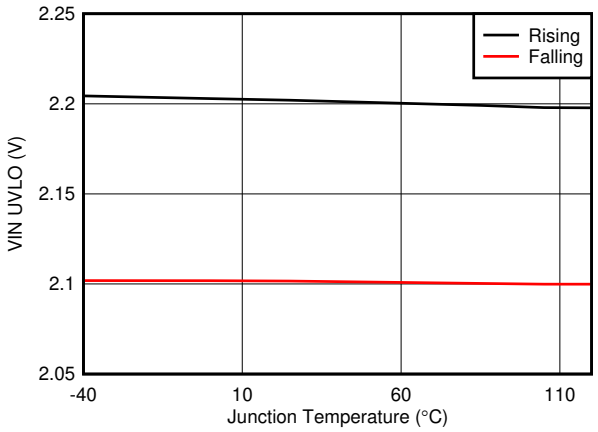


图 7-16. VIN UVLO vs Temperature

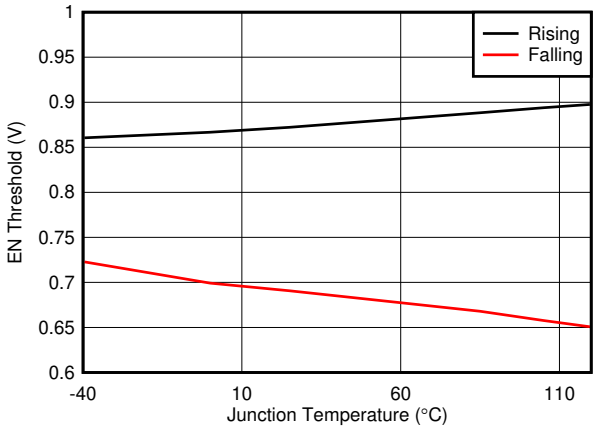


图 7-17. EN Threshold vs Temperature

8 Detailed Description

8.1 Overview

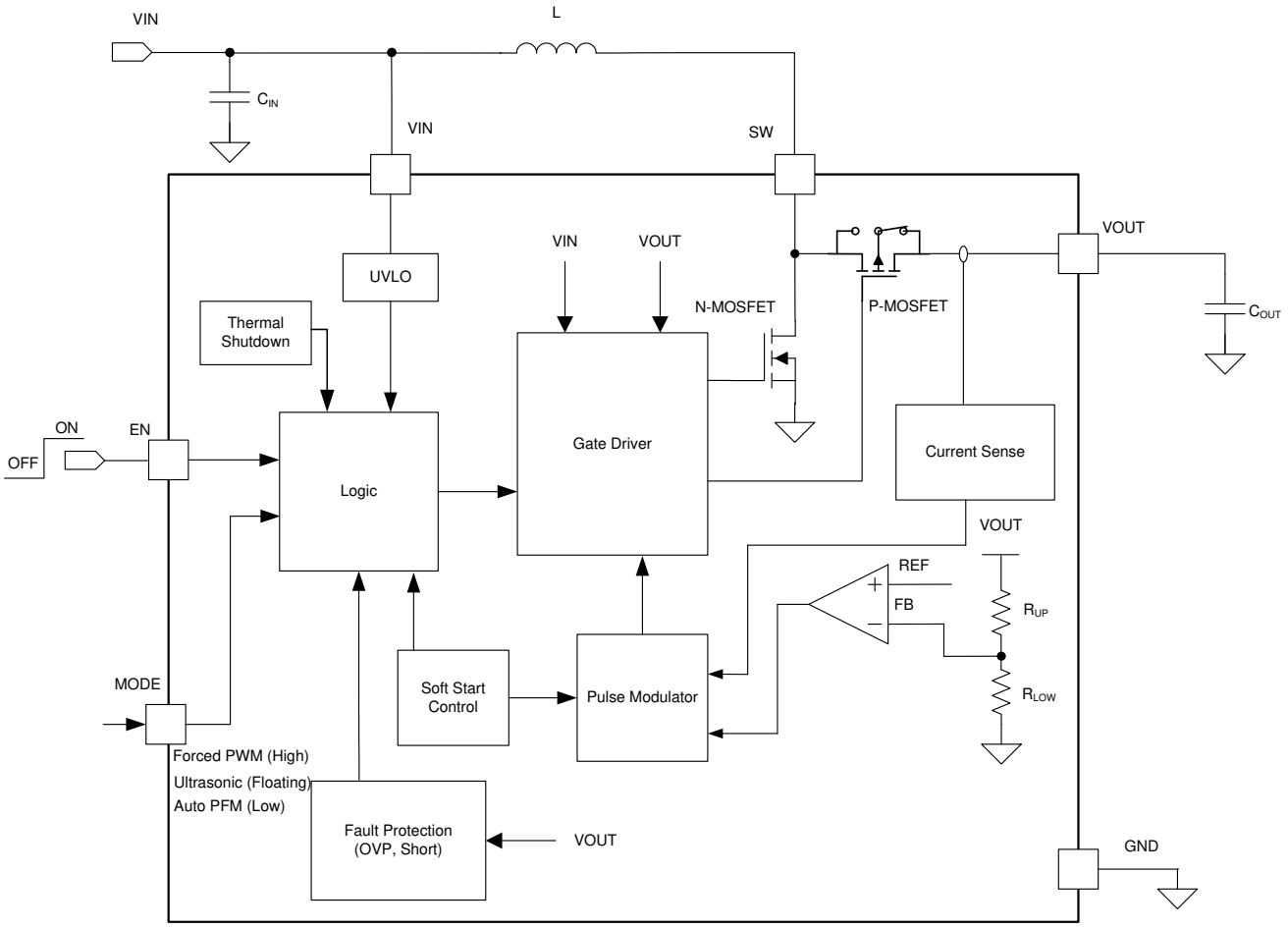
The TPS6125xA synchronous step-up converter typically operates at a quasi-constant 3.8-MHz frequency pulse width modulation (PWM) from the moderate-to-heavy load currents. During the PWM operation, the converter uses a quasi-constant on-time valley current mode control scheme to achieve the excellent line / load regulation and allows the use of a small inductor and ceramic capacitors. Based on the V_{IN} / V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch is turned on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier FET is turned on and the inductor current decays to a preset valley current threshold. Then, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

At the light load current conditions, the TPS6125xA can be flexibly configured at the Auto PFM mode, the forced PWM or the ultrasonic mode. At the Auto PFM mode, the TPS6125xA converter operates in Power Save Mode with pulse frequency modulation (PFM) and improves the efficiency. For forced PWM mode, the switching frequency is the same at the light load as that of heavy load. The ultrasonic mode is a unique control feature that keeps the switching frequency above 25 kHz to avoid the acoustic audible frequencies toward virtually no load condition.

In general, a dc/dc step-up converter can only operate in "true" boost mode, that is the output “boosted” by a certain amount above the input voltage. The TPS6125xA device operates differently as it can smoothly transition in and out of pass-through operation (V_{IN} exceeds the preset out of Boost). Therefore the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive.

Internal soft start and loop compensation simplify the design process while minimizing the number of external components.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Start-up

The TPS6125xA integrates an internal circuit that controls the ramp up of the output voltage during start-up and prevents the converter from the large inrush current. When the device is enabled, the high-side rectifying switch turns on to charge the output capacitor linearly which is called the pre-charge phase. During the pre-charge phase, the output current is limited to the pre-charge current limit ILIM_DC. The pre-charge phase terminates until the output voltage getting close to the input voltage.

Once the output capacitor has been biased close to the input voltage, the device starts switching which is called the soft-start phase. During the soft start phase, there is a soft-start voltage controlling the FB pin voltage, and the output voltage rising slope follows the soft-start voltage slope. The device finishes the soft-start phase and operates normally when the nominal output voltage is reached.

表 8-1. Start-up Mode Description

MODE	DESCRIPTION	CONDITION
Pre-charge	V_{OUT} linearly starts up without switching	$V_{OUT} < V_{IN}$ - 300 mV
Boost soft start	V_{OUT} starts up wih switching phrase	$V_{OUT\_BOOST} \geq V_{OUT} \geq V_{IN}$ - 300 mV

8.3.2 Enable and Disable

The device is enabled by setting EN pin to a voltage above 1.2 V and V_{IN} above UVLO threshold. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the start-up is activated

and the output voltage ramps up. With the EN pin pulled to ground, the device enters shutdown mode. In shutdown mode, the TPS6125xA stops switching and the internal control circuitry is turned off.

8.3.3 Undervoltage Lockout (UVLO)

The undervoltage lockout circuit prevents the device from malfunctioning at the low input voltage of the battery from the excessive discharge. The device starts operation once the rising V_{IN} trips the undervoltage lockout (UVLO) threshold and it disables the output stage of the converter once the V_{IN} is below UVLO falling threshold.

8.3.4 Current Limit Operation

During the start-up phase, the output current is limited to the pre-charge current limit which is specified as the ILIM_DC in *节 7.5*.

The TPS6125xA employs a valley current sensing scheme at the normal boost switching phase. When the output load is increased, the cycle-by-cycle valley current limit will be triggered. As shown in 图 8-1, the maximum continuous output current, prior to entering the current limit operation, can be defined by 方程式 1:

$$I_{OUT\_LIM} = (1-D) \times (I_{VALLEY\_LIM} + \frac{1}{2}\Delta I_L) \quad (1)$$

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \quad (2)$$

$$\Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \quad (3)$$

where

- I_{OUT_LIM} is the output current limit, I_{VALLEY_LIM} is switching valley current limit
- Δ_{IL} is the peak-peak inductor current ripple
- D is the duty cycle, f is the switching frequency, η is the efficiency, L is the inductor
- V_{OUT} is the output voltage, V_{IN} is the input voltage

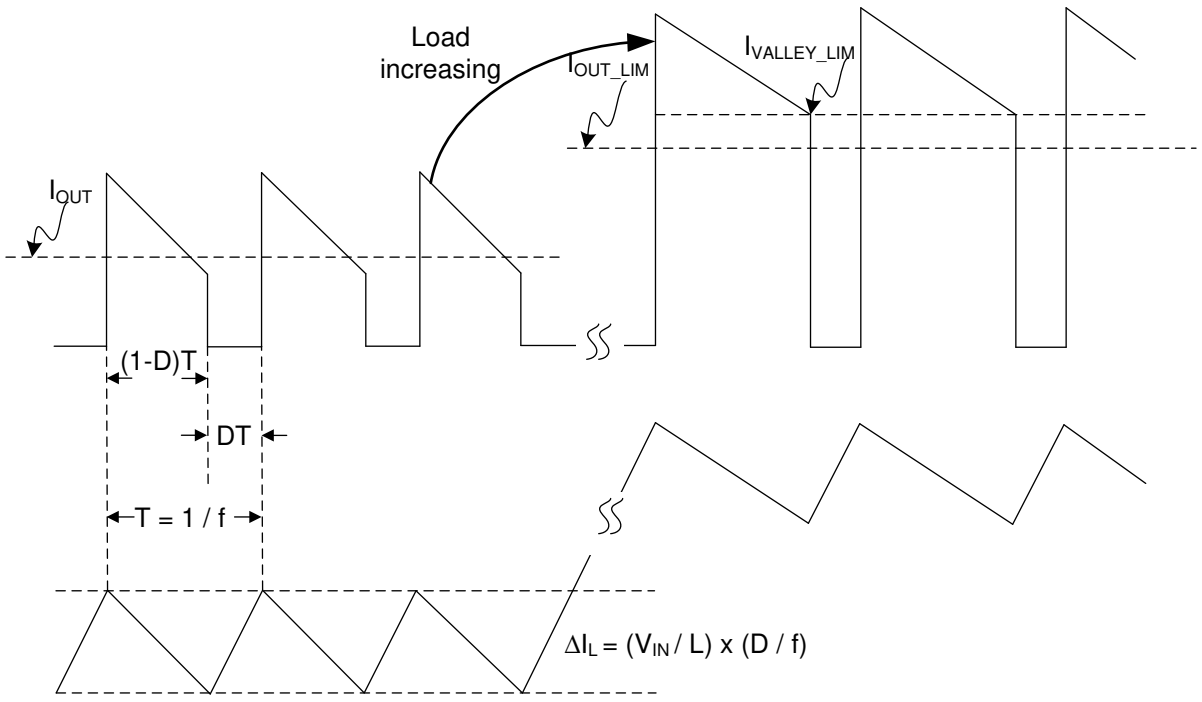


图 8-1. Current Limit Operation

If the output current is further increased and triggers the short protection threshold (typical 6 A of inductor current), the TPS6125xA enters into hiccup mode. Once the hiccup is triggered, the device turns on the high-side FET for around 1 ms with the pre-charge current limit and stops for around 20 ms. The hiccup on / off cycle repeats again and again if the short condition is present. 图 8-2 illustrates the TPS6125xA working scheme of the hiccup mode. The average current and thermal will be much lowered at the hiccup steady state and the device can recover automatically as long as the short releases.

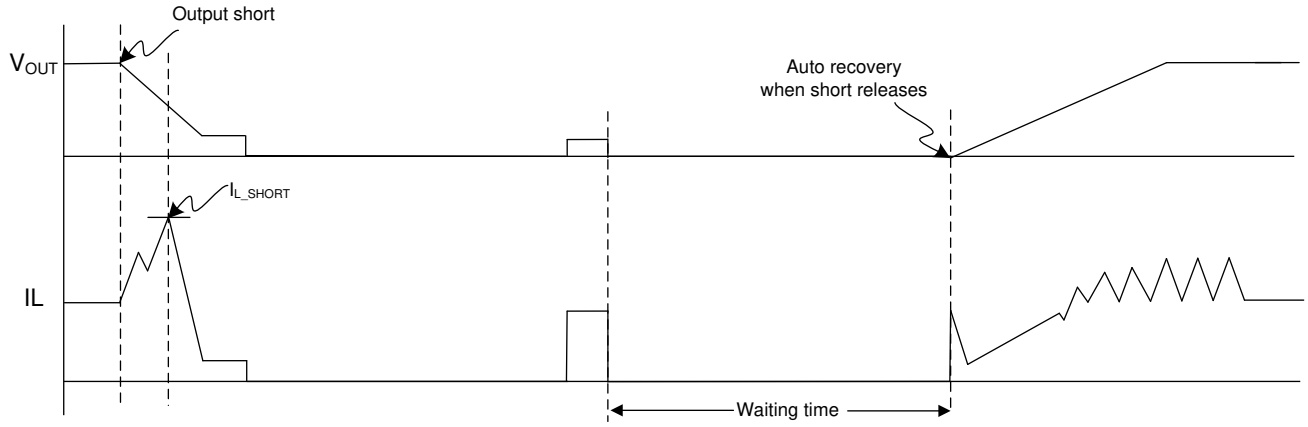


图 8-2. Hiccup Mode Short Protection

8.3.5 Load Disconnection

The advantage of TPS6125xA is that this converter disconnects the output from the input of the power supply when it is disabled. In case of a connected battery, it prevents it from being discharged during shutdown of the converter.

8.3.6 Thermal Shutdown

The TPS6125xA has a built-in temperature sensor that monitors the internal junction temperature, T_J. If the junction temperature exceeds the threshold (typical 150 °C), the device goes into the thermal shutdown, and the high-side and low-side FETs are turned off. When the junction temperature falls below the thermal shutdown falling threshold (typical 130 °C), the device resumes the operation.

8.4 Device Functional Modes

8.4.1 Auto PFM Mode

The device integrates Power Save Mode with pulse frequency modulation (Auto PFM) to improve the efficiency at the light load. At the light load operation, when the valley current of the inductor triggers the Auto PFM threshold, the device enters into Auto PFM mode operation. During the Auto PFM operation, the output voltage is regulated at typically 100.8% of voltage of the heavy load with the off-time extended to lower the switching frequency. The Auto PFM operation exists when valley current exceeds the Auto PFM threshold. 图 8-3 shows the output voltage behavior of Auto PFM operation.

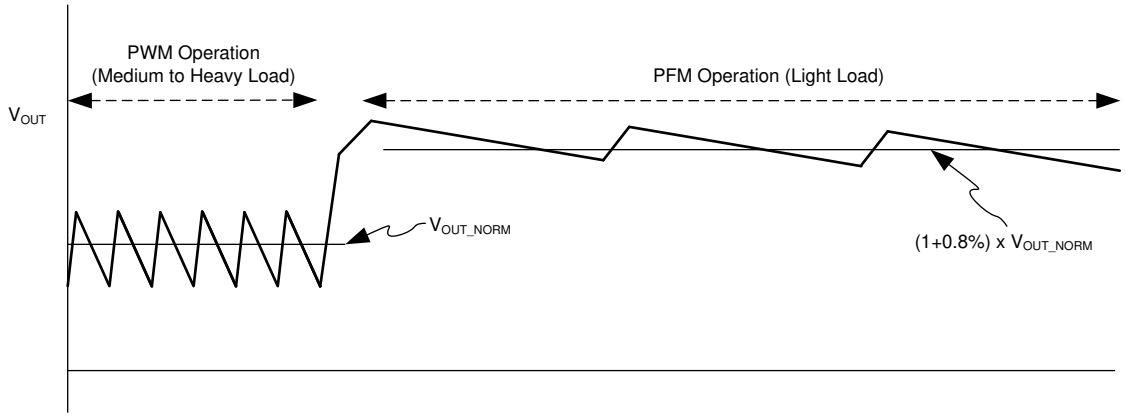


图 8-3. Output Voltage in Auto PFM / PWM Mode

8.4.2 Forced PWM Mode

In forced PWM mode, the TPS6125xA keeps the switching frequency being constant for the whole load range. When the load current decreases, the output of the internal error amplifier decreases as well to lower the inductor peak current and delivers less power from input to output. The high-side FET is not turned off even if the current through the FET goes negative to keep the switching frequency being the same as that of the heavy load.

8.4.3 Ultrasonic Mode

The ultrasonic mode is an unique control feature that keeps the switching frequency above the acoustic audible frequency toward no load condition. The ultrasonic mode control circuit monitors the switching frequency and keeps the switching frequency above 25 kHz to avoid the acoustic band. The output voltage becomes typically 1.6% higher than PWM operation. 图 8-4 illustrates the details of ultrasonic mode operation.

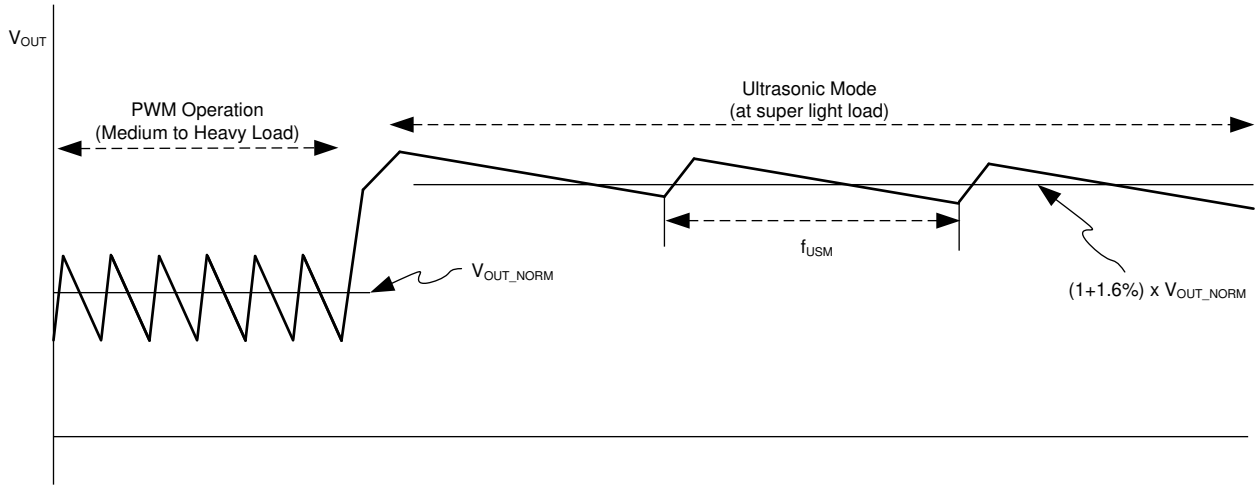


图 8-4. Ultrasonic Mode Operation

8.4.4 Pass-Through Mode

When the input voltage is higher than V_{OUT} + 0.1 V and V_{OUT} is higher than the nominal output voltage, the device automatically enters Pass-Through mode. In Pass-Through mode, the high-side FET is fully turned on and the low-side switch is turned off. The output voltage follows the input with the drop caused by the inductor resistance and the high-side FET resistance.

9 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

With a wide input voltage range of 2.3 V to 5.5 V, the TPS6125xA supports applications powered by Li-Ion batteries with extended voltage range. Intended for the low-power applications, it supports up to 1500-mA load current from a battery discharged as low as 3 V and allows the use of low cost chip inductor and capacitors. Different fixed voltage output versions are available from 4.5 V o 5.2 V. The TPS6125xA offers a very small solution size due to minimum amount of external components. It allows the use of small inductors and input capacitors to achieve a small solution size. During the pass-through mode, the output voltage is biased to the input voltage.

9.2 Typical Application

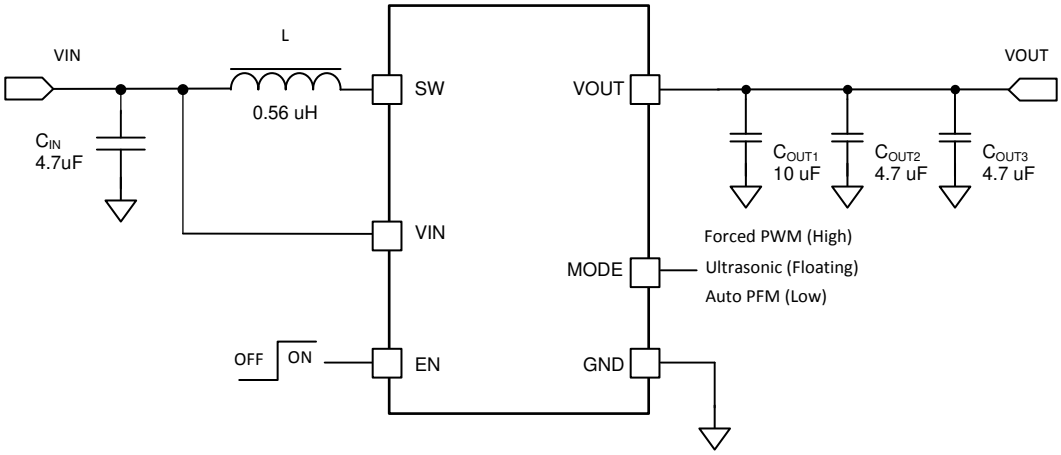


图 9-1. Typical Application Circuit

9.2.1 Design Requirements

In this example, TPS6125xA is used to design a 5-V output Boost converter. The TPS6125xA can be powered by one-cell Li-ion battery. It supports up to 1500-mA output current from the input voltage as low as 3.0 V. During shutdown, the load is completely disconnected from the battery.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61253A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion, an inductor and an output capacitor. It is advisable to select an inductor with a saturation current rating higher than the possible peak current flowing through the power switches.

The inductor peak current varies as a function of the load, the input and output voltages. It can be estimated using 方程式 4.

$$I_{L(PEAK)} = \frac{V_{IN} \cdot D}{2 \cdot f \cdot L} + \frac{I_{OUT}}{(1-D)} \quad \text{with} \quad D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \tag{4}$$

Selecting an inductor with insufficient saturation current can lead to excessive peak current in the converter. This could eventually harm the device and reduce its reliability. When selecting the inductor, as well as the inductance, parameters of importance are: the maximum current rating, series resistance, and operating temperature. The inductor DC current rating should be greater (by some margin) than the maximum input average current, refer to 方程式 5 for more details.

$$I_{L(DC)} = \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{\eta} \cdot I_{OUT} \tag{5}$$

The TPS6125xA series of step-up converters could support operating with an effective inductance in the range of 0.33 µH to 1.3 µH and with effective output capacitance in the range of 3.5 µF to 30 µF. The internal compensation is optimized for an output filter of the inductance between 0.56 µH and 1 µH and output capacitance from 5 µF to10 µF. Larger or smaller inductor and capacitor values can be used to optimize the performance of the device for specific operating conditions. For more details, see *节 9.2.2.5*.

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (that is, quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS current, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, R(DC) , and the following frequency dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS6125xA converters.

表 9-1. List of Inductors

MANUFACTURER(1)	SERIES	DESCRIPTION	DIMENSIONS (W × L × H)
Colicraft	XEL3515-561MEB	0.56 µH, 21.5 mΩ DCR, 6.5 A I_{sat}	3.2 mm × 3.5 mm × 1.5 mm
Murata	1277AS-H-1R0M=P2	1 µH, 34 mΩ DCR, 4.6 A I_{sat}	3.2 mm × 2.5 mm × 1.2 mm

(1) See *节 11.1.1*.

9.2.2.3 Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, 方程式 6 can be used.

$$C_{MIN} = \frac{I_{OUT} \cdot (V_{OUT} - V_{IN})}{f \cdot \Delta V \cdot V_{OUT}} \quad (6)$$

where

- f is the switching frequency which is 3.8 MHz (typ.)
- ΔV is the maximum allowed output ripple

With a chosen ripple voltage of 25 mV, a minimum effective capacitance of 7 µF is needed for maximum 1500-mA load. The capacitor can be smaller if the load is lower or the ripple can be larger. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using 方程式 7

$$V_{ESR} = I_{OUT} \cdot R_{ESR} \quad (7)$$

An MLCC capacitor with twice the value of the calculated minimum should be used due to DC bias effects. This is required to maintain control loop stability. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients but the total effective output capacitance value should not exceed ca. 30 µF.

DC bias effect: high cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the effective capacitance of the device. Therefore, the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and effective capacitance. For instance, a 10-µF X5R 6.3-V 0603 MLCC capacitor would typically show an effective capacitance of less than 4 µF under 5 V bias condition.

9.2.2.4 Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter since they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 4.7-µF input capacitor is sufficient for most applications, larger values can be used to reduce input current ripple without limitations.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

9.2.2.5 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

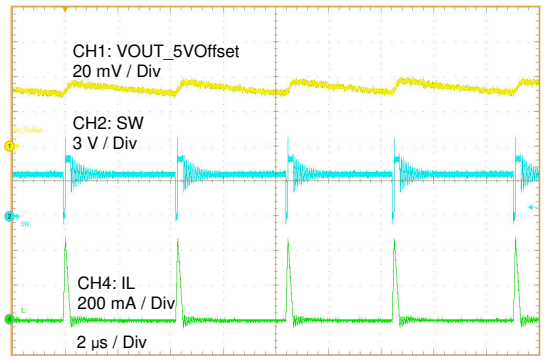
These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the oscillation happens for the output voltage or inductor current, the regulation loop can be unstable. This is often a result of board layout, L-C combination, or both.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the high-side FET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ × ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error

signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

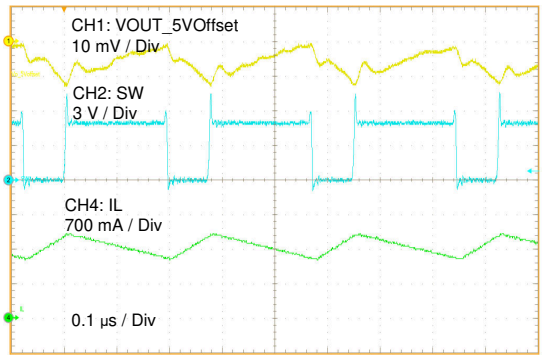
During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing that helps judge the stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependent, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

9.2.2.6 Application Curves



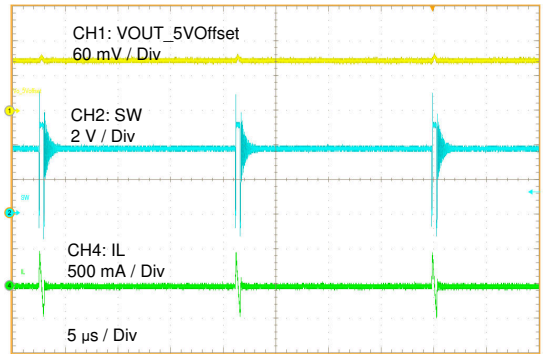
V_{IN} = 3.6 V V_{OUT} = 5 A L = 0.56 µH
C_{OUT} = 10 µF + 2x 4.7 µF Load = 10 mA Auto PFM

图 9-2. Steady 10 mA



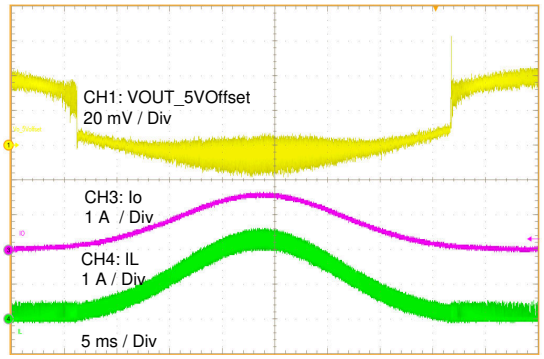
V_{IN} = 3.6 V V_{OUT} = 5 A L = 0.56 µH
C_{OUT} = 10 µF + 2x 4.7 µF Load = 1000 mA Auto PFM

图 9-3. Steady 1000 mA



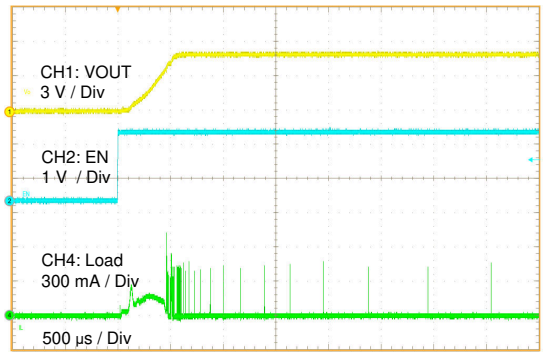
V_{IN} = 3.6 V V_{OUT} = 5 A L = 0.56 µH
C_{OUT} = 10 µF + 2x 4.7 µF Load = 0 mA Auto PFM

图 9-4. Steady Ultrasonic Mode



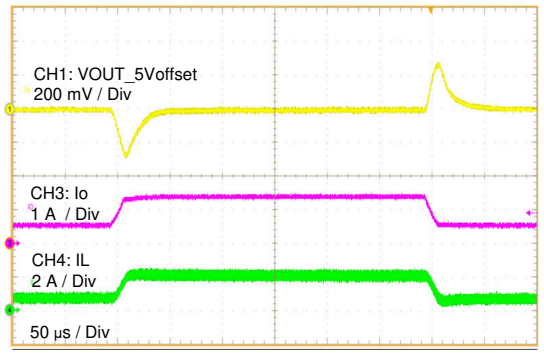
V_{IN} = 3.6 V V_{OUT} = 5 A L = 0.56 µH
C_{OUT} = 10 µF + 2x 4.7 µF Auto PFM

图 9-5. Load Sweep



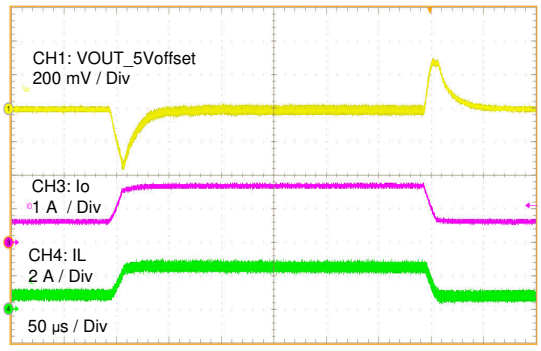
V_{IN} = 3.6 V V_{OUT} = 5 A L = 0.56 µH
C_{OUT} = 10 µF + 2x 4.7 µF Load = 0 mA Auto PFM

图 9-6. Start-up by EN



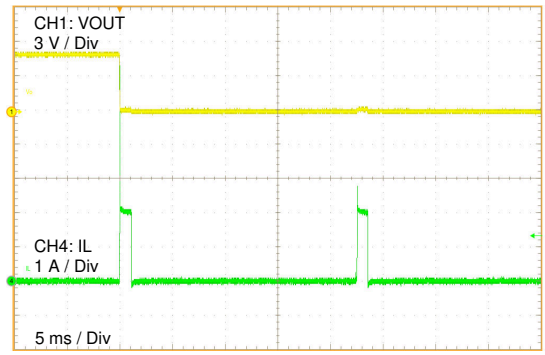
V_{IN} = 3.6 V V_{OUT} = 5 V L = 0.56 µH
C_{OUT} = 10 µF + 2x4.7 µF Load = 0.5 A to 1 A, 20 µs/A Auto PFM

图 9-7. Load Transient



V_{IN} = 3.6 V
C_{OUT} = 10 µF
V_{OUT} = 5 V
Load = 0.5 A to 1 A,
20 µs/A
L = 0.56 µH
Auto PFM

图 9-8. Load Transient with 10 µF C_{OUT}



V_{IN} = 3.6 V
C_{OUT} = 10 µF +
2x4.7 µF
V_{OUT} = 5 V
Auto PFM
L = 0.56 µH

图 9-9. Short Output

9.2.3 System Examples

For the < 1000 mA output current application, the output capacitors could be less. 图 9-10 shows the typical application circuit for the lower current applications.

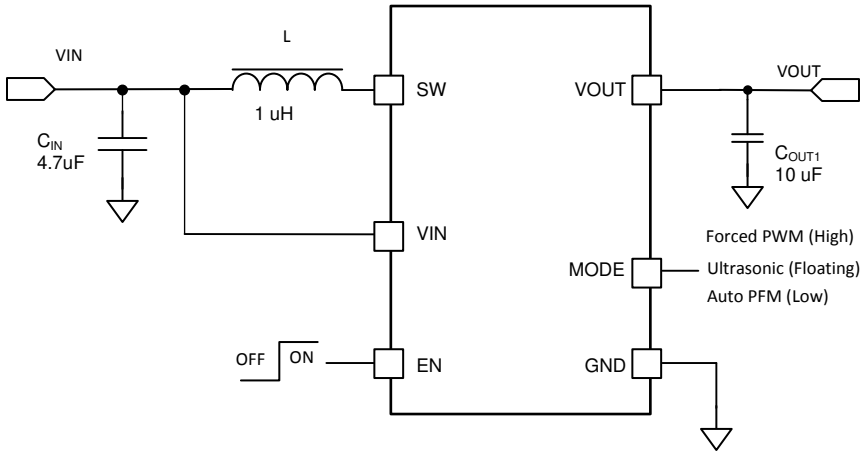


图 9-10. Typical Application with Minimum Output Capacitance

Power Supply Recommendations

The power supply can be three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. The input supply should be well regulated with the rating of TPS6125xA. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pins of the IC.

10.2 Layout Example

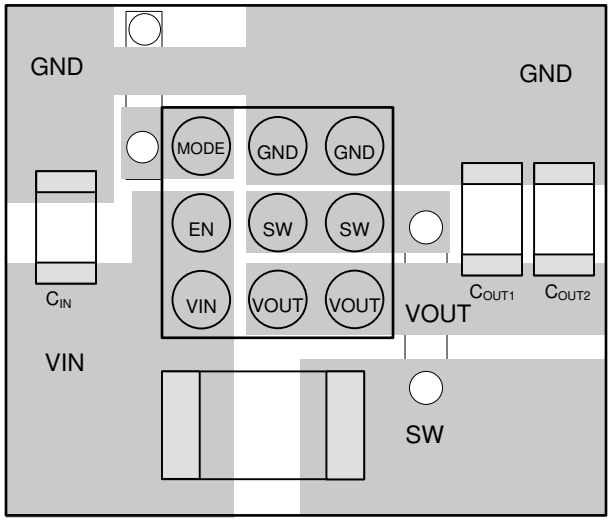


图 10-1. Recommended Layout

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

The following are three basic approaches for enhancing thermal performance:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

As power demand in portable designs is more and more important, designers must figure the best trade-off between efficiency, power dissipation and solution size. Due to integration and miniaturization, junction temperature can increase significantly which could lead to bad application behaviors (that is, premature thermal shutdown or worst case reduce device reliability).

Junction-to-ambient thermal resistance is highly dependent on application and board-layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The device operating junction temperature (T_J) should be kept below 125°C.

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61253A device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

TPS61253AEVM-803 User's Guide, SLVUAP5

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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11.6 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS612532AYFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	2CHI	Samples
TPS61253AYFFR	ACTIVE	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17NI	Samples
TPS61253AYFFT	ACTIVE	DSBGA	YFF	9	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	17NI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

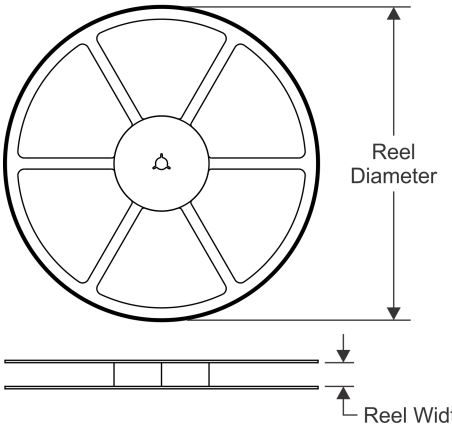
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

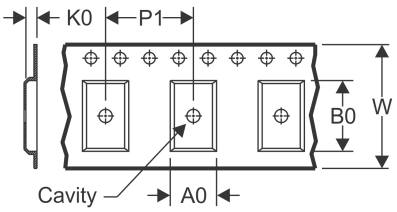
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

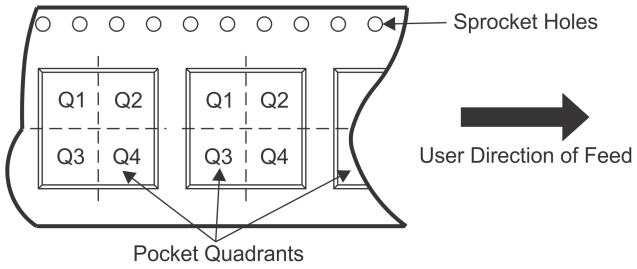


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

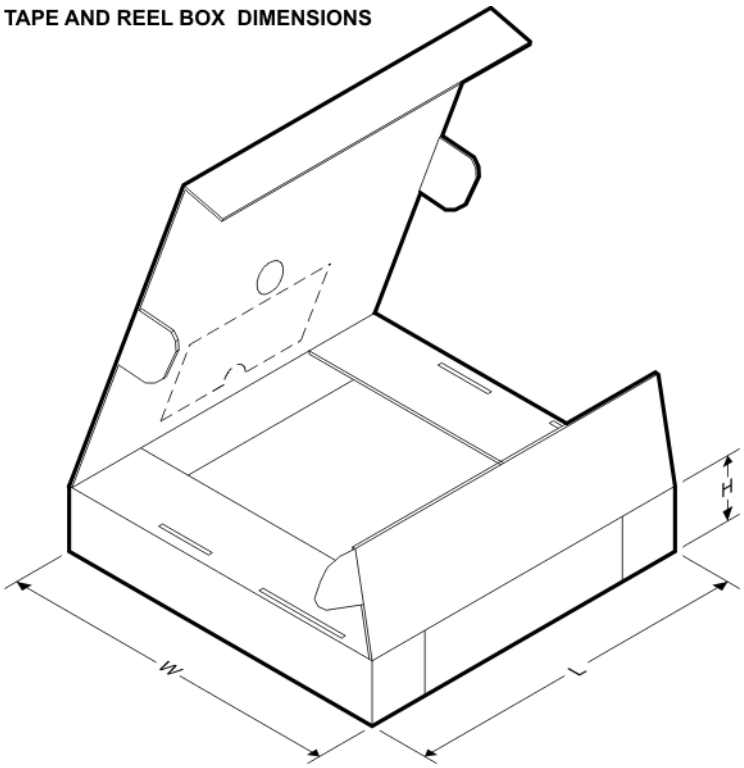
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS612532AYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.31	1.41	0.69	4.0	8.0	Q1
TPS61253AYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.31	1.41	0.69	4.0	8.0	Q1
TPS61253AYFFT	DSBGA	YFF	9	250	180.0	8.4	1.31	1.41	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

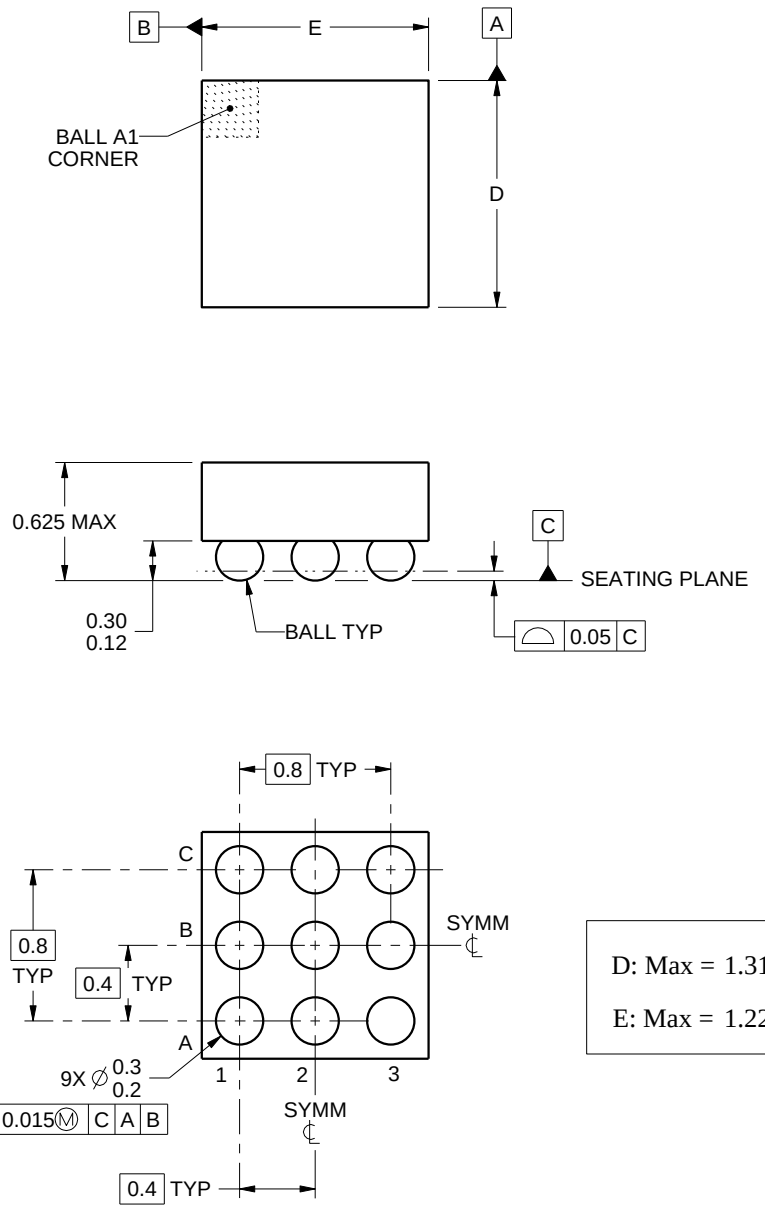
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS612532AYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61253AYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61253AYFFT	DSBGA	YFF	9	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.318 mm, Min =1.258 mm

E: Max = 1.222 mm, Min =1.162 mm

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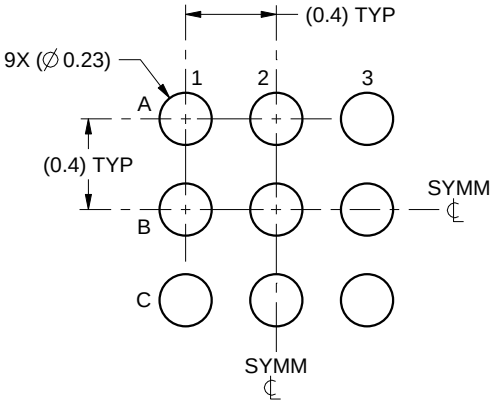
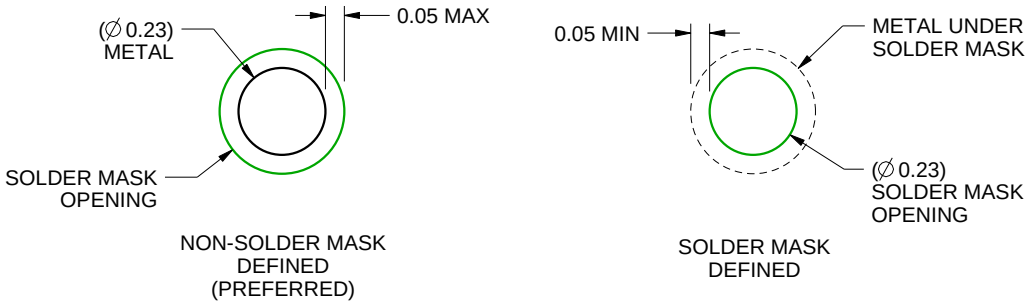
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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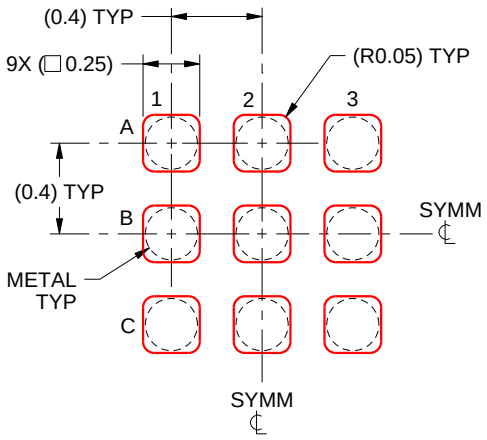
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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