TPS54325-Q1 具有集成 FET 的 4.5V 至 18V 3A 输出同步 SWIFT 降压开关

1 特性

- 符合汽车应用要求
- D-CAP2™ 模式支持快速瞬态响应
- 低输出纹波且支持陶瓷输出电容器
- 4.5V 至 18V 宽 V_{CC} 输入电压范围
- 2.0V 至 18V 宽 V_{IN} 输入电压范围
- 0.76V 至 5.5V 输出电压范围
- 高效率集成型 FET
  针对较低占空比应用进行了优化
  - 120mΩ（高侧）和 70mΩ（低侧）
- 高效率，关断时流耗少于 10 μA
- 高初始带隙基准精度
- 可调软启动
- 预偏置软启动
- 700kHz 开关频率 (f_{SW})
- 逐周期过流限制
- 电源正常状态输出
- 使用 TPS54325-Q1 并借助 WEBENCH® Power Designer 创建定制设计

2 应用

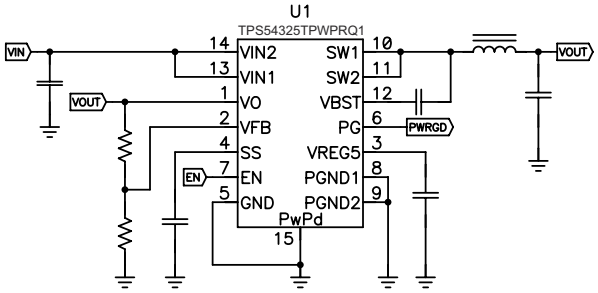
- 低电压系统的广泛应用
  - 数字电视电源
  - 高清 Blue-ray Disc™ 播放器
  - 网络家庭终端设备
  - 数字机顶盒 (STB)

3 说明

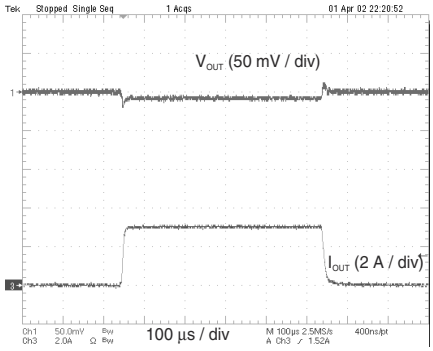
TPS54325-Q1 是一款自适应接通时间 D-CAP2 模式同步降压转换器。TPS54325-Q1 可帮助系统设计人员通过低成本、低元件数量的低待机电流解决方案，为各种终端设备设计电源总线稳压器。TPS54325-Q1 的主控制环路采用 D-CAP2 模式控制，无需外部元件即可实现极快的瞬态响应。TPS54325-Q1 的专有电路还可使其适应低等效串联电阻 (ESR) 输出电容器（如 POSCAP 或 SP-CAP）和超低 ESR 陶瓷电容器。该器件采用 4.5V 至 18V VCC 以及 2.0V 至 18V V_{IN} 输入电源电压。可以在 0.76V 和 5.5V 之间对输出电压进行编程。该器件还具有可调缓慢启动时间和电源正常功能。TPS54325-Q1 采用 14 引脚 HTSSOP 封装，工作温度为 -40°C 至 105°C。

器件信息

器件型号	封装	封装尺寸（标称值）
TPS54325-Q1	HTSSOP	5.00mm × 4.40mm



简化版原理图



负载瞬态响应

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (June 2011) to Revision A (July 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式。	1
• 添加了 *ESD 额定值、引脚配置和功能、详细说明、功能方框图、特性说明、器件功能模式、应用和实现、应用信息、典型应用、设计要求、详细设计过程、应用曲线、电源相关建议、布局、布局指南、布局示例、器件和文档支持以及机械、封装和可订购信息*	1
• Corrected thermal information	5

5 Pin Configuration and Functions

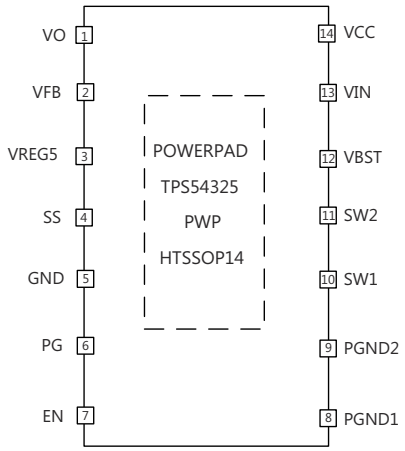


图 5-1. 14-Pin PWP HTSSOP Pinout

表 5-1. Pin Functions

Pin		Description
Name	NO.	
VO	1	Connect this pin to the output of the converter. This pin is used for on-time adjustment.
VFB	2	Converter feedback input. Connect this pin with a feedback resistor divider.
VREG5	3	5.5-V power supply output. Connect a capacitor (typically 1 μF) to GND.
SS	4	Soft-start control. Connect an external capacitor to GND.
GND	5	Signal ground pin
PG	6	Open-drain power-good output
EN	7	Enable control input
PGND1, PGND2	8, 9	Ground returns for low-side MOSFET. These ground returns also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC.
SW1, SW2	10, 11	Switch node connections between the high-side NFET and low-side NFET. These connections also serve as inputs to current comparators.
VBST	12	Supply input for high-side NFET gate driver (boost terminal). Connect a capacitor from this pin to respective SW1 and SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin.
VIN	13	Power input and connected to high-side NFET drain
VCC	14	Supply input for the 5-V internal linear regulator for the control circuitry
PowerPAD	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Connect to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage range	V_{IN}, V_{CC}, EN	–0.3	20	V
		V_{BST}	–0.3	26	
		V_{BST} (vs SW1, SW2)	–0.3	6.5	
		V_{FB}, V_O, SS, PG	–0.3	6.5	
		SW1, SW2	–2	20	
		SW1, SW2 (10-ns transient)	–3	20	
V_O	Output voltage range	V_{REG5}	–0.3	6.5	V
		P_{GND1}, P_{GND2}	–0.3	0.3	
V_{diff}	Voltage from GND to POWERPAD		–0.2	0.2	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under the absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the recommended operating conditions is not implied. Exposure to absolute maximum rated condition for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range, VCC, V_{IN} = 12 V (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply input voltage range		4.5	18	V
V_{IN}	Power input voltage range		2	18	V
V_I	Input voltage range	V_{BST}	–0.1	24	V
		V_{BST}, (vs SW1, SW2)	–0.1	6	
		SS, PG	–0.1	6	
		EN	–0.1	18	
		V_O, V_{FB}	–0.1	5.5	
		SW1, SW2	–1.8	18	
		SW1, SW2 (10-ns transient)	–3	18	
		P_{GND1}, P_{GND2}	–0.1	0.1	
V_O	Output voltage range	V_{REG5}	–0.1	6	V
I_O	Output current range	I_{VREG5}	0	10	mA
T_A	Operating free-air temperature		–40	105	°C
T_J	Operating junction temperature		–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		PWP	UNIT
		14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VCC}	Operating – nonswitching supply current	V_{CC} current, T_A = 25°C, EN = 5 V, V_{FB} = 0.8 V		850	1300	µA
I_{CCSDN}	Shutdown supply current	V_{CC} current, T_A = 25°C, EN = 0 V			10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	2			V
V_{ENL}	EN low-level input voltage	EN			0.4	V
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V	757	765	775	mV
		T_A = 0°C to 105°C, V_O = 1.05 V	753		777	
		T_A = –40°C to 105°C, V_O = 1.05 V	750		780	
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V, T_A = 25°C		0	±0.1	µA
R_{Dischg}	V_O discharge resistance	EN = 0 V, V_O = 0.5 V, T_A = 25°C		50	100	Ω
V_{REG5} OUTPUT						
V_{VREG5}	V_{REG5} output voltage	T_A = 25°C, 6.0 V < V_{CC} < 18 V, 0 < I_{VREG5} < 5 mA	5.3	5.5	5.7	V
V_{LN5}	Line regulation	6.0 V < V_{CC} < 18 V, I_{VREG5} = 5 mA			20	mV
V_{LD5}	Load regulation	0 mA < I_{VREG5} < 5 mA			100	mV
I_{REG5}	Output current	V_{CC} = 6 V, V_{REG5} = 4.0 V, T_A = 25°C		70		mA
MOSFET						
R_{dsonh}	High-side switch resistance	25°C, V_{BST} – SW1, SW2 = 5.5 V		120		mΩ
R_{dsonl}	Low-side switch resistance	25°C		70		mΩ
CURRENT LIMIT						
I_{ocl}	Current limit	T_A = 25°C to 105°C	3.5	4.1		A
		T_A = –40°C	3.25	3.5		
THERMAL SHUTDOWN						
t_{SDN}	Thermal shutdown threshold	Shutdown temperature		150		°C
		Hysteresis		25		
ON-TIME TIMER CONTROL						
t_{ON}	On time	V_{IN} = 12 V, V_O = 1.05 V		145		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.7 V		260		ns
SOFT START						

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SSC}	SS charge current	V_{SS} = 0 V	1.4	2.0	2.6	µA
I_{SSD}	SS discharge current	V_{SS} = 0.5 V	0.1	0.2		mA
POWER GOOD						
V_{THPG}	PG threshold	V_{FB} rising (good)	85%	90%	95%	
		V_{FB} falling (fault)		85%		
I_{PG}	PG sink current	PG = 0.5 V	2.5	5		mA
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	115%	120%	125%	
T_{OVPDEL}	Output OVP prop delay			5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65%	70%	75%	
		Hysteresis		10%		
t_{UVPDEL}	Output UVP delay			0.25		ms
t_{UVPEN}	Output OVP enable delay	Relative to soft-start time		× 1.7		
UVLO						
V_{UVLO}	UVLO threshold	Wake-up V_{REG5} voltage	3.45	3.70	3.95	V
		Hysteresis V_{REG5} voltage	0.15	0.25	0.35	

6.6 Typical Characteristics

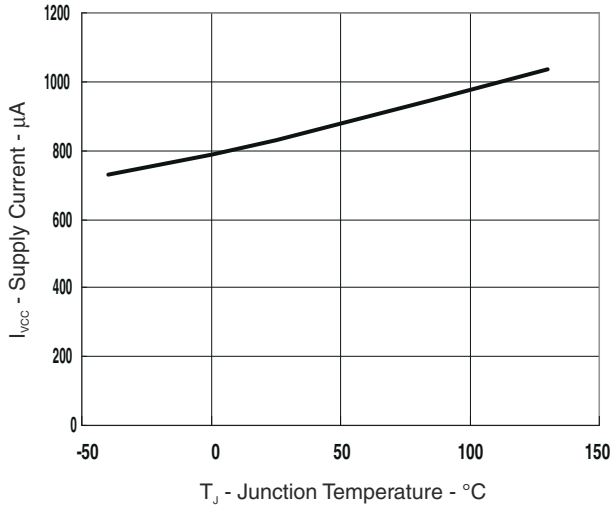


图 6-1. V_{CC} Temperature vs Junction Temperature

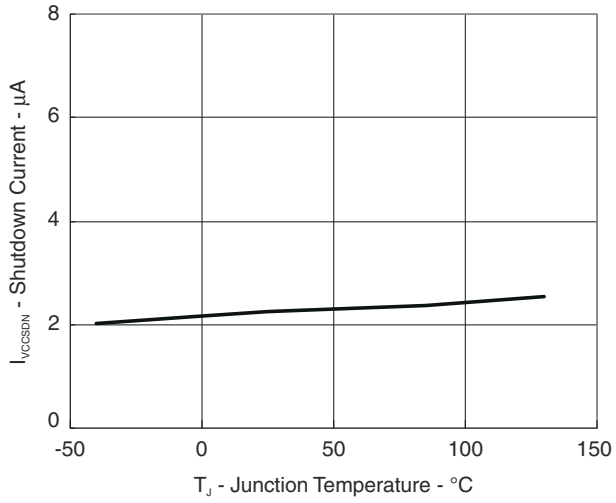


图 6-2. V_{CC} Shutdown Current vs Junction Temperature

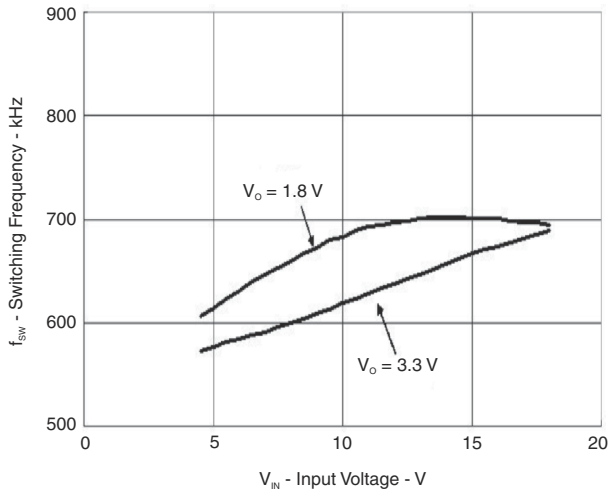


图 6-3. Switching Frequency vs Input Voltage (I_O = 1 A)

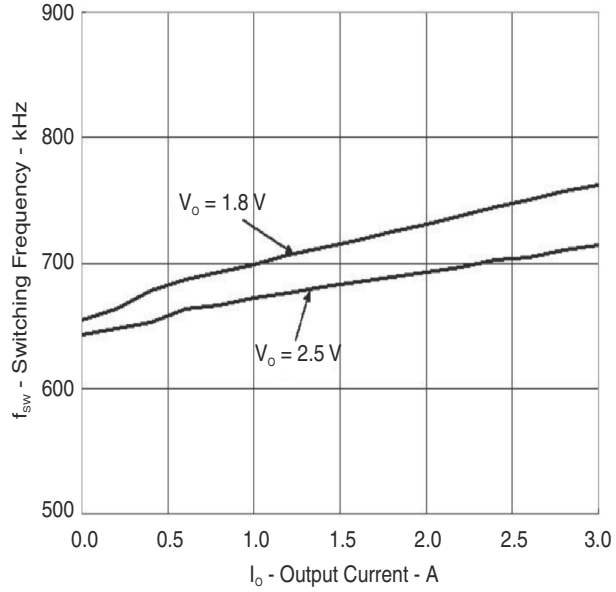


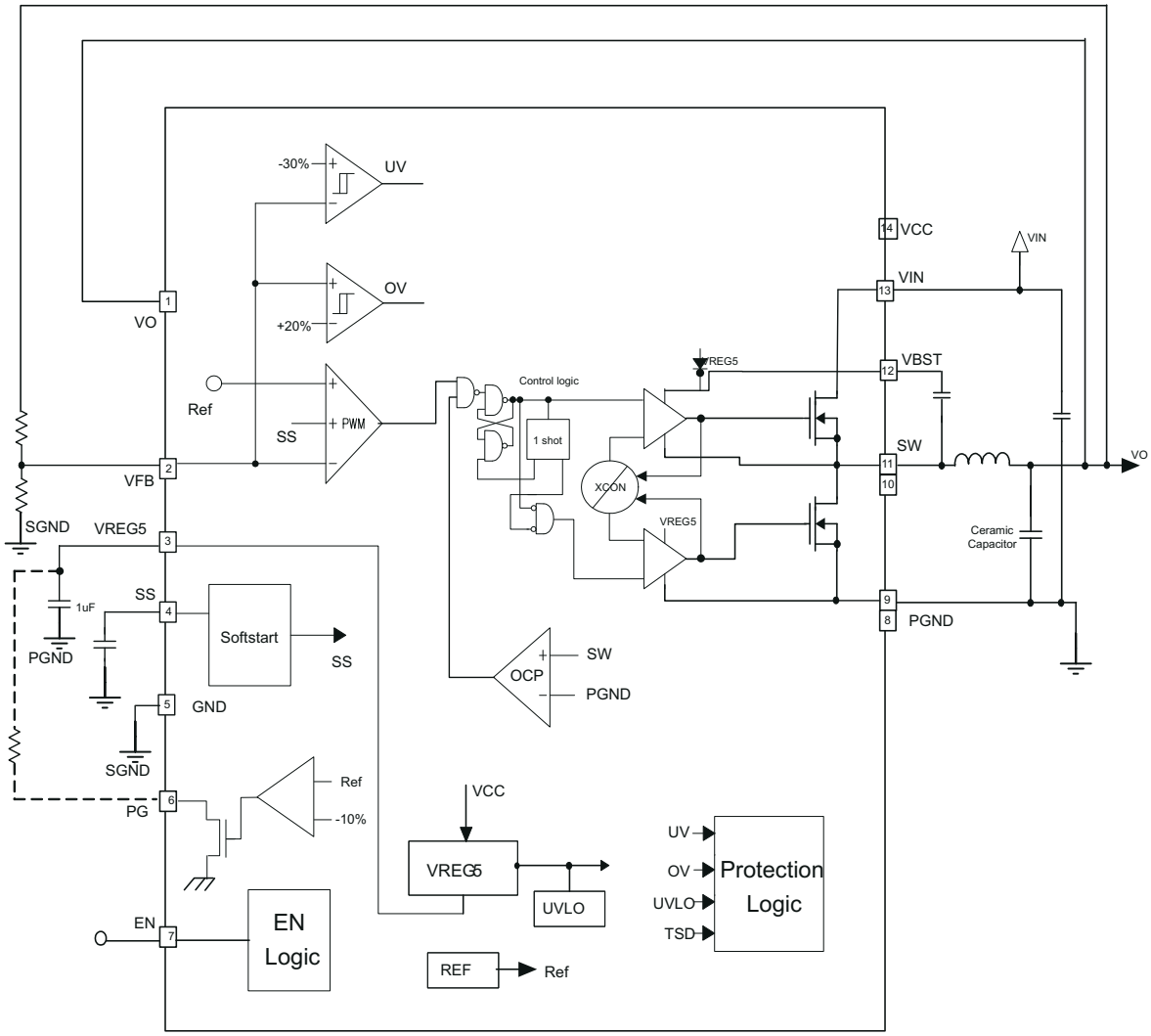
图 6-4. Switching Frequency vs Output Current

7 Detailed Description

7.1 Overview

The TPS54325-Q1 is a 3-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. The device operates using D-CAP2 mode control. The fast transient response of D-CAP2 control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low-ESR output capacitors including ceramic and special polymer types.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start and Pre-Biased Soft Start

The TPS54325-Q1 has an adjustable soft start. When the EN pin becomes high, 2.0-μA current begins charging the capacitor, which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start-up. Use the following equation to find the slow-start time. VFB voltage is 0.765 V and SS pin source current is 2 μA.

$$T_{SS}(ms) = \frac{C6(nF) \times V_{REF}}{I_{SS}(\mu A)} = \frac{C6(nF) \times 0.765}{2} \quad (1)$$

The TPS54325-Q1 contains a unique circuit to prevent current from being pulled from the output during start-up in the condition the output is prebiased. When the soft start commands a voltage higher than the prebias level (internal soft start becomes greater than feedback voltage (V_{FB})), the controller slowly activates synchronous rectification by starting the first low-side FET gate driver pulses with a narrow on time. The device then increments that on time on a cycle-by-cycle basis until it coincides with the time dictated by (1 – D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the prebias output, and ensures that the out voltage (V_O) starts and ramps up smoothly into regulation and the control loop is given time to transition from prebiased start-up to normal mode operation.

7.3.2 Power Good

The TPS54325-Q1 has a power-good output. The power-good function is activated after soft start has finished. If the output voltage becomes within –10% of the target value, internal comparators detect a power-good state and the power-good signal becomes high. During start-up, power good start after 1.7 times the soft-start time to avoid a glitch of power-good signal. If the feedback voltage goes under 15% of the target value, the power-good signal becomes low after a 10-μs internal delay.

7.3.3 Output Discharge Control

The TPS54325-Q1 discharges the output when EN is low or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). The device discharges outputs using an internal 50-Ω M,OSFET which is connected to VO and PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

7.3.4 Current Protection

The TPS54325-Q1 has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the off state and the controller keeps the off state when the inductor current is larger than the overcurrent trip level. In order to provide both good accuracy and cost effective solution, the device supports temperature compensated internal MOSFET $R_{DS(on)}$ sensing.

The inductor current is monitored by the voltage between PGND pin and SW1 and SW2 pins. In an overcurrent condition, the current to the load exceeds the current to the output capacitor, thus the output voltage tends to fall off. Eventually, the output voltage ends up crossing the undervoltage protection threshold and shutdown.

7.3.5 Overvoltage and Undervoltage Protection

The TPS54325-Q1 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 μs, the device latches off both internal top and bottom MOSFET. This function is enabled approximately 1.7 × soft-start time.

7.3.6 UVLO Protection

The TPS54325-Q1 has undervoltage lockout protection (UVLO) that monitors the voltage of VREG5 pin. When the VREG5 voltage is lower than UVLO threshold voltage, the TPS54325-Q1 is shut off. This is non-latch protection.

7.3.7 Thermal Shutdown

The TPS54325-Q1 monitors the temperature of itself. If the temperature exceeds the threshold value (typically 150°C), the device is shut off. This is non-latch protection.

7.4 Device Functional Modes

7.4.1 PWM Operation

The main control loop of the TPS54325-Q1 is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. D-CAP2 mode control combines constant on-time control with an

internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. This mode is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal the one shot timer expires. This one shot timer is set by the converter input voltage ,V_{IN}, and the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR-induced output ripple from D-CAP2 mode control.

7.4.2 PWM Frequency and Adaptive On-Time Control

The TPS54325-Q1 uses an adaptive on-time control scheme and does not have a dedicated on-board oscillator. The TPS54325-Q1 runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on time is inversely proportional to the input voltage and proportional to the output voltage, therefore, when the duty ratio is V_{OUT} / V_{IN}, the frequency is constant

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS54325-Q1 device is typically used as a step-down converter, which converts a voltage in the range of 4.5 V to 18 V to a lower voltage. WEBENCH software is available to aid in the design and analysis of circuits

8.2 Typical Application

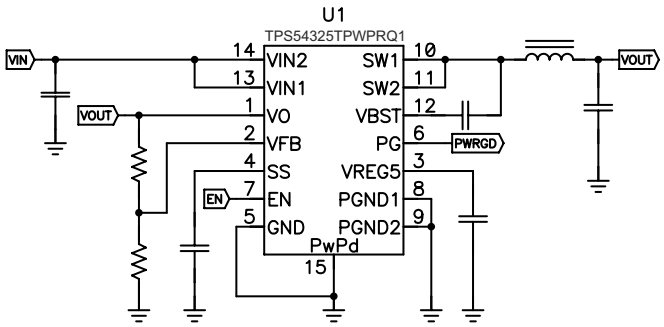


图 8-1. Schematic Diagram for Design Example

8.2.1 Design Requirements

表 8-1. Design Parameters

Parameter	Conditions	MIN	TYP	MAX	Unit
Input voltage		5			V
Output voltage			1.05		V
Operating frequency	V_I = 12 V, I_O = 1 A		700		kHz
Output current		0		3	A
Output ripple voltage	V_I = 12 V, I_O = 3 A		9		mVpp
Efficiency	V_I = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 1.2 A		91%		

8.2.2 Detailed Design Procedure

To begin the design process, define these parameters for the application:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54325-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Inductor Selection

The inductance value is selected to provide approximately 30% peak-to-peak ripple current at maximum load. Larger ripple current increases output ripple voltage, improves S/N ratio, and contributes to stable operation. Smaller ripple currents result in lower output voltage ripple. When using low-ESR output capacitors, output ripple voltage is usually low, so larger ripple currents are acceptable. The coefficient Kind represents the percentage of ripple current. The value of Kind must not be greater than 0.4. Use 0.3 when using low-ESR output capacitors. 方程式 2 can be used to calculate L1. Use 700 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 方程式 4 and the RMS current of 方程式 5.

$$L_O = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{I_{OUT} \times f_{SW} \times Kind} \tag{2}$$

$$Ilp - p = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{3}$$

$$I_{lpeak} = I_O + \frac{Ilp - p}{2} \tag{4}$$

$$I_{Lo(RMS)} = \sqrt{I_0^2 + \frac{1}{12} Ilp - p^2} \tag{5}$$

8.2.2.3 Output Capacitor Selection

The capacitor value and ESR determines the amount of output voltage ripple. TI recommends using ceramic output capacitor. Using the following equations, an initial estimate for the capacitor value, ESR, and RMS current can be calculated. If the load transients are significant, consider using the load step, instead of ripple current to calculate the maximum ESR. Minimum C_O must be over 20 μF.

$$C_O > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{O(ripple)}}{I_{ripple}} - R_{ESR}\right)} \tag{6}$$

$$R_{ESR} < \frac{V_{O(ripple)}}{I_{l(ripple)}} \tag{7}$$

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{8}$$

8.2.2.4 Input Capacitor Selection

The TPS54325-Q1 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage. In case of separate VCC and VIN, then a ceramic capacitor over 10 μF is recommended for the VIN and also placing ceramic capacitor over 0.1 μF for the VCC is recommended.

8.2.2.5 Bootstrap Capacitor Selection

A 0.1-μF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends using a ceramic capacitor.

8.2.2.6 VREG5 Capacitor Selection

A 1-μF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. TI recommends using a ceramic capacitor.

8.2.2.7 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends using 1% tolerance or better divider resistors. Start by using the following equations to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance is more susceptible to noise and voltage errors from the VFB input current is more noticeable

For output voltage from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad (9)$$

For output voltage over 2.5 V:

$$V_{OUT} = (0.763 + 0.0017 \times V_{OUT}) \times \left(1 + \frac{R1}{R2}\right) \quad (10)$$

8.2.3 Application Performance Plots

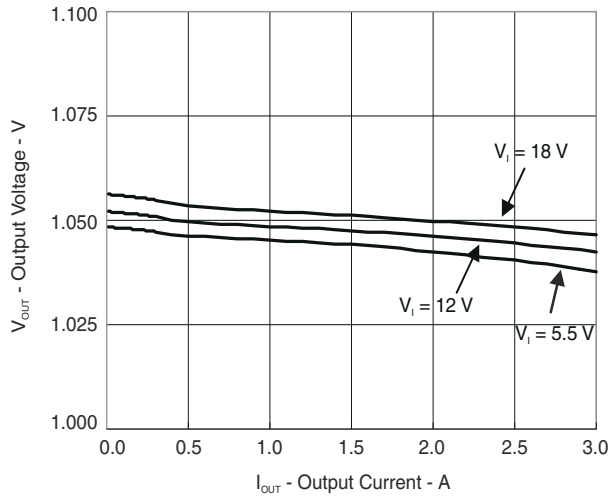


图 8-2. 1.05-V Output Voltage vs Output Current

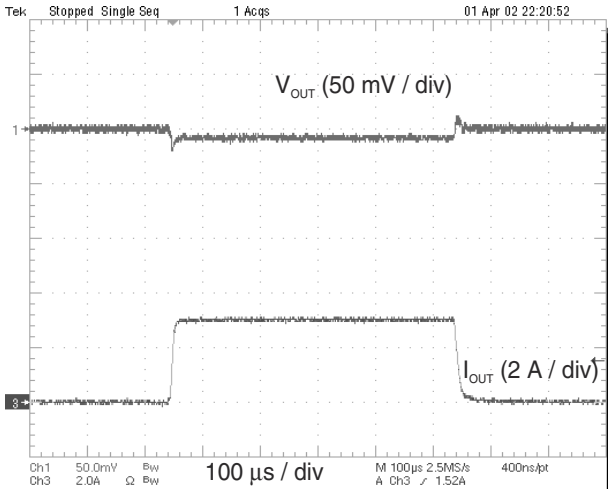


图 8-3. 1.05-V, 0-A to 3-A Load Transient Response

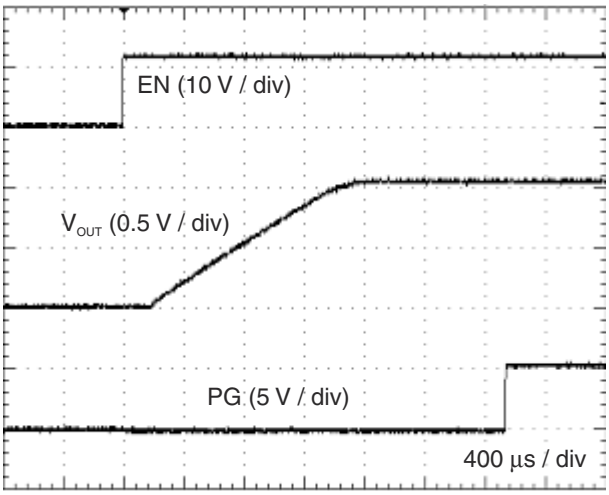


图 8-4. Start-Up Waveform

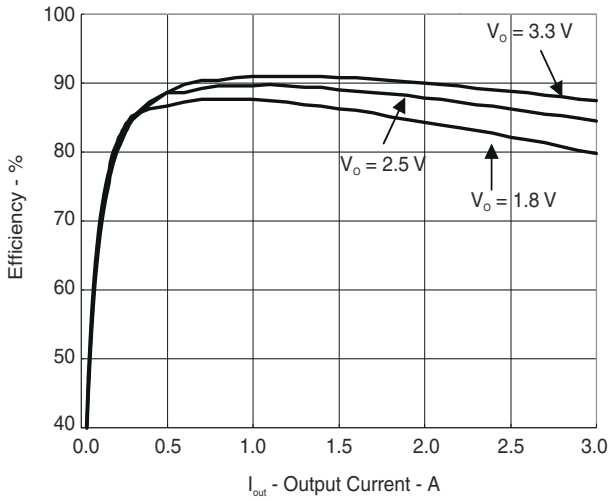


图 8-5. Efficiency vs Output Current (V_{IN} = 12 V)

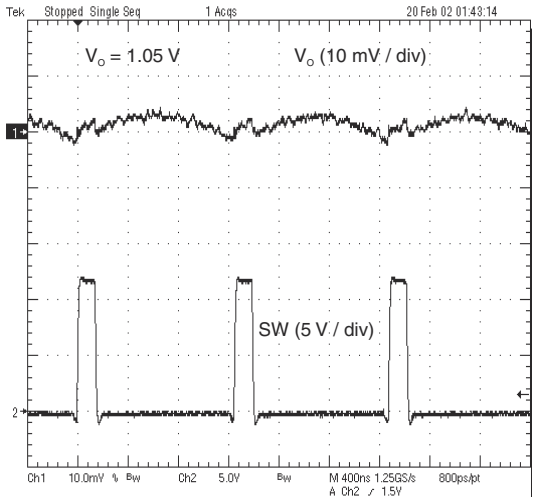


图 8-6. Voltage Ripple at Output

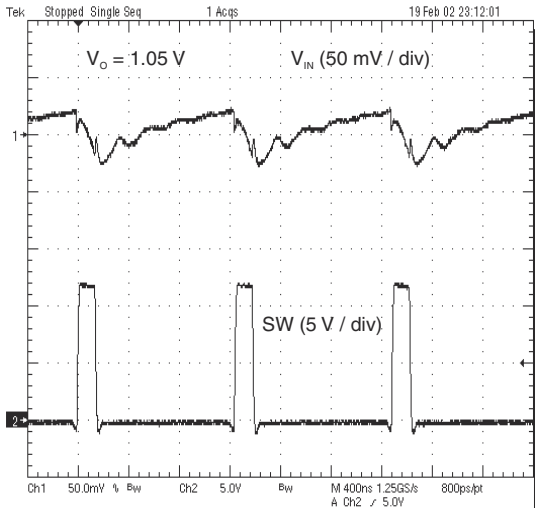


图 8-7. Voltage Ripple at Input

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 4.5 V and 18 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 μF is a typical choice.

10 Layout

10.1 Layout Guidelines

- Keep the input switching current loop as small as possible.
- Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections must be brought from the output to the feedback pin of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.
- Do not allow switching current to flow under the device.
- Keep the pattern lines for VIN and PGND broad.
- Exposed pad of device must be connected to PGND with solder.
- VREG5 capacitor must be placed near the device and connected PGND.
- Output capacitor must be connected to a broad pattern of the PGND.
- Voltage feedback loop must be as short as possible, and preferably with ground shield.
- Lower resistor of the voltage divider, which is connected to the VFB pin must be tied to SGND.
- Providing sufficient via is preferable for VIN, SW, and PGND connection.
- PCB pattern for VIN, SW, and PGND must be as broad as possible.
- If VIN and VCC is shorted, VIN and VCC patterns need to be connected with broad pattern lines.
- Place the V_{IN} capacitor as close as possible to the device.

10.2 Layout Example

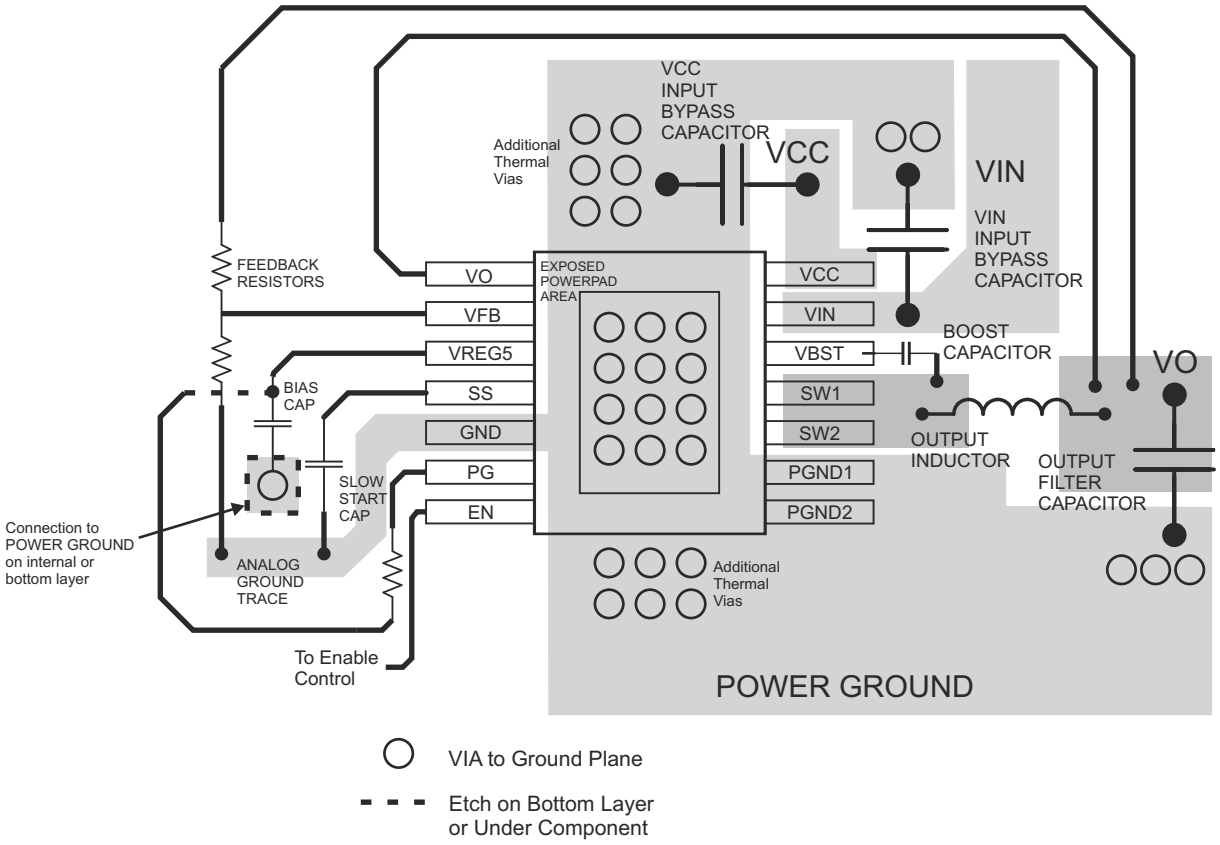


图 10-1. PCB Layout

10.3 Thermal Information

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be connected to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to the *PowerPAD™ Thermally Enhanced Package* and *PowerPAD Made Easy* application notes.

The exposed thermal pad dimensions for this package are shown in the following illustration.

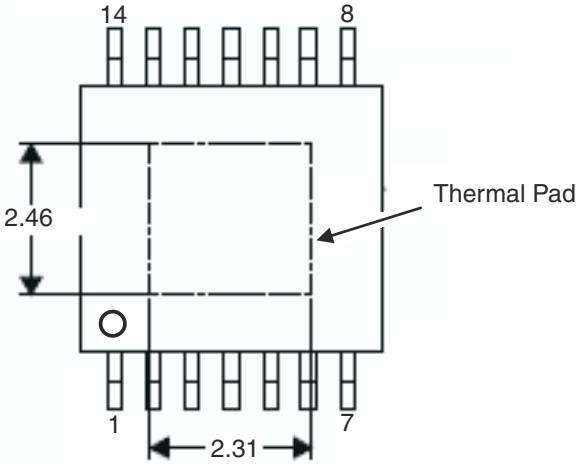


图 10-2. Thermal Pad Dimensions

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Device Support

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.1.2 Development Support

11.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54325-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get the information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.5 Trademarks

D-CAP2™ and TI E2E™ are trademarks of Texas Instruments.
Blue-ray Disc™ is a trademark of Blu-ray Disc.
WEBENCH® is a registered trademark of Texas Instruments.
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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54325TPWPRQ1	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	54325Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS54325-Q1 :

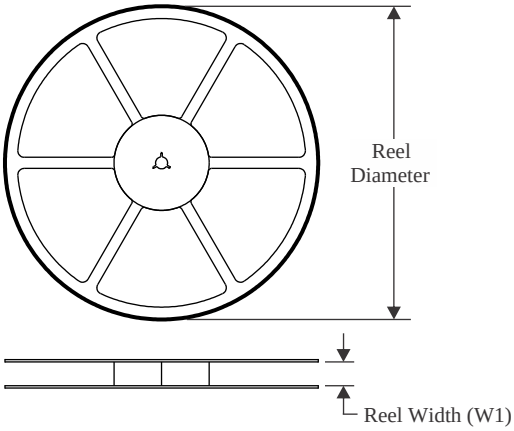
- Catalog : TPS54325

NOTE: Qualified Version Definitions:

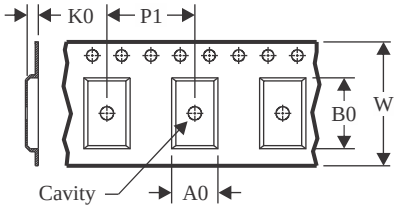
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

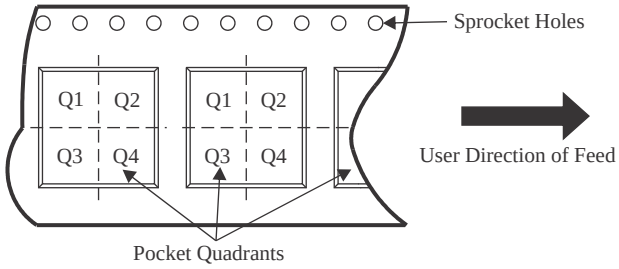


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

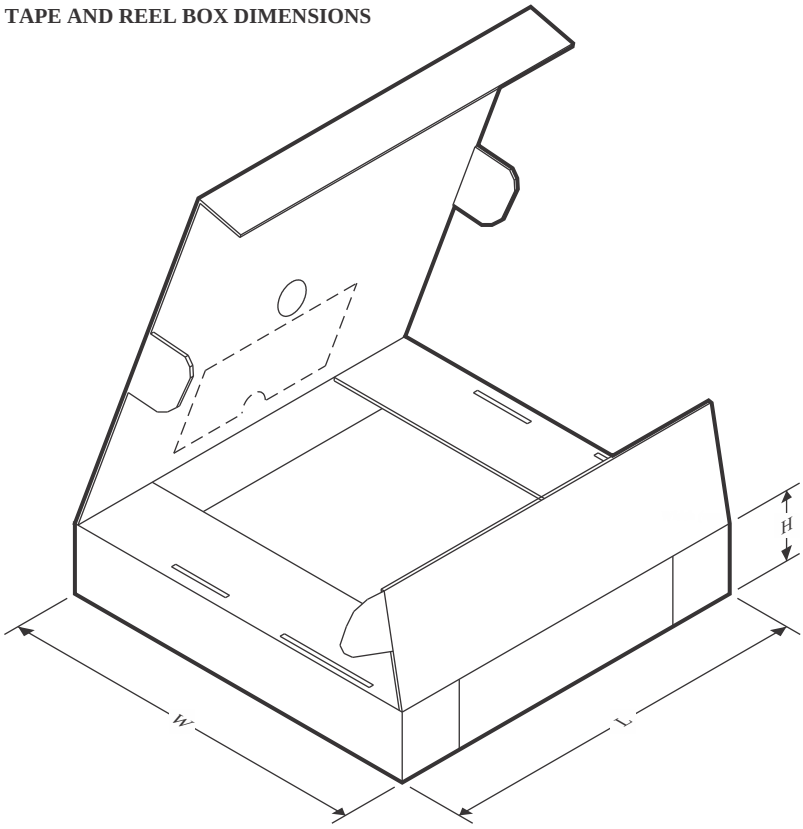
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54325TPWPRQ1	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54325TPWPRQ1	HTSSOP	PWP	14	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

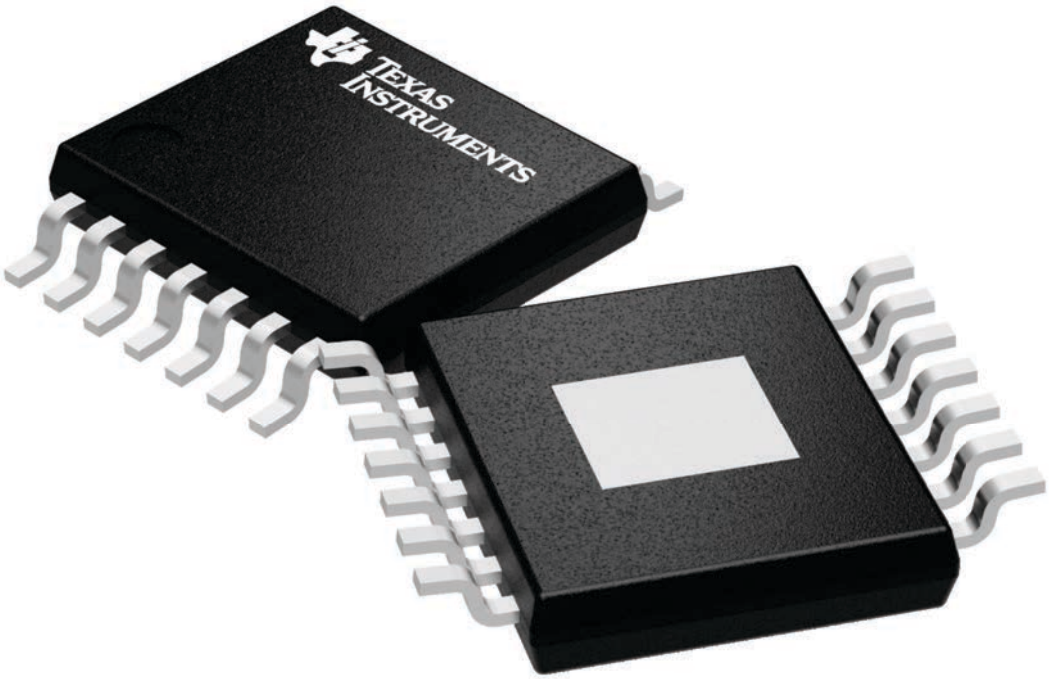
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

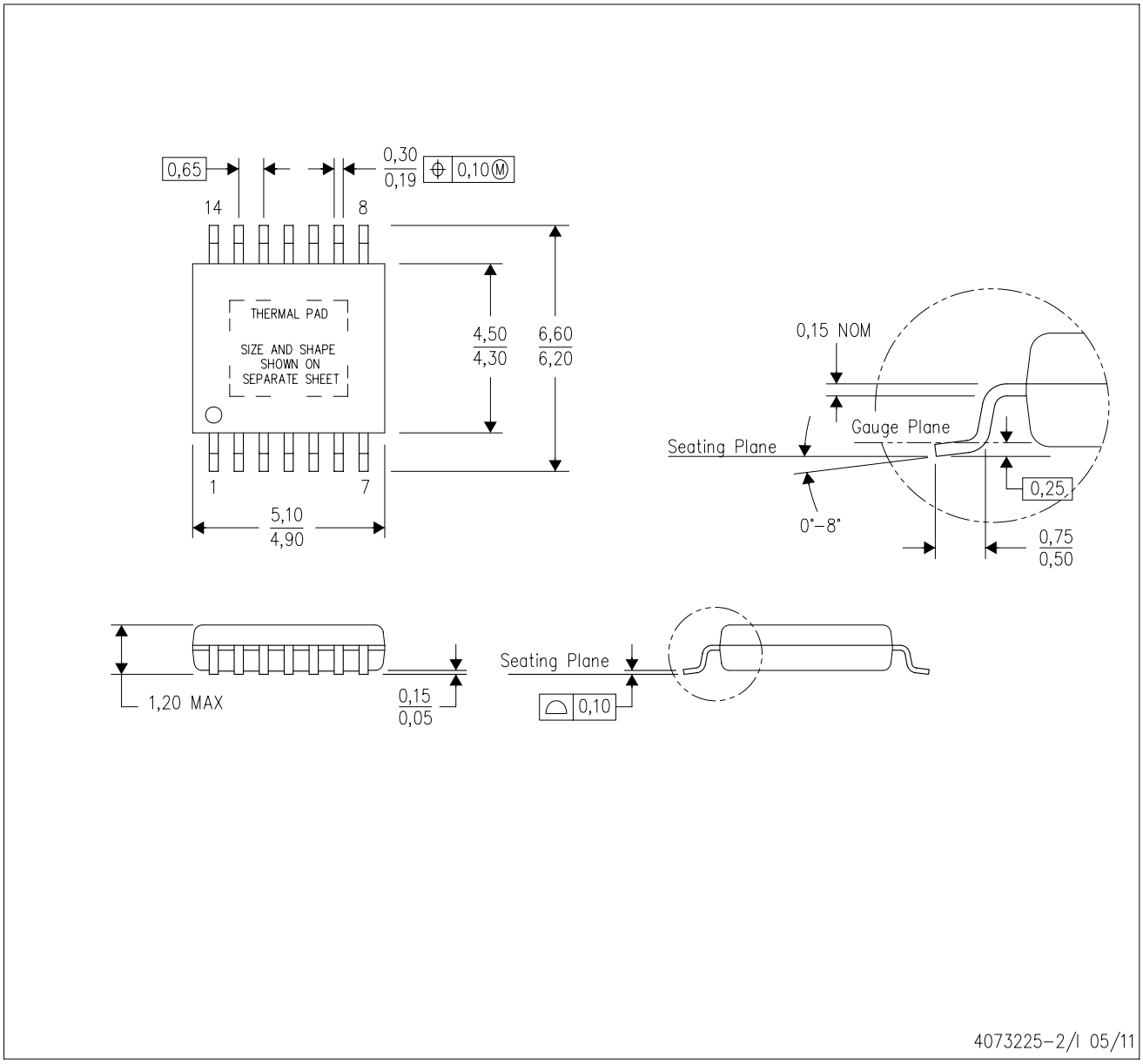
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224995/A

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

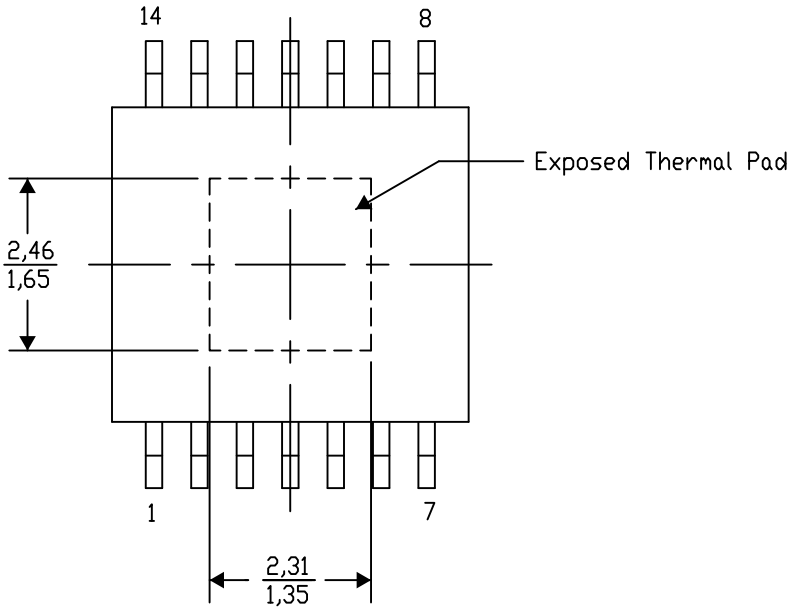
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

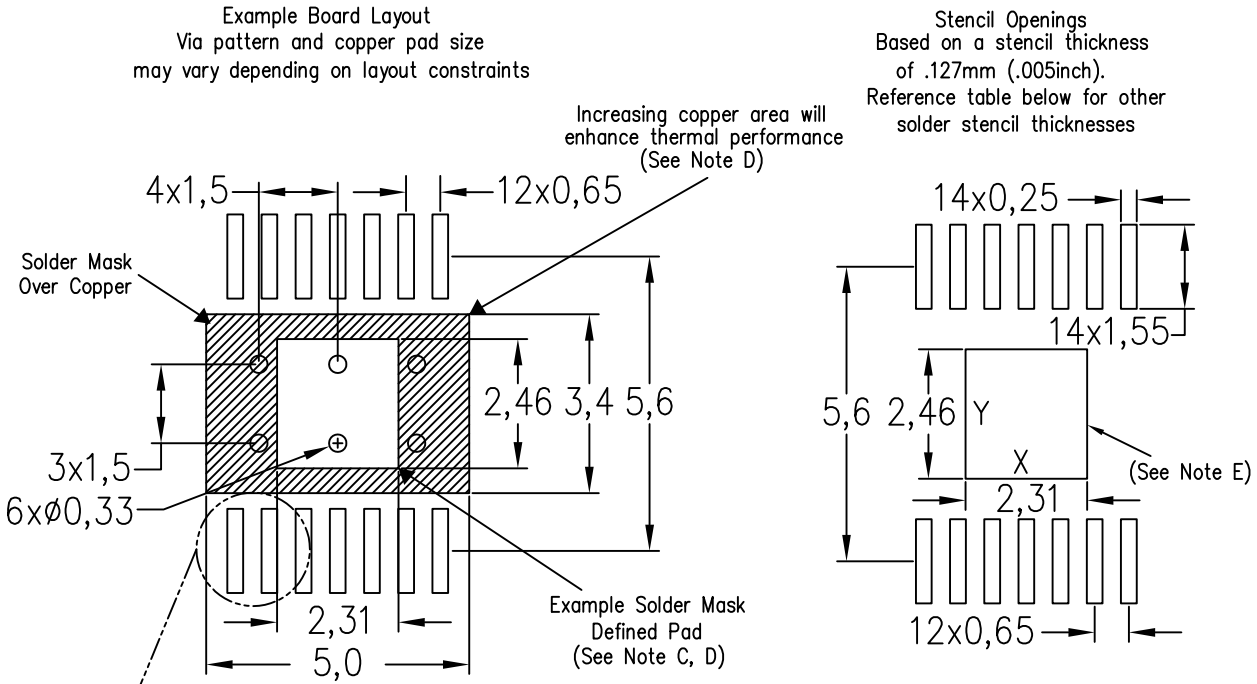
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE

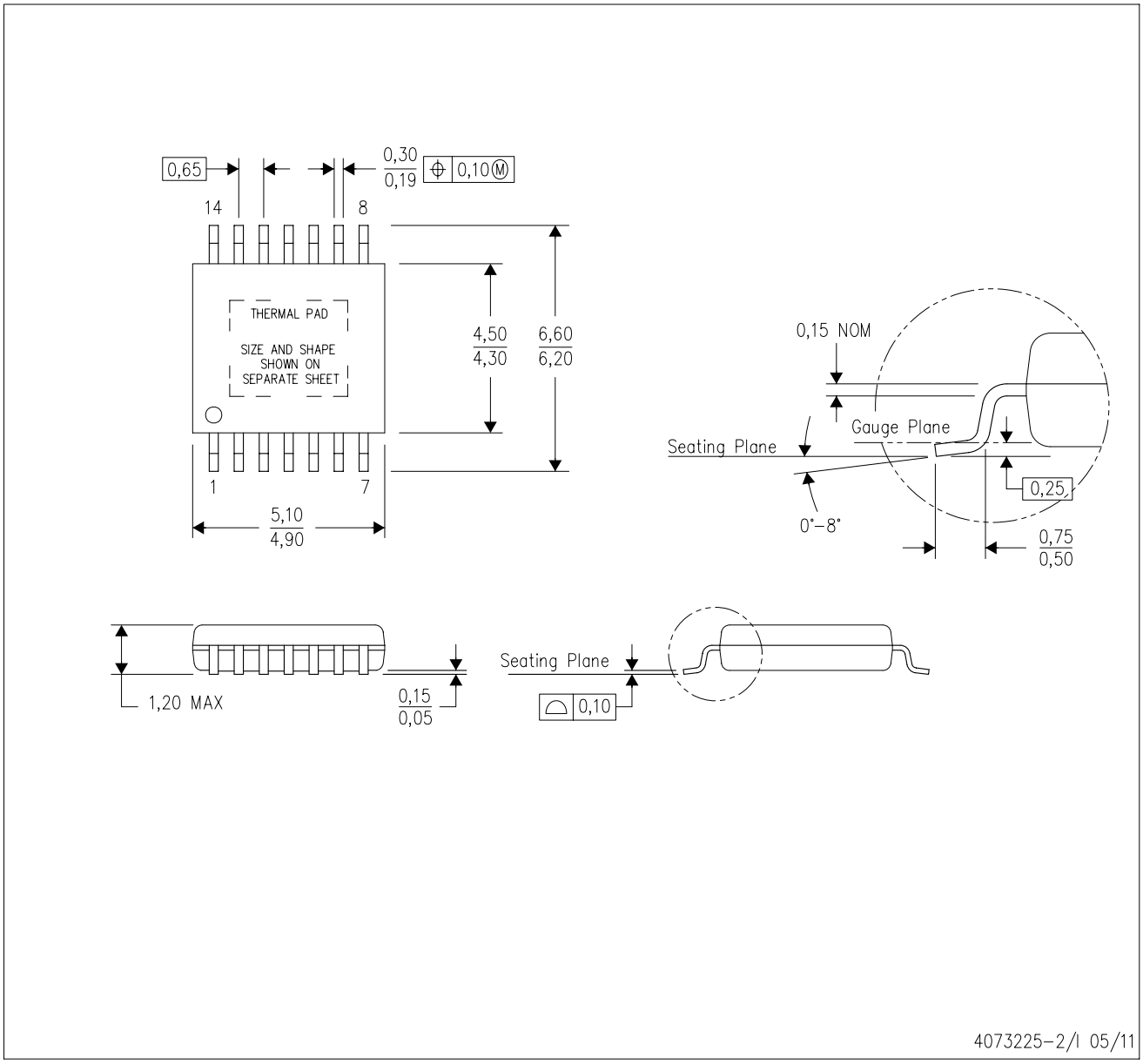


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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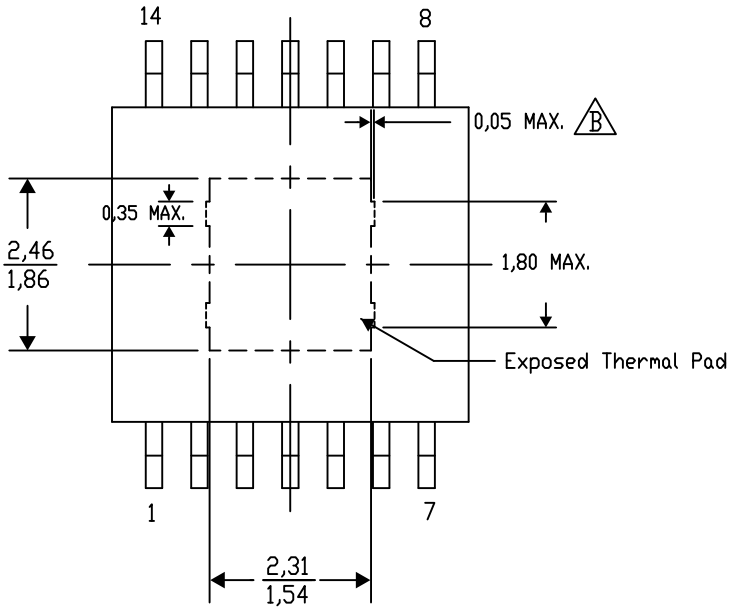


Top View

Exposed Thermal Pad Dimensions

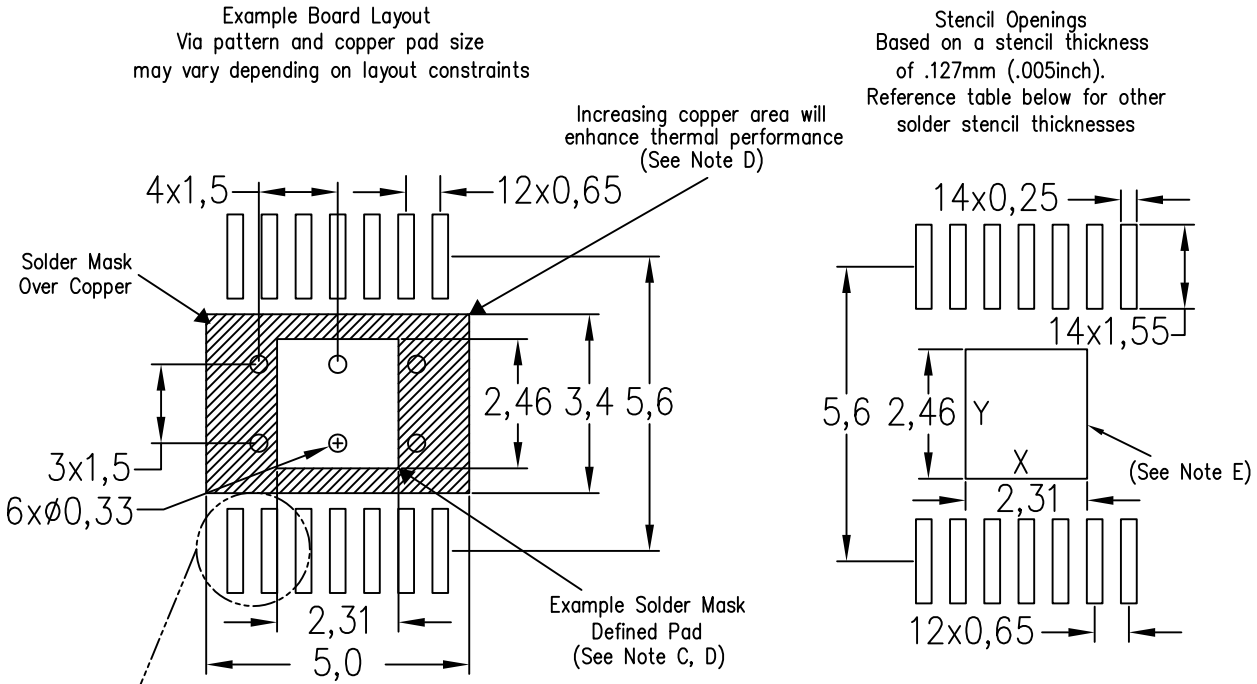
4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
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C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
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E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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