

## TMUX1247 5V 双向、2:1 (SPDT) 通用开关

### 1 特性

- 轨至轨运行
- 双向信号路径
- 1.8V 逻辑兼容
- 失效防护逻辑
- 低导通电阻: 3Ω
- 宽电源电压范围: 1.08V 至 5.5V
- -40°C 至 +125°C 的工作温度
- 低电源电流: 4nA
- 转换时间: 14ns
- 先断后合开关
- ESD 保护 HBM: 2000V

### 2 应用

- 模拟和数字开关
- I2C 和 SPI 总线多路复用
- 远程无线电单元
- 有源天线系统 mMIMO (AAS)
- 条形码扫描仪
- 电机驱动器
- 楼宇自动化
- 模拟输入模块
- 电力输送
- 视频监控
- 电子销售终端
- 电器
- 消费类音频

### 3 说明

TMUX1247 是一款通用互补金属氧化物半导体 (CMOS) 单极双投 (SPDT) 开关。TMUX1247 可根据 SEL 引脚的状态在两个输入电源之间切换。1.08V 至 5.5V 的宽电源电压工作范围可支持从个人电子设备到楼宇自动化的各种应用。该器件可在源极 (Sx) 和漏极 (D) 引脚上支持从 GND 到 V<sub>DD</sub> 范围的双向模拟和数字信号。4nA 的低电源电流可用于便携式应用。

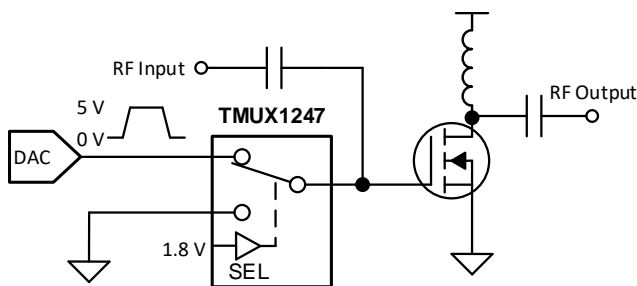
所有逻辑输入均具有兼容 1.8V 逻辑的阈值，当器件在有效电源电压范围内运行时，这些阈值可确保 TTL 和 CMOS 逻辑兼容性。失效防护逻辑电路允许在电源引脚之前的控制引脚上施加电压，从而保护器件免受潜在的损害。

器件信息(1)

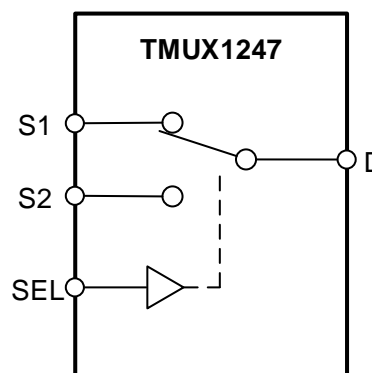
器件型号	封装	封装尺寸 (标称值)
TMUX1247	SC70 (6)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

应用示例



TMUX1247 方框图



## 目录

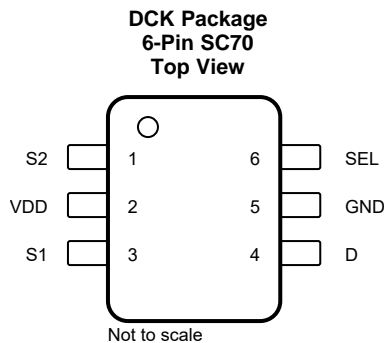
1	特性 .....	1	7.6	Charge Injection .....	15
2	应用 .....	1	7.7	Off Isolation .....	16
3	说明 .....	1	7.8	Crosstalk .....	16
4	修订历史记录 .....	2	7.9	Bandwidth .....	17
5	<b>Pin Configuration and Functions</b> .....	3	8	<b>Detailed Description</b> .....	18
6	<b>Specifications</b> .....	4	8.1	Overview .....	18
6.1	Absolute Maximum Ratings .....	4	8.2	Functional Block Diagram .....	18
6.2	ESD Ratings .....	4	8.3	Feature Description .....	18
6.3	Recommended Operating Conditions .....	4	8.4	Device Functional Modes .....	19
6.4	Thermal Information .....	4	8.5	Truth Tables .....	19
6.5	Electrical Characteristics ( $V_{DD} = 5\text{ V} \pm 10\%$ ), GND = 0 V unless otherwise specified. ....	5	9	<b>Application and Implementation</b> .....	20
6.6	Electrical Characteristics ( $V_{DD} = 3.3\text{ V} \pm 10\%$ ), GND = 0 V unless otherwise specified. ....	7	9.1	Application Information .....	20
6.7	Electrical Characteristics ( $V_{DD} = 1.8\text{ V} \pm 10\%$ ), GND = 0 V unless otherwise specified. ....	9	9.2	Typical Application .....	20
6.8	Electrical Characteristics ( $V_{DD} = 1.2\text{ V} \pm 10\%$ ), GND = 0 V unless otherwise specified. ....	11	10	<b>Power Supply Recommendations</b> .....	23
6.9	Typical Characteristics .....	12	11	<b>Layout</b> .....	24
7	<b>Parameter Measurement Information</b> .....	13	11.1	Layout Guidelines .....	24
7.1	On-Resistance .....	13	11.2	Layout Example .....	24
7.2	Off-Leakage Current .....	13	12	<b>器件和文档支持</b> .....	25
7.3	On-Leakage Current .....	14	12.1	文档支持 .....	25
7.4	Transition Time .....	14	12.2	接收文档更新通知 .....	25
7.5	Break-Before-Make .....	15	12.3	社区资源 .....	25
			12.4	商标 .....	25
			12.5	静电放电警告 .....	25
			12.6	Glossary .....	25
			13	<b>机械、封装和可订购信息</b> .....	25

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
8月2019年	*	初始发行版。

## 5 Pin Configuration and Functions



### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
S2	1	I/O	Source pin 2. Can be an input or output.
V <sub>DD</sub>	2	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 μF to 10 μF between V <sub>DD</sub> and GND.
S1	3	I/O	Source pin 1. Can be an input or output.
D	4	I/O	Drain pin. Can be an input or output.
GND	5	P	Ground (0 V) reference
SEL	6	I	Select pin: controls state of the switch according to <a href="#">表 1</a> . (Logic Low = S1 to D, Logic High = S2 to D)

(1) I = input, O = output, I/O = input and output, P = power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)<sup>(1)(2)(3)</sup>

		MIN	MAX	UNIT
$V_{DD}$	Supply voltage	-0.5	6	V
$V_{SEL}$ or $V_{EN}$	Logic control input pin voltage (SEL)	-0.5	6	V
$I_{SEL}$ or $I_{EN}$	Logic control input pin current (SEL)	-30	30	mA
$V_S$ or $V_D$	Source or drain voltage (Sx, D)	-0.5	$V_{DD}+0.5$	V
$I_S$ or $I_D$ (CONT)	Source or drain continuous current (Sx, D)	-50	50	mA
$I_K$	Diode clamp current <sup>(4)</sup>	-30	30	mA
$T_{stg}$	Storage temperature	-65	150	°C
$T_J$	Junction temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
- (3) All voltages are with respect to ground, unless otherwise specified.
- (4) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD}$	Supply voltage	1.08		5.5	V
$V_S$ or $V_D$	Signal path input/output voltage (source or drain pin) (Sx, D)	0		$V_{DD}$	V
$V_{SEL}$	Logic control input pin voltage (SEL)	0		5.5	V
$T_A$	Ambient temperature	-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMUX1247	UNIT
		DCK (SC70)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	243.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	106.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	89.1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	106.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics ( $V_{DD} = 5\text{ V} \pm 10\%$ ), $GND = 0\text{ V}$ unless otherwise specified.

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to <a href="#">On-Resistance</a>	25°C	3			$\Omega$
			-40°C to +85°C			5	$\Omega$
			-40°C to +125°C			6	$\Omega$
$\Delta R_{ON}$	On-resistance matching between channels	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to <a href="#">On-Resistance</a>	25°C	0.15			$\Omega$
			-40°C to +85°C			1	$\Omega$
			-40°C to +125°C			1	$\Omega$
$R_{ON\ FLAT}$	On-resistance flatness	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to <a href="#">On-Resistance</a>	25°C	1.5			$\Omega$
			-40°C to +85°C			2	$\Omega$
			-40°C to +125°C			3	$\Omega$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	$V_{DD} = 5\text{ V}$ Switch Off $V_D = 4.5\text{ V} / 1.5\text{ V}$ $V_S = 1.5\text{ V} / 4.5\text{ V}$ Refer to <a href="#">Off-Leakage Current</a>	25°C	$\pm 75$			nA
			-40°C to +85°C	-150		150	nA
			-40°C to +125°C	-175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 5\text{ V}$ Switch On $V_D = V_S = 4.5\text{ V} / 1\text{ V}$ Refer to <a href="#">On-Leakage Current</a>	25°C	$\pm 200$			nA
			-40°C to +85°C	-500		500	nA
			-40°C to +125°C	-750		750	nA
<b>LOGIC INPUTS</b>							
$V_{IH}$	Input logic high		-40°C to 125°C	1.42		5.5	V
$V_{IL}$	Input logic low		-40°C to 125°C	0		0.87	V
$I_{IH}$ $I_{IL}$	Input leakage current		25°C	$\pm 0.005$			$\mu\text{A}$
			-40°C to +125°C			$\pm 0.05$	$\mu\text{A}$
$C_{IN}$	Digital input capacitance		25°C	1			pF
$C_{IN}$	Digital input capacitance		-40°C to +125°C			2	pF
<b>POWER SUPPLY</b>							
$I_{DD}$	$V_{DD}$ supply current	Digital Inputs = 0 V or 5.5 V	25°C	0.007			$\mu\text{A}$
			-40°C to +125°C			1.5	$\mu\text{A}$

(1) When  $V_S$  is 4.5 V,  $V_D$  is 1.5 V or when  $V_S$  is 1.5 V,  $V_D$  is 4.5 V.

**Electrical Characteristics ( $V_{DD} = 5\text{ V} \pm 10\%$ ),  $GND = 0\text{ V}$  unless otherwise specified. (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
<b>DYNAMIC CHARACTERISTICS</b>							
$t_{\text{TRAN}}$	Switching time between channels	$V_S = 3\text{ V}$ $R_L = 200\ \Omega$ , $C_L = 15\text{ pF}$	25°C		12		ns
			–40°C to +85°C			18	ns
			–40°C to +125°C			19	ns
$t_{\text{OPEN}}$ (BBM)	Break before make time	$V_S = 3\text{ V}$ $R_L = 200\ \Omega$ , $C_L = 15\text{ pF}$	25°C		8		ns
			–40°C to +85°C		1		ns
			–40°C to +125°C		1		ns
$Q_C$	Charge Injection	$V_S = V_{DD}/2$ $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$	25°C		–10		pC
$O_{\text{ISO}}$	Off Isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	25°C		–65		dB
		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$	25°C		–45		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	25°C		–65		dB
		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$	25°C		–45		dB
$BW$	Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$	25°C		250		MHz
$C_{\text{SOFF}}$	Source off capacitance	$f = 1\text{ MHz}$	25°C		7		pF
$C_{\text{SON}}$ $C_{\text{DON}}$	On capacitance	$f = 1\text{ MHz}$	25°C		23		pF

## 6.6 Electrical Characteristics ( $V_{DD} = 3.3\text{ V} \pm 10\%$ ), $GND = 0\text{ V}$ unless otherwise specified.

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to <a href="#">On-Resistance</a>	25°C		4.5		$\Omega$
			-40°C to +85°C			12.5	$\Omega$
			-40°C to +125°C			13	$\Omega$
$\Delta R_{ON}$	On-resistance matching between channels	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to <a href="#">On-Resistance</a>	25°C		0.15		$\Omega$
			-40°C to +85°C			1	$\Omega$
			-40°C to +125°C			1	$\Omega$
$R_{ON\text{ FLAT}}$	On-resistance flatness	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to <a href="#">On-Resistance</a>	25°C		3.5		$\Omega$
			-40°C to +85°C			4	$\Omega$
			-40°C to +125°C			5	$\Omega$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	$V_{DD} = 3.3\text{ V}$ Switch Off $V_D = 3\text{ V} / 1\text{ V}$ $V_S = 1\text{ V} / 3\text{ V}$ Refer to <a href="#">Off-Leakage Current</a>	25°C		$\pm 75$		nA
			-40°C to +85°C		-150	150	nA
			-40°C to +125°C		-175	175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 3.3\text{ V}$ Switch On $V_D = V_S = 3\text{ V} / 1\text{ V}$ Refer to <a href="#">On-Leakage Current</a>	25°C		$\pm 200$		nA
			-40°C to +85°C		-500	500	nA
			-40°C to +125°C		-750	750	nA
<b>LOGIC INPUTS</b>							
$V_{IH}$	Input logic high		-40°C to 125°C	1.35		5.5	V
$V_{IL}$	Input logic low		-40°C to 125°C	0		0.8	V
$I_{IH}$ $I_{IL}$	Input leakage current		25°C		$\pm 0.005$		$\mu\text{A}$
			-40°C to +125°C			$\pm 0.05$	$\mu\text{A}$
$C_{IN}$	Logic input capacitance		25°C		1		pF
$C_{IN}$	Logic input capacitance		-40°C to +125°C			2	pF
<b>POWER SUPPLY</b>							
$I_{DD}$	$V_{DD}$ supply current	Digital Inputs = 0 V or 5.5 V	25°C		0.004		$\mu\text{A}$
			-40°C to +125°C			0.8	$\mu\text{A}$

(1) When  $V_S$  is 3 V,  $V_D$  is 1 V or when  $V_S$  is 1 V,  $V_D$  is 3 V.

**Electrical Characteristics ( $V_{DD} = 3.3\text{ V} \pm 10\%$ ), GND = 0 V unless otherwise specified. (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
<b>DYNAMIC CHARACTERISTICS</b>							
$t_{\text{TRAN}}$	Switching time between channels	$V_S = 2\text{ V}$ $R_L = 200\ \Omega$ , $C_L = 15\text{ pF}$	25°C	14			ns
			–40°C to +85°C		20		ns
			–40°C to +125°C		22		ns
$t_{\text{OPEN}}$ (BBM)	Break before make time	$V_S = 2\text{ V}$ $R_L = 200\ \Omega$ , $C_L = 15\text{ pF}$	25°C	8			ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$Q_C$	Charge Injection	$V_S = V_{DD}/2$ $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$	25°C		–6		pC
$O_{\text{ISO}}$	Off Isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to <a href="#">Off Isolation</a>	25°C		–65		dB
		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to <a href="#">Off Isolation</a>	25°C		–45		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to <a href="#">Crosstalk</a>	25°C		–65		dB
		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to <a href="#">Crosstalk</a>	25°C		–45		dB
BW	Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ Refer to <a href="#">Bandwidth</a>	25°C		250		MHz
$C_{\text{SOFF}}$	Source off capacitance	$f = 1\text{ MHz}$	25°C		7		pF
$C_{\text{SON}}$ $C_{\text{DON}}$	On capacitance	$f = 1\text{ MHz}$	25°C		23		pF



## 6.7 Electrical Characteristics ( $V_{DD} = 1.8\text{ V} \pm 10\%$ ), $GND = 0\text{ V}$ unless otherwise specified.

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to <a href="#">On-Resistance</a>	25°C	40			$\Omega$
			-40°C to +85°C			80	$\Omega$
			-40°C to +125°C			80	$\Omega$
$\Delta R_{ON}$	On-resistance matching between channels	$V_S = 0\text{ V to }V_{DD}$ $I_{SD} = 10\text{ mA}$ Refer to <a href="#">On-Resistance</a>	25°C	0.4			$\Omega$
			-40°C to +85°C			1.5	$\Omega$
			-40°C to +125°C			1.5	$\Omega$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	$V_{DD} = 1.98\text{ V}$ Switch Off $V_D = 1.8\text{ V} / 1\text{ V}$ $V_S = 1\text{ V} / 1.8\text{ V}$ Refer to <a href="#">Off-Leakage Current</a>	25°C	$\pm 75$			nA
			-40°C to +85°C	-150		150	nA
			-40°C to +125°C	-175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 1.98\text{ V}$ Switch On $V_D = V_S = 1.62\text{ V} / 1\text{ V}$	25°C	$\pm 200$			nA
			-40°C to +85°C	-500		500	nA
			-40°C to +125°C	-750		750	nA
<b>DIGITAL INPUTS</b>							
$V_{IH}$	Input logic high		-40°C to +125°C	1.07		5.5	V
$V_{IL}$	Input logic low		-40°C to +125°C	0		0.68	V
$I_{IH}$ $I_{IL}$	Input leakage current		25°C	$\pm 0.005$			$\mu\text{A}$
$I_{IH}$ $I_{IL}$	Input leakage current		-40°C to +125°C			$\pm 0.05$	$\mu\text{A}$
$C_{IN}$	Logic input capacitance		25°C	1			pF
$C_{IN}$	Logic input capacitance		-40°C to +125°C			2	pF
<b>POWER SUPPLY</b>							
$I_{DD}$	$V_{DD}$ supply current	Logic Inputs = 0 V or 5.5 V	25°C	0.002			$\mu\text{A}$
			-40°C to +125°C			0.52	$\mu\text{A}$

(1) When  $V_S$  is 1.8 V,  $V_D$  is 1 V or when  $V_S$  is 1 V,  $V_D$  is 1.8 V.

**Electrical Characteristics ( $V_{DD} = 1.8\text{ V} \pm 10\%$ ), GND = 0 V unless otherwise specified. (continued)**

 at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.8\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
<b>LOGIC INPUTS</b>							
$t_{\text{TRAN}}$	Switching time between channels	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$ , $C_L = 15\text{ pF}$	25°C	24			ns
			–40°C to +85°C			44	ns
			–40°C to +125°C			45	ns
$t_{\text{OPEN}}$ (BBM)	Break before make time	$V_S = 1\text{ V}$ $R_L = 200\ \Omega$ , $C_L = 15\text{ pF}$	25°C	16			ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$Q_C$	Charge Injection	$V_S = V_{DD}/2$ $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$	25°C		–3		pC
$O_{\text{ISO}}$	Off Isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to <a href="#">Off Isolation</a>	25°C		–65		dB
		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to <a href="#">Off Isolation</a>	25°C		–45		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 1\text{ MHz}$ Refer to <a href="#">Crosstalk</a>	25°C		–65		dB
		$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $f = 10\text{ MHz}$ Refer to <a href="#">Crosstalk</a>	25°C		–45		dB
BW	Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$	25°C		250		MHz
$C_{\text{SOFF}}$	Source off capacitance	$f = 1\text{ MHz}$	25°C		7		pF
$C_{\text{SON}}$ $C_{\text{DON}}$	On capacitance	$f = 1\text{ MHz}$	25°C		23		pF

## 6.8 Electrical Characteristics ( $V_{DD} = 1.2\text{ V} \pm 10\%$ ), $GND = 0\text{ V}$ unless otherwise specified.

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.2\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
<b>ANALOG SWITCH</b>							
$R_{ON}$	On-resistance	$V_S = 0\text{ V to }V_{DD}$ $I_{DS} = 10\text{ mA}$	25°C		70		$\Omega$
			-40°C to +85°C			105	$\Omega$
			-40°C to +125°C			105	$\Omega$
$\Delta R_{ON}$	On-resistance matching between channels	$V_S = 0\text{ V to }V_{DD}$ $I_{DS} = 10\text{ mA}$	25°C		0.4		$\Omega$
			-40°C to +85°C			1.5	$\Omega$
			-40°C to +125°C			1.5	$\Omega$
$I_{S(OFF)}$	Source off leakage current <sup>(1)</sup>	$V_{DD} = 1.32\text{ V}$ Switch Off $V_D = 1.2\text{ V} / 1\text{ V}$ $V_S = 1\text{ V} / 1.2\text{ V}$	25°C		$\pm 75$		nA
			-40°C to +85°C		-150	150	nA
			-40°C to +125°C		-175	175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	$V_{DD} = 1.32\text{ V}$ Switch On $V_D = V_S = 1\text{ V} / 0.8\text{ V}$	25°C		$\pm 200$		nA
			-40°C to +85°C		-500	500	nA
			-40°C to +125°C		-750	750	nA
<b>DIGITAL INPUTS</b>							
$V_{IH}$	Input logic high		-40°C to +125°C	0.96			V
$V_{IL}$	Input logic low		-40°C to +125°C			0.36	V
$I_{IH}$ $I_{IL}$	Input leakage current		25°C		$\pm 0.005$		$\mu\text{A}$
			-40°C to +125°C			$\pm 0.10$	$\mu\text{A}$
$C_{IN}$	Digital input capacitance		25°C		1		pF
$C_{IN}$	Digital input capacitance		-40°C to +125°C			2	pF
<b>POWER SUPPLY</b>							
$I_{DD}$	$V_{DD}$ supply current	Digital Inputs = 0 V or 5.5 V	25°C		0.0015		$\mu\text{A}$
			-40°C to +125°C			0.45	$\mu\text{A}$
<b>DYNAMIC CHARACTERISTICS</b>							
$t_{TRAN}$	Switching time between channels	$V_{IN} = V_{DD}$ $V_S = 1\text{ V}$ $R_L = 200\ \Omega, C_L = 15\text{ pF}$	25°C		40		ns
			-40°C to +85°C			175	ns
			-40°C to +125°C			175	ns
$t_{OPEN}$ (BBM)	Break before make time	$V_S = 1\text{ V}$ $R_L = 200\ \Omega, C_L = 15\text{ pF}$	25°C		27		ns
			-40°C to +85°C		1		ns
			-40°C to +125°C		1		ns
$Q_C$	Charge Injection	$V_S = (V_{DD} + V_{SS})/2$ $R_S = 0\ \Omega, C_L = 1\text{ nF}$	25°C		$\pm 5$		pC
$O_{ISO}$	Off Isolation	$R_L = 50\ \Omega, C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	25°C		-64		dB
		$R_L = 50\ \Omega, C_L = 5\text{ pF}$ $f = 10\text{ MHz}$	25°C		-44		dB
$X_{TALK}$	Crosstalk	$R_L = 50\ \Omega, C_L = 5\text{ pF}$ $f = 1\text{ MHz}$	25°C		-64		dB
		$R_L = 50\ \Omega, C_L = 5\text{ pF}$ $f = 10\text{ MHz}$	25°C		-44		dB
$BW$	Bandwidth	$R_L = 50\ \Omega, C_L = 5\text{ pF}$	25°C		250		MHz
$C_{SOFF}$	Source off capacitance	$f = 1\text{ MHz}$	25°C		7		pF
$C_{SON}$ $C_{DON}$	On capacitance	$f = 1\text{ MHz}$	25°C		23		pF

(1) When  $V_S$  is 1 V,  $V_D$  is 1.2 V or when  $V_S$  is 1.2 V,  $V_D$  is 1 V.

### 6.9 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

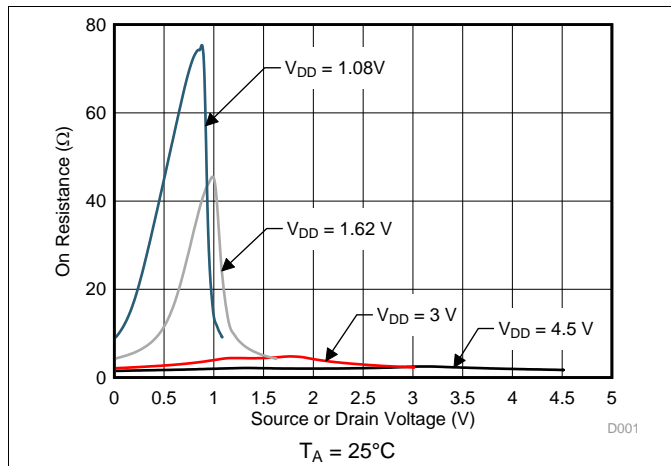


图 1. On-Resistance vs Source or Drain Voltage

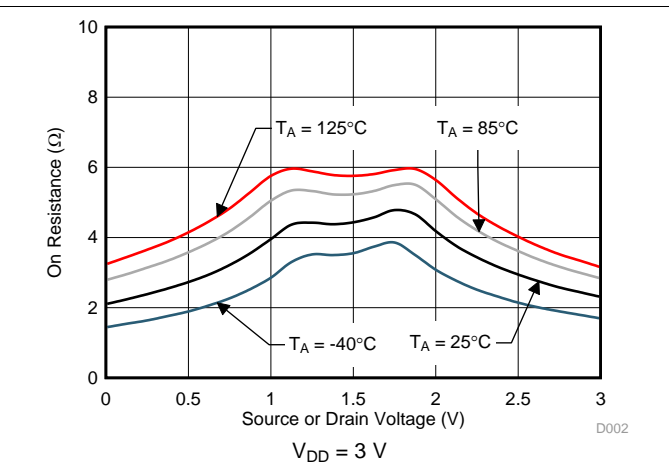


图 2. On-Resistance vs Source or Drain Voltage

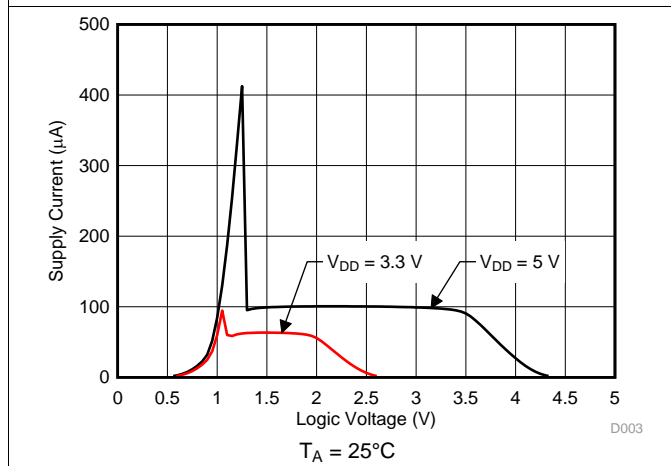


图 3. Supply Current vs Logic Voltage

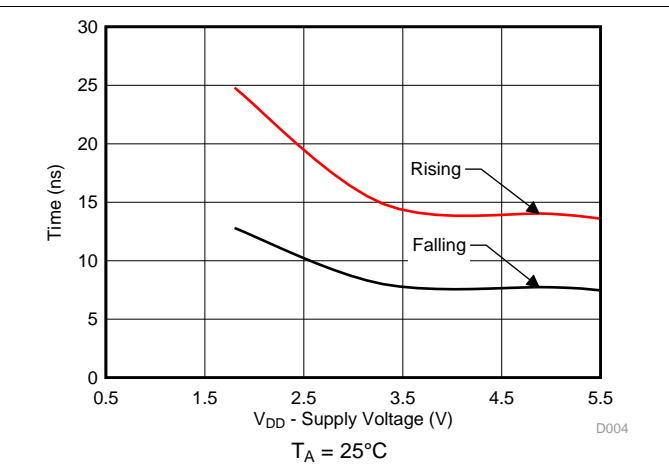


图 4.  $T_{\text{transition}}$  vs Supply Voltage

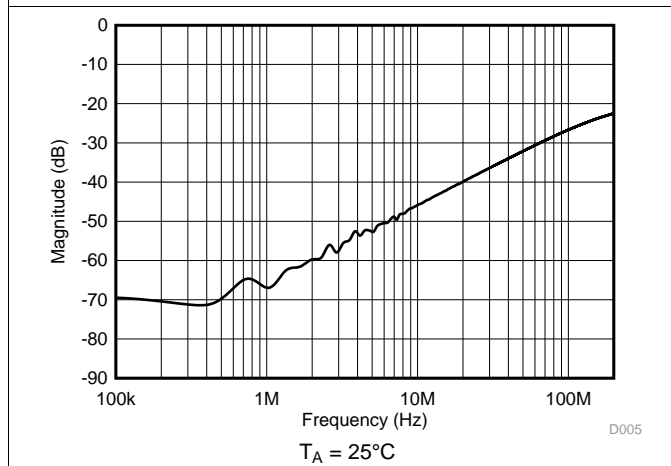


图 5. Crosstalk and Off-Isolation vs Frequency

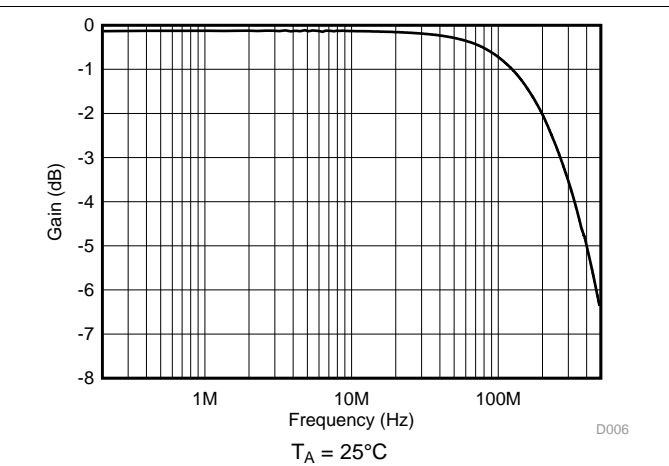


图 6. Frequency Response

## 7 Parameter Measurement Information

### 7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol  $R_{ON}$  is used to denote on-resistance. The measurement setup used to measure  $R_{ON}$  is shown in 图 7. Voltage (V) and current ( $I_{SD}$ ) are measured using this setup, and  $R_{ON}$  is computed with  $R_{ON} = V / I_{SD}$ :

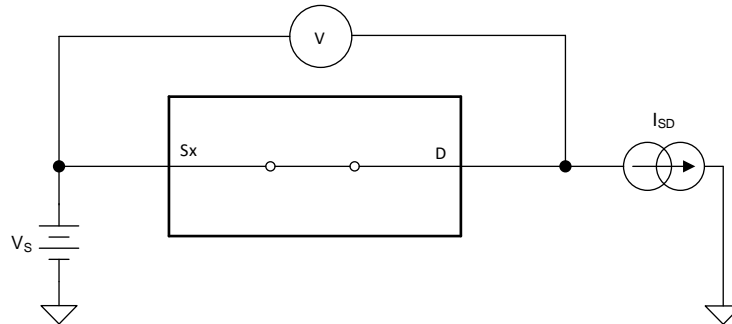


图 7. On-Resistance Measurement Setup

### 7.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol  $I_{S(OFF)}$ .

The setup used to measure off-leakage current is shown in 图 8.

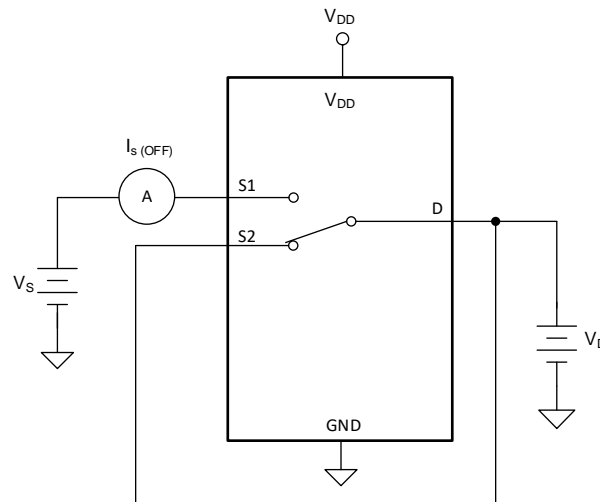
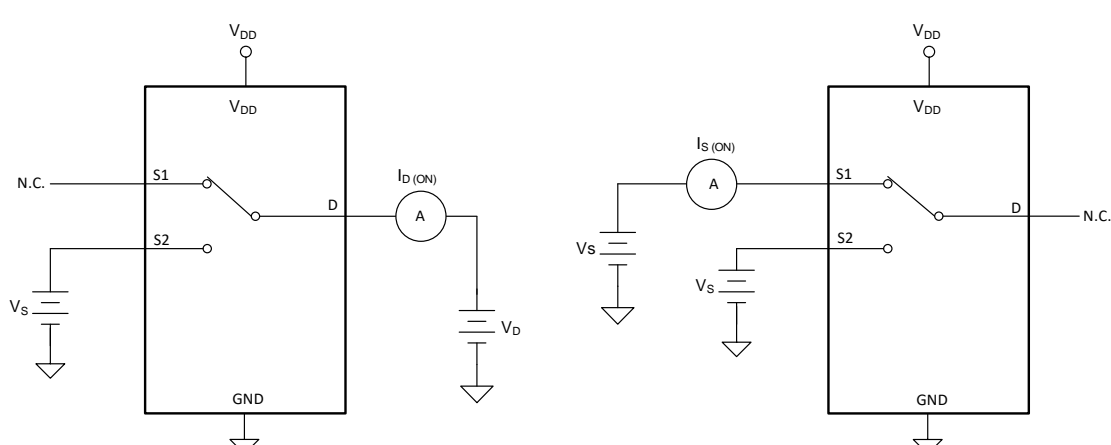


图 8. Off-Leakage Measurement Setup

### 7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol  $I_{S(ON)}$ .

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol  $I_{D(ON)}$ .

Either the source pin or drain pin is left floating during the measurement.  shows the circuit used for measuring the on-leakage current, denoted by  $I_{S(ON)}$  or  $I_{D(ON)}$ .

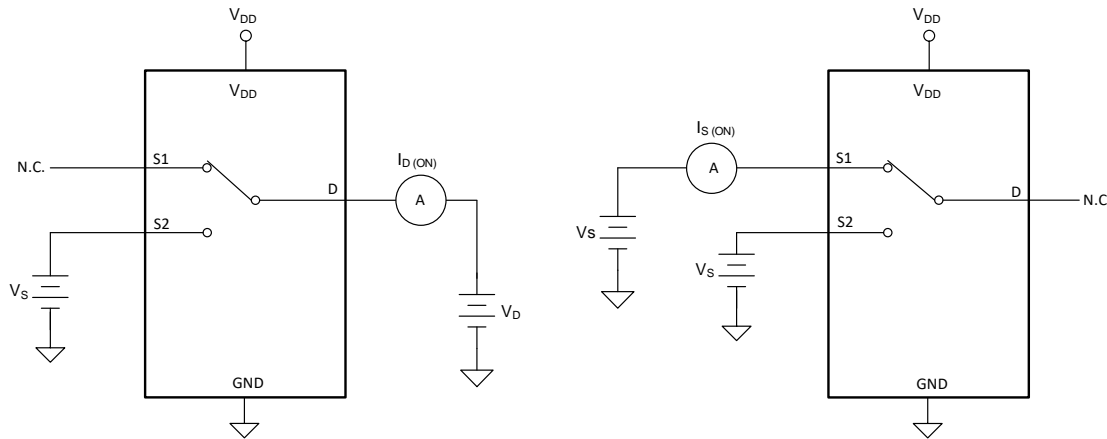
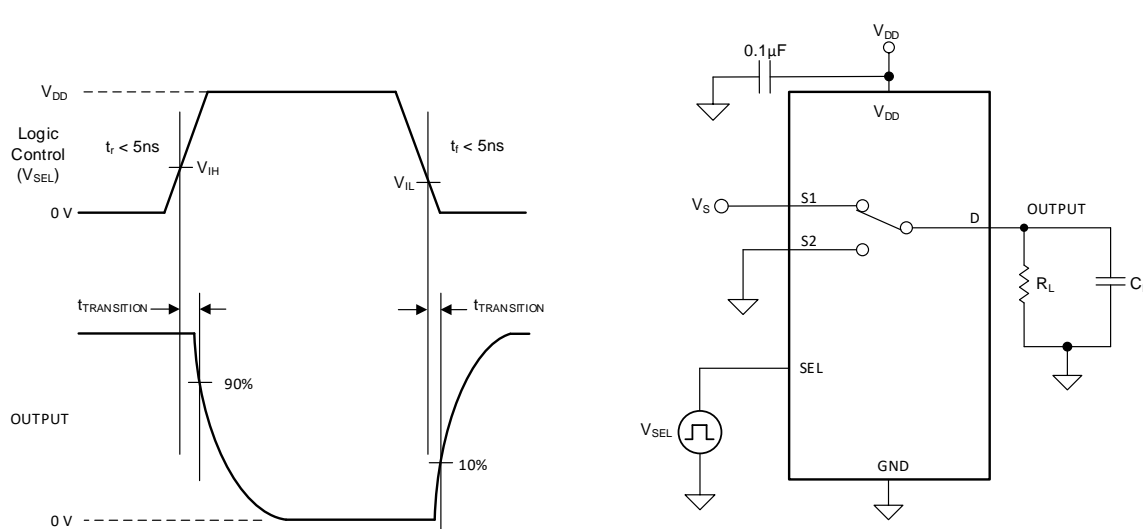


图 9. On-Leakage Measurement Setup

### 7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the logic control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance.  shows the setup used to measure transition time, denoted by the symbol  $t_{TRANSITION}$ .

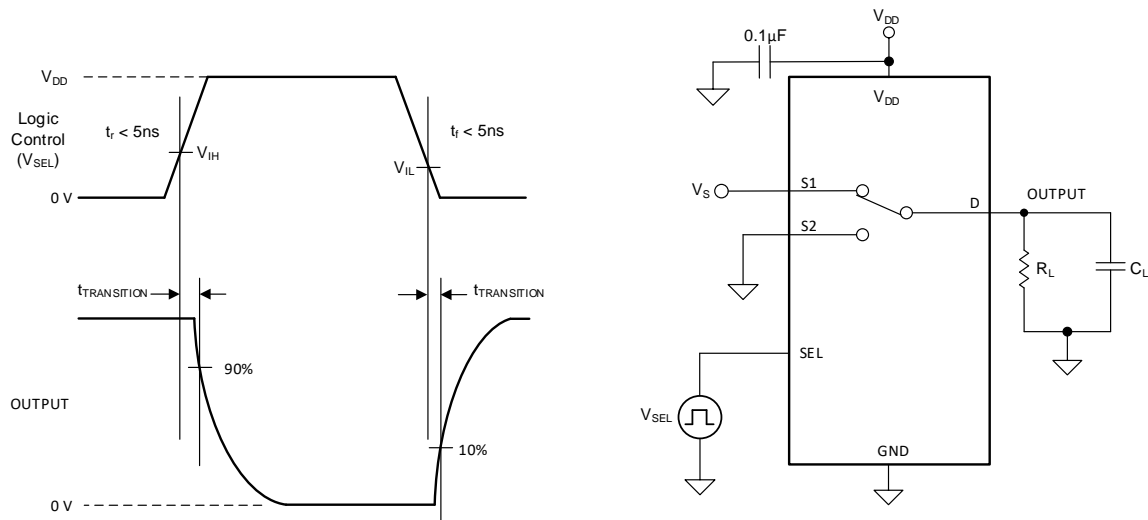


图 10. Transition-Time Measurement Setup

### 7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 11 shows the setup used to measure break-before-make delay, denoted by the symbol  $t_{\text{OPEN(BBM)}}$ .

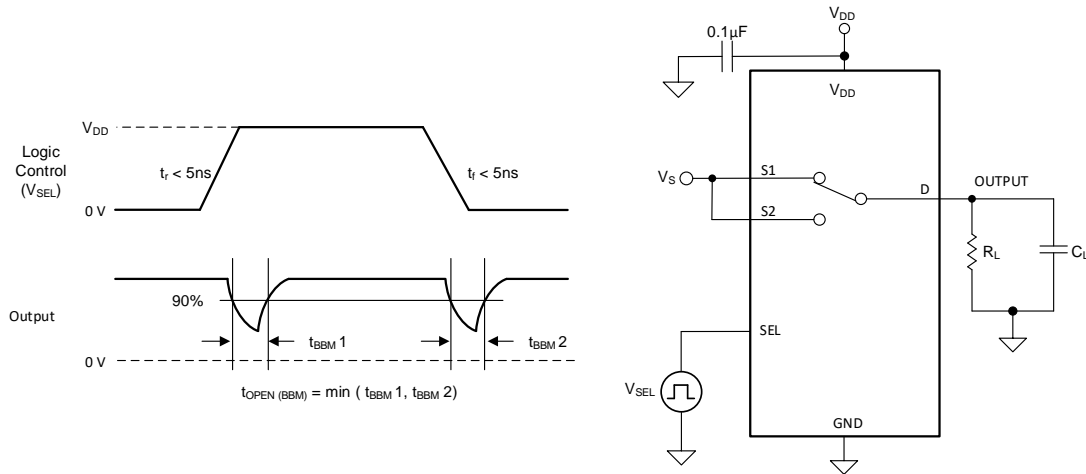


图 11. Break-Before-Make Delay Measurement Setup

### 7.6 Charge Injection

The TMUX1247 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol  $Q_C$ . Figure 12 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

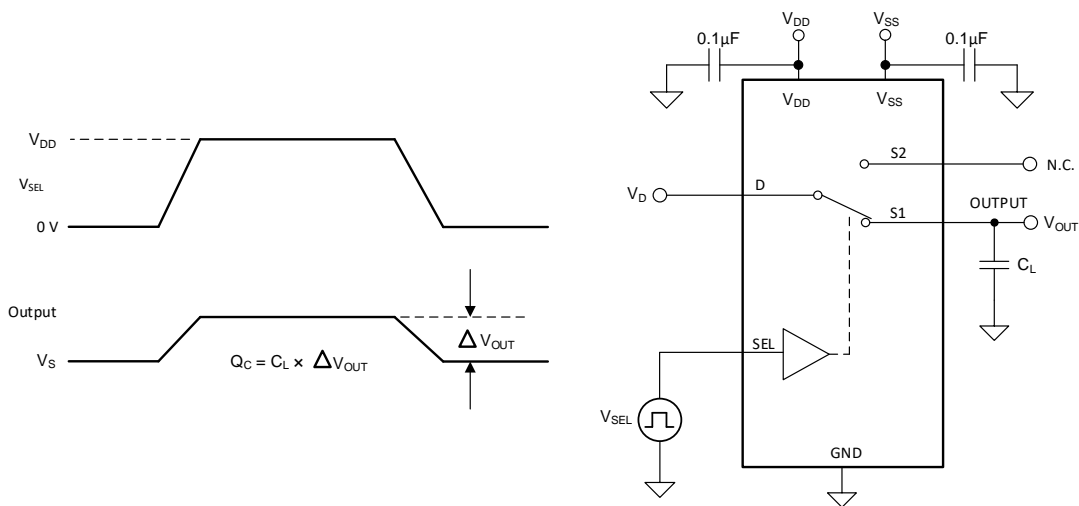


图 12. Charge-Injection Measurement Setup

## 7.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 13 shows the setup used to measure, and the equation used to calculate off isolation.

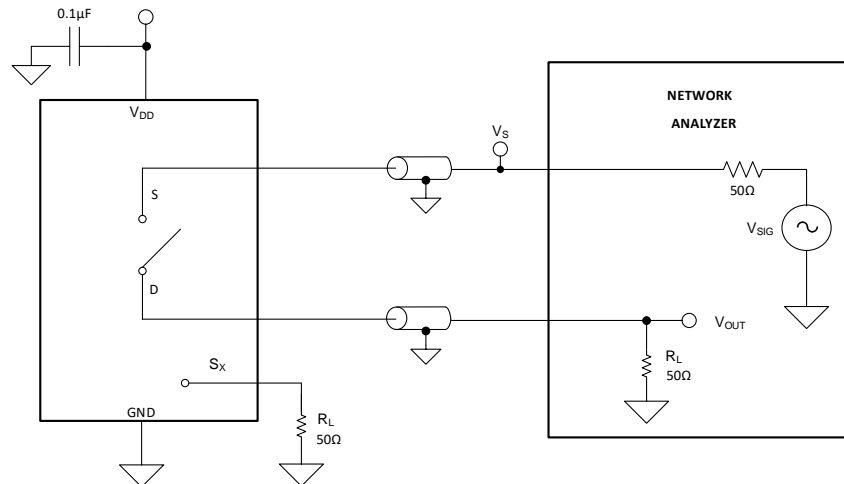


图 13. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log} \left( \frac{V_{\text{OUT}}}{V_{\text{S}}} \right) \quad (1)$$

## 7.8 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 14 shows the setup used to measure, and the equation used to calculate crosstalk.

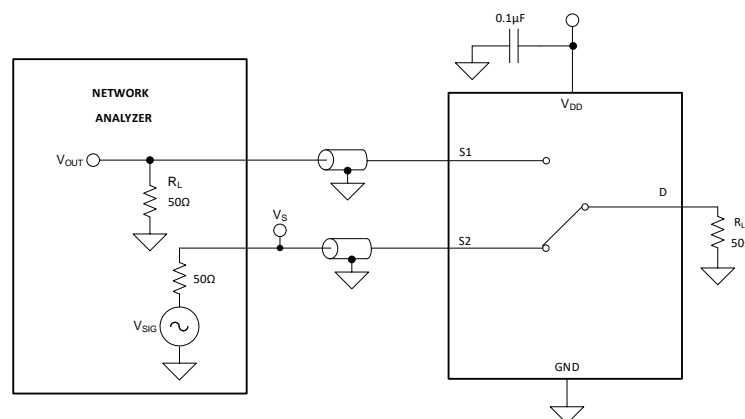


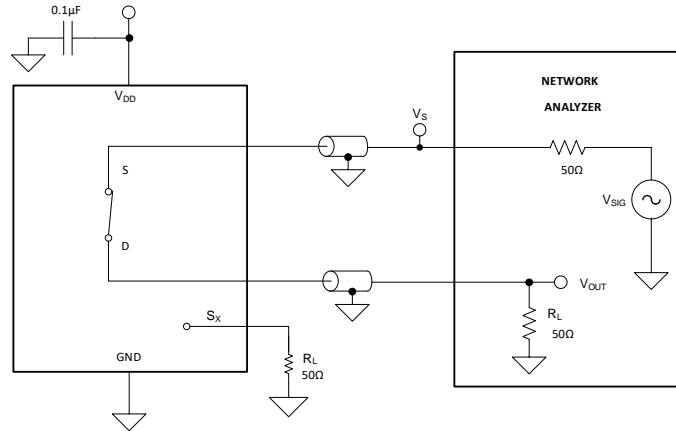
图 14. Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log} \left( \frac{V_{\text{OUT}}}{V_{\text{S}}} \right) \quad (2)$$



## 7.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 15 shows the setup used to measure bandwidth.



**图 15. Bandwidth Measurement Setup**

## 8 Detailed Description

### 8.1 Overview

The TMUX1247 is an 2:1 (SPDT), 1-channel switch where the input is controlled with a single select (SEL) control pin.

### 8.2 Functional Block Diagram

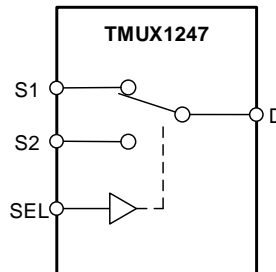


图 16. TMUX1247 Functional Block Diagram

### 8.3 Feature Description

#### 8.3.1 Bidirectional Operation

The TMUX1247 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

#### 8.3.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1247 ranges from GND to  $V_{DD}$ .

#### 8.3.3 1.8 V Logic Compatible Inputs

The TMUX1247 has 1.8-V logic compatible control for the logic control input (SEL). The logic input threshold scales with supply but still provides 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allow the TMUX1247 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to [Simplifying Design with 1.8 V logic Muxes and Switches](#)

#### 8.3.4 Fail-Safe Logic

The TMUX1247 supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the TMUX1247 to be ramped to 5.5 V while  $V_{DD} = 0$  V. Additionally, the feature enables operation of the TMUX1247 with  $V_{DD} = 1.2$  V while allowing the select pin to interface with a logic level of another device up to 5.5 V.

## 8.4 Device Functional Modes

The select (SEL) pin of the TMUX1247 controls which switch is connected to the drain of the device. When a given input is not selected, that source pin is in high impedance mode (HI-Z). The control pins can be as high as 5.5 V.

The TMUX1247 can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or  $V_{DD}$  in order to ensure the device does not consume additional current as highlighted in [Implications of Slow or Floating CMOS Inputs](#). Unused signal path inputs (Sx or D) should be connected to GND.

## 8.5 Truth Tables

表 1. TMUX1247 Truth Table

CONTROL LOGIC (SEL)	Selected Source (Sx) Connected To Drain (D) Pin
0	S1
1	S2

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TMUX12xx family offers good system performance across a wide operating supply (1.08V to 5.5V). These devices include 1.8V logic compatible control input pins that enable operation in systems with 1.8V I/O rails. Additionally, the control input pin supports Fail-Safe Logic which allows for operation up to 5.5V, regardless of the state of the supply pin. This protection stops the logic pins from back-powering the supply rail. These features of the TMUX12xx, a family of general purpose multiplexers and switches, reduce system complexity, board size, and overall system cost.

### 9.2 Typical Application

#### 9.2.1 Input Control for Power Amplifier

One application of the TMUX1247 is for input control of a power amplifier. Utilizing a switch allows a system to control when the DAC is connected to the power amplifier, and can stop biasing the power amplifier by switching the gate to GND. 图 17 shows the TMUX1247 configured for control of the power amplifier.

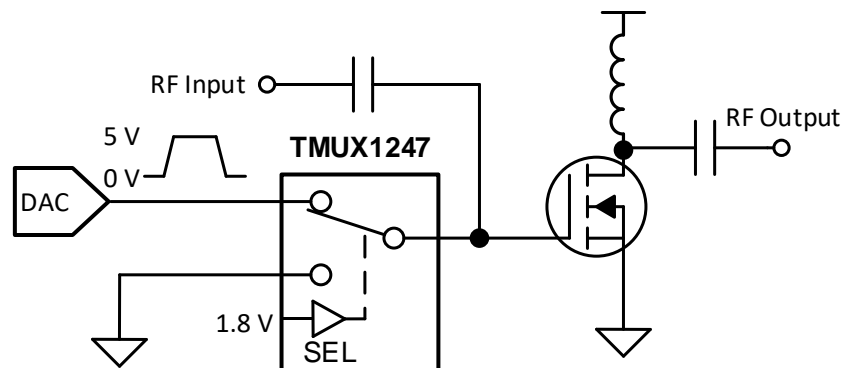


图 17. Input Control of Power Amplifier

## Typical Application (接下页)

### 9.2.1.1 Design Requirements

This design example uses the parameters listed in 表 3.

表 2. Design Parameters

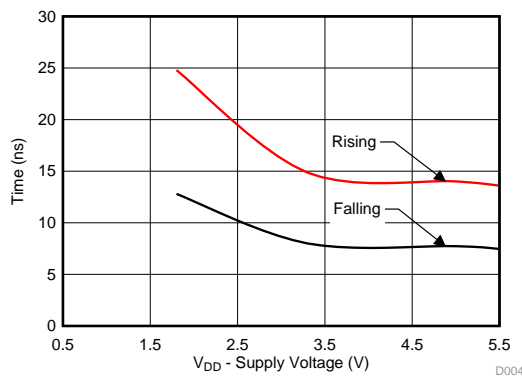
PARAMETERS	VALUES
Supply ( $V_{DD}$ )	5 V
Mux I/O signal range	0 V to $V_{DD}$ (Rail to Rail)
Control logic thresholds	1.8 V compatible (up to 5.5V)

### 9.2.1.2 Detailed Design Procedure

The application shown in 图 17 demonstrates how to toggle between the DAC output and GND for control of a power amplifier using a single control input. The DAC output is utilized to bias the gate of the power amplifier and can be disconnected from the circuit using the select pin of the switch. The TMUX1247 can support 1.8-V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX1247 can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a weak pull-down or pull-up resistor to ensure the input is in a known state. All inputs to the switch must fall within the recommend operating conditions of the TMUX1247 including signal range and continuous current. For this design with a supply of 5 V the signal range can be 0 V to 5 V and the max continuous current can be 30 mA.

### 9.2.1.3 Application Curve

A key parameter for this application is the transition time of the device. Faster transition time allows the system to toggle between input sources at a faster rate and allows the output to settle to the final value. The TMUX1247 has a transition time that varies with supply voltage and is shown in 图 18



$$T_A = 25^\circ\text{C}$$

图 18.  $T_{\text{transition}}$  vs Supply Voltage

## 9.2.2 Switchable Operational Amplifier Gain Setting

Another example application of the TMUX1247 is to change an Op Amp from unity gain setting to an inverting amplifier configuration. Utilizing a switch allows a system to have a configurable gain and allows the same architecture to be utilized across the board for various inputs to the system. 图 19 shows the TMUX1247 configured for gain setting application.

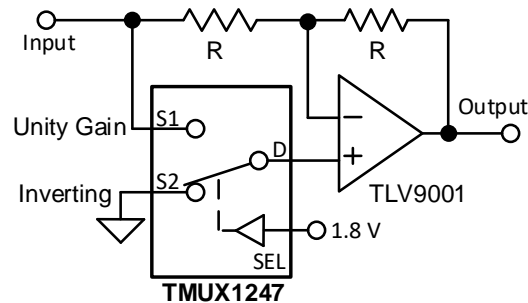


图 19. Switchable Op Amp Gain Setting

### 9.2.2.1 Design Requirements

This design example uses the parameters listed in 表 3.

表 3. Design Parameters

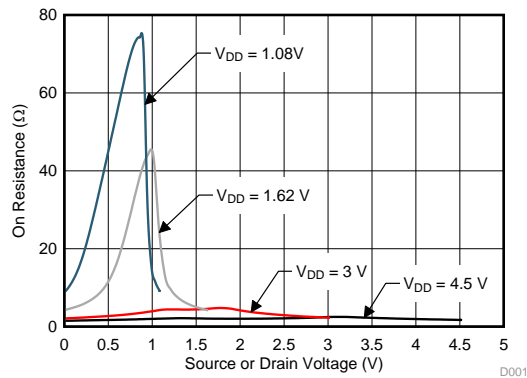
PARAMETERS	VALUES
Input Signal	0 V to 2.75 V
Mux Supply ( $V_{DD}$ )	2.75 V
Op Amp Supply ( $V_{+}/V_{-}$ )	$\pm 2.75$ V
Mux I/O signal range	0 V to $V_{DD}$ (Rail to Rail)
Control logic thresholds	1.8 V compatible (up to 5.5V)

### 9.2.2.2 Detailed Design Procedure

The application shown in 图 19 demonstrates how to use a single control input and toggle between gain settings of -1 and +1. If switching between inverting and unity gain is not required, the TMUX1247 can be utilized in the feedback path to select different feedback resistors and provide scalable gain settings for configurable signal conditioning.

The TMUX1247 can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a weak pull-down or pull-up resistor to ensure the input is in a known state. All inputs to the switch must fall within the recommend operating conditions of the TMUX1247 including signal range and continuous current. For this design with a supply of 2.75 V the signal range can be 0 V to 2.75 V and the max continuous current can be 30 mA.

### 9.2.2.3 Application Curve



$T_A = 25^\circ\text{C}$

图 20. On-Resistance vs Source or Drain Voltage

## 10 Power Supply Recommendations

The TMUX1247 operates across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the  $V_{DD}$  supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1  $\mu\text{F}$  to 10  $\mu\text{F}$  from  $V_{DD}$  to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

## 11 Layout

### 11.1 Layout Guidelines

#### 11.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. [图 21](#) shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

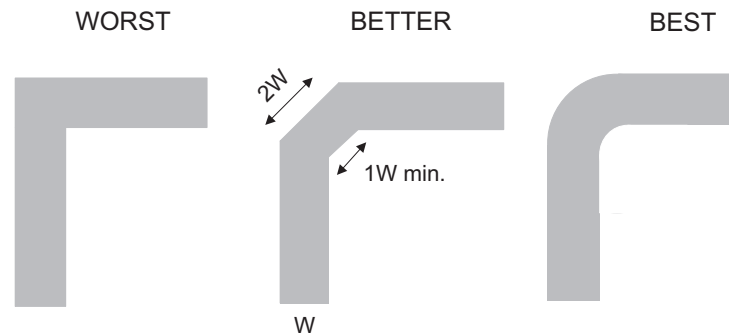


图 21. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

[图 22](#) illustrates an example of a PCB layout with the TMUX1247. Some key considerations are:

- Decouple the  $V_{DD}$  pin with a 0.1- $\mu\text{F}$  capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the  $V_{DD}$  supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

### 11.2 Layout Example

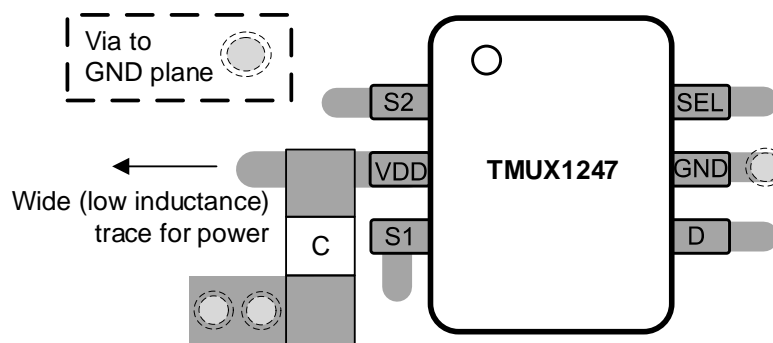


图 22. TMUX1247 Layout Example



## 12 器件和文档支持

### 12.1 文档支持

#### 12.1.1 相关文档

德州仪器 (TI), 《使用低 CON 多路复用器改善稳定性问题》。

德州仪器 (TI), 《使用 1.8V 逻辑多路复用器和开关简化设计》。

德州仪器 (TI), 《利用关断保护信号开关消除电源排序》。

德州仪器 (TI), 《高电压模拟多路复用器的系统级保护》。

### 12.2 接收文档更新通知

要接收文档更新通知, 请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册, 即可每周接收产品信息更改摘要。有关更改的详细信息, 请查看任何已修订文档中包含的修订历史记录。

### 12.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 商标

E2E is a trademark of Texas Instruments.

### 12.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序, 可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级, 大至整个器件故障。精密的集成电路可能更容易受到损坏, 这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更, 恕不另行通知, 且不会对此文档进行修订。如需获取此数据表的浏览器版本, 请查阅左侧的导航栏。

## 重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122  
Copyright © 2019 德州仪器半导体技术（上海）有限公司

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX1247DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	247	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1247DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1247DCKR	SC70	DCK	6	3000	180.0	180.0	18.0

DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

## 重要声明和免责声明

TI 均以“原样”提供技术性 & 可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证其中不含任何瑕疵，且不做任何明示或暗示的担保，包括但不限于对适销性、适合某特定用途或不侵犯任何第三方知识产权的暗示担保。

所述资源可供专业开发人员应用 TI 产品进行设计使用。您将对以下行为独自承担全部责任：(1) 针对您的应用选择合适的 TI 产品；(2) 设计、验证并测试您的应用；(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。所述资源如有变更，恕不另行通知。TI 对您使用所述资源的授权仅限于开发资源所涉及 TI 产品的相关应用。除此之外不得复制或展示所述资源，也不提供其它 TI 或任何第三方的知识产权授权许可。如因使用所述资源而产生任何索赔、赔偿、成本、损失及债务等，TI 对此概不负责，并且您须赔偿由此对 TI 及其代表造成的损害。

TI 所提供产品均受 TI 的销售条款 (<http://www.ti.com.cn/zh-cn/legal/termsofsale.html>) 以及 [ti.com.cn](http://www.ti.com.cn) 上或随附 TI 产品提供的其他可适用条款的约束。TI 提供所述资源并不扩展或以其他方式更改 TI 针对 TI 产品所发布的可适用的担保范围或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122

Copyright © 2020 德州仪器半导体技术（上海）有限公司