具有 400mV 基准电压的 TLV6703 微功耗、18V 比较器

1 特性

- 宽电源电压范围：1.8V 至 18V
- 可调节阈值：低至 400mV
- 高阈值精度：
  - 最高 0.5% (25°C)
  - 在工作温度范围内最高 1.0%
- 低静态电流：5.5µA（典型值）
- 漏极开路输出
- 内部滞后：5.5mV（典型值）
- 温度范围：-40°C 至 +125°C
- 封装：超薄 SOT-23-6

2 应用

- 笔记本电脑和平板电脑
- 智能手机
- 数码相机
- 视频游戏控制器
- 中继器和断路器
- 便携式医疗设备
- 门窗传感器
- 便携式和电池供电类产品

3 说明

TLV6703 是一款高电压比较器，工作电压范围为 1.8V 至 18V。TLV6703 具有一个内部基准电压为 400mV 的高精度比较器和一个额定电压为 18V 的开漏输出，用于实现精确的电压检测。可以使用外部电阻设置监视电压。

当 SENSE 引脚上的电压下降至低于 (V_{IT-}) 时，OUT 引脚被驱动至低电平，而当电压返回到对应阈值 (V_{IT+}) 之上时，OUT 引脚变为高电平。TLV6703 中的比较器具有拒绝短暂干扰的内置迟滞，确保稳定的输出运行，不会引起误触发。

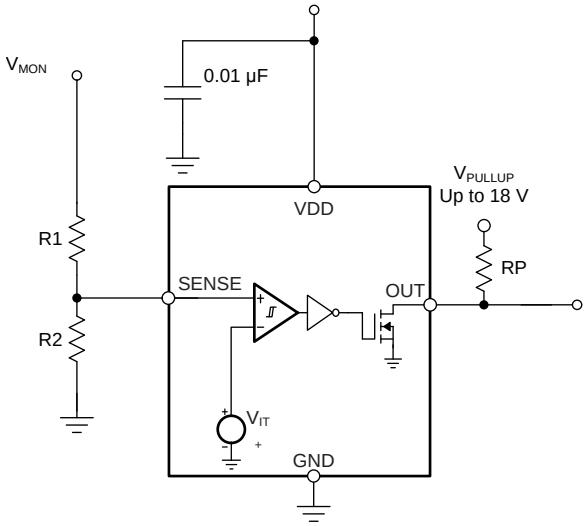
TLV6703 采用超薄 SOT-23-6 封装，额定结温范围为 –40°C 至 +125°C。

器件信息 (1)

器件型号	封装	封装尺寸（标称值）
TLV6703	SOT-23 (6)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

简化框图



目录

4 修订历史记录

Changes from Original (January 2018) to Revision A **Page**

- 已更改 从“预告信息”更改成了“生产数据” ... 1

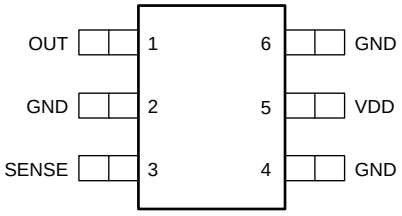
5 Device Comparison Table

Table 1. TLV67xx Integrated Comparator Family

PART NUMBER	CONFIGURATION	OPERATING VOLTAGE RANGE	THRESHOLD ACCURACY OVER TEMPERATURE
TLV6700	Window	1.8 V to 18 V	1%
TLV6703	Non-Inverting Single Channel	1.8 V to 18 V	1%
TLV6710	Window	1.8 V to 36 V	0.75%
TLV6713	Non-Inverting Single Channel	1.8 V to 36 V	0.75%

6 Pin Configuration and Functions

DDC Package
6-Pin SOT
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	DDC		
GND	2, 4, 6	—	Connect all three pins to ground.
OUT	1	O	SENSE comparator open-drain output. OUT is driven low when the voltage at this comparator is below (V_{IT-}). The output goes high when the sense voltage returns above the respective threshold (V_{IT+}).
SENSE	3	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT is driven low.
VDD	5	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage(2)	VDD	–0.3	20	V
	OUT	–0.3	20	
	SENSE	–0.3	7	
Current	OUT (output sink current)		40	mA
Temperature	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage		1.8		18	V
V_I	Input voltage	SENSE	0		6.5	V
V_O	Output voltage	OUT	0		18	V

7.4 Thermal Information

THERMAL METRIC (1)		TLV6703 DDC (SOT) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	204.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	52.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor an IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to +125°C, and 1.8 V < V_{DD} < 18 V (unless otherwise noted). Typical values are at T_J = 25°C and V_{DD} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(POR)}$	Power-on reset voltage (1)	V_{OL}max = 0.2 V, output sink current = 15 µA			0.8	V
V_{IT+}	Positive-going input threshold voltage	V_{DD} = 1.8V and 18 V, T_J = 25°C	398	400	402.5	mV
		V_{DD} = 1.8V and 18 V, T_J = –40°C to 125°C	396		404	
$V_{IT–}$	Negative-going input threshold voltage	V_{DD} = 1.8V and 18 V, T_J = 25°C	391.6	394.5	397.5	mV
		V_{DD} = 1.8V and 18 V, T_J = –40°C to 125°C	387		400	
V_{hys}	Hysteresis voltage (hys = V_{IT+} – $V_{IT–}$)			5.5	12	mV
$I_{(SENSE)}$	Input current (at the SENSE pin)	V_{DD} = 1.8 V and 18 V, V_I = 6.5 V	–25	1	25	nA
V_{OL}	Low-level output voltage	V_{DD} = 1.3 V, output sink current = 0.4 mA			250	mV
		V_{DD} = 1.8 V, output sink current = 3 mA			250	
		V_{DD} = 5 V, output sink current = 5 mA			250	
$I_{lkg(OD)}$	Open-drain output leakage-current	V_{DD} = 1.8 V and 18 V, V_O = V_{DD}			300	nA
		V_{DD} = 1.8 V, V_O = 18 V			300	
I_{DD}	Supply current	V_{DD} = 1.8 V, no load		5.5	11	µA
		V_{DD} = 5 V		6	13	
		V_{DD} = 12 V		6	13	
		V_{DD} = 18 V		7	13	
UVLO	Undervoltage lockout (2)	V_{DD} falling	1.3		1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) When V_{DD} falls below UVLO, OUT is driven low. The output cannot be determined below $V_{(POR)}$.

7.6 Timing Requirements

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$t_{pd(HL)}$	High-to-low propagation delay (1)	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV, see Figure 1		18		µs
$t_{pd(LH)}$	Low-to-high propagation delay (1)	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV, see Figure 1		29		µs
$t_{d(start)}$	Start-up delay (2)			150		µs

(1) High-to-low and low-to-high refers to the transition at the input pin (SENSE).
(2) During power on, V_{DD} must exceed 1.8 V for at least 150 µs before the output is in a correct state.

7.7 Switching Characteristics

over operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		2.2		µs
t_f	Output fall time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		0.22		µs

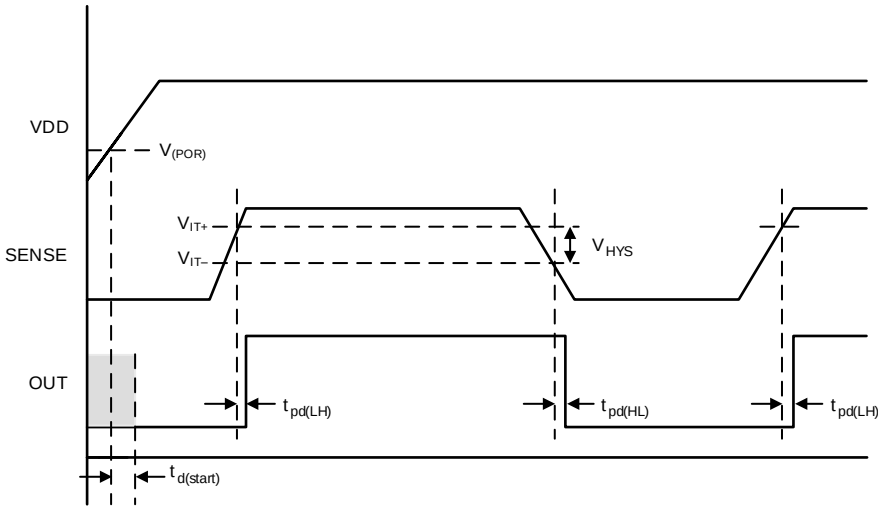


Figure 1. Timing Diagram

7.8 Typical Characteristics

at T_J = 25°C and V_{DD} = 5 V (unless otherwise noted)

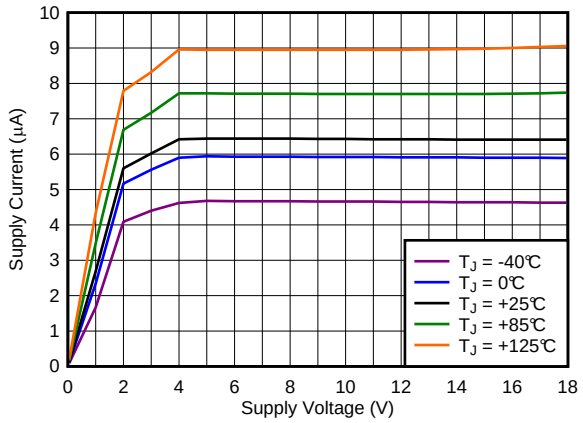


Figure 2. Supply Current (I_{DD}) vs Supply Voltage (V_{DD})

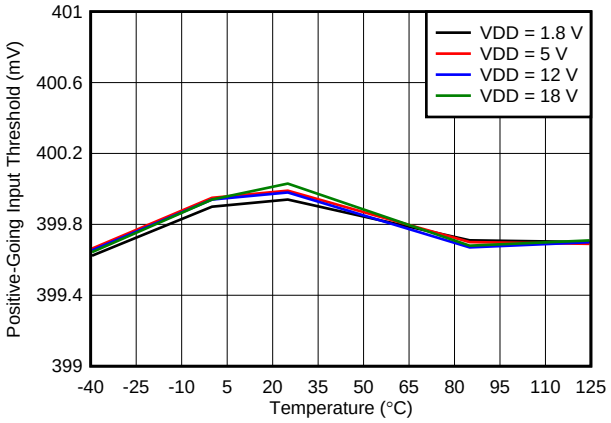


Figure 3. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

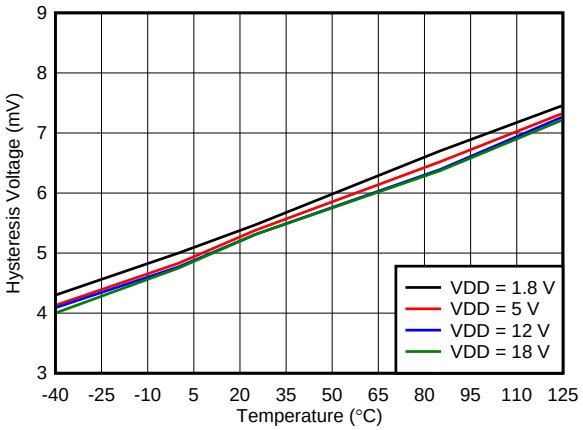


Figure 4. Hysteresis (V_{hys}) vs Temperature

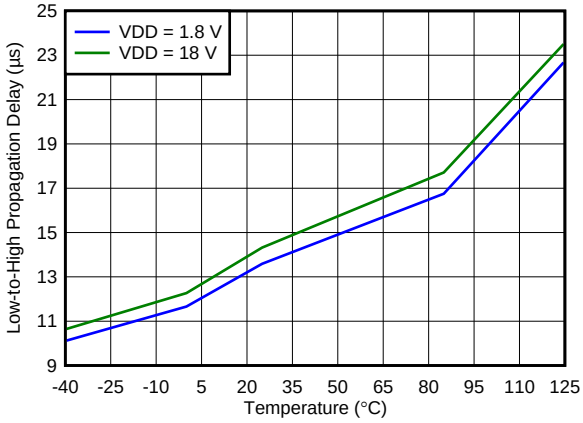


Figure 5. Propagation Delay vs Temperature (High-to-Low Transition at Sense)

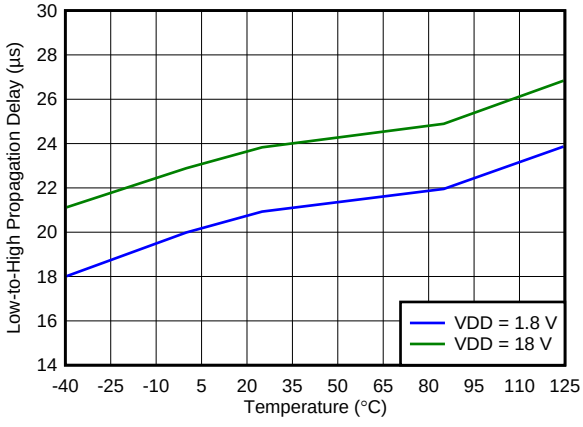


Figure 6. Propagation Delay vs Temperature (Low-to-High Transition at Sense)

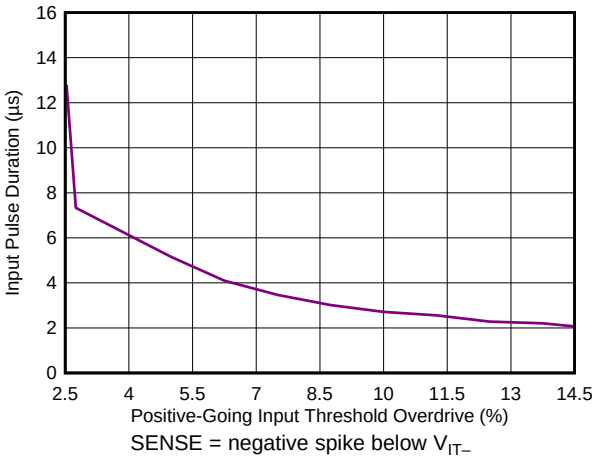


Figure 7. Minimum Pulse Width vs Threshold Overdrive Voltage

Typical Characteristics (continued)

at T_J = 25°C and V_{DD} = 5 V (unless otherwise noted)

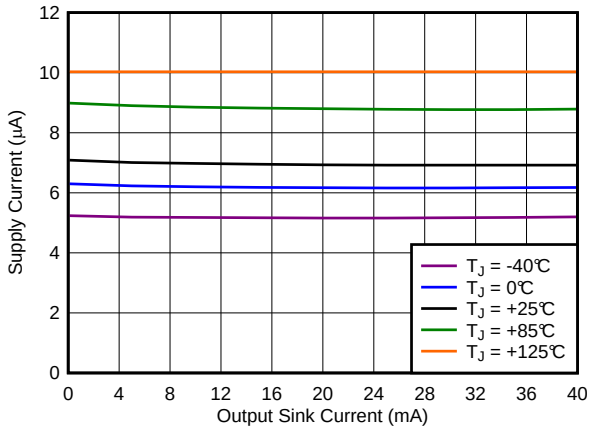


Figure 8. Supply Current (I_{DD}) vs Output Sink Current

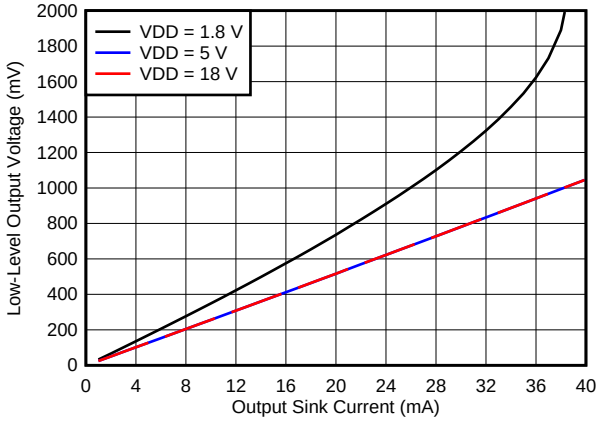


Figure 9. Output Voltage Low (V_{OL}) vs Output Sink Current (–40°C)

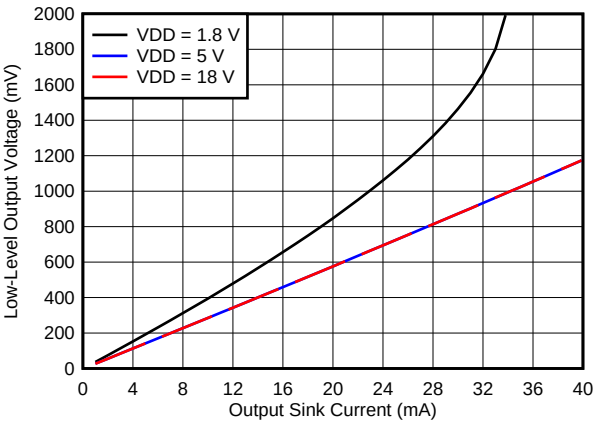


Figure 10. Output Voltage Low (V_{OL}) vs Output Sink Current (0°C)

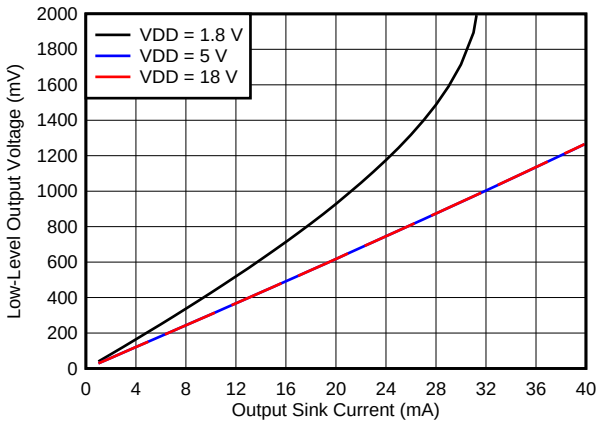


Figure 11. Output Voltage Low (V_{OL}) vs Output Sink Current (25°C)

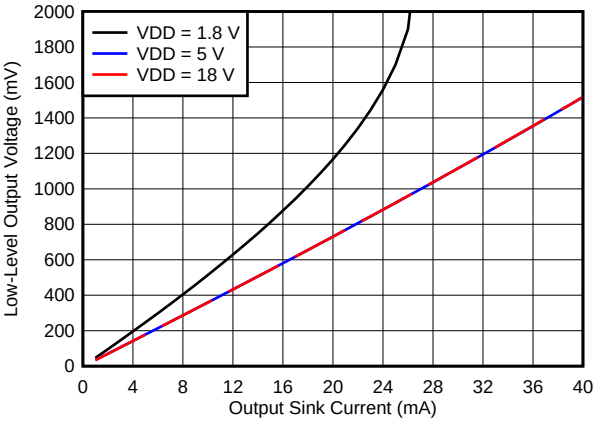


Figure 12. Output Voltage Low (V_{OL}) vs Output Sink Current (85°C)

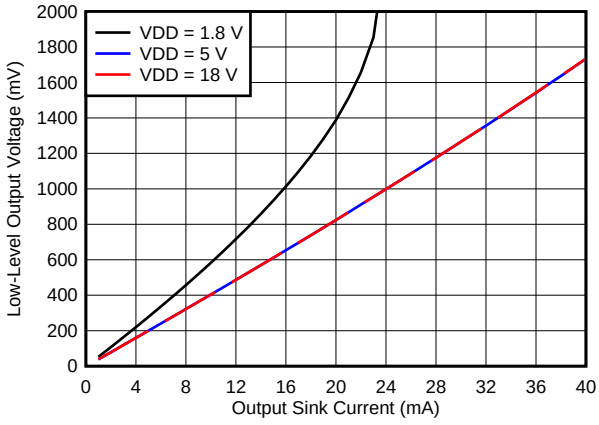


Figure 13. Output Voltage Low (V_{OL}) vs Output Sink Current (125°C)

8 Detailed Description

8.1 Overview

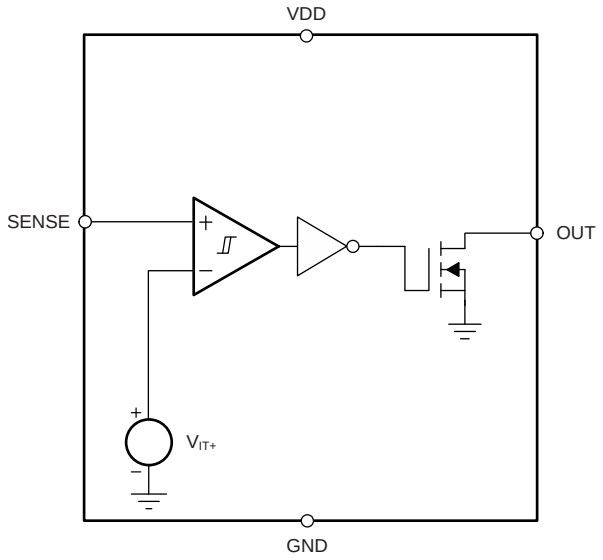
The TLV6703 provides precision voltage detection. The TLV6703 is a wide-supply voltage range (1.8 V to 18 V) comparator with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The output is also rated to 18 V, independant of supply voltage, and can sink up to 40 mA.

The TLV6703 asserts the output signal, as shown in Table 2. To monitor any voltage above 0.4 V, set the input using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. Broad voltage thresholds are supported that enable the device for use in a wide array of applications.

Table 2. TLV6703 Truth Table

CONDITION	OUTPUT	OUTPUT STATE
SENSE > V_{IT+}	OUT high	Output high impedance
SENSE < V_{IT-}	OUT low	Output sinking

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Pin (SENSE)

The TLV6703 comparator has two inputs: one external input, and one input internally connected to the internal 400mV reference. The comparator rising threshold is trimmed to be equal to the reference voltage (400 mV). The comparator also has a built-in falling hysteresis that makes the device less sensitive to supply-rail noise and provides stable operation.

The comparator input (SENSE) is able to swing from ground to 6.5 V, regardless of the device supply voltage. Although not required in most cases, to reduce sensitivity to transients and layout parasitics for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor at the comparator input.

OUT is driven to logic low when the input SENSE voltage drops below (V_{IT-}). When the voltage exceeds V_{IT+}, the output (OUT) goes to a high-impedance state; see Figure 1.

8.3.2 Output Pin (OUT)

In a typical TLV6703 application, the output is connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6703 device provides an open-drain output (OUT). Use a pullup resistor to hold this line high when the output goes to high impedance (not asserted). To connect the output to another device at the correct interface-voltage level, connect a pullup resistor to the proper voltage rail. The TLV6703 output can be pulled up to 18 V, independent of the device supply voltage.

Table 2 and the *Input Pin (SENSE)* section describe how the output is asserted or deasserted. See Figure 1 for a timing diagram that describes the relationship between threshold voltage and the respective output.

8.3.3 Immunity to Input-Pin Voltage Transients

The TLV6703 is relatively immune to short voltage transient spikes on the sense pin. Sensitivity to transients depends on both transient duration and amplitude; see Figure 7, *Minimum Pulse Width vs Threshold Overdrive Voltage*.

8.4 Device Functional Modes

8.4.1 Normal Operation (V_{DD} > UVLO)

When the voltage on V_{DD} is greater than 1.8 V for at least 150 µs, the OUT signal correspond to the voltage on SENSE as listed in Table 2.

8.4.2 Undervoltage Lockout ($V_{(POR)} < V_{DD} <$ UVLO)

When the voltage on V_{DD} is less than the device UVLO voltage, and greater than the power-on reset voltage, $V_{(POR)}$, the OUT signal is asserted regardless of the voltage on SENSE.

8.4.3 Power-On Reset ($V_{DD} < V_{(POR)}$)

When the voltage on V_{DD} is lower than the required voltage to internally pull the asserted output to GND ($V_{(POR)}$), SENSE is in a high-impedance state.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV6703 device is a wide-supply voltage comparator that operates over a V_{DD} range of 1.8 V to 18 V. The device has a high-accuracy comparator with an internal 400-mV reference and an open-drain output rated to 18 V for precision voltage detection. The device can be used as a voltage monitor. The monitored voltage are set with the use of external resistors.

9.1.1 V_{PULLUP} to a Voltage Other Than V_{DD}

The output is often tied to V_{DD} through a resistor. However, some applications may require the output to be pulled up to a higher or lower voltage than V_{DD} to correctly interface with the reset and enable pins of other devices.

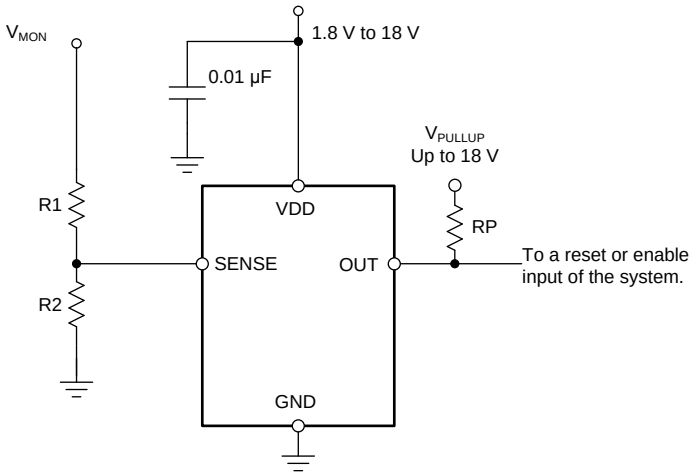


Figure 14. Interfacing to a Voltage Other Than V_{DD}

Application Information (continued)

9.1.2 Monitoring V_{DD}

Many applications monitor the same rail that is powering V_{DD}. In these applications the resistor divider is simply connected to the V_{DD} rail.

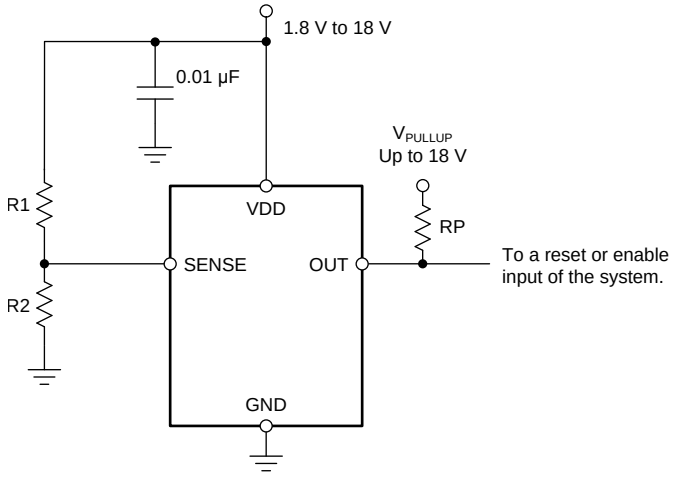
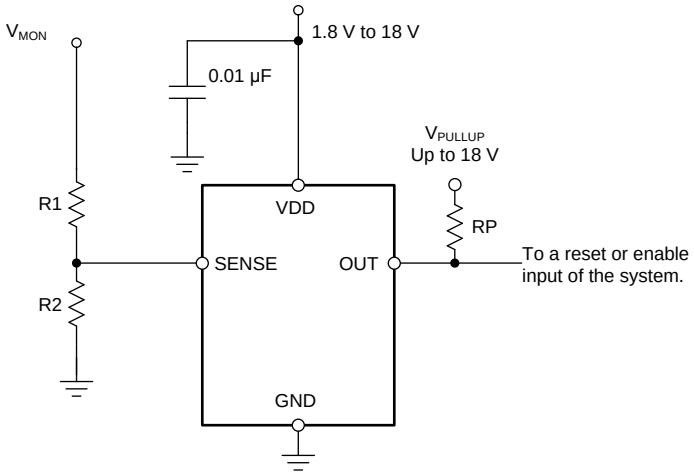


Figure 15. Monitoring the Same Voltage as V_{DD}

9.1.3 Monitoring a Voltage Other Than V_{DD}

Some applications monitor rails other than the one that is powering V_{DD}. In these types of applications the resistor divider used to set the desired threshold is connected to the rail that is being monitored.



NOTE: The input can monitor a voltage greater than maximum V_{DD} with the use of an external resistor divider network.

Figure 16. Monitoring a Voltage Other Than V_{DD}

9.2 Typical Application

The TLV6703 device is a wide-supply voltage comparator that operates over a V_{DD} range of 1.8 to 18 V. The monitored voltage is set with the use of external resistors, so the device can be used either as a precision voltage monitor.

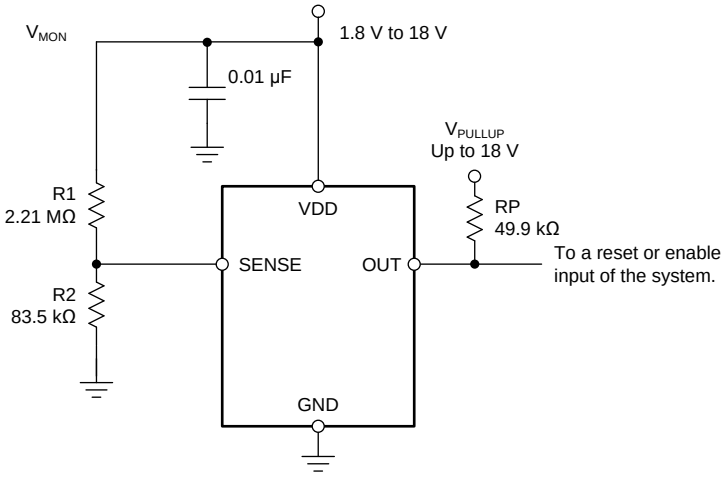


Figure 17. Wide VIN Voltage Monitor

9.2.1 Design Requirements

For this design example, use the values summarized in Table 3 as the input parameters.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	12-V nominal rail with maximum falling threshold of 10%	$V_{MON(UV)}$= 10.99 V (8.33%)

9.2.2 Detailed Design Procedure

9.2.2.1 Resistor Divider Selection

The resistor divider values and target threshold voltage can be calculated by using Equation 1 to determine $V_{MON(UV)}$.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-} \quad (1)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected

Choose R_{TOTAL} (= R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSE pin. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, refer to application report SLVA450, *Optimizing Resistor Dividers at a Comparator Input*, available for download from www.ti.com.

9.2.2.2 Pullup Resistor Selection

To ensure the proper voltage level, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ($I_{lkg(OD)}$) multiplied by the resistor is greater than the desired logic-high voltage. These values are specified in the *Electrical Characteristics* .

Use Equation 2 to calculate the value of the pullup resistor.

$$\frac{(V_{HI} - V_{PU})}{I_{lkg(OD)}} \geq R_{PU} \geq \frac{V_{PU}}{I_O} \quad (2)$$

9.2.2.3 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 0.1-µF low equivalent series resistance (ESR) capacitor across the VDD and GND pins. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

9.2.2.4 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1-nF to 10-nF bypass capacitor from the comparator input (SENSE) to the GND pin for good analog design practice. This capacitor placement reduces device sensitivity to transients.

9.2.3 Application Curves

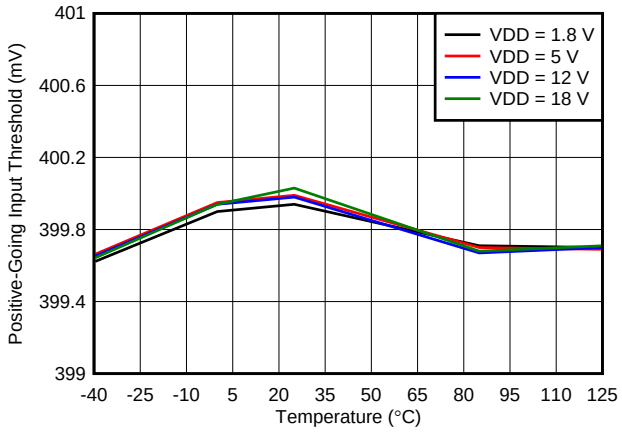


Figure 18. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

9.3 Dos and Don'ts

Do connect a 0.1-µF decoupling capacitor from V_{DD} to GND for best system performance.

If the monitored rail is noisy, do connect a decoupling capacitor from the comparator input (sense) to GND.

Don't use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparator without also accounting for the effect to the accuracy.

Don't use a pullup resistor that is too small, because the larger current sunk by the output then exceeds the desired low-level output voltage (V_{OL}).

10 Power-Supply Recommendations

These devices operate from an input voltage supply range between 1.8 V and 18 V.

11 Layout

11.1 Layout Guidelines

Placing a 0.1-µF capacitor close to the VDD pin to reduce the input impedance to the device is good analog design practice.

11.2 Layout Example

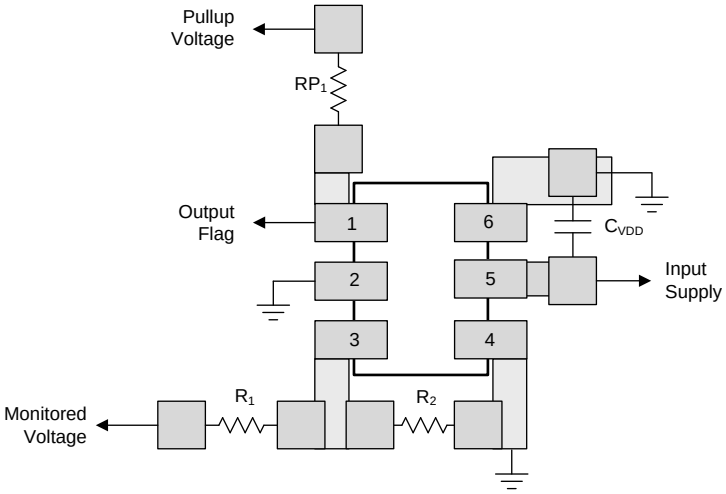


Figure 19. Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

*DIP 适配器评估模块*可以将 SOT-23-6 封装转换为标准 DIP-6 引脚排列以便轻松构建原型和进行工作台评估。

12.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV6703DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MR1	Samples
TLV6703DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1MR1	Samples
TLV6703DSER	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

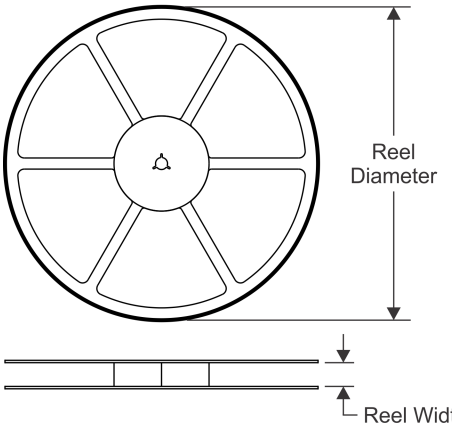
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

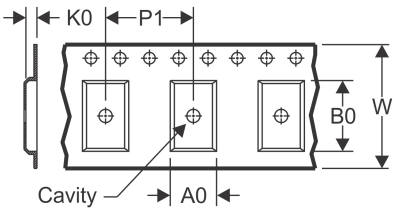
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

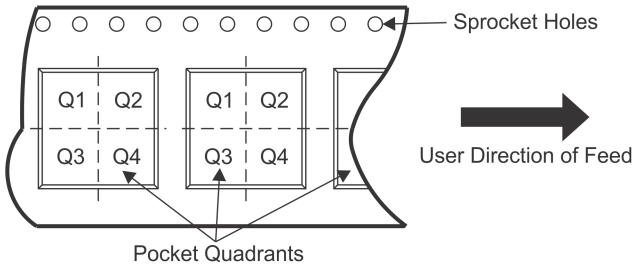


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

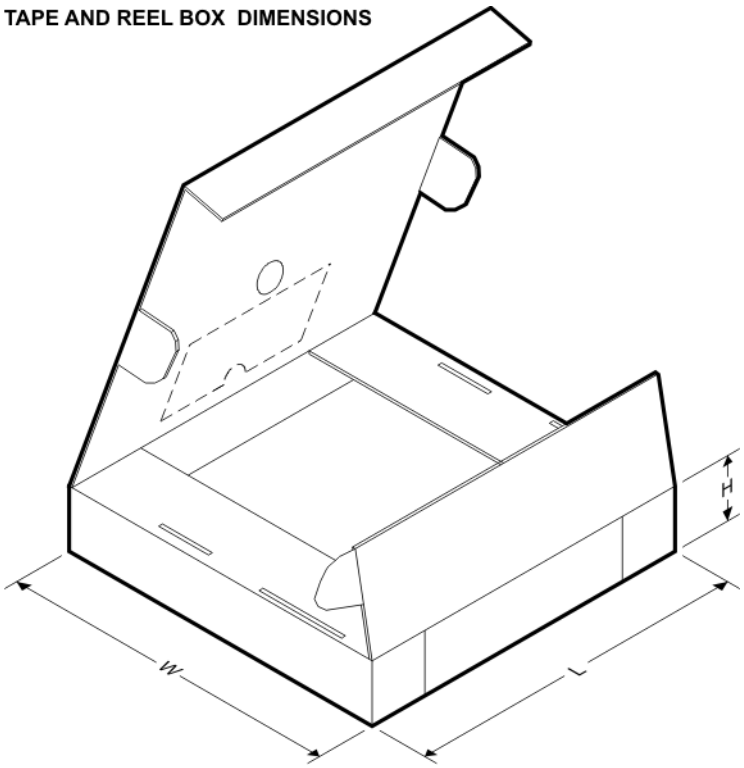
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6703DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6703DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6703DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2

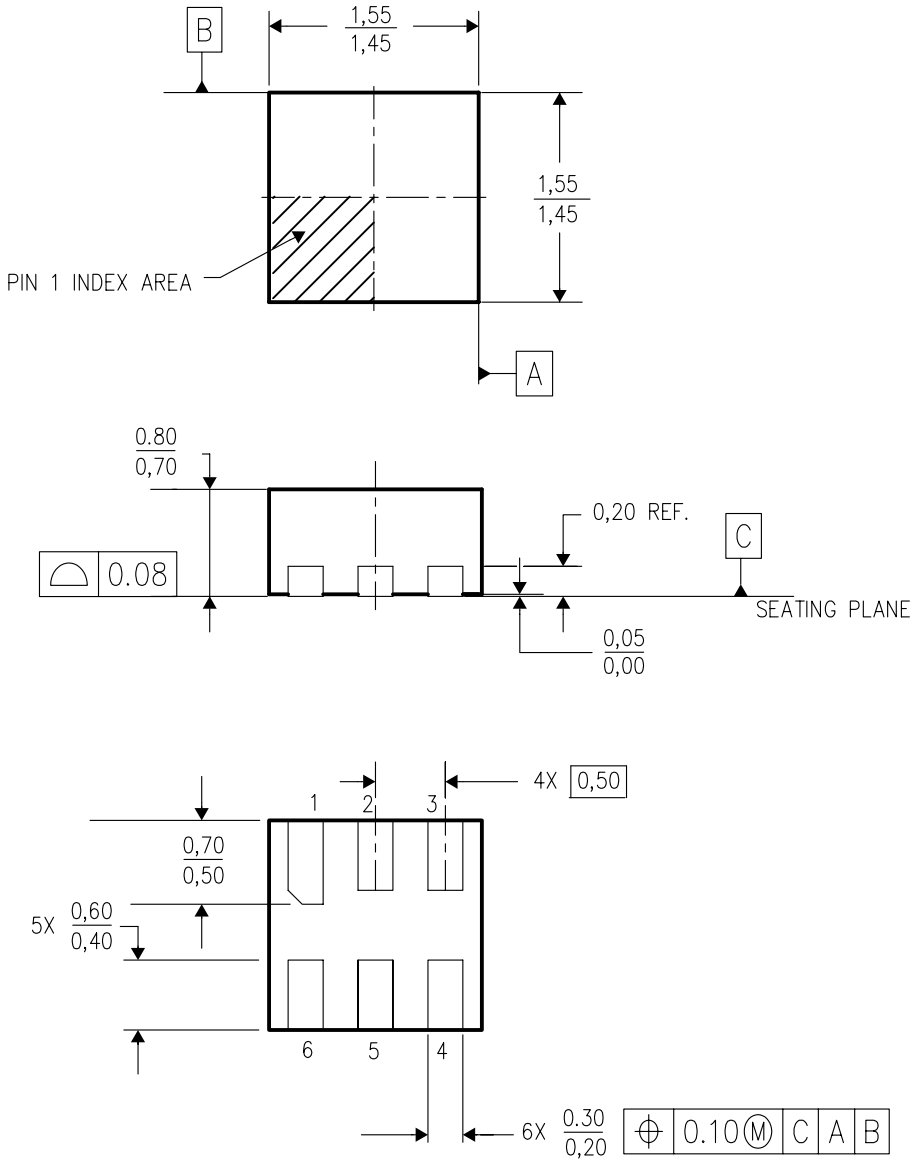
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6703DDCR	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TLV6703DDCT	SOT-23-THIN	DDC	6	250	213.0	191.0	35.0
TLV6703DSER	WSON	DSE	6	3000	205.0	200.0	33.0

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

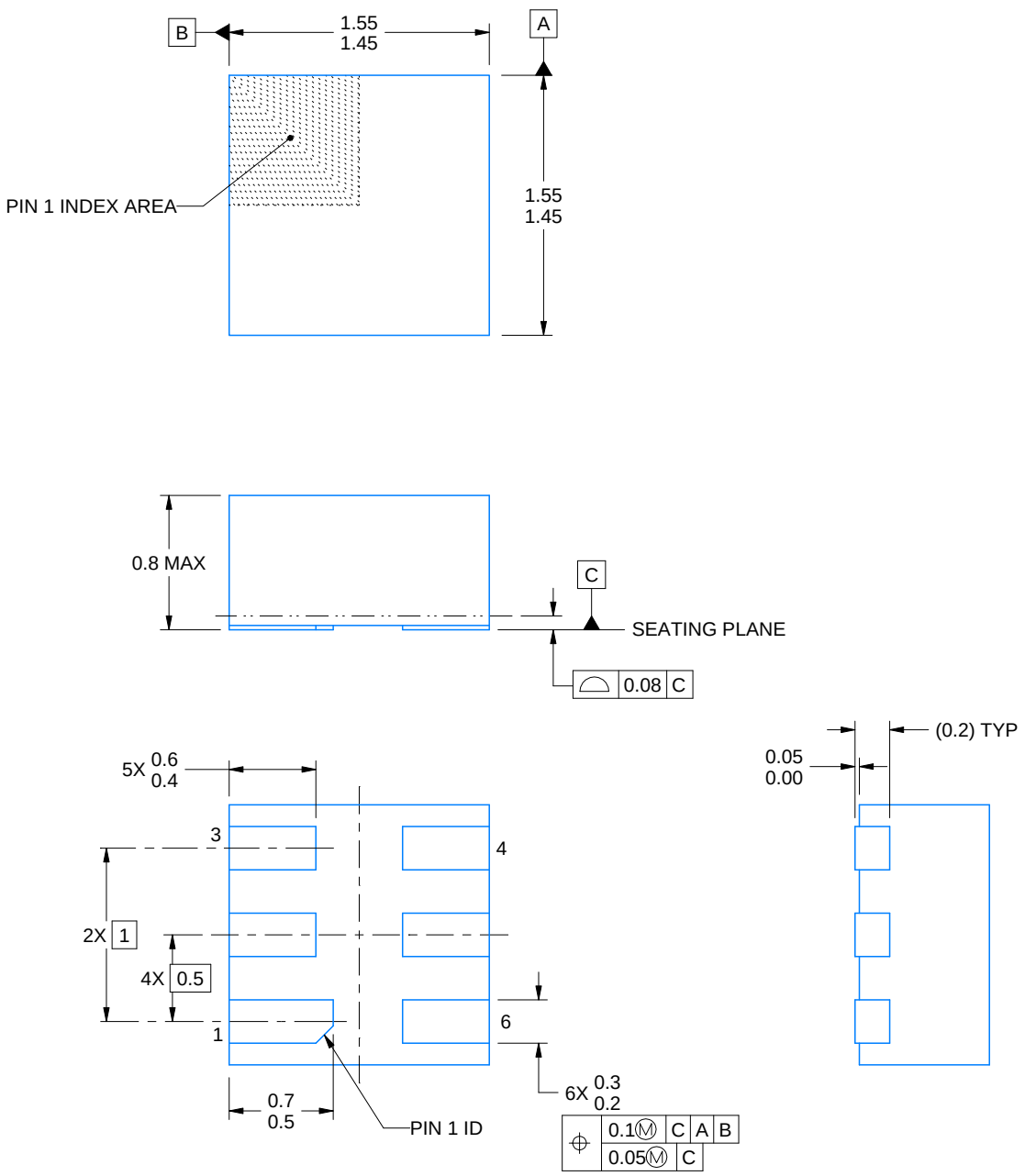
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

DSE0006A

PACKAGE OUTLINE

WSON - 0.8 mm max height

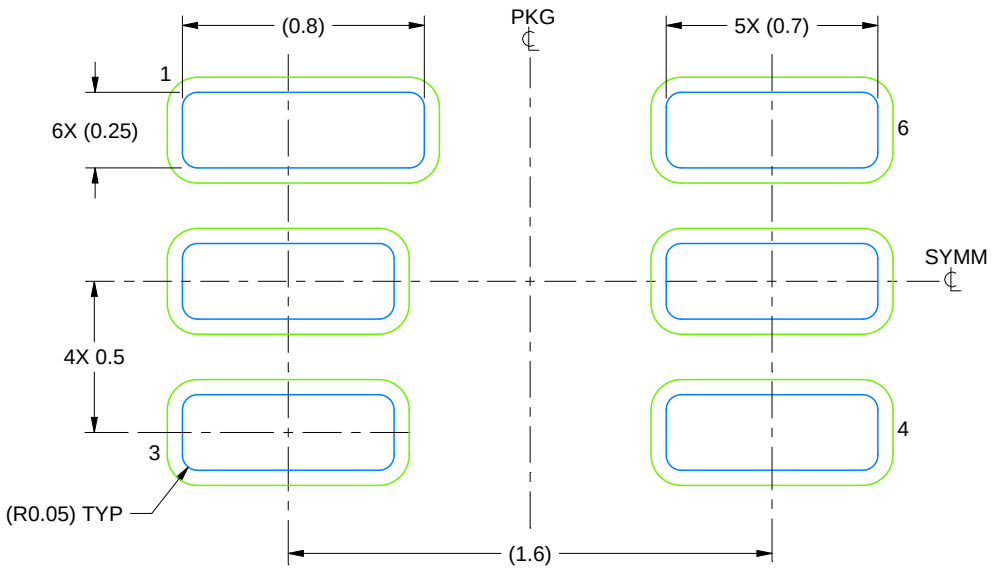
PLASTIC SMALL OUTLINE - NO LEAD



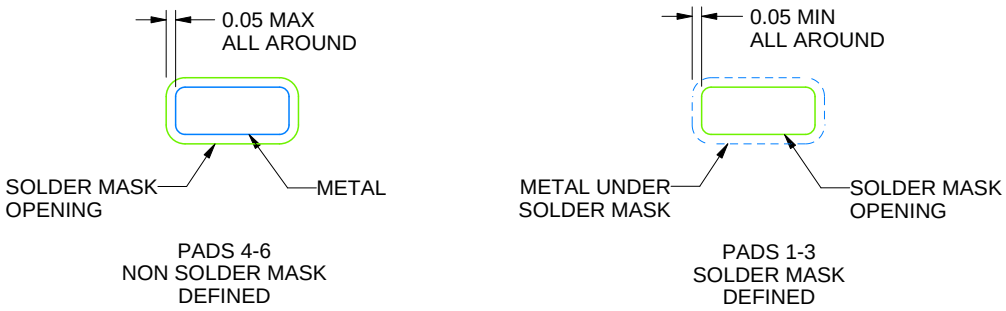
4220552/A 04/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X

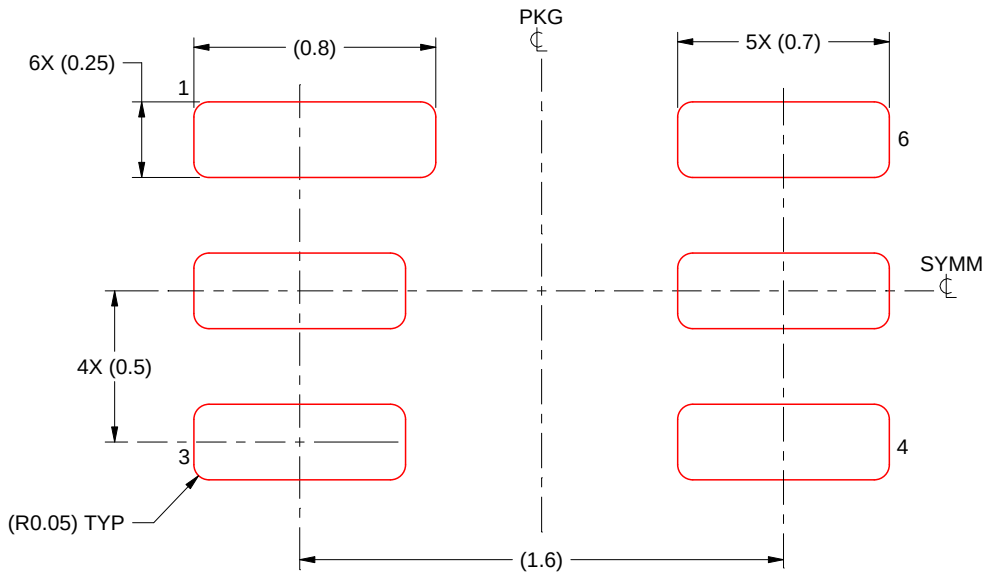


SOLDER MASK DETAILS

4220552/A 04/2021

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

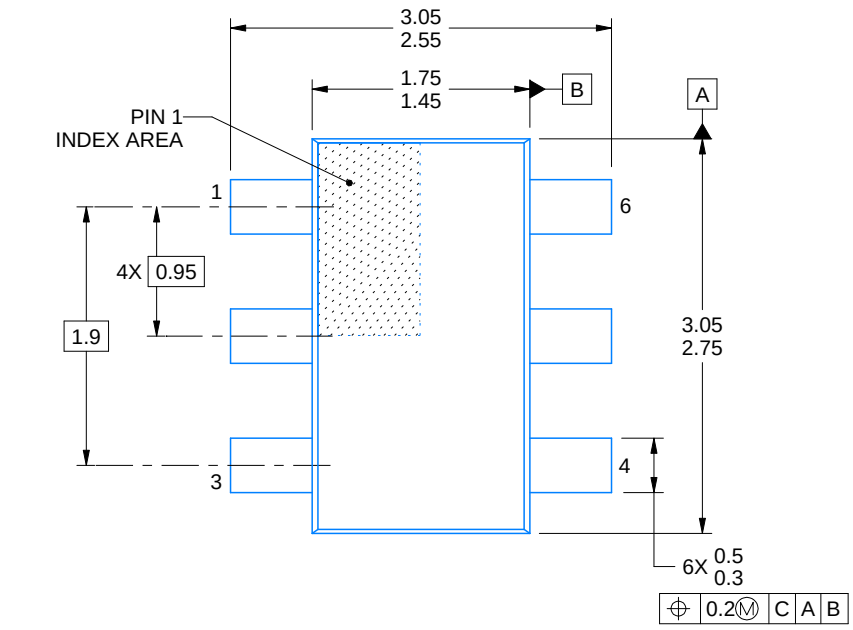
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

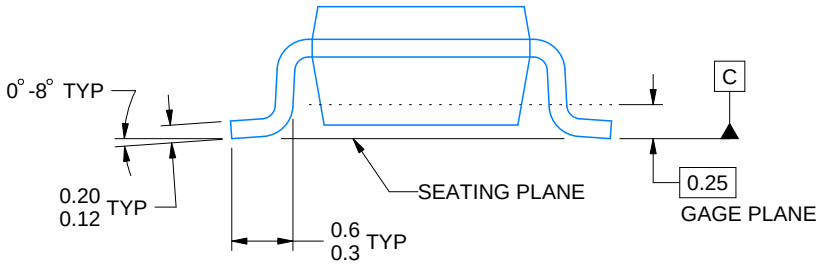
PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

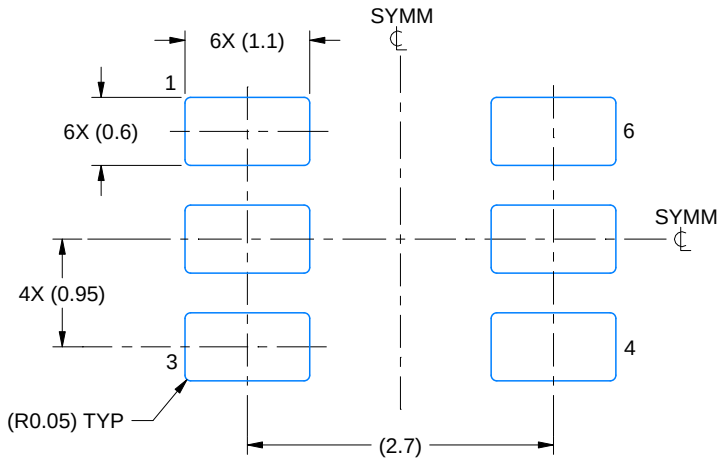




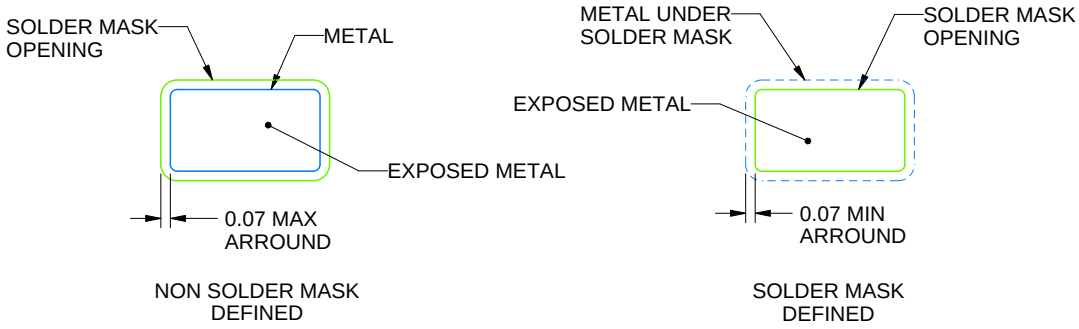
4214841/C 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

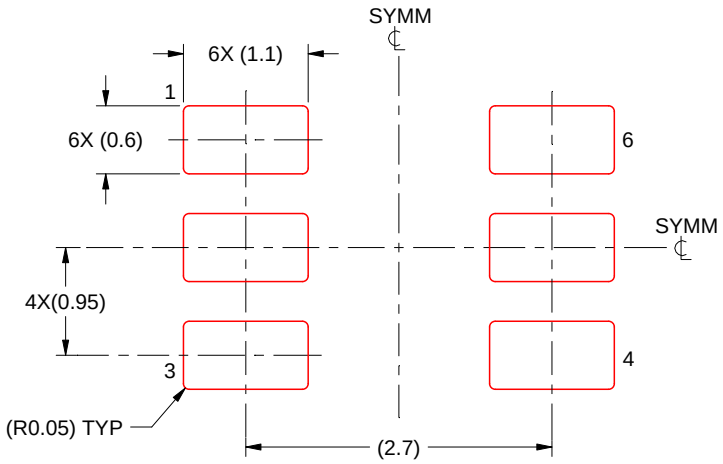


SOLDERMASK DETAILS

4214841/C 04/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/C 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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