

# SN54ABTH245, SN74ABTH245 OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS663D – APRIL 1996 – REVISED SEPTEMBER 1999

- State-of-the-Art *EPIC-IIB*<sup>™</sup> BiCMOS Design Significantly Reduces Power Dissipation
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- High-Drive Outputs (–32-mA  $I_{OH}$ , 64-mA  $I_{OL}$ )
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), Thin Shrink Small-Outline (PW), and Thin Very Small-Outline (DGV) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

## description

These octal bus transceivers are designed for asynchronous communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

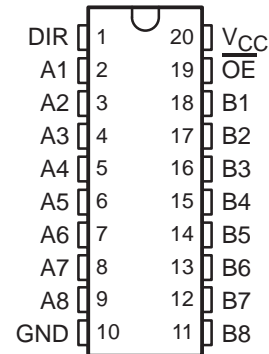
When  $V_{CC}$  is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

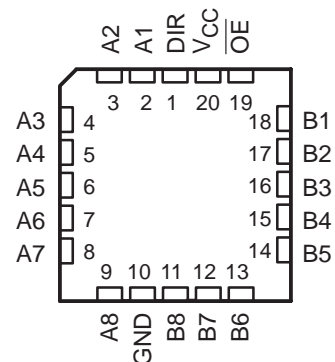
Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN54ABTH245 is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABTH245 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABTH245 . . . J OR W PACKAGE  
SN74ABTH245 . . . DB, DGV, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ABTH245 . . . FK PACKAGE  
(TOP VIEW)



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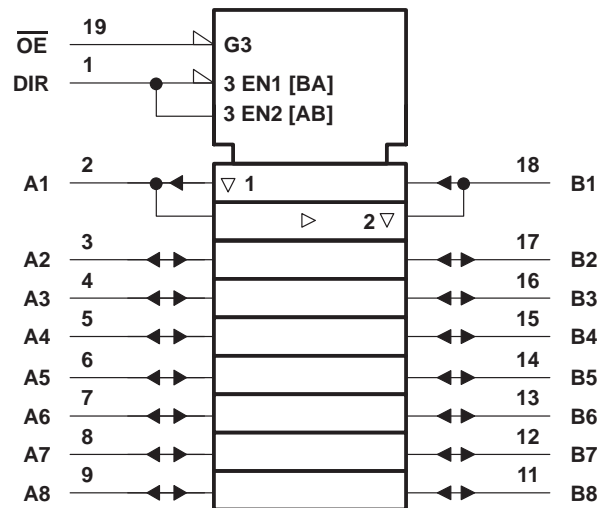
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SCBS663D – APRIL 1996 – REVISED SEPTEMBER 1999

FUNCTION TABLE

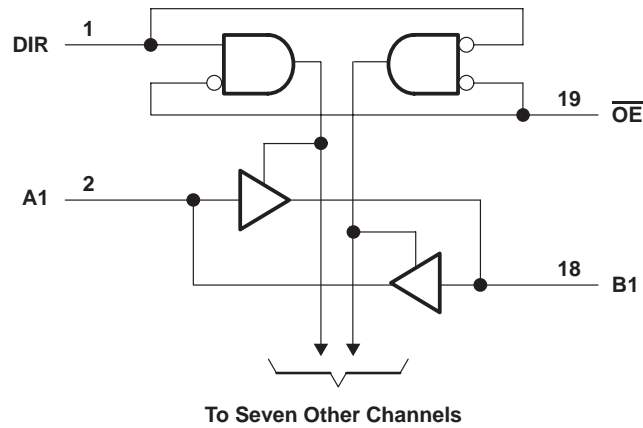
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



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SCBS663D – APRIL 1996 – REVISED SEPTEMBER 1999

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 7 V
Input voltage range, $V_I$ (except I/O ports) (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ .....	–0.5 V to 5.5 V
Current into any output in the low state, $I_O$ : SN54ABTH245 .....	96 mA
SN74ABTH245 .....	128 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–18 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package .....	70°C/W
DGV package .....	92°C/W
DW package .....	58°C/W
N package .....	69°C/W
PW package .....	83°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51.

## recommended operating conditions (see Note 3)

		SN54ABTH245		SN74ABTH245		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	4.5	5.5	4.5	5.5	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5		5	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate				200	$\mu$ s/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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SCBS663D – APRIL 1996 – REVISED SEPTEMBER 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T <sub>A</sub> = 25°C			SN54ABTH245		SN74ABTH245		UNIT		
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX			
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2		-1.2		-1.2	V		
V <sub>OH</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -3 mA			2.5		2.5		2.5	V		
	V <sub>CC</sub> = 5 V, I <sub>OH</sub> = -3 mA			3		3		3			
	V <sub>CC</sub> = 4.5 V	I <sub>OH</sub> = -24 mA			2		2				
I <sub>OH</sub> = -32 mA				2*				2			
V <sub>OL</sub>	V <sub>CC</sub> = 4.5 V	I <sub>OL</sub> = 48 mA				0.55		0.55	V		
		I <sub>OL</sub> = 64 mA				0.55*		0.55			
V <sub>hys</sub>				100					mV		
I <sub>I</sub>	Control inputs	V <sub>CC</sub> = 0 to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND				±1		±1	±1	µA	
	A or B ports	V <sub>CC</sub> = 2.1 V to 5.5 V, V <sub>I</sub> = V <sub>CC</sub> or GND				±20		±100	±20		
I <sub>I</sub> (hold)	V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0.8 V			100		100		100	µA	
		V <sub>I</sub> = 2 V			-100		-100		-100		
I <sub>OZPU</sub>	V <sub>CC</sub> = 0 to 2.1 V, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$					±50**		±50**	±50	µA	
I <sub>OZPD</sub>	V <sub>CC</sub> = 2.1 V to 0, V <sub>O</sub> = 0.5 V to 2.7 V, $\overline{OE} = X$					±50**		±50**	±50	µA	
I <sub>off</sub>	V <sub>CC</sub> = 0, V <sub>I</sub> or V <sub>O</sub> ≤ 4.5 V					±100			±100	µA	
I <sub>CEX</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 5.5 V	Outputs high				50		50	50	µA	
I <sub>O‡</sub>	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 2.5 V				-50	-140	-180	-50	-180	-180	mA
I <sub>CC</sub>	A or B ports	V <sub>CC</sub> = 5.5 V, I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND	Outputs high			5	250		250	250	µA
			Outputs low			22	30		30	30	mA
			Outputs disabled			1	250		250	250	µA
ΔI <sub>CC</sub> §	Data inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	Outputs enabled			1.5		1.5		1.5	mA
			Outputs disabled			1.5		1.5		1.5	mA
	Control inputs	V <sub>CC</sub> = 5.5 V, One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND				1.5		1.5		1.5	mA
C <sub>i</sub>	Control inputs	V <sub>I</sub> = 2.5 V or 0.5 V				4				pF	
C <sub>io</sub>	A or B ports	V <sub>O</sub> = 2.5 V or 0.5 V				8				pF	

\* On products compliant to MIL-PRF-38535, this parameter does not apply.

\*\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at V<sub>CC</sub> = 5 V.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V<sub>CC</sub> or GND.



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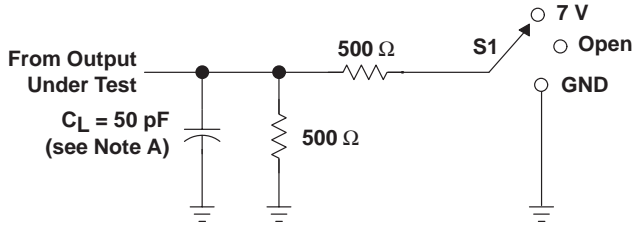
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5$ V, $T_A = 25^\circ$ C			SN54ABTH245		SN74ABTH245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A or B	B or A	1	2	3.2	0.8	3.8	1	3.6	ns
$t_{PHL}$			1	2.6	3.5	0.8	4.2	1	3.9	
$t_{PZH}$	$\overline{OE}$	A or B	2	3.5	4.5	1.2	6.2	2	5.6	ns
$t_{PZL}$			1.9	4	5.3	1.3	7	1.9	6.2	
$t_{PHZ}$	$\overline{OE}$	A or B	2.2	4.4	5.4	2.2	6.1	2.2	5.9	ns
$t_{PLZ}$			1.5	3	4	1	4.9	1.5	4.5	
$t_{sk(o)}$					0.5			0.5	ns	

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**OCTAL BUS TRANSCEIVERS**  
**WITH 3-STATE OUTPUTS**

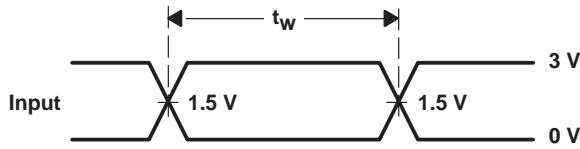
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**PARAMETER MEASUREMENT INFORMATION**

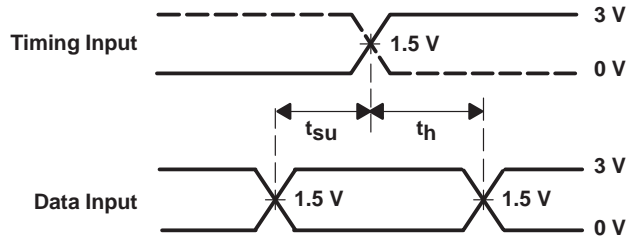


TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open

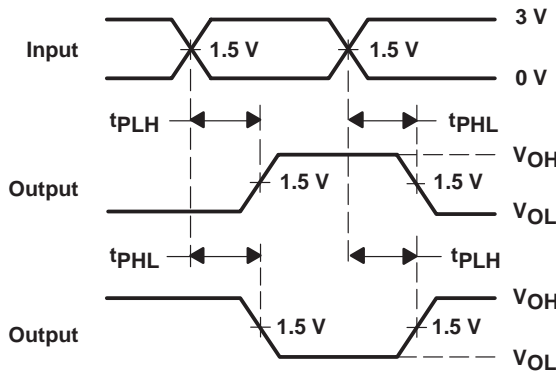
**LOAD CIRCUIT**



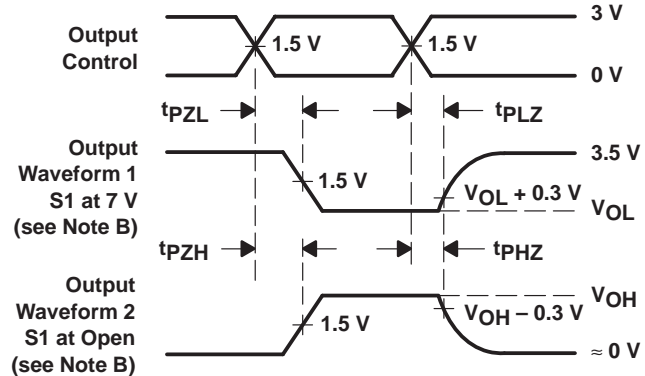
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 D. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9762301Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9762301Q2A SNJ54ABTH 245FK	<a href="#">Samples</a>
5962-9762301QSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9762301QS A SNJ54ABTH245W	<a href="#">Samples</a>
SN74ABTH245DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABH245	<a href="#">Samples</a>
SN74ABTH245DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH245	<a href="#">Samples</a>
SN74ABTH245DWE4	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH245	<a href="#">Samples</a>
SN74ABTH245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABTH245	<a href="#">Samples</a>
SN74ABTH245N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABTH245N	<a href="#">Samples</a>
SN74ABTH245PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABH245	<a href="#">Samples</a>
SNJ54ABTH245FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9762301Q2A SNJ54ABTH 245FK	<a href="#">Samples</a>
SNJ54ABTH245W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9762301QS A SNJ54ABTH245W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ABTH245, SN74ABTH245 :**

- Catalog : [SN74ABTH245](#)
- Military : [SN54ABTH245](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABTH245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABTH245DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ABTH245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABTH245DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74ABTH245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ABTH245PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9762301Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9762301QSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74ABTH245DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABTH245DWE4	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ABTH245N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ABTH245FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54ABTH245W	W	CFP	20	1	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

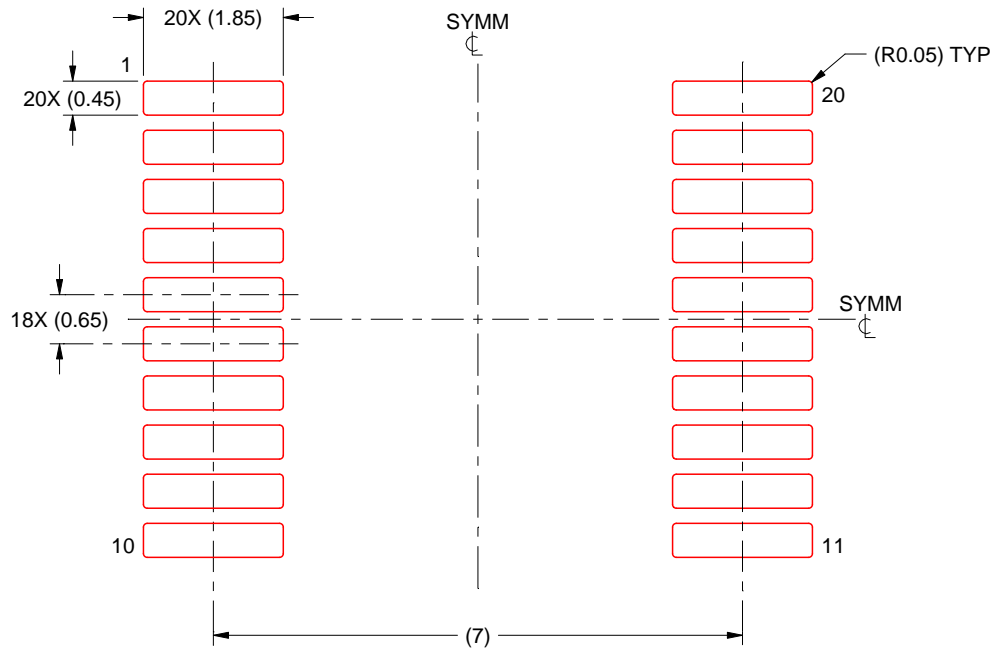
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

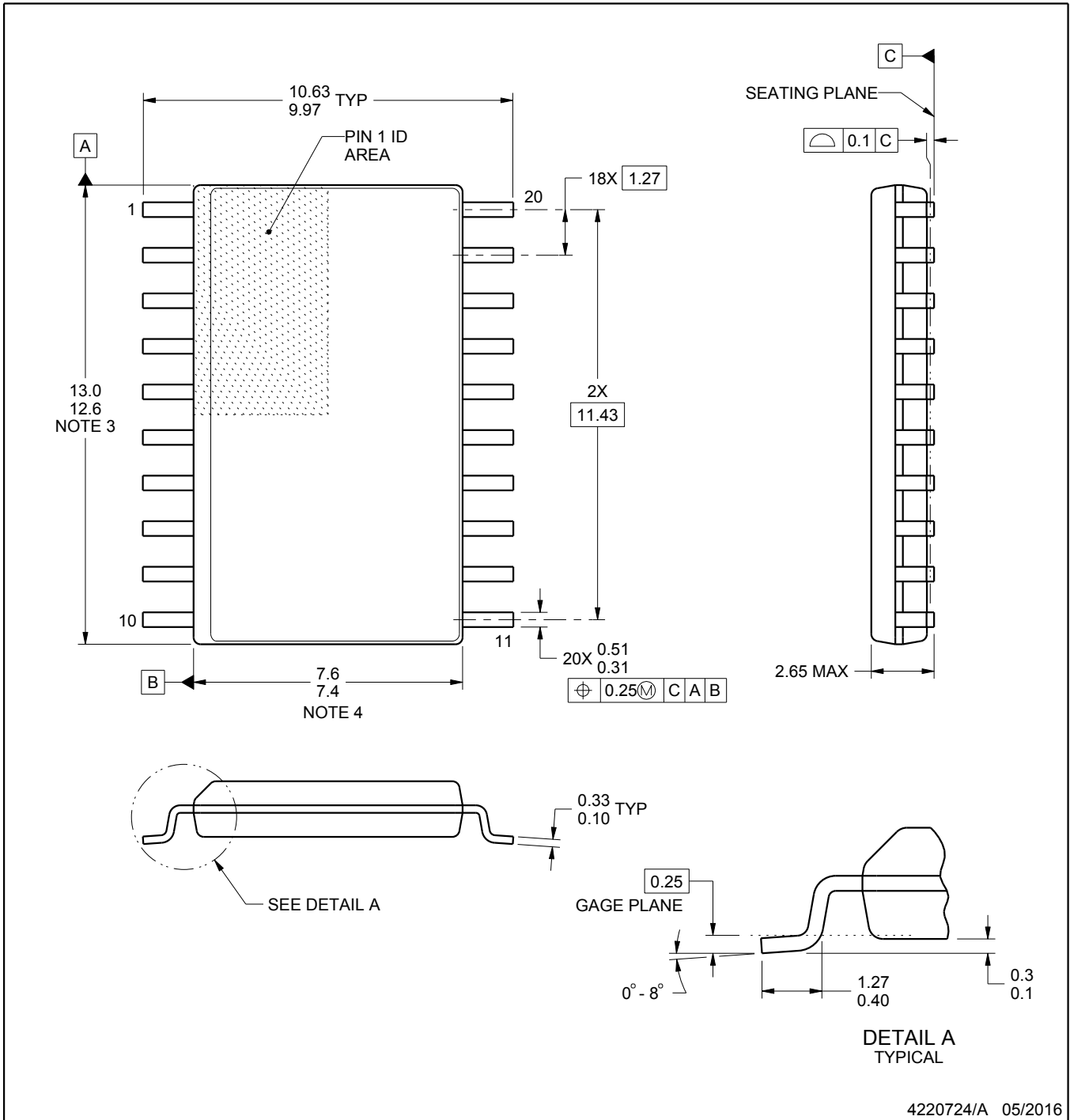
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

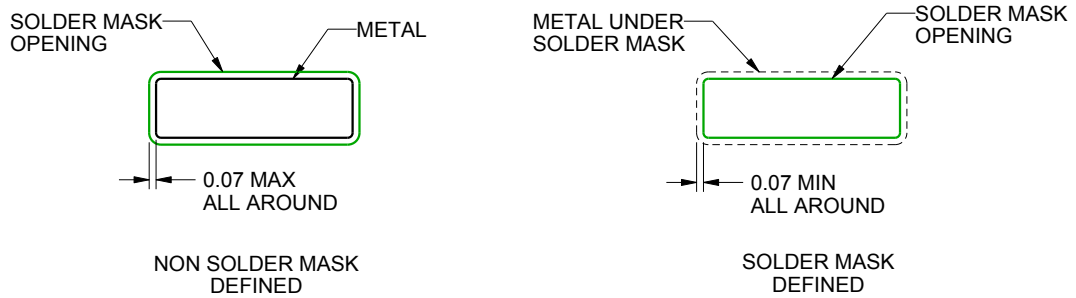
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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