适用于 DLP553x-Q1 芯片组的 DLPC230-Q1 汽车用 DMD 控制器

1 特性

- 符合汽车类应用的 要求
- 具有符合 AEC-Q100 标准的下列特性： 中
  - 器件温度等级 2 级：环境工作温度范围为 –40°C 至 105°C
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- DMD 显示控制器支持：
  - DLP5530-Q1 汽车内部显示屏芯片组
  - DLP5531-Q1 汽车外部照明芯片组
- 视频处理
  - 扩展输入图像以匹配 DMD 分辨率
  - 边框调整：垂直图像位置 ±50%，水平图像位置 ±10%，降低了机械对齐 (HUD) 需求
  - 支持两倍或四倍像素，以允许低分辨率视频输入
  - 伽马校正
- 具备错误矫正 (ECC) 功能的嵌入式 处理器
  - 片上诊断和自检能力
  - 系统诊断包括温度监控、器件接口监控和光电二极管监控
  - 集成平滑调光管理
  - 可配置 GPIO
- 无需外部 RAM，内部 SRAM 可用于图像处理
- 600MHz Sub-LVDS DMD 接口，以实现低功率和低排放
- 扩频计时，以降低 EMI
- 视频输入接口
  - 高达 110MHz 的单 OpenLDI (FPD-Link I) 端口
  - 高达 110MHz 的 24 位 RGB 并行接口 中的并行接口最大像素时钟，并进行了水平边框调整
- 可配置主机控制接口
  - 串行外设接口 (SPI) 10MHz
  - I^2C (400kHz)
  - 主机 IRQ 信号，用于针对重大系统错误提供实时反馈
- TPS99000-Q1 系统管理和照明控制器接口

2 应用

- 宽视野和增强现实抬头显示屏 (HUD)
- 高分辨率前照灯

3 说明

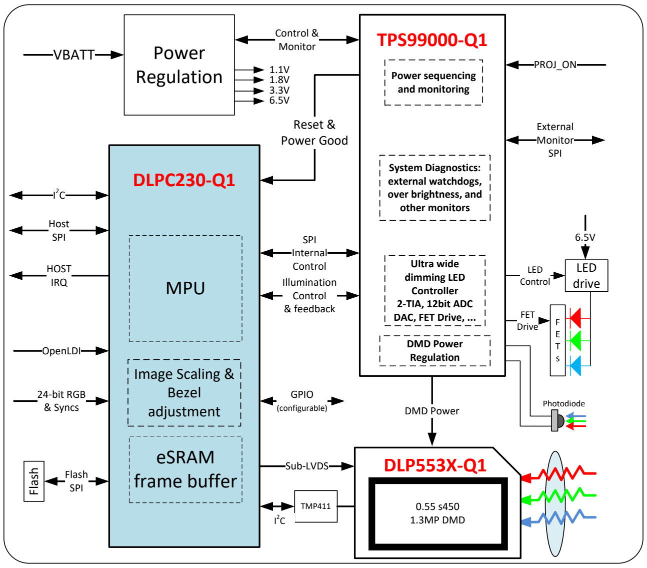
汽车用 DLPC230-Q1 应用 DMD 显示屏控制器是两种 DMD 芯片组：DLP5530-Q1（内部显示屏 应用，例如 HUD）和 DLP5531-Q1（外部照明 应用，例如高分辨率前照灯）的组成部分。两种芯片组均包含 0.55 英寸 DMD 和 TPS99000-Q1 系统管理和照明控制器。DLPC230-Q1 集成了具备错误代码校正 (SECDED ECC) 功能的嵌入式 处理器，支持主机控制和实时反馈、片上诊断和系统监控。还包括片上 SRAM，无需外部 DRAM。DLPC230-Q1 与 TPS99000-Q1 结合使用，可支持 HUD 应用超过 5000:1 的高动态范围调光。Sub-LVDS 600MHz DMD 接口支持高 DMD 刷新率，以无缝生成优质数字图像，同时降低辐射发射。

器件信息[1]

器件型号	封装	封装尺寸（标称值）
DLPC230-Q1	BGA (324)	23.00mm x 23.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

DLP553x-Q1 DLP®芯片组系统方框图


VBATT
Power Regulation
Control & Monitor
1.1V
1.8V
3.3V
6.5V
TPS99000-Q1
PROJ_ON
Power sequencing and monitoring
Reset & Power Good
External Monitor SPI
System Diagnostics: external watchdogs, over brightness, and other monitors
DLPC230-Q1
I²C
Host SPI
HOST IRQ
MPU
SPI
Internal Control
Illumination Control & feedback
6.5V
LED Control
LED drive
Ultra wide dimming LED Controller
2-TIA, 12bit ADC
DAC, FET Drive, ...
FET Drive
FETS
OpenLDI
DMD Power Regulation
Image Scaling & Bezel adjustment
24-bit RGB & Syncs
GPIO (configurable)
DMD Power
Photodiode
eSRAM frame buffer
Flash
Flash SPI
Sub-LVDS
DLP553X-Q1
TMP411
I²C
0.55 s450 1.3MP DMD

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。 有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。 TI 不保证翻译的准确性和有效性。 在实际设计之前，请务必参考最新版本的英文版本。

English Data Sheet: DLPS054

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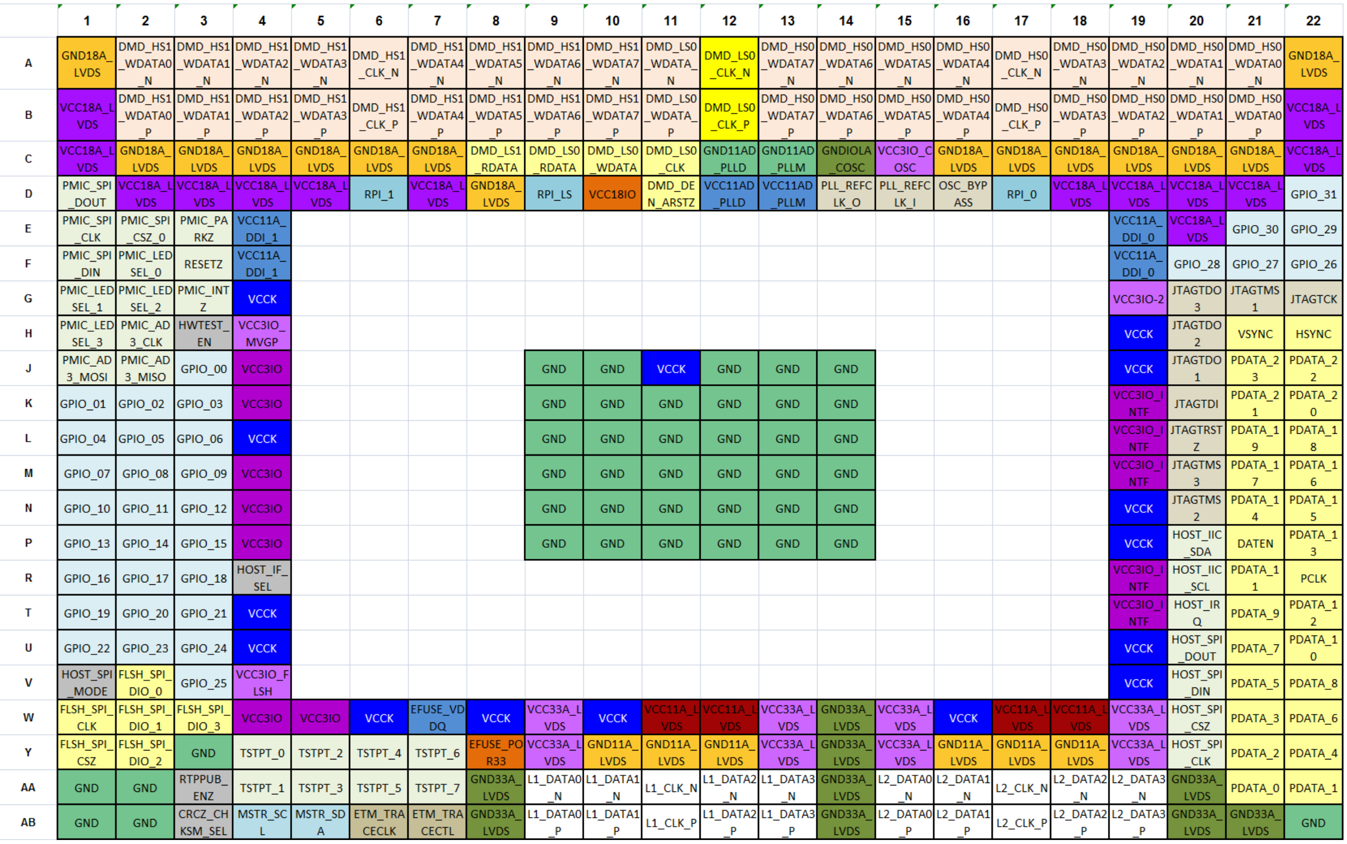
4 修订历史记录

Changes from Revision D (May 2018) to Revision E	**Page**
• 已更改 将器件状态从“*预告信息*”更改为“*生产数据*”	1

5 Pin Configuration and Functions

ZDQ Package
324-Pin BGA
Top View



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
A	GND18A_LVDS	DMD_HS1_WDATA0_N	DMD_HS1_WDATA1_N	DMD_HS1_WDATA2_N	DMD_HS1_WDATA3_N	DMD_HS1_CLK_N	DMD_HS1_WDATA4_N	DMD_HS1_WDATA5_N	DMD_HS1_WDATA6_N	DMD_HS1_WDATA7_N	DMD_LS0_WDATA_N	DMD_LS0_CLK_N	DMD_HS0_WDATA7_N	DMD_HS0_WDATA6_N	DMD_HS0_WDATA5_N	DMD_HS0_WDATA4_N	DMD_HS0_CLK_N	DMD_HS0_WDATA3_N	DMD_HS0_WDATA2_N	DMD_HS0_WDATA1_N	DMD_HS0_WDATA0_N	GND18A_LVDS
B	VCC18A_LVDS	DMD_HS1_WDATA0_P	DMD_HS1_WDATA1_P	DMD_HS1_WDATA2_P	DMD_HS1_WDATA3_P	DMD_HS1_CLK_P	DMD_HS1_WDATA4_P	DMD_HS1_WDATA5_P	DMD_HS1_WDATA6_P	DMD_HS1_WDATA7_P	DMD_LS0_WDATA_P	DMD_LS0_CLK_P	DMD_HS0_WDATA7_P	DMD_HS0_WDATA6_P	DMD_HS0_WDATA5_P	DMD_HS0_WDATA4_P	DMD_HS0_CLK_P	DMD_HS0_WDATA3_P	DMD_HS0_WDATA2_P	DMD_HS0_WDATA1_P	DMD_HS0_WDATA0_P	VCC18A_LVDS
C	VCC18A_LVDS	GND18A_LVDS	GND18A_LVDS	GND18A_LVDS	GND18A_LVDS	GND18A_LVDS	GND18A_LVDS	DMD_LS1_RDATA	DMD_LS0_RDATA	DMD_LS0_WDATA	DMD_LS0_CLK	GND11AD_PLLD	GND11AD_PLLM	GNDIOLA_COSC	VCC3IO_COSC	GND18A_LVDS	GND18A_LVDS	GND18A_LVDS	GND18A_LVDS	GND18A_LVDS	GND18A_LVDS	VCC18A_LVDS
D	PMIC_SPI_DOUT	VCC18A_LVDS	VCC18A_LVDS	VCC18A_LVDS	VCC18A_LVDS	RPI_1	VCC18A_LVDS	GND18A_LVDS	RPI_LS	VCC18IO	DMD_DEN_ARSTZ	VCC11AD_PLLD	VCC11AD_PLLM	PLL_REFCLK_O	PLL_REFCLK_I	OSC_BYPASS	RPI_0	VCC18A_LVDS	VCC18A_LVDS	VCC18A_LVDS	VCC18A_LVDS	GPIO_31
E	PMIC_SPI_CLK	PMIC_SPI_CSZ_0	PMIC_PARKZ	VCC11A_DDI_1															VCC11A_DDI_0	VCC18A_LVDS	GPIO_30	GPIO_29
F	PMIC_SPI_DIN	PMIC_LEDSEL_0	RESETZ	VCC11A_DDI_1															VCC11A_DDI_0	GPIO_28	GPIO_27	GPIO_26
G	PMIC_LEDSEL_1	PMIC_LEDSEL_2	PMIC_INTZ	VCCK															VCC3IO-2	JTAGTDO3	JTAGTMS1	JTAGTCK
H	PMIC_LEDSEL_3	PMIC_AD3_CLK	HWTEST_EN	VCC3IO_MVGP															VCCK	JTAGTDO2	VSYNC	HSYNC
J	PMIC_AD3_MOSI	PMIC_AD3_MISO	GPIO_00	VCC3IO					GND	GND	VCCK	GND	GND	GND					VCCK	JTAGTDO1	PDATA_23	PDATA_22
K	GPIO_01	GPIO_02	GPIO_03	VCC3IO					GND	GND	GND	GND	GND	GND					VCC3IO_INTF	JTAGTDI	PDATA_21	PDATA_20
L	GPIO_04	GPIO_05	GPIO_06	VCCK					GND	GND	GND	GND	GND	GND					VCC3IO_INTF	JTAGTRSTZ	PDATA_19	PDATA_18
M	GPIO_07	GPIO_08	GPIO_09	VCC3IO					GND	GND	GND	GND	GND	GND					VCC3IO_INTF	JTAGTMS3	PDATA_17	PDATA_16
N	GPIO_10	GPIO_11	GPIO_12	VCC3IO					GND	GND	GND	GND	GND	GND					VCCK	JTAGTMS2	PDATA_14	PDATA_15
P	GPIO_13	GPIO_14	GPIO_15	VCC3IO					GND	GND	GND	GND	GND	GND					VCCK	HOST_IIC_SDA	DATEN	PDATA_13
R	GPIO_16	GPIO_17	GPIO_18	HOST_IF_SEL															VCC3IO_INTF	HOST_IIC_SCL	PDATA_11	PCLK
T	GPIO_19	GPIO_20	GPIO_21	VCCK															VCC3IO_INTF	HOST_IRQ	PDATA_9	PDATA_12
U	GPIO_22	GPIO_23	GPIO_24	VCCK															VCCK	HOST_SPI_DOUT	PDATA_7	PDATA_10
V	HOST_SPI_MODE	FLSH_SPI_DIO_0	GPIO_25	VCC3IO_FLSH															VCCK	HOST_SPI_DIN	PDATA_5	PDATA_8
W	FLSH_SPI_CLK	FLSH_SPI_DIO_1	FLSH_SPI_DIO_3	VCC3IO	VCC3IO	VCCK	EFUSE_VDDQ	VCCK	VCC33A_LVDS	VCCK	VCC11A_LVDS	VCC11A_LVDS	VCC33A_LVDS	GND33A_LVDS	VCC33A_LVDS	VCCK	VCC11A_LVDS	VCC11A_LVDS	VCC33A_LVDS	HOST_SPI_CSZ	PDATA_3	PDATA_6
Y	FLSH_SPI_CSZ	FLSH_SPI_DIO_2	GND	TSTPT_0	TSTPT_2	TSTPT_4	TSTPT_6	EFUSE_POR33	VCC33A_LVDS	GND11A_LVDS	GND11A_LVDS	GND11A_LVDS	VCC33A_LVDS	GND33A_LVDS	VCC33A_LVDS	GND11A_LVDS	GND11A_LVDS	GND11A_LVDS	VCC33A_LVDS	HOST_SPI_CLK	PDATA_2	PDATA_4
AA	GND	GND	RTPPUB_ENZ	TSTPT_1	TSTPT_3	TSTPT_5	TSTPT_7	GND33A_LVDS	L1_DATA0_N	L1_DATA1_N	L1_CLK_N	L1_DATA2_N	L1_DATA3_N	GND33A_LVDS	L2_DATA0_N	L2_DATA1_N	L2_CLK_N	L2_DATA2_N	L2_DATA3_N	GND33A_LVDS	PDATA_0	PDATA_1
AB	GND	GND	CRCZ_CHKSM_SEL	MSTR_SCL	MSTR_SDA	ETM_TRACECLK	ETM_TRACECTL	GND33A_LVDS	L1_DATA0_P	L1_DATA1_P	L1_CLK_P	L1_DATA2_P	L1_DATA3_P	GND33A_LVDS	L2_DATA0_P	L2_DATA1_P	L2_CLK_P	L2_DATA2_P	L2_DATA3_P	GND33A_LVDS	GND33A_LVDS	GND

Note that there is one VCCK power ball located in the thermal ball array.

Pin Functions – Board Level Test, Debug, and Initialization

PIN		I/O (1)	DESCRIPTION
NAME	NUMBER		
RESETZ	F3	I_7	Active low power-on reset for the DLPC230-Q1. A low-to-high transition starts self-configuration and initialization of the ASIC. ('0' = Reset, '1' = Normal Operation) All ASIC power and input clocks must be stable before this reset is de-asserted high. The signals listed below should be forced low by external pull-down, and will then be driven low as the power supplies stabilize with RESETZ asserted. *PMIC_LEDSEL_0, PMIC_LEDSEL_1, PMIC_LEDSEL_2, PMIC_LEDSEL_3, DMD_DEN_ARSTZ, PMIC_AD3_CLK, and PMIC_AD3_MOSI* All other bi-directional and output signals will be tri-stated while reset is asserted. External pull-ups or pull-downs must be added where necessary to protect external devices that would typically be driven by the ASIC to prevent device malfunction. This pin includes hysteresis. Specific timing requirements for this signal are shown in *Power Supply and Reset Timing Requirements*.

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(1) See Table 1 for more information on I/O definitions.

Pin Functions – Board Level Test, Debug, and Initialization (continued)

PIN		I/O[(1)]	DESCRIPTION
NAME	**NUMBER**		
PMIC_PARKZ	E3	I_7	DMD Park Control ('0' = Park, '1' = Un-Park) The TI TPS99000-Q1 device is used to control this signal. As part of this function, it monitors power to the DLPC230-Q1 watching for an imminent power loss condition, upon which it will drive the PMIC_PARKZ signal accordingly. The specific timing requirements for this signal are shown in *Power Supply and Reset Timing Requirements*.
HOST_IF_SEL	R4	$B_{13,14}$	Selects which input interface port will be used for Host Command and Control. The port that is not selected as the Host Command and Control port will be available as a Diagnostic Processor monitoring port. ('0' = Host SPI, '1' = Host I^{2}C) This pin includes a weak internal pull-down. If a pull-up is used to obtain a '1' value, the pull-up value must be ≤ 8 kΩ. Tri-stated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5 µs after RESETZ is de-asserted. It may be driven as an output for TI debug use after sampling.
HOST_SPI_MODE	V1	$B_{13,14}$	Selects the SPI mode (clock phase and polarity) that will be used with the HOST SPI interface. This value is applicable regardless of whether the Host SPI interface is used for Host Command and Control, or for the Diagnostic Processor monitoring port. ('0' = SPI Mode 0 or 3, '1' = SPI Mode 1 or 2) This pin includes a weak internal pull-down. If a pull-up is used to obtain a '1' value, the pull-up value must be ≤ 8 kΩ. Tri-stated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5 µs after RESETZ is de-asserted. It may be driven as an output for TI debug use after sampling.
RTPPUB_ENZ	AA3	$B_{13,14}$	TI internal use. Must be left unconnected. Includes a weak pull-down.
CRCZ_CHKSUM_SEL	AB3	$B_{13,14}$	Selects whether the Host will use 8-bit CRC or Checksum on the Host Command and Control interface. This value is only applicable for the Host Command and Control interface. The value for the Diagnostic Processor monitoring port will be specified in Flash. ('0' = 8-bit CRC, '1' = 8-bit Checksum) This pin includes a weak internal pull-down. If a pull-up is used to obtain a '1' value, the pull-up value must be ≤ 8 kΩ. Tri-stated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5 µs after RESETZ is de-asserted. It may be driven as an output for TI debug use after sampling.
ETM_TRACECLK	AB6	O_{13}	TI internal use. Must be left unconnected. (Clock for Trace Debug)
ETM_TRACECTL	AB7	O_{13}	TI internal use. Must be left unconnected. (Control for Trace Debug)
TSTPT_0	Y4	$B_{13,14}$	Test pin 0 / STAY-IN-BOOT: Selects whether the system should stay in the Boot Application, or proceed with the normal load of the Main Application. ('0' = Load Main Application, '1' = Stay in Boot Application) This pin includes a weak internal pull-down. If a pull-up is being used to obtain a '1' value, the pull-up value must be ≤ 8 kΩ. Tri-stated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5 µs after RESETZ is de-asserted. It may be driven as an output for debug use after sampling as described in *Debug Support*.
TSTPT_1	AA4	$B_{13,14}$	Test pin 1: This pin must be externally pulled down, left open or unconnected. Includes a weak pull-down. It may be driven as an output for debug use as described in *Debug Support*.
TSTPT_2	Y5	$B_{13,14}$	Test pin 2: This pin must be externally pulled down, left open or unconnected. Includes a weak pull-down. It may be driven as an output for debug use as described in *Debug Support*.
TSTPT_3	AA5	$B_{13,14}$	Test pin 3: This pin must be externally pulled down, left open or unconnected. Includes a weak pull-down. It may be driven as an output for debug use as described in *Debug Support*.

Pin Functions – Board Level Test, Debug, and Initialization (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NUMBER		
TSTPT_4	Y6	$B_{13,14}$	Test pin 4: This pin must be externally pulled down, left open or unconnected. Includes a weak pull-down. It may be driven as an output for debug use as described in *Debug Support*.
TSTPT_5	AA6	$B_{13,14}$	Test pin 5 / Spread Spectrum Disable: Selects whether spread spectrum flash settings are used or whether spread spectrum clocking will be disabled. ('0' = Spread Spectrum Disabled, '1' = Use flash Spread Spectrum settings) This pin includes a weak internal pull-down. If a pull-up is being used to obtain a '1' value, the pull-up value must be ≤ 8 kΩ. This signal is tri-stated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5 µs after RESETZ is de-asserted. It may be driven as an output for debug use after sampling as described in *Debug Support*.
TSTPT_6	Y7	$B_{13,14}$	Test pin 6: An external pull-up resistor must be used (≤ 8 kΩ since pin includes a weak pull-down). This signal is tri-stated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5 µs after RESETZ is de-asserted. It may be driven as an output for debug use after sampling as described in *Debug Support*.
TSTPT_7	AA7	$B_{13,14}$	Test pin 7: This pin must be externally pulled down, left open or unconnected. Includes a weak pull-down. It may be driven as an output for debug use as described in *Debug Support*.
HWTEST_EN	H3	I_{14}	Manufacturing test enable signal. This signal must be connected directly to ground on the PCB. Includes weak internal pull-down and hysteresis.
JTAGTCK	G22	I_{11}	JTAG Serial Data Clock Includes a weak internal pull-up.
JTAGTMS1	G21	I_{11}	JTAG Test Mode Select Includes weak internal pull-up.
JTAGTRSTZ	L20	I_{11}	JTAG Reset Includes a weak internal pull-up and Hysteresis. For normal operation, this pin must be pulled to ground through an external 8 kΩ or less resistor. **Failure to pull this pin low during normal operation will cause start-up and initialization problems.** For JTAG Boundary Scan, this pin must be pulled-up or left disconnected.
JTAGTDI	K20	I_{11}	JTAG Serial Data In Includes a weak internal pull-up.
JTAGTDO1	J20	$B_{10,11}$	JTAG Serial Data Out Includes weak internal pull-up.
JTAGTDO2	H20	$B_{10,11}$	This pin must be left open or unconnected. Includes a weak internal pull-up.
JTAGTDO3	G20	$B_{10,11}$	This pin must be left open or unconnected. Includes a weak internal pull-up.
JTAGTMS2	N20	I_{11}	This pin must be left open or unconnected. Includes a weak internal pull-up. See *Debug Support* for important debug access considerations.
JTAGTMS3	M20	I_{11}	This pin must be left open or unconnected. Includes a weak internal pull-up. See *Debug Support* for important debug access considerations.

Pin Functions – Parallel Port Input Data and Control(1)

PIN		I/O(2)	DESCRIPTION PARALLEL RGB MODE
NAME	**NUMBER**		
PCLK	R22	I_{11}	Pixel clock
VSYNC	H21	I_{11}	Vsync(3)
HSYNC	H22	I_{11}	Hsync(3)
DATEN	P21	I_{11}	Data Valid
			(TYPICAL RGB 888)
PDATA_0 PDATA_1 PDATA_2 PDATA_3 PDATA_4 PDATA_5 PDATA_6 PDATA_7	AA21 AA22 Y21 W21 Y22 V21 W22 U21	I_{11}	Blue (bit weight 1) Blue (bit weight 2) Blue (bit weight 4) Blue (bit weight 8) Blue (bit weight 16) Blue (bit weight 32) Blue (bit weight 64) Blue (bit weight 128)
			(TYPICAL RGB 888)
PDATA_8 PDATA_9 PDATA_10 PDATA_11 PDATA_12 PDATA_13 PDATA_14 PDATA_15	V22 T21 U22 R21 T22 P22 N21 N22	I_{11}	Green (bit weight 1) Green (bit weight 2) Green (bit weight 4) Green (bit weight 8) Green (bit weight 16) Green (bit weight 32) Green (bit weight 64) Green (bit weight 128)
			(TYPICAL RGB 888)
PDATA_16 PDATA_17 PDATA_18 PDATA_19 PDATA_20 PDATA_21 PDATA_22 PDATA_23	M22 M21 L22 L21 K22 K21 J22 J21	I_{11}	Red (bit weight 1) Red (bit weight 2) Red (bit weight 4) Red (bit weight 8) Red (bit weight 16) Red (bit weight 32) Red (bit weight 64) Red (bit weight 128)

(1) Unused inputs should be grounded or pulled down to ground through an external resistor (≤ 10 kΩ).
(2) See Table 1 for more information on I/O definitions.
(3) VSYNC and HSYNC polarity are software programmable.

Pin Functions – OpenLDI Ports Input Data and Control[1][2]

PIN		I/O[3]	DESCRIPTION
NAME	NUMBER		
L1_CLK_P L1_CLK_N	AB11 AA11	I_{18}	OpenLDI (FPD Link I) Port 1 Clock Lane
L1_DATA0_P L1_DATA0_N L1_DATA1_P L1_DATA1_N L1_DATA2_P L1_DATA2_N L1_DATA3_P L1_DATA3_N	AB9 AA9 AB10 AA10 AB12 AA12 AB13 AA13	I_{18}	OpenLDI (FPD Link I) Port 1 Data Lanes: Intra-port data lane swapping can be done on a product configuration basis to support board considerations.
L2_CLK_P L2_CLK_N	AB17 AA17	I_{18}	OpenLDI (FPD Link I) Port 2 Clock Lane
L2_DATA0_P L2_DATA0_N L2_DATA1_P L2_DATA1_N L2_DATA2_P L2_DATA2_N L2_DATA3_P L2_DATA3_N	AB15 AA15 AB16 AA16 AB18 AA18 AB19 AA19	I_{18}	OpenLDI (FPD Link I) Port 2 Data Lanes: Intra-port data lane swapping can be done on a product configuration basis to support board considerations.

(1) The system only supports the operational use of one port. As two ports are available, the host can select which port they wish to be active (to optimize board routing as an example).
(2) The inputs for any un-used port(s) should be left unconnected, and will be powered down by the system.
(3) See Table 1 for more information on I/O definitions.

Pin Functions – DMD Reset and Bias Control Interfaces(1)(2)

PIN		I/O(3)	DESCRIPTION
NAME	**NUMBER**		
DMD_DEN_ARSTZ	D11	O_1	DMD driver enable signal ('1' = Enabled, '0' = Reset) This signal will be driven low after the DMD is parked and before power is removed from the DMD. If the 1.8-V power to the DLPC230-Q1 is independent of the 1.8-V power to the DMD, then an external pull-down resistor (≤ 2.2 kΩ) must be used to hold the signal low in the event DLPC230-Q1 power is inactive while DMD power is applied.
DMD_LS0_CLK	C11	O_2	TI internal use. Must be left unconnected.
DMD_LS0_WDATA	C10	O_2	TI internal use. Must be left unconnected.
DMD_LS0_RDATA	C9	I_3	DMD, low-speed single-ended serial read data
DMD_LS1_RDATA	C8	I_3	DMD, low-speed single-ended serial read data (Training data response for second port of DMD)
DMD_LS0_CLK_P DMD_LS0_CLK_N	B12 A12	O_4	DMD low-speed differential interface clock
DMD_LS0_WDATA_P DMD_LS0_WDATA_N	B11 A11	O_4	DMD low-speed differential interface write data

(1) The low-speed write control interface to the DMD is differential.
(2) All control interface reads will make use of the single-ended low-speed signals. The read data will be clocked by the write clock.
(3) See Table 1 for more information on I/O definitions.

Pin Functions – DMD Sub-LVDS Interfaces

PIN		I/O(1)	DESCRIPTION
NAME	**NUMBER**		
DMD_HS0_CLK_P DMD_HS0_CLK_N	B17 A17	O_4	DMD high-speed interface, Port 0 Clock Lane.
DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N	B21 A21 B20 A20 B19 A19 B18 A18 B16 A16 B15 A15 B14 A14 B13 A13	O_4	DMD high-speed interface, Port 0 Data Lanes: The true numbering and application of the DMD_HS_DATA pins are software configuration dependent as discussed in *DMD (Sub-LVDS) Interface*.
DMD_HS1_CLK_P DMD_HS1_CLK_N	B6 A6	O_4	DMD high-speed interface, Port 1 Clock Lane.
DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N	B2 A2 B3 A3 B4 A4 B5 A5 B7 A7 B8 A8 B9 A9 B10 A10	O_4	DMD high-speed interface, Port 1 Data Lanes: The true numbering and application of the DMD_HS_DATA pins are software configuration dependent as discussed in *DMD (Sub-LVDS) Interface*.

(1) See Table 1 for more information on I/O definitions.

Pin Functions – Peripheral Interfaces

PIN		I/O[1]	DESCRIPTION
NAME	NUMBER		
HOST_IRQ[2]	T20	O_{10}	Host interrupt (output active HIGH) This signal is used to indicate that the DLPC230-Q1 has detected a serious error for which the ASIC has initiated an Emergency Shutdown. This is discussed further in *HOST_IRQ Usage Model*. The DLPC230-Q1 tri-states this output during reset. An external pull-down (≤ 10 kΩ) is required to drive this signal to its inactive state.
HOST_IIC_SCL	R20	B_{12}	I^2C Port (Slave), Host Command and Control to ASIC, SCL (bidirectional, open-drain): An external pull-up is required.
HOST_IIC_SDA	P20	B_{12}	I^2C Port (Slave), Host Command and Control to ASIC, SDA. (bidirectional, open-drain): An external pull-up is required.
HOST_SPI_CLK	Y20	I_{11}	SPI Port (Slave), Host Command and Control to ASIC, clock
HOST_SPI_CSZ	W20	I_{11}	SPI Port (Slave), Host Command and Control to ASIC, chip select (active low input) An external pull-up resistor (≤ 2.2 kΩ) is required to avoid a floating chip select input to the ASIC
HOST_SPI_DIN	V20	I_{11}	SPI Port (Slave), Host Command and Control to ASIC, receive data in
HOST_SPI_DOUT	U20	O_{10}	SPI Port (Slave), Host Command and Control to ASIC, transmit data out
FLSH_SPI_CSZ	Y1	O_8	SPI Port (Master), Control Interface to Flash device, chip select (active low output) An external pullup resistor (≤ 10 kΩ) is required to avoid a floating chip select input to the Flash
FLSH_SPI_CLK	W1	O_8	SPI Port (Master), Control Interface to Flash device, clock
FLSH_SPI_DIO_0	V2	$B_{8,9}$	SPI Port (Master), Control Interface to Flash device, transmit and receive data An external pullup resistor (≤ 10 kΩ) is required
FLSH_SPI_DIO_1	W2	$B_{8,9}$	SPI Port (Master), Control Interface to Flash device, transmit and receive data An external pullup resistor (≤ 10 kΩ) is required
FLSH_SPI_DIO_2	Y2	$B_{8,9}$	SPI Port (Master), Control Interface to Flash device, transmit and receive data An external pullup resistor (≤ 3.3 kΩ) is required
FLSH_SPI_DIO_3	W3	$B_{8,9}$	SPI Port (Master), Control Interface to Flash device, transmit and receive data An external pullup resistor (≤ 3.3 kΩ) is required
PMIC_INTZ[2]	G3	I_7	TPS99000-Q1 interrupt (input with hysteresis) The ASIC provides a weak internal pull-up
PMIC_SPI_CLK	E1	O_6	SPI Port (Master), General Control Interface to TPS99000-Q1, clock
PMIC_SPI_CSZ0	E2	O_6	SPI Port (Master), General Control Interface to TPS99000-Q1, chip select 0 (active low output) An external pullup resistor (≤ 10 kΩ) must be used to avoid floating chip select inputs to the external SPI device during ASIC reset assertion.
PMIC_SPI_DIN	F1	I_7	SPI Port (Master), General Control Interface to TPS99000-Q1, receive data in
PMIC_SPI_DOUT	D1	O_6	SPI Port (Master), General Control Interface to TPS99000-Q1, transmit data out
PMIC_AD3_CLK	H2	O_{20}	Sequencer Clock / TPS99000-Q1 primary system clock An external pull-down resistor (≤ 10 kΩ) must be used to avoid uncontrolled behavior during ASIC reset assertion.
PMIC_AD3_MISO	J2	I_{14}	Measurement control interface to TPS99000-Q1, receive data in
PMIC_AD3_MOSI	J1	O_{20}	Measurement control interface to TPS99000-Q1, transmit data out An external pull-down resistor (≤ 10 kΩ) must be used to avoid uncontrolled behavior during ASIC reset assertion.
PMIC_LEDSEL_0	F2	O_6	LED Control Interface to TPS99000-Q1 An external pull-down resistor (≤ 10 kΩ) must be used to avoid uncontrolled illumination during ASIC reset assertion.
PMIC_LEDSEL_1	G1	O_6	LED Control Interface to TPS99000-Q1 An external pull-down resistor (≤ 10 kΩ) must be used to avoid uncontrolled illumination during ASIC reset assertion.
PMIC_LEDSEL_2	G2	O_6	LED Control Interface to TPS99000-Q1 An external pull-down resistor (≤ 10 kΩ) must be used to avoid uncontrolled illumination during ASIC reset assertion.

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(1) See Table 1 for more information on I/O definitions.
(2) For more information about usage, see *HOST_IRQ Usage Model*.

Pin Functions – Peripheral Interfaces (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NUMBER		
PMIC_LEDSEL_3	H1	O_6	LED Control Interface to TPS99000-Q1 An external pull-down resistor (≤ 10 kΩ) must be used to avoid uncontrolled illumination during ASIC reset assertion.
MSTR_SDA	AB5	B_{15}	I^{2}C Port (Master), SDA. (bidirectional, open-drain) An external pull-up is required. Typical use of the Master I^{2}C port is communication with temperature sensing devices and an optional EEPROM. The Master I^{2}C I/Os are powered by VCC3IO (3.3 V only).
MSTR_SCL	AB4	B_{15}	I^{2}C Port (Master), SCL. (bidirectional, open-drain) An external pull-up is required. Typical use of the Master I^{2}C port is communication with temperature sensing devices and an optional EEPROM. The Master I^{2}C I/Os are powered by VCC3IO (3.3 V only).

Pin Functions – GPIO Peripheral Interface(1)(2)

PIN		I/O(3)	DESCRIPTION
NAME	NUMBER		
GPIO_31	D22	$B_{20,14}$	General purpose I/O 31
GPIO_30	E21	$B_{20,14}$	General purpose I/O 30
GPIO_29	E22	$B_{20,14}$	General purpose I/O 29
GPIO_28	F20	$B_{20,14}$	General purpose I/O 28
GPIO_27	F21	$B_{20,14}$	General purpose I/O 27
GPIO_26	F22	$B_{20,14}$	General purpose I/O 26
GPIO_25	V3	$B_{20,14}$	General purpose I/O 25
GPIO_24	U3	$B_{20,14}$	General purpose I/O 24
GPIO_23	U2	$B_{20,14}$	General purpose I/O 23
GPIO_22	U1	$B_{20,14}$	General purpose I/O 22
GPIO_21	T3	$B_{20,14}$	General purpose I/O 21
GPIO_20	T2	$B_{20,14}$	General purpose I/O 20
GPIO_19	T1	$B_{20,14}$	General purpose I/O 19
GPIO_18	R3	$B_{20,14}$	General purpose I/O 18
GPIO_17	R2	$B_{20,14}$	General purpose I/O 17
GPIO_16	R1	$B_{20,14}$	General purpose I/O 16
GPIO_15	P3	$B_{20,14}$	General purpose I/O 15
GPIO_14	P2	$B_{20,14}$	General purpose I/O 14
GPIO_13	P1	$B_{20,14}$	General purpose I/O 13
GPIO_12	N3	$B_{20,14}$	General purpose I/O 12
GPIO_11	N2	$B_{20,14}$	General purpose I/O 11
GPIO_10	N1	$B_{20,14}$	General purpose I/O 10
GPIO_09	M3	$B_{20,14}$	General purpose I/O 09
GPIO_08	M2	$B_{20,14}$	General purpose I/O 08
GPIO_07	M1	$B_{20,14}$	General purpose I/O 07
GPIO_06	L3	$B_{20,14}$	General purpose I/O 06
GPIO_05	L2	$B_{20,14}$	General purpose I/O 05
GPIO_04	L1	$B_{20,14}$	General purpose I/O 04
GPIO_03	K3	$B_{20,14}$	General purpose I/O 03
GPIO_02	K2	$B_{20,14}$	General purpose I/O 02
GPIO_01	K1	$B_{20,14}$	General purpose I/O 01
GPIO_00	J3	$B_{20,14}$	General purpose I/O 00

(1) Some GPIO signals are reserved for specific purposes. These signals vary per product configuration. These product allocations are discussed further in *GPIO Supported Functionality*. All GPIO that are available for Host use must be configured as an input, a standard output, or an open-drain output. This is set in the flash configuration or by command using the Host command interface. The reset default for all GPIO is as an input signal. An external pull-up (≤ 10 kΩ) is required for each signal configured as open-drain.
(2) All GPIO include hysteresis.
(3) See Table 1 for more information on I/O definitions.

Pin Functions – Clock and PLL Support

PIN		I/O[1]	DESCRIPTION
NAME	NUMBER		
PLL_REFCLK_I	D15	I_{17}	Reference clock crystal input. *If an external oscillator is used in place of a crystal, this pin should be left unconnected (floating with no added capacitive load).*
PLL_REFCLK_O	D14	$B_{16,17}$	Reference clock crystal return. *If an external oscillator is used in place of a crystal, this pin must be used for the oscillator input.*
OSC_BYPASS	D16	I_{19}	Selects whether an external crystal or external oscillator will be used to drive the internal PLL. ('0' = Crystal, '1' = Oscillator) This pin includes a weak internal pull-down. If a pull-up is being used to obtain a '1' value, the pull-up value must be ≤ 8 kΩ.

(1) See Table 1 for more information on I/O definitions.

Pin Functions – Power and Ground

PIN		I/O[1]	DESCRIPTION
NAME	NUMBER		
VCC18A_LVDS	B1, B22, C1, C22, D2, D3, D4, D5, D7, D18, D19, D20, D21, E20	PWR	1.8-V Power for the differential High-Speed and Low-Speed DMD Interfaces
GND18A_LVDS	A1, A22, C2, C3, C4, C5, C6, C7, C16, C17, C18, C19, C20, C21, D8	RTN	1.8-V GND for the differential High-Speed and Low-Speed DMD Interfaces
VCC18IO	D10	PWR	1.8-V Power for 1.8-V IO
VCC3IO_MVGP	H4	PWR	3.3-V Power for TPS99000-Q1 Interfaces
VCC3IO_FLSH	V4	PWR	3.3-V Power for the Serial Flash Interface
VCC3IO_INTF	K19, L19, M19, R19, T19	PWR	3.3-V Power for the Parallel Data, JTAG, and Host Command Interfaces
VCC3IO_COSC	C15	PWR	3.3-V I/O Power for the Crystal Oscillator
GNDIOLA_COSC	C14	RTN	3.3-V I/O GND for the Crystal Oscillator
VCC3IO	J4, K4, M4, N4, P4, W4, W5, G19	PWR	3.3-V I/O Power for all "other" I/O (such as GPIO, TSTPT, PMIC_AD3)
VCC33A_LVDS	W9, W13, W15, W19, Y9, Y13, Y15, Y19	PWR	3.3-V I/O Power for the OpenLDI Interface
GND33A_LVDS	W14, Y14, AA8, AA14, AA20, AB8, AB14, AB20, AB21	RTN	3.3-V I/O GND for the OpenLDI Interface
VCC11AD_PLLM	D13	PWR	1.1-V Analog/Digital Power for MCG (Master Clock Generator) PLL
GND11AD_PLLM	C13	RTN	1.1-V Analog/Digital GND for MCG (Master Clock Generator) PLL
VCC11AD_PLLD	D12	PWR	1.1-V Analog/Digital Power for DCG (DMD Clock Generator) PLL
GND11AD_PLLD	C12	RTN	1.1-V Analog/Digital GND for DCG (DMD Clock Generator) PLL
VCC11A_DDI_0	E19, F19	PWR	1.1-V Filtered Core Power - External Filter Group A (HS DMD Interface 0)
VCC11A_DDI_1	E4, F4	PWR	1.1-V Filtered Core Power - External Filter Group B (HS DMD Interface 1)
VCC11A_LVDS	W11, W12, W17, W18	PWR	1.1-V Filtered Core Power - External Filter Group C (OpenLDI Interface)
VCCK	G4, H19, (J11), J19, L4, N19, P19, T4, U4, U19, V19, W6, W8, W10, W16	PWR	1.1-V Core Power (Ball numbers in parenthesis are also used as thermal ball and are located within the package center region)

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(1) See Table 1 for more information on I/O definitions.

Pin Functions – Power and Ground (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NUMBER		
GND	(J9, J10, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13,P14), Y3, AA1, AA2, AB1, AB2, AB22, Y10, Y11, Y12, Y16, Y17, Y18	RTN	1.1-V Core GND (Ball numbers in parenthesis are also used as thermal ball and are located within the package center region)
EFUSE_VDDQ	W7		Manufacturing use only. Must be tied to ground.
EFUSE_POR33	Y8		Manufacturing use only. Must be tied to ground.
RPI_0	D17	I_5	Bandgap Reference for sub-LVDS drivers (Supports DMD_HS0_xxxx). Requires a resistor (1% Tolerance) to GND18A_LVDS - Value specified in Table 18.
RPI_1	D6	I_5	Bandgap Reference for sub-LVDS drivers (Supports DMD_HS1_xxxx). Requires a resistor (1% Tolerance) to GND18A_LVDS - Value specified in Table 18.
RPI_LS	D9	I_5	Bandgap References for sub-LVDS drivers (Supports DMD_LS0_xxxx differential bus signals). Requires a resistor (1% Tolerance) to GND18A_LVDS - Value specified in Table 18.

Table 1. I/O Type Subscript Definition

I/O		SUPPLY REFERENCE	ESD STRUCTURE
SUBSCRIPT	DESCRIPTION		
1	1.8-V LVCMOS Input	VCC18IO	ESD diode to GND and supply rail
2	1.8-V LVCMOS Output	VCC18IO	ESD diode to GND and supply rail
3	1.8-V LVCMOS Input	VCC18IO	ESD diode to GND and supply rail
4	1.8-V sub-LVDS Output	VCC18A_LVDS	ESD diode to GND and supply rail
5	1.8-V sub-LVDS Input	VCC18A_LVDS	ESD diode to GND and supply rail
6	3.3-V LVCMOS Output	VCC3IO_MVGP	ESD diode to GND and supply rail
7	3.3-V LVCMOS Input	VCC3IO_MVGP	ESD diode to GND and supply rail
8	3.3-V LVCMOS Output	VCC3IO_FLSH	ESD diode to GND and supply rail
9	3.3-V LVCMOS Input	VCC3IO_FLSH	ESD diode to GND and supply rail
10	3.3-V LVCMOS Output	VCC3IO_INTF	ESD diode to GND and supply rail
11	3.3-V LVCMOS Input	VCC3IO_INTF	ESD diode to GND and supply rail
12	3.3-V I^{2}C I/O	VCC3IO_INTF	ESD diode to GND and supply rail
13	3.3-V LVCMOS Output	VCC3IO	ESD diode to GND and supply rail
14	3.3-V LVCMOS Input	VCC3IO	ESD diode to GND and supply rail
15	3.3-V I^{2}C I/O with 3-mA drive	VCC3IO	ESD diode to GND and supply rail
16	3.3-V LVCMOS Output	VCC3IO_OSC	ESD diode to GND and supply rail
17	3.3-V LVCMOS Input	VCC3IO_OSC	ESD diode to GND and supply rail
18	3.3-V LVDS Input	VCC33A_LVDS	ESD diode to GND and supply rail
19	3.3-V LVCMOS Input	VCC3IO_OSC	ESD diode to GND and supply rail
20	3.3-V LVCMOS Output	VCC3IO	ESD diode to GND and supply rail
TYPE			
I	Input	N/A	
O	Output		
B	Bidirectional		
PWR	Power		
RTN	Ground return		

Table 2. Internal Pull-up and Pull-down Characteristics(1)(2)

INTERNAL PULL-UP AND PULL-DOWN RESISTOR CHARACTERISTICS	VCCIO	MIN	MAX	UNIT
Weak pull-up resistance	3.3 V	40	190	kΩ
Weak pull-down resistance	3.3 V	30	190	kΩ

(1) The resistance is dependent on the supply voltage level applied to the I/O.

(2) An external 8-kΩ or less pull-up or pull-down (if needed) will work for any voltage condition to correctly override any associated internal pull-ups or pull-downs.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)(1)

		MIN	MAX	UNIT
SUPPLY VOLTAGE(2)				
$V_{(VCCK)}$ (Core)		–0.5	1.5	V
$V_{(VCC11A\_DDIx)}$ (Core)		–0.5	1.5	V
$V_{(VCC11A\_LVDS)}$ (Core)		–0.5	1.5	V
$V_{(VCC11AD\_PLLM)}$ (Core)		–0.5	1.5	V
$V_{(VCC11AD\_PLLD)}$ (Core)		–0.5	1.5	V
$V_{(VCC18A\_LVDS)}$		–0.5	2.5	V
$V_{(VCC18IO)}$		–0.5	2.5	V
$V_{(VCC3IO\_MVGP)}$		–0.5	4.6	V
$V_{(VCC3IO\_INF)}$		–0.5	4.6	V
$V_{(VCC3IO\_FLSH)}$		–0.5	4.6	V
$V_{(VCC3IO\_OSC)}$		–0.5	4.6	V
$V_{(VCC3IO)}$		–0.5	4.6	V
$V_{(VCC33A\_LVDS)}$		–0.5	4.6	V
GENERAL				
T_J	Operating junction temperature	–40	125	°C
T_C	Operating case temperature	–40	124(3)	°C
I_{lat}	Latch-up	–100	100	mA
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Value calculated using package parameters defined in *Thermal Information*.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins (except corner pins)	±500	
			Corner pins (A1, A22, AB0, and AB22) only	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{(VCCK)}$	Core power 1.1 V (main 1.1 V)	±5% tolerance	1.045	1.1	1.155	V
$V_{(VCC11A\_DDI\_0)}$	Core power 1.1 V (External Filter Group A - HS DMD Interface 0)	±8.18% tolerance(1)	1.01	1.1	1.19	V
$V_{(VCC11A\_DDI\_1)}$	Core power 1.1 V (External Filter Group B - HS DMD Interface 1)	±8.18% tolerance(1)	1.01	1.1	1.19	V
$V_{(VCC11A\_LVDS)}$	Core power 1.1 V (External Filter Group C - OpenLDI Interface)	±8.18% tolerance(1)	1.01	1.1	1.19	V
$V_{(VCC11AD\_PLLM)}$	MCG PLL 1.1-V power (Analog/Digital)	±8.18% tolerance(1)	1.01	1.1	1.19	V
$V_{(VCC11AD\_PLLD)}$	DCG PLL 1.1-V power (Analog/Digital)	±8.18% tolerance(1)	1.01	1.1	1.19	V
$V_{(VCC18IO)}$	1.8-V I/O power (Supports DMD Single-Ended LS interface I/O)	±8.3% tolerance	1.65	1.8	1.95	V
$V_{(VCC18A\_LVDS)}$	1.8-V I/O power (Supports High-Speed and Low-Speed differential DMD interfaces)	±8.3% tolerance	1.65	1.8	1.95	V
$V_{(VCC3IO\_MVGP)}$	3/3-V I/O power (Supports TPS99000-Q1: SPI, interrupt, park, RESETZ, and LEDSEL interfaces	±8.5% tolerance	3.02	3.3	3.58	V
$V_{(VCC3IO\_FLSH)}$	3/3-V I/O power (Supports serial flash interface)	±8.5% tolerance	3.02	3.3	3.58	V
$V_{(VCC3IO\_INTF)}$	3.3-V I/O power (Supports: host command (SPI and I^2C), parallel data interface, HOST_IRQ, and JTAG	±8.5% tolerance	3.02	3.3	3.58	V
$V_{(VCC3IO\_OSC)}$	3.3-V I/O power (Supports Oscillator)	±8.5% tolerance	3.02	3.3	3.58	V
$V_{(VCC33A\_LVDS)}$	3.3-V I/O power (Supports OpenLDI interface)	±8.5% tolerance	3.02	3.3	3.58	V
$V_{(VCC3IO)}$	3.3-V I/O power (Supports all remaining I/O including: GPIO, PMIC_AD3, TSTPT, ETM_TRACE, et cetera)	±8.5% tolerance	3.02	3.3	3.58	V
T_J	Operating junction temperature		–40		125	°C
T_C	Operating case temperature		–40		124	°C
T_A	Operating ambient temperature(2)		–40		105	°C

(1) These I/O supply ranges are wider to facilitate additional external filtering.
(2) Operating ambient temperature is dependent on system thermal design. Operating case temperature may not exceed its specified range across ambient temperature conditions.

6.4 Thermal Information

THERMAL METRIC(1)		DLPC230-Q1 ZDQ (BGA) 324 PINS	UNIT
ψ_{JT}(2)	Temperature variance from junction to package top center temperature, per unit power dissipation	0.77	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) (1.22 W) × (0.77°C/W) ≈ 1.00°C temperature difference.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX(2)	UNIT
TOTAL						
$I_{(VCC11)}$	1.1-V total current			201	743.9	mA
$I_{(VCC18)}$	1.8-V total current			71	122.9	mA
$I_{(VCC33)}$	3.3-V total current			28.1	30.1	mA
ESTIMATED CURRENT PER SUPPLY(3)						
$I_{(VCCK)}$	1.1-V Core current			131.5	667.5	mA
$I_{(VCC11A\_DDI\_0)}$	1.1-V Core current (Filtered)	At 600-MHz data rate		15.8	17.4	mA
$I_{(VCC11A\_DDI\_1)}$	1.1-V Core current (Filtered)	At 600-MHz data rate		15.8	17.4	mA
$I_{(VCC11A\_LVDS)}$	1.1-V Core current (Filtered)	OpenLDI Interface, single port, 5 lanes active		22.5	24.8	mA
$I_{(VCC11AD\_PLLM)}$	1.1-V Core current (MCG PLL)			7.7	8.4	mA
$I_{(VCC11AD\_PLLD)}$	1.1-V Core current (DCG PLL)			7.7	8.4	mA
$I_{(VCC18A\_LVDS)}$	1.8-V I/O current (Both 8-bit ports - DMD HS differential Interface)	At 600-MHz data rate		63.3	106.6	mA
$I_{(VCC18A\_LVDS)}$	1.8-V I/O current (DMD LS differential Interface)	At 120-MHz data rate		5.2	8.7	mA
$I_{(VCC18IO)}$	1.8-V I/O current (DMD LS single-ended interfaces, DMD reset)			2.5	7.6	mA
$I_{(VCC3IO\_MVGP)}$	3.3-V I/O current (TPS99000-Q1 SPI, TPS99000-Q1 Reset, PMIC_PARKZ, RESETZ)			1.7	1.8	mA
$I_{(VCC3IO\_INTF)}$	3.3-V I/O current (Host SPI, Host I^2C, Host IRQ, JTAG, Parallel Port)			1.7	1.8	mA
$I_{(VCC3IO\_FLSH)}$	3.3-V I/O current (Serial Flash SPI interface)			5.5	5.9	mA
$I_{(VCC3IO\_OSC)}$	3.3-V I/O current (Crystal/Oscillator)	With 3-kΩ external series resistor (R_S)		0.975	1.3	mA
$I_{(VCC3IO)}$	3.3-V I/O current (GPIO, PMIC_AD3, Mstr I^2C, TSTPT, ETM, and so forth)			12.6	13.5	mA
$I_{(VCC33A\_LVDS)}$	3.3-V I/O current (OpenLDI Interface - each port - 5 lanes active)			6.3	6.8	mA

(1) Typical-case power measured with PVT condition = nominal process, typical voltage, typical temperature (25°C junction). Input source 1152 × 576 24-bit 60-Hz OpenLDI with RGBW ramp image.

(2) Worst-case power PVT condition = corner process, high voltage, high temperature (125°C junction). Input source 1152 × 1152 24-bit. 60 Hz OpenLDI with pseudo-random noise image.

(3) Estimated current per supply was not directly measured. These values are based on an approximate expected current consumption percentage of the total measured current drawn by each voltage rail.

6.6 Electrical Characteristics for Fixed Voltage I/O

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	1.8-V LVCMOS (I/O type 3)		0.7 × VCC18IO			V
		3.3-V LVCMOS (I/O type 7)		2.0			
		3.3-V LVCMOS (I/O type 9)		2.0			
		3.3-V LVCMOS (I/O type 11)		2.0			
		3.3-V I^{2}C buffer (I/O type 12)		0.7 × VCC_INTF			
		3.3-V LVCMOS (I/O type 14)		2.0			
		3.3-V LVCMOS (I/O type 16,17)		0.7 × VCC3IO			
		3.3-V LVCMOS (I/O type 19)		2.0			
		3.3-V I^{2}C buffer (I/O type 15)		0.7 × VCC3IO			
V_{IL}	Low-level input threshold voltage	1.8-V LVCMOS (I/O type 3)				0.3 × VCC18IO	V
		3.3-V LVCMOS (I/O type 7)				0.8	
		3.3-V LVCMOS (I/O type 9)				0.8	
		3.3-V LVCMOS (I/O type 11)				0.8	
		3.3-V I^{2}C buffer (I/O type 12)				0.3 × VCC_INTF	
		3.3-V LVCMOS (I/O type 14)				0.8	
		3.3-V LVCMOS (I/O type 16,17)				0.3 × VCC3IO	
		3.3-V LVCMOS (I/O type 19)				0.8	
		3.3-V I^{2}C buffer (I/O type 15)				0.3 × VCC3IO	
V_{OH}	High-level output voltage	1.8-V LVCMOS (I/O type 1,2)	I_{OH} = Max rated	0.75 × VCC18IO			V
		3.3-V LVCMOS (I/O type 6)	I_{OH} = Max rated	2.4			
		3.3-V LVCMOS (I/O type 8)	I_{OH} = Max rated	2.4			
		3.3-V LVCMOS (I/O type 10)	I_{OH} = Max rated	2.4			
		3.3-V I^{2}C buffer (I/O type 12)	I_{OH} = Max rated	N/A			
		3.3-V LVCMOS (I/O type 13)	I_{OH} = Max rated	2.4			
		3.3-V I^{2}C buffer (I/O type 15)	I_{OH} = Max rated	N/A			
		3.3-V LVCMOS (I/O type 20)	I_{OH} = Max rated	2.4			
V_{OL}	Low-level output voltage	1.8-V LVCMOS (I/O type 1,2)	I_{OL} = Max rated			0.4	V
		3.3-V LVCMOS (I/O type 6)	I_{OL} = Max rated			0.4	
		3.3-V LVCMOS (I/O type 8)	I_{OL} = Max rated			0.4	
		3.3-V LVCMOS (I/O type 10)	I_{OL} = Max rated			0.4	
		3.3-V I^{2}C buffer (I/O type 12)	I_{OL} = Max rated			0.4	
		3.3-V LVCMOS (I/O type 13)	I_{OL} = Max rated			0.4	
		3.3-V I^{2}C buffer (I/O type 15)	I_{OL} = Max rated			0.4	
		3.3-V LVCMOS (I/O type 20)	I_{OL} = Max rated			0.4	
I_{OH}	High-level output current	1.8-V LVCMOS (I/O type 1)		6			mA
		1.8-V LVCMOS (I/O type 2)		7.2			
		3.3-V LVCMOS (I/O type 6)		6			
		3.3-V LVCMOS (I/O type 8)		6			
		3.3-V LVCMOS (I/O type 10)		6			
		3.3-V I^{2}C buffer (I/O type 12)		N/A			
		3.3-V LVCMOS (I/O type 13)		8			
		3.3-V I^{2}C buffer (I/O type 15)		N/A			
		3.3-V LVCMOS (I/O type 20)		6			

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(1) The number inside each parenthesis for the I/O refers to the type defined in Table 1.

Electrical Characteristics for Fixed Voltage I/O (continued)

over operating free-air temperature range (unless otherwise noted)(1)

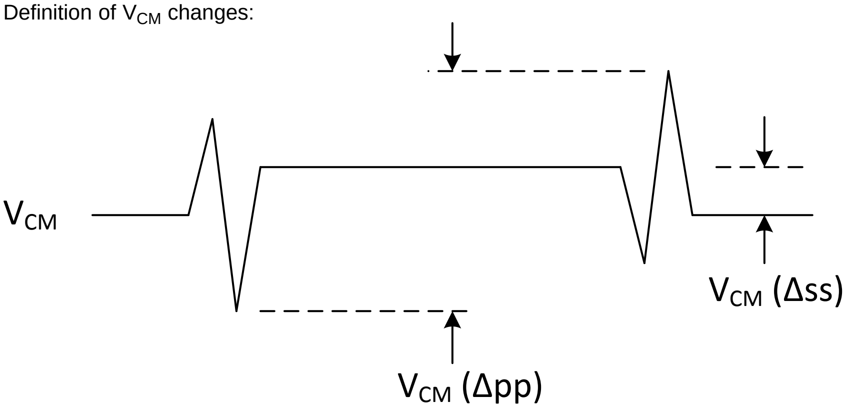
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Low-level output current	1.8-V LVCMOS (I/O type 1)		6			mA
		1.8-V LVCMOS (I/O type 2)		7.2			
		3.3-V LVCMOS (I/O type 6)		6			
		3.3-V LVCMOS (I/O type 8)		6			
		3.3-V LVCMOS (I/O type 10)		6			
		3.3-V I^2C buffer (I/O type 12)		3			
		3.3-V LVCMOS (I/O type 13)		8			
		3.3-V I^2C buffer (I/O type 15)		3			
		3.3-V LVCMOS (I/O type 20)		6			
I_{OZ}	High-impedance leakage current	1.8-V LVCMOS (I/O type 1,2)			±1.0	±10	µA
		3.3-V LVCMOS (I/O type 6)			±1.0	±10	
		3.3-V LVCMOS (I/O type 8)			±1.0	±10	
		3.3-V LVCMOS (I/O type 10)			±1.0	±10	
		3.3-V I^2C buffer (I/O type 12)				±10	
		3.3-V LVCMOS (I/O type 13)			±1.0	±10	
		3.3-V LVCMOS (I/O type 16)			±1.0		
		3.3-V I^2C buffer (I/O type 15)				±10	
		3.3-V LVCMOS (I/O type 20)			±1.0	±10	

6.7 DMD High-Speed Sub-LVDS Electrical Characteristics

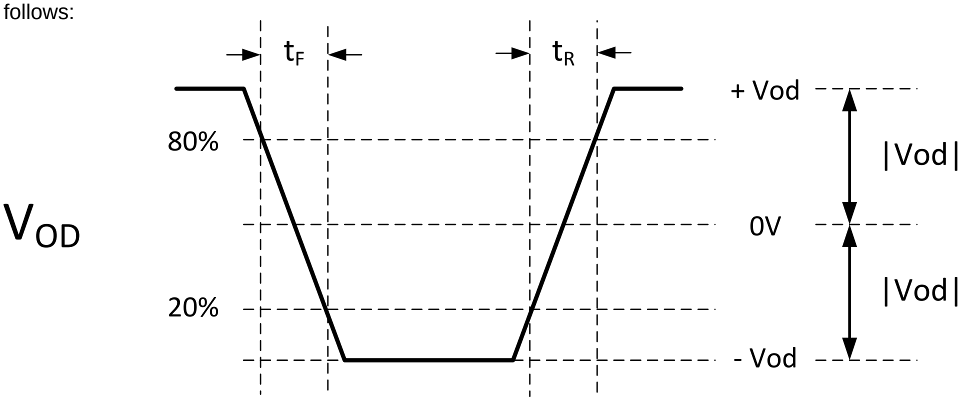
over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CM}	Steady-state common mode voltage	1.8-V sub-LVDS (I/O type 4,5)	0.8	0.9	1.0	V
V_{CM} (Δpp)(1)	V_{CM} change peak-to-peak (during switching)	1.8-V sub-LVDS (I/O type 4,5)			75	mV
V_{CM} (Δss)(1)	V_{CM} change steady state	1.8-V sub-LVDS (I/O type 4,5)	–10		10	mV
$\|V_{OD}\|$(2)	Differential output voltage magnitude. R_{BGR} = 75kΩ.	1.8-V sub-LVDS (I/O type 4,5)	155	200	250	mV
V_{OD} (Δ)(3)	V_{OD} change (between logic states)	1.8-V sub-LVDS (I/O type 4,5)	–10		10	mV
V_{OH}	Single-ended output voltage high	1.8-V sub-LVDS (I/O type 4,5)	0.88	1.00	1.125	V
V_{OL}	Single-ended output voltage low	1.8-V sub-LVDS (I/O type 4,5)	0.675	0.80	0.925	V
t_R(2)	Differential output rise time	1.8-V sub-LVDS (I/O type 4,5)			250	ps
t_F(2)	Differential output fall time	1.8-V sub-LVDS (I/O type 4,5)			250	ps
f_{MAX}	Max switching rate	1.8-V sub-LVDS (I/O type 4,5)			1200	Mbps
DCout	Output duty cycle	1.8-V sub-LVDS (I/O type 4,5)	45%	50%	55%	
Tx_{term}(1)	Internal differential termination	1.8-V sub-LVDS (I/O type 4,5)	80	100	120	Ω

(1) Definition of V_{CM} changes:



(2) Note that V_{OD} is the differential voltage swing measured across a 100-Ω termination resistance connected directly between the transmitter differential pins. $|V_{OD}|$ is the magnitude of the peak to peak voltage swing across the P and N output pins. Since V_{CM} cancels out when measured differentially, V_{OD} voltage swings relative to 0. Rise and fall times are defined for the differential V_{OD} signal as follows:



Differential Output Signal
(Note: V_{CM} is removed when signals are viewed differentially)

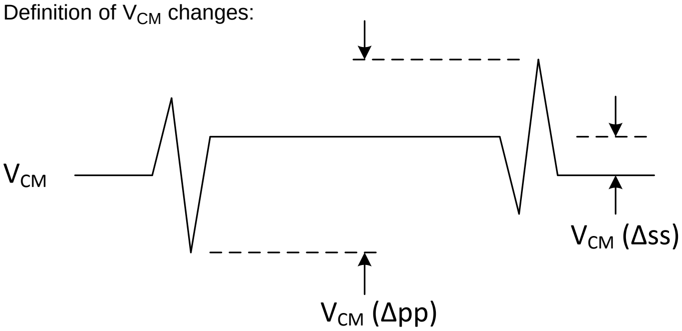
(3) When TX data input = '1', differential output voltage V_{OD1} is defined. When TX data input = '0', differential output voltage V_{OD0} is defined. As such, the steady state magnitude of the difference is: $|V_{OD}|$ (Δ) = $||V_{OD1}| - |V_{OD0}||$.

6.8 DMD Low-Speed Sub-LVDS Electrical Characteristics

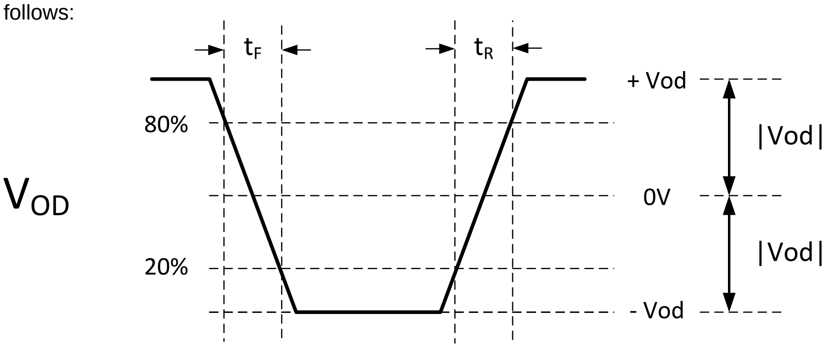
over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CM}	Steady-state common mode voltage	1.8-V sub-LVDS (I/O type 4,5)	0.8	0.9	1.0	V
V_{CM} (Δpp)(1)	V_{CM} change peak-to-peak (during switching)	1.8-V sub-LVDS (I/O type 4,5)			75	mV
V_{CM} (Δss)(1)	V_{CM} change steady state	1.8-V sub-LVDS (I/O type 4,5)	–10		10	mV
$\|V_{OD}\|$(2)	Differential output voltage magnitude. R_{BGR} = 75kΩ.	1.8-V sub-LVDS (I/O type 4,5)	155	200	250	mV
V_{OD} (Δ)(3)	V_{OD} change (between logic states)	1.8-V sub-LVDS (I/O type 4,5)	–10		10	mV
V_{OH}	Single-ended output voltage high	1.8-V sub-LVDS (I/O type 4,5)	0.88	1.00	1.125	V
V_{OL}	Single-ended output voltage low	1.8-V sub-LVDS (I/O type 4,5)	0.675	0.80	0.925	V
t_R(2)	Differential output rise time	1.8-V sub-LVDS (I/O type 4,5)			250	ps
t_F(2)	Differential output fall time	1.8-V sub-LVDS (I/O type 4,5)			250	ps
t_{MAX}	Max switching rate	1.8-V sub-LVDS (I/O type 4,5)			240	Mbps
DCout	Output duty cycle	1.8-V sub-LVDS (I/O type 4,5)	45%	50%	55%	
Tx_{term}	Internal differential termination	1.8-V sub-LVDS (I/O type 4,5)	80	100	120	Ω

(1) Definition of V_{CM} changes:



(2) Note that V_{OD} is the differential voltage swing measured across a 100-Ω termination resistance connected directly between the transmitter differential pins. $|V_{OD}|$ is the magnitude of the peak to peak voltage swing across the P and N output pins. Since V_{CM} cancels out when measured differentially, V_{OD} voltage swings relative to 0. Rise and fall times are defined for the differential V_{OD} signal as follows:



Differential Output Signal

(Note: V_{CM} is removed when signals are viewed differentially)

(3) When TX data input = '1', differential output voltage V_{OD1} is defined. When TX data input = '0', differential output voltage V_{OD0} is defined. As such, the steady state magnitude of the difference is: $|V_{OD}|$ (Δ) = $||V_{OD1}| - |V_{OD0}||$.

6.9 OpenLDI LVDS Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	NOM	MAX	UNIT
V_{CM}	Steady-state common mode voltage	3.3-V LVDS (I/O type 18)	0.35	1.2	1.6	V
$\|V_{ID}\|$	Differential Input Voltage	3.3-V LVDS (I/O type 18)	100		700	mV
Rx_{term}	Internal differential termination	3.3-V LVDS (I/O type 18)	90	111	132	Ω

6.10 Power Dissipation Characterisics

PARAMETER		VALUE	UNIT
P_{MAX}	Package - Maximum Power	1.22	W

6.11 System Oscillators Timing Requirements

			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, MOSC(1)		15.997	16.000	16.003	MHz
t_c	Cycle time, MOSC (1)		62.488	62.500	62.512	ns
$t_{w(H)}$	Pulse duration(2), MOSC, high	50% to 50% reference points (signal)	40% of t_c			
$t_{w(L)}$	Pulse duration(2), MOSC, low	50% to 50% reference points (signal)	40% of t_c			
t_t	Transition time(2), MOSC, $t_t = t_f / t_r$	20% to 80% reference points (signal)	0.2		2	ns
t_{jp}	Long term periodic jitter(2), MOSC (that is the deviation in period from ideal period due solely to high frequency jitter)				100	ps

(1) The MOSC input cannot support spread spectrum clock spreading.
(2) Applies only when driven through an external digital oscillator. This is a 1 sigma RMS value.

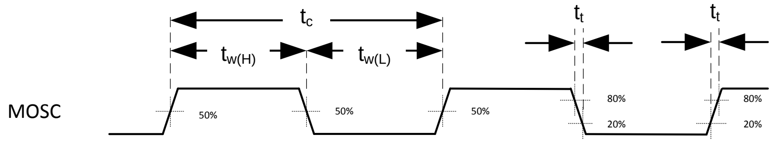


Figure 1. System Oscillators

Table 3. Crystal / Oscillator Electrical Characteristics

PARAMETER	NOMINAL	UNIT
PLL_REFCLK_I TO GND capacitance	3.5	pF
PLL_REFCLK_O TO GND capacitance	3.45	pF

6.12 Power Supply and Reset Timing Requirements

			MIN	MAX	UNIT
TPS99000-Q1 REQUIREMENTS[1]					
t_{ramp}	Power supply ramp time[2]	Power supply ramp to minimum recommended operating voltage	0.5	10	ms
t_{ps_aln}	1.1-V Power Supply Alignment[3]	Leading edge for application or removal of power. Each 1.1-V power supply to the DLPC230-Q1 must be applied simultaneously within this time.		10	µs
t_{rst}	RESETZ low to Power Supply disable[4]	Leading edge for removal of power	1.0		µs
$t_{w(L1)}$	Pulse duration, active low, RESETZ[4]	95% power to 50% RESETZ reference point At initial application of power	5.0		ms
$t_{w(L2)}$	Pulse duration, active low, RESETZ	50% to 50% reference points (RESETZ) Subsequent resets after initial application of power	1.0		µs
t_t	Transition time, RESETZ, $t_t = t_f$ and t_r	20% to 80% reference points (signal)		6	µs

(1) The TPS99000-Q1 controls power supply timing for the DLPC230-Q1. Refer to the TPS99000-Q1 data sheet for additional system power timing requirements.

(2) Power supplies do not need to ramp simultaneously, but each supply must reach its minimum voltage within the maximum ramp time specified.

(3) The DLPC230-Q1 does not require specific sequencing or alignment of 1.8-V and 3.3-V supplies. However, the TPS99000-Q1 enforces sequencing of the 1.1-V, 1.8-V, and 3.3-V voltage rails. The following describes DLPC230-Q1 behavior when the voltage rails are not brought up simultaneously:
   (a) VCCK (1.1-V core) Power = On, I/O Power = Off, RESETZ = '0': While this condition exists, additional leakage current may be drawn, and all outputs are unknown (likely to be a weak "low").
   (b) VCCK (1.1-V core) Power = Off, I/O Power = On, RESETZ = '0': While this condition exists all outputs are tri-stated.
   Neither of these two conditions will impact normal DLPC230-Q1 reliability.

(4) RESETZ must be held low if any supply (Core or I/O) is less than its minimum specified on value. For more information on RESETZ, see *Pin Configuration and Functions*.

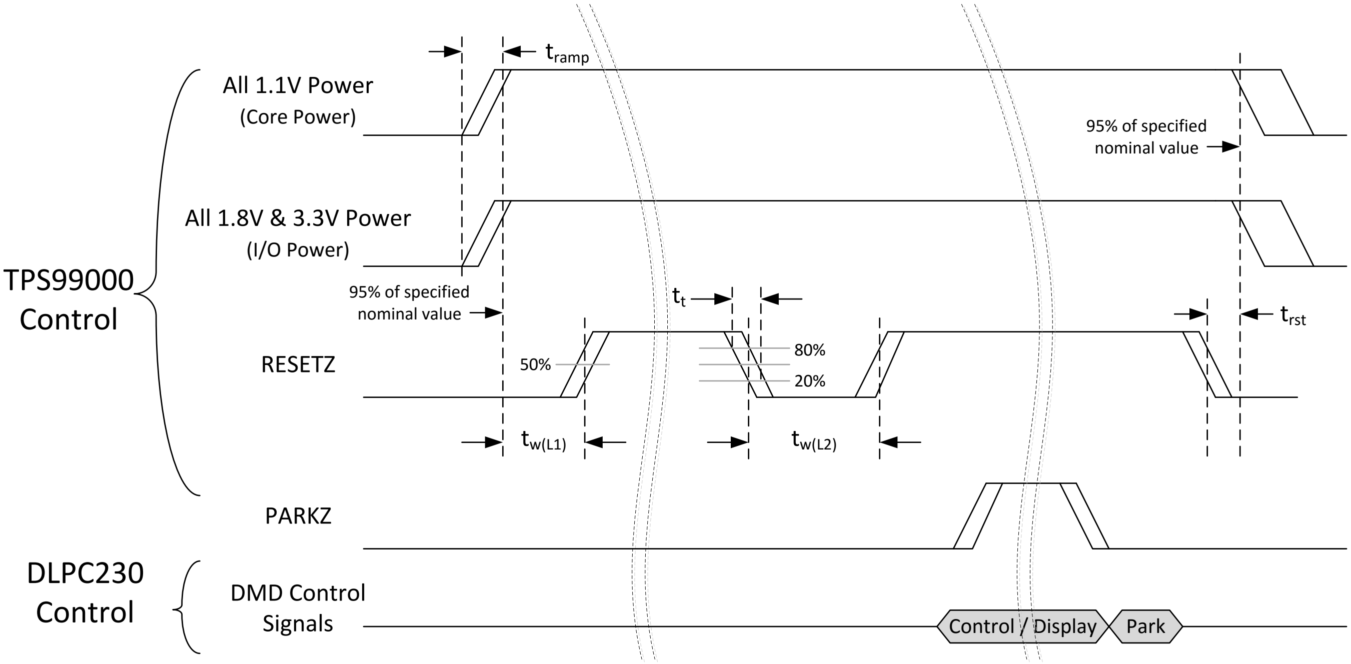

t_{ramp}
All 1.1V Power
(Core Power)
95% of specified nominal value
All 1.8V & 3.3V Power
(I/O Power)
TPS99000 Control
95% of specified nominal value
t_t
t_{rst}
RESETZ
50%
80%
20%
$t_{w(L1)}$
$t_{w(L2)}$
PARKZ
DLPC230 Control
DMD Control Signals
Control / Display
Park

Figure 2. Power Supply and RESETZ Timing

6.13 Parallel Interface General Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PCLK		12.0	110.0	MHz
t_{p_clkper}	Clock period, PCLK	50% reference points	9.091	83.33	ns
t_{p_wh}	Pulse duration low, PCLK	50% reference points	2.286		ns
t_{p_wl}	Pulse duration high, PCLK	50% reference points	2.286		ns
t_{p_su}	Setup time – HSYNC, DATEN, PDATA(23:0) valid before the active edge of PCLK	50% reference points	0.8		ns
t_{p_h}	Hold time – HSYNC, DATEN, PDATA(23:0) valid after the active edge of PCLK	50% reference points	0.8		ns
t_{t_clk}	Transition time – PCLK	20% to 80% reference points		6	ns
t_t	Transition time – all other signals on this port	20% to 80% reference points		6	ns
f_{spread}	Supported Spread Spectrum range	Percent of f_{clock} rate	–1%	+1% (1)	
f_{mod}	Supported Spread Spectrum Modulation Frequency (1) (2)		25	65 (3)	kHz
t_{p_clkjit}	Clock jitter, PCLK			t_{p_clkper} – 5.414	ps

(1) This value is limited by the maximum clock frequency for f_{clock} (that is, if f_{clock} = max clock freq, then f_{spread} max = 0%).
(2) Modulation Waveforms supported: Sine and Triangle.
(3) Spread spectrum modulation tested at a maximum of 35 kHz. Simulated up to 65 kHz.

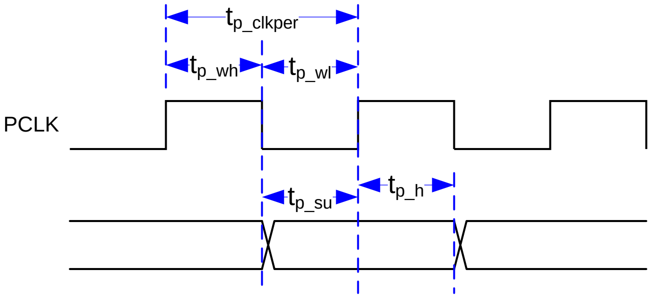


Figure 3. Parallel Interface General Timing

6.14 OpenLDI Interface General Timing Requirements

The DLPC230-Q1 ASIC input interface supports a subset of the industry standard OpenLDI (FPD-Link I) interface (Open LVDS Display Interface Specification v0.95 - May 13, 1999). Specifically, from the standard, the ASIC supports the 24-bit, Single Pixel Format, using the Unbalanced Operating Mode and Pixel Mapping.

			MIN	NOM	MAX	UNIT
f_{clock}	Clock frequency, L1_CLK_P/N, L2_CLK_P/N		20.0		110	MHz
t_p	Clock period, PCLK	50% reference points	9.091		50	ns
t_{skew}	Skew Margin (between clock and data)	f_{clock} > 85 MHz	–150	0	150	ps
		f_{clock} ≤ 85 MHz	–400	0	400	ps
t_{ip1}	Input data position 0		$-t_{skew}$	0	t_{skew}	ps
t_{ip0}	Input data position 1		$(t_p / 7) - t_{skew}$	$(t_p / 7)$	$(t_p / 7) + t_{skew}$	ps
t_{ip6}	Input data position 2		$2 * (t_p / 7) - t_{skew}$	$2 * (t_p / 7)$	$2 * (t_p / 7) + t_{skew}$	ps
t_{ip5}	Input data position 3		$3 * (t_p / 7) - t_{skew}$	$3 * (t_p / 7)$	$3 * (t_p / 7) + t_{skew}$	ps
t_{ip4}	Input data position 4		$4 * (t_p / 7) - t_{skew}$	$4 * (t_p / 7)$	$4 * (t_p / 7) + t_{skew}$	ps
t_{ip3}	Input data position 5		$5 * (t_p / 7) - t_{skew}$	$5 * (t_p / 7)$	$5 * (t_p / 7) + t_{skew}$	ps
t_{ip2}	Input data position 6		$6 * (t_p / 7) - t_{skew}$	$6 * (t_p / 7)$	$6 * (t_p / 7) + t_{skew}$	ps
t_{jitter}	Input Jitter Tolerance (cycle to cycle, peak to peak)				100	ps
f_{spread}	Supported Spread Spectrum range	percent of f_{clock} rate	–1%(1)		+1%(2)	
f_{mod}	Supported Spread Spectrum Modulation Frequency(3)(4)		25		65	kHz

(1) This value is limited by the minimum clock frequency for f_{clock} (that is, if f_{clock} = min clock freq, then f_{spread} max = 0%).
(2) This value is limited by the maximum clock frequency for f_{clock} (that is, if f_{clock} = max clock freq, then f_{spread} max = 0%).
(3) Modulation Waveforms supported: Sine and Triangle.
(4) Spread spectrum on OpenLDI interfaces was simulated, but not tested.

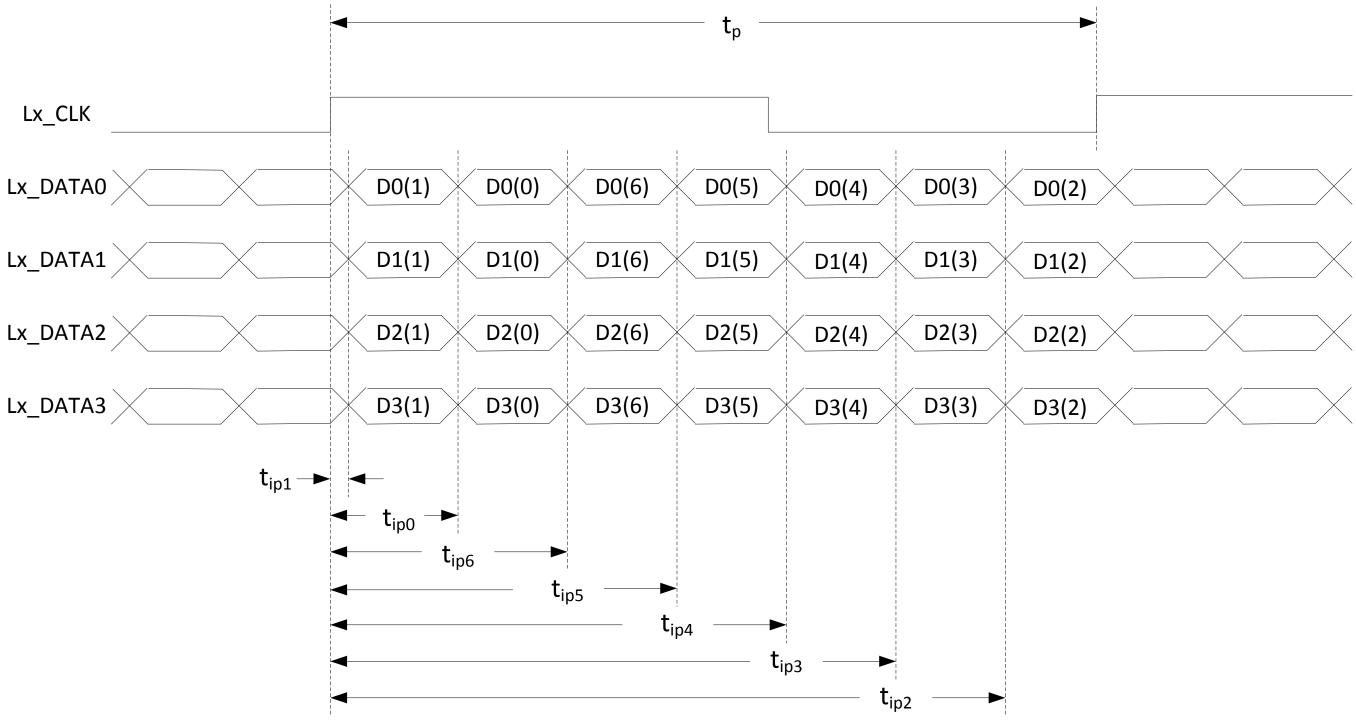


Figure 4. OpenLDI Interface Timing

6.15 Parallel/OpenLDI Interface Frame Timing Requirements

See (1)

			MIN	MAX	UNIT
VSYNC	Vertical Sync Rate (for the specified active source resolution)	1152 × 576 See *Supported Input Sources*	58	61	Hz
VSYNC	Vertical Sync Rate (for the specified active source resolution)	1152 × 1152 See *Supported Input Sources*	58	61	Hz
VSYNC	Vertical Sync Rate (for the specified active source resolution)	576 × 288 See *Supported Input Sources*	58	61	Hz
t_{p_vsw}	Pulse duration – VSYNC high	50% reference points	1		lines
t_{p_vbp}	Vertical back porch (VBP) – time from the leading edge of VSYNC to the leading edge HSYNC for the first active line (includes t_{p_vsw}).	50% reference points	2		lines
t_{p_vfp}	Vertical front porch (VFP) – time from the leading edge of the HSYNC following the last active line in a frame to the leading edge of VSYNC	50% reference points	1		lines
t_{p_tvb}	Total vertical blanking – time from the leading edge of HSYNC following the last active line of one frame to the leading edge of HSYNC for the first active line in the next frame. (This is equal to the sum of VBP (t_{p_vbp}) + VFP (t_{p_vfp}))	50% reference points	14		lines
t_{p_hsw}	Pulse duration – HSYNC high	50% reference points	8		PCLKs
t_{p_hbp}	Horizontal back porch – time from rising edge of HSYNC to rising edge of DATEN (includes t_{p_hsw})	50% reference points	9		PCLKs
t_{p_hfp}	Horizontal front porch – time from falling edge of DATEN to rising edge of HSYNC	50% reference points	8		PCLKs
t_{p_thb}	Total horizontal blanking	50% reference points	64		PCLKs
TPPL	Total Pixels Per Line			8191	Pixels

(1) While these requirements are not specific to the OpenLDI interface, they are appropriate for any source that drives an OpenLDI transmitter connected to the ASIC OpenLDI interface.

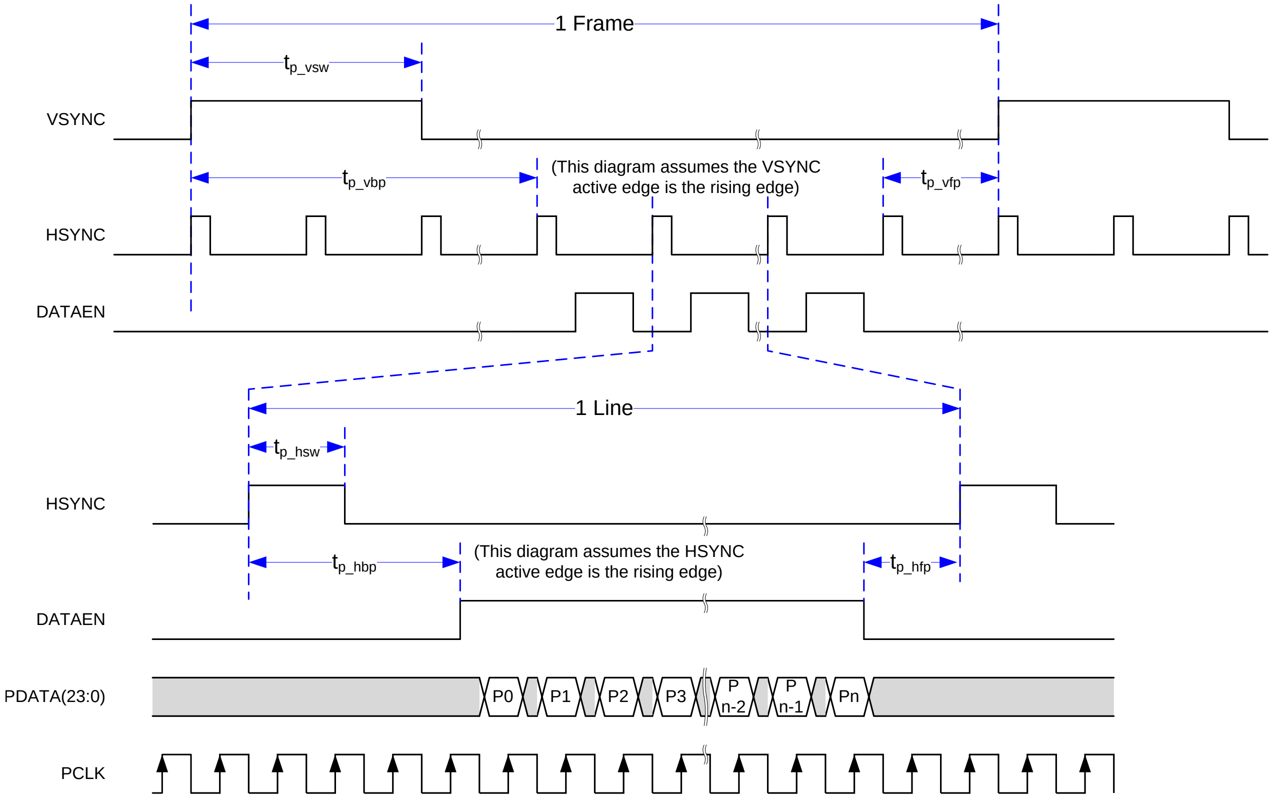

1 Frame
t_{p_vsw}
VSYNC
t_{p_vbp}
(This diagram assumes the VSYNC active edge is the rising edge)
t_{p_vfp}
HSYNC
DATAEN
1 Line
t_{p_hsw}
HSYNC
t_{p_hbp}
(This diagram assumes the HSYNC active edge is the rising edge)
t_{p_hfp}
DATAEN
PDATA(23:0)
P0
P1
P2
P3
P n-2
P n-1
Pn
PCLK

Figure 5. Source Frame Timing

6.16 Host/Diagnostic Port SPI Interface Timing Requirements

The DLPC230-Q1 ASIC Host/Diagnostic SPI port interface timing requirements are shown below.(1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, HOST_SPI_CLK (50% reference points)			10.00	MHz
t_{p_wh}	Pulse duration low, HOST_SPI_CLK (50% reference points)		45.0		ns
t_{p_wl}	Pulse duration high, HOST_SPI_CLK (50% reference points)		45.0		ns
t_t	Transition time – all input signals	20% to 80% reference points		6	ns
t_{p_su}	Setup time – HOST_SPI_DIN valid before HOST_SPI_CLK capture edge (50% reference points)		10.0		ns
t_{p_h}	Hold time – HOST_SPI_DIN valid after HOST_SPI_CLK capture edge	50% reference points	18.0		ns
t_{out}	Clock-to-Data out - HOST_SPI_DOUT from HOST_SPI_CLK launch edge (50% reference points)		0.0	35.0	ns

(1) The DLPC230-Q1 Host/Diagnostic Port SPI interface supports SPI Modes 0, 1, 2, and 3 (that is, both clock polarities and both clock phases). The HOST_SPI_MODE input must be set to match the SPI mode being used.

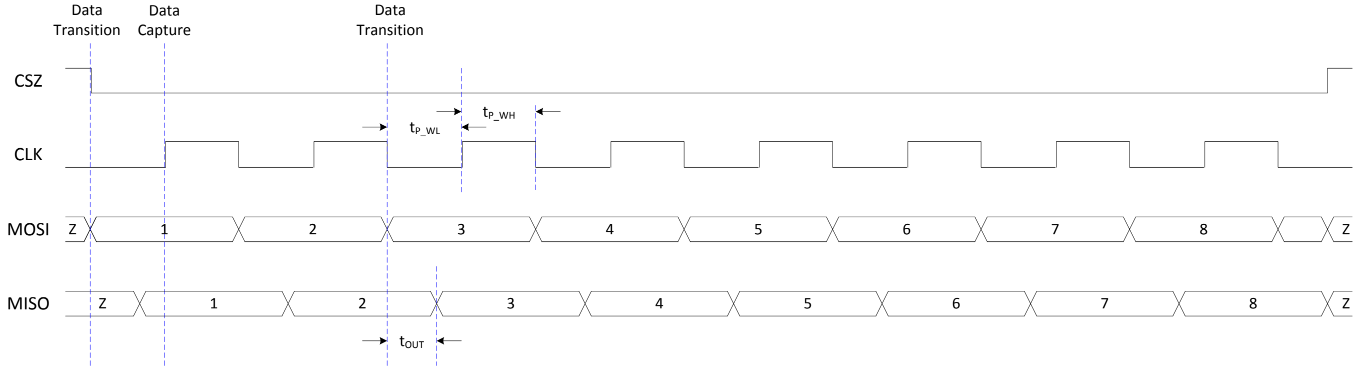


Figure 6. Host/Diagnostic Port SPI Interface Timing
(Example: SPI Mode 0 (Clock Polarity = 0, Clock Phase = 0))

6.17 Host/Diagnostic Port I^{2}C Interface Timing Requirements

The DLPC230-Q1 ASIC Host/Diagnostic I^{2}C port interface timing requirements are shown below.(1)(2)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, HOST_I^{2}C_SCL (50% reference points)	Fast-Mode		400	kHz
		Standard Mode		100	
C_L	Capacitive Load (for each bus line)			200	pF

(1) Meets all I^{2}C timing per the I^{2}C Bus Specification (except for capacitive loading as specified above). For reference see version 2.1 of the Phillips/NXP specification.

(2) The maximum clock frequency does not account for rise time, nor added capacitance of PCB or external components which may adversely impact this value.

6.18 Flash Interface Timing Requirements(1)

The DLPC230-Q1 ASIC flash memory interface consists of a SPI serial interface. See *Serial Flash Interface*.

			MIN	MAX	UNIT
f_{clock}	Clock frequency, FLSH_SPI_CLK	When VCC3IO_FLSH = 3.3 VDC	9.998	50.01(2)	MHz
t_{p_clkper}	Clock period, FLSH_SPI_CLK (50% reference points)	When VCC3IO_FLSH = 3.3 VDC	20.0	100	ns
t_{p_wh}	Pulse duration low, FLSH_SPI_CLK (50% reference points)	When VCC3IO_FLSH = 3.3 VDC	9		ns
t_{p_wl}	Pulse duration high, FLSH_SPI_CLK (50% reference points)	When VCC3IO_FLSH = 3.3 VDC	9		ns
t_t	Transition time – all input signals	20% to 80% reference points		6	ns
t_{p_su}	Setup time – FLSH_SPI_DIO[3:0] valid before FLSH_SPI_CLK falling edge (50% reference points)	When VCC3IO_FLSH = 3.3 VDC	7.0		ns
t_{p_h}	Hold time – FLSH_SPI_DIO[3:0] valid after FLSH_SPI_CLK falling edge	50% reference points	0.0		ns
t_{p_clqv}	FLSH_SPI_DIO[3:0] output delay valid time (with respect to falling edge of FLSH_SPI_CLK or falling edge of FLSH_SPI_CSZ) (50% reference points)	When VCC3IO_FLSH = 3.3 VDC	–3.0	3.0	ns

(1) The DLPC230-Q1 communicates with flash devices using a slight variant of SPI Transfer Mode 0 (that is, clock polarity = 0, clock phase = 0). Instead of capturing MISO data on the clock edge opposite from that used to transmit MOSI data, the DLPC230-Q1 captures MISO data on the same clock edge used to transmit the next MOSI data. As such, the DLPC230-Q1 Flash SPI interface requires that MISO data from the flash device remain active until the end of the full clock cycle to allow the last data bit to be captured. This is shown in Figure 8.

(2) The actual maximum clock rate driven from the DLPC230-Q1 may be slightly less than this value.

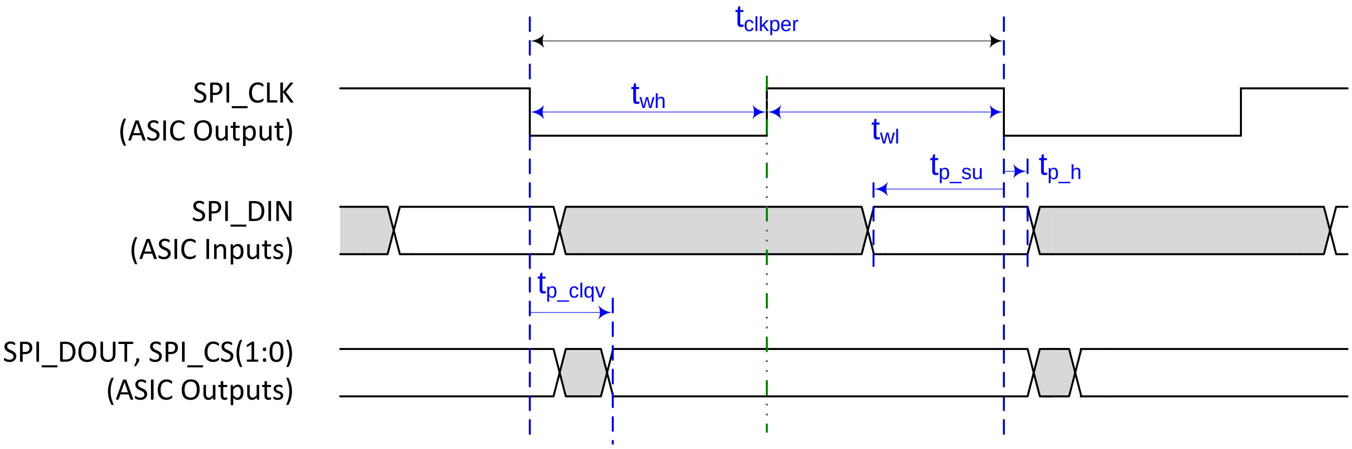


Figure 7. Flash Interface Timing

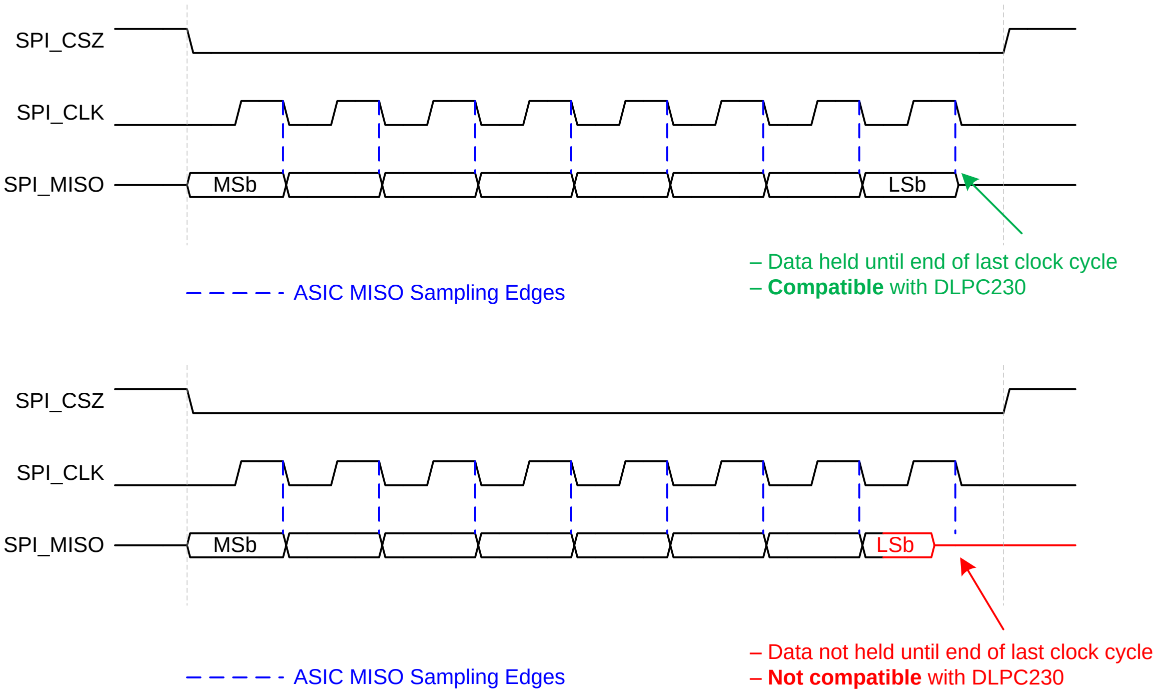

SPI_CSZ
SPI_CLK
SPI_MISO
MSb
LSb
– Data held until end of last clock cycle
– Compatible with DLPC230
ASIC MISO Sampling Edges
SPI_CSZ
SPI_CLK
SPI_MISO
MSb
LSb
– Data not held until end of last clock cycle
– Not compatible with DLPC230
ASIC MISO Sampling Edges

Figure 8. Flash Interface Data Capture Requirements

6.19 TPS99000-Q1 SPI Interface Timing Requirements[(1)]

The DLPC230-Q1 ASIC to TPS99000-Q1 interface consists of a SPI serial interface.

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PMIC_SPI_CLK		9.998	30.006	MHz
t_{p_clkper}	Clock period, PMIC_SPI_CLK (50% reference points)		33.3	100	ns
t_{p_wh}	Pulse duration high, PMIC_SPI_CLK (50% reference points)		11.5		ns
t_{p_wl}	Pulse duration low, PMIC_SPI_CLK (50% reference points)		11.5		ns
t_t	Transition time – all input signals	20% to 80% reference points		6	ns
t_{p_su}	Setup time – PMIC_SPI_DIN valid before PMIC_SPI_CLK falling edge (50% reference points)		7.0		ns
t_{p_h}	Hold time – PMIC_SPI_DIN valid after PMIC_SPI_CLK falling edge	50% reference points	0.0		ns
t_{p_clqv}	PMIC_SPI_DOUT output delay (valid) time (with respect to falling edge of PMIC_SPI_CLK or falling edge of PMIC_SPI_CSZ0) (50% reference points)		–3.0	3.0	ns

(1) The DLPC230-Q1 communicates with the TPS99000-Q1 using a slight variant of SPI Transfer Mode 0 (that is, clock polarity = 0, clock phase = 0). Instead of capturing MISO data on the clock edge opposite from that used to transmit MOSI data, the DLPC230-Q1 captures MISO data on the same clock edge used to transmit the next MOSI data. As such, the DLPC230-Q1 SPI interface to the TPS99000-Q1 requires that MISO data from the TPS99000-Q1 remain active until the end of the full clock cycle to allow the last data bit to be captured. This is shown in Figure 12.

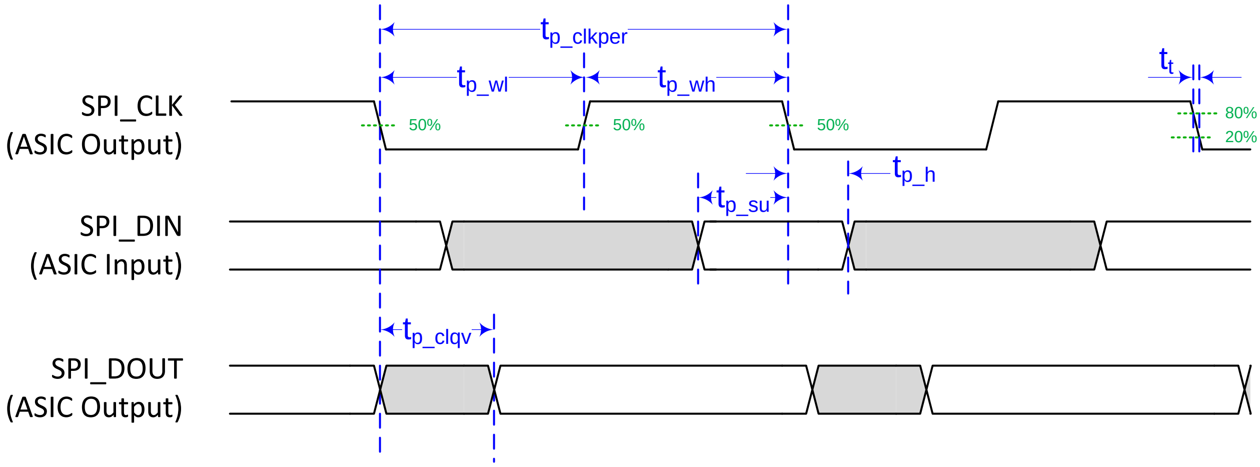


Figure 9. TPS99000-Q1 Interface Timing

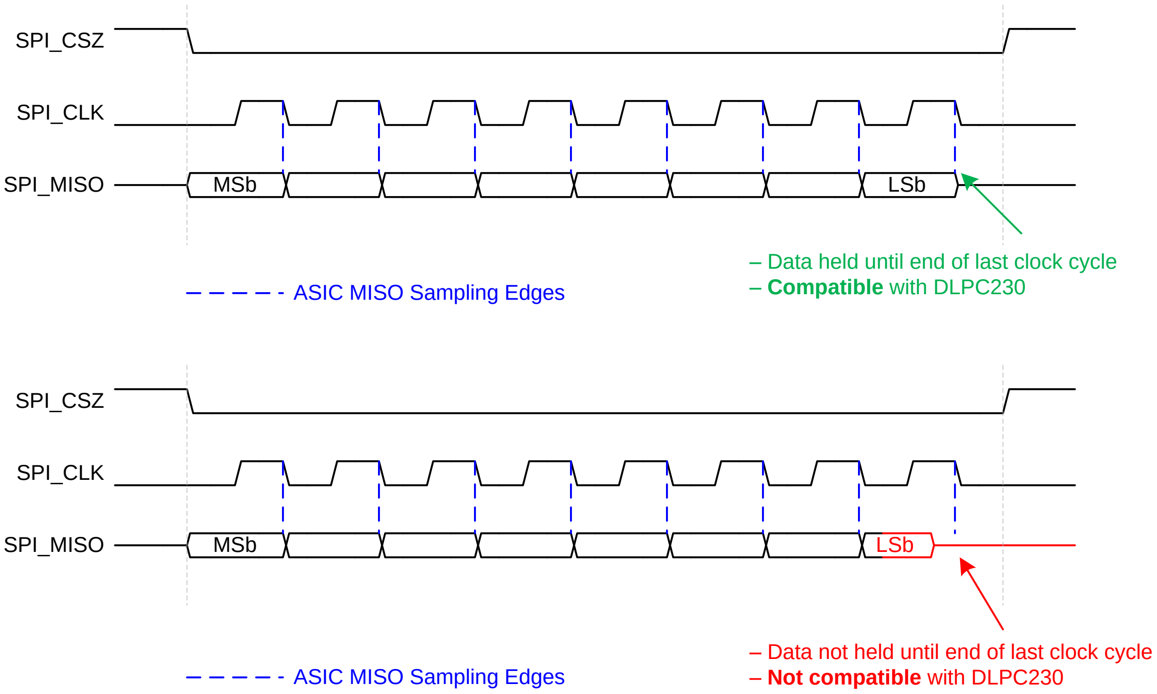

SPI_CSZ
SPI_CLK
SPI_MISO
MSb
LSb
– Data held until end of last clock cycle
– Compatible with DLPC230
ASIC MISO Sampling Edges
SPI_CSZ
SPI_CLK
SPI_MISO
MSb
LSb
– Data not held until end of last clock cycle
– Not compatible with DLPC230
ASIC MISO Sampling Edges

Figure 10. TPS99000-Q1 Interface Data Capture Requirements

6.20 TPS99000-Q1 AD3 Interface Timing Requirements(1)(2)(3)

The DLPC230-Q1 ASIC to TPS99000-Q1 AD3 interface is used to retrieve ADC measurements from the TPS99000-Q1. The interface is similar to SPI and includes a clock, MOSI, and MISO signal.

			MIN	MAX	UNIT
f_{clock}	Clock frequency, PMIC_AD3_CLK		29.326	30.006	MHz
t_{p_clkper}	Clock period, PMIC_AD3_CLK (50% reference points)		33.327	34.100	ns
t_{p_wh}	Pulse duration high, PMIC_AD3_CLK (50% reference points) (Referenced to t_{p_clkper})		40%		
t_{p_wl}	Pulse duration low, PMIC_AD3_CLK (50% reference points) (Referenced to t_{p_clkper})		40%		
t_t	Transition time – all input signals	20% to 80% reference points		6	ns
t_{p_su}	Setup time – PMIC_AD3_MISO valid before PMIC_AD3_CLK rising edge (50% reference points)		14.5		ns
t_{p_h}	Hold time – PMIC_AD3_MISO valid after PMIC_AD3_CLK rising edge (50% reference points)		0		ns
t_{p_clqv}	PMIC_AD3_MOSI output delay (valid) time (with respect to falling edge of PMIC_SPI_CLK) (50% reference points)		–2.0	2.0	ns

(1) PMIC_AD3_MOSI (Master (DLPC230-Q1) Output / Slave (TPS99000-Q1) Input) is transmitted on the falling edge of PMIC_AD3_CLK.
(2) PMIC_AD3_MISO (Master (DLPC230-Q1) Input / Slave (TPS99000-Q1) Output) is captured on the rising edge of PMIC_AD3_CLK.
(3) PMIC_AD3_CLK is used as the primary TPS99000-Q1 system clock in addition to supporting the AD3 interface.

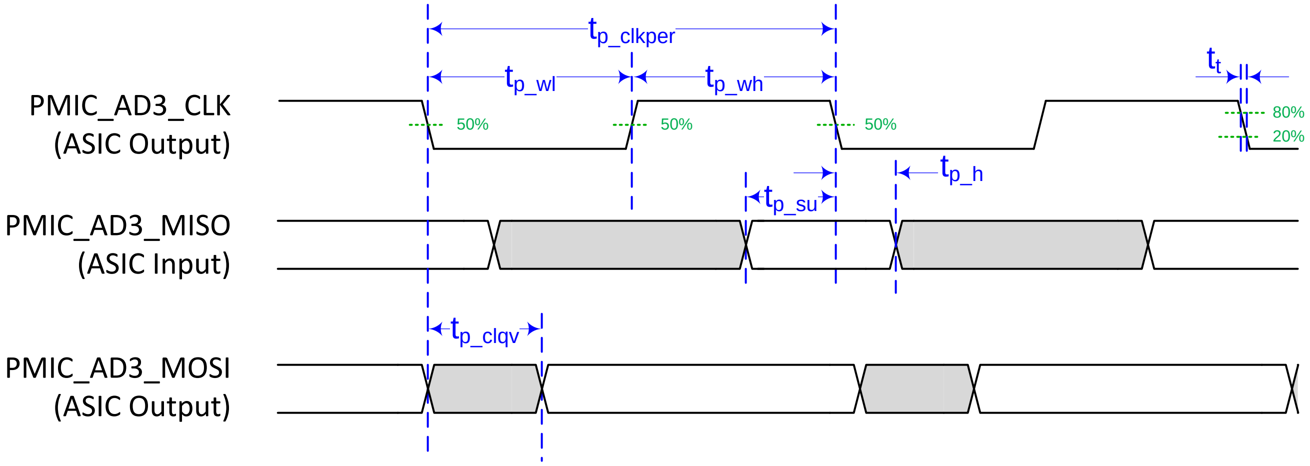

PMIC_AD3_CLK (ASIC Output)
PMIC_AD3_MISO (ASIC Input)
PMIC_AD3_MOSI (ASIC Output)
t_{p_clkper}
t_{p_wl}
t_{p_wh}
t_t
50%
50%
50%
80%
20%
t_{p_su}
t_{p_h}
t_{p_clqv}

Figure 11. TPS99000-Q1 AD3 Interface Timing

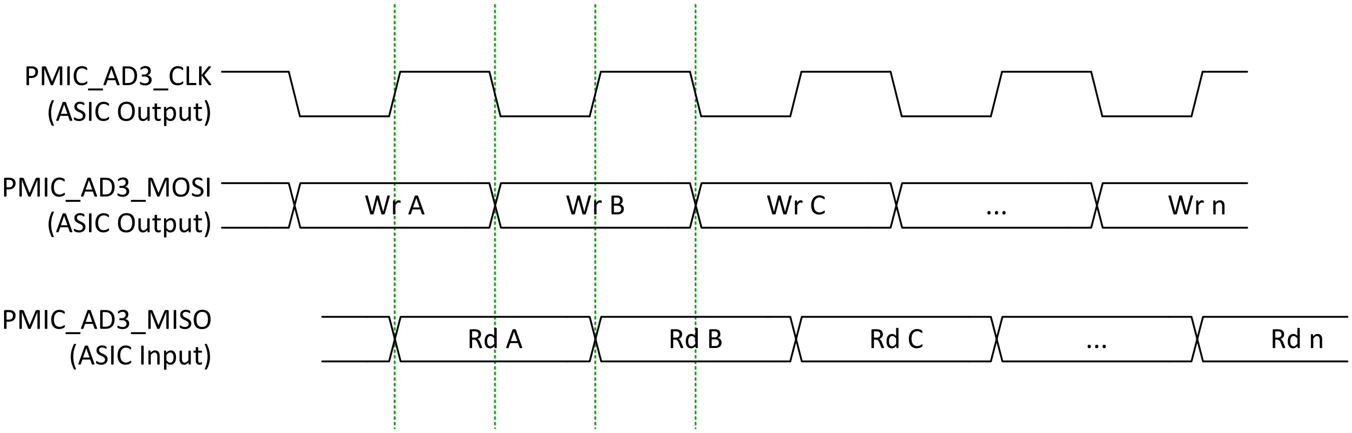

PMIC_AD3_CLK (ASIC Output)
PMIC_AD3_MOSI (ASIC Output)
PMIC_AD3_MISO (ASIC Input)
Wr A
Wr B
Wr C
...
Wr n
Rd A
Rd B
Rd C
...
Rd n

Figure 12. TPS99000-Q1 AD3 Data Capture and Transition

6.21 Master I^{2}C Port Interface Timing Requirements[1][2]

The DLPC230-Q1 ASIC Master I^{2}C port interface timing requirements are shown below.

			MIN	MAX	UNIT
f_{clock}	Clock frequency, MSTR_SCL (50% reference points)	Fast-Mode		400	kHz
		Standard Mode		100	
C_L	Capacitive Load (for each bus line)			200	pF

(1) Meets all I^{2}C timing per the I^{2}C Bus Specification (except for Capacitive Loading as specified above).
(2) The maximum clock frequency does not account for rise time, nor added capacitance of PCB or external components which may adversely impact this value.

6.22 Chipset Component Usage Specification

TI DLP® chipsets include a DMD and one or more controllers. Reliable function and operation of TI DMDs requires that they be used in conjunction with all of the other components in the applicable chipset, including those components that contain or implement TI DMD control technology, such as the DLPC230-Q1. TI DMD control technology is the TI technology and devices for operating or controlling a DLP® products DMD.

7 Parameter Measurement Information

7.1 HOST_IRQ Usage Model

In the DLPC230-Q1, the Host_IRQ signal is used to serve as an indication that a serious system error has occurred for which the ASIC has executed an emergency shutdown. The specific error(s) that precipitated the shutdown can be retrieved via the Host Command and Control interface. The actions that are taken by the ASIC for an emergency shutdown are:

- LEDs are disabled
- The DMD is parked and powered-down
- The ASIC operational mode is transitioned to Standby
- The precipitating errors are captured for later review
- The Host_IRQ signal is set to a high state

  To recover from an emergency shutdown, the system will require a full power cycle (De-assertion of PROJ_ON). The host should be sure to obtain the error history from the ASIC prior to this full reset, as the reset will remove all error history from the system.

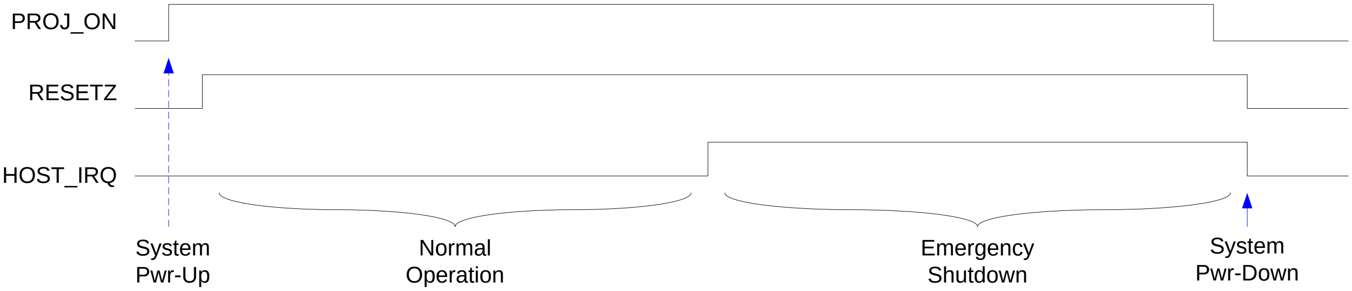


Figure 13. Host IRQ Timing

7.2 Input Source

The video input source can be configured to accomodate various desired input resolutions. Image processing such as scaling and line replication may be applied in order to achieve the necessary display resolution. The desired input resolution may depend on product configuration.

7.2.1 Supported Input Sources

The supported sources with typical timings are shown in Table 4. These typical timing examples do not minimize blanking or pixel clock rate. Refer to *Parallel/OpenLDI Interface Frame Timing Requirements* for minimum timing specifications.

Table 4. Typical Timing for Supported Source Resolutions

HORIZONTAL RESOLUTION	VERTICAL RESOLUTION	HORIZONTAL BLANKING				VERTICAL BLANKING				VERTICAL RATE (Hz)	PIXEL CLOCK (MHz)
		TOTAL[1]	SYNC (PIXEL CLOCKS)	BACK PORCH (PIXEL CLOCKS)	FRONT PORCH (PIXEL CLOCKS)	TOTAL[1]	SYNC (LINES)	BACK PORCH (LINES)	FRONT PORCH (LINES)		
576	288	322	8	154	160	181	8	83	90	60	25.270
1152	576	80	8	32	40	25	8	14	3	60	44.426
1152	1152	80	8	32	40	33	8	6	19	60	87.595

(1) Sync clocks/lines are counted as a part of total blanking in these examples (Total Blanking = sync + back porch + front porch). Note that the specifications in *Parallel/OpenLDI Interface Frame Timing Requirements* include sync width as part of back porch (Total Blanking = back porch + front porch).

7.2.2 Parallel Interface Supported Data Transfer Formats

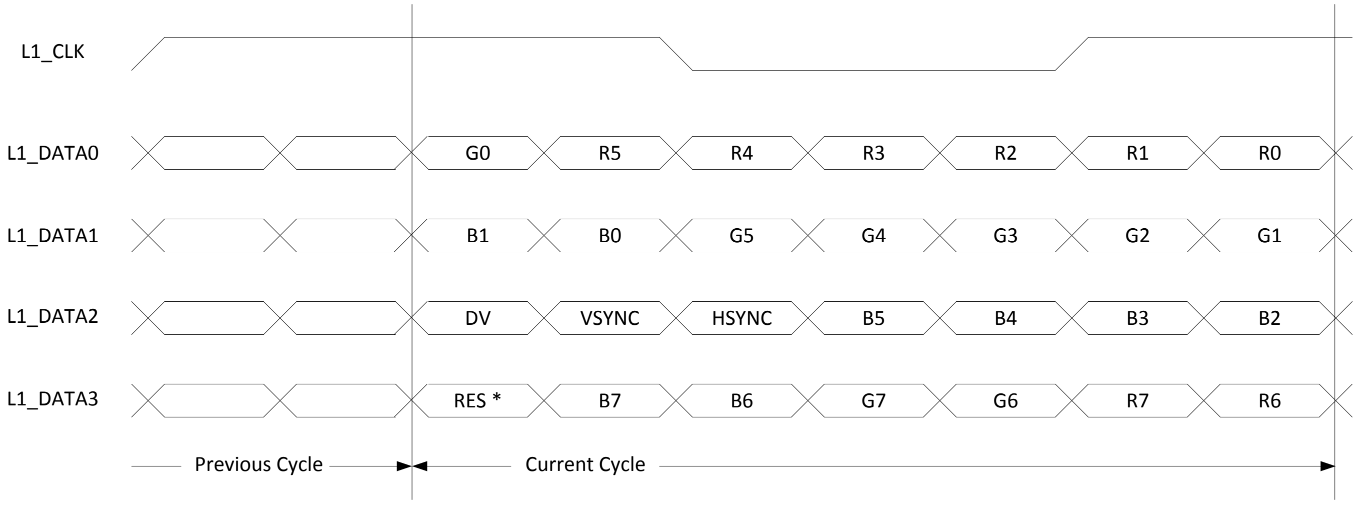
- 24-bit RGB888 on a 24 data wire interface

7.2.2.1 OpenLDI Interface Supported Data Transfer Formats

- 1X 24-bit RGB888 on a 5-lane differential interface

OpenLDI Interface Bit Mapping Modes shows the required OpenLDI bus mapping for the supported data transfer formats.

7.2.2.1.1 OpenLDI Interface Bit Mapping Modes


L1_CLK
L1_DATA0
G0
R5
R4
R3
R2
R1
R0
L1_DATA1
B1
B0
G5
G4
G3
G2
G1
L1_DATA2
DV
VSYNC
HSYNC
B5
B4
B3
B2
L1_DATA3
RES *
B7
B6
G7
G6
R7
R6
Previous Cycle
Current Cycle

A. * = Use is undefined/reserved

Figure 14. OpenLDI 24-bit Single Port

8 Detailed Description

8.1 Overview

The automotive DLP® Products chipset consists of three components – the DLP553X-Q1, the DLPC230-Q1, and the TPS99000-Q1. The DLPC230-Q1 is the display controller for the DMD - it formats incoming video and controls the timing of the DMD. It also controls TPS99000-Q1 light source signal timing to coordinate with DMD timing in order to synchronize light output with DMD mirror movement. The DLPC230-Q1 is designed for automotive applications with a wide operating temperature range and diagnostic features to identify and correct specific system-level failures. The DLPC230-Q1 provides interfaces such as OpenLDI (video) and sub-LVDS (DMD interface) to minimize power consumption and EMI. Applications include head-up display (HUD) and adaptive high beam and smart headlight.

8.2 Functional Block Diagram

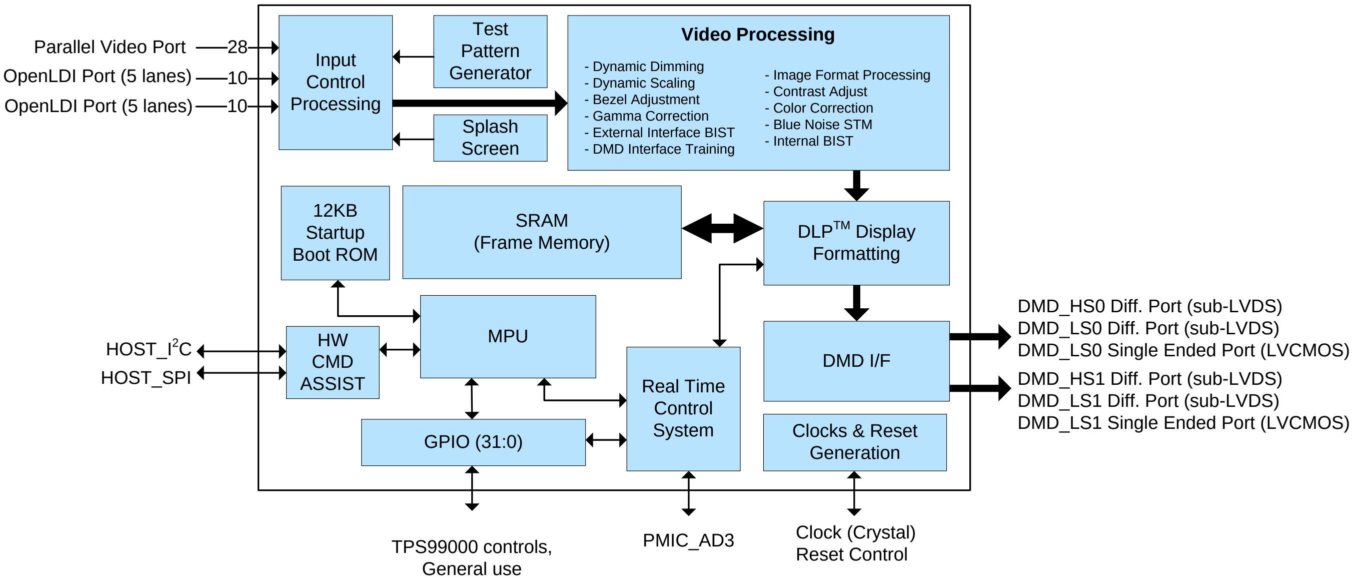

Parallel Video Port
28
OpenLDI Port (5 lanes)
10
OpenLDI Port (5 lanes)
10
Input Control Processing
Test Pattern Generator
Splash Screen
Video Processing
- Dynamic Dimming
- Dynamic Scaling
- Bezel Adjustment
- Gamma Correction
- External Interface BIST
- DMD Interface Training
- Image Format Processing
- Contrast Adjust
- Color Correction
- Blue Noise STM
- Internal BIST
12KB Startup Boot ROM
SRAM (Frame Memory)
DLP™ Display Formatting
HOST_I2C
HOST_SPI
HW CMD ASSIST
MPU
Real Time Control System
DMD I/F
Clocks & Reset Generation
GPIO (31:0)
DMD_HS0 Diff. Port (sub-LVDS)
DMD_LS0 Diff. Port (sub-LVDS)
DMD_LS0 Single Ended Port (LVCMOS)
DMD_HS1 Diff. Port (sub-LVDS)
DMD_LS1 Diff. Port (sub-LVDS)
DMD_LS1 Single Ended Port (LVCMOS)
TPS99000 controls, General use
PMIC_AD3
Clock (Crystal) Reset Control

Figure 15. Functional Block Diagram

8.3 Feature Description

8.3.1 Parallel Interface

The parallel interface complies with standard graphics interface protocol, which includes a vertical sync signal (VSYNC), horizontal sync signal (HSYNC), data valid signal (DATEN), a 24-bit data bus (PDATA_x), and a pixel clock (PCLK). Figure 5 shows the relationship of these signals.

NOTE

VSYNC must remain active at all times. If VSYNC is lost, the DMD must be transitioned to a safe state. When the system detects a VSYNC loss, it will switch to a test pattern or splash image as specified in flash by the Host.

The parallel interface supports intra-interface bit multiplexing (specified in flash) that can help with board layout as needed. The intra-interface bit multiplexing allows the mapping of any PDATA_x input to any internal data bus bit. When utilizing this feature, each unique input pin can only be mapped to one unique destination bit. The typical mapping is shown in Figure 16. An example of an alternate mapping is shown in Figure 17.

Feature Description (continued)

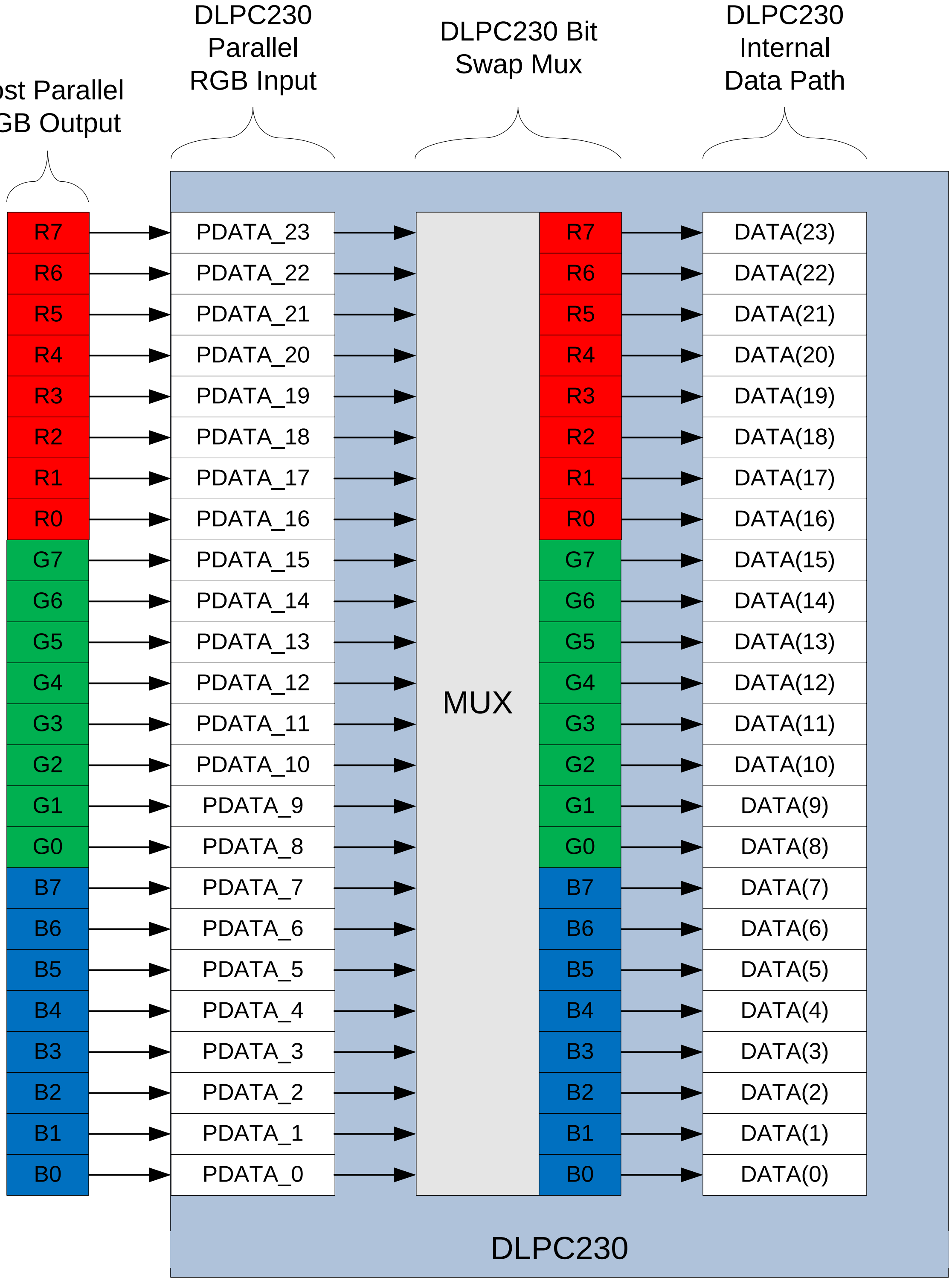

Host Parallel RGB Output
DLPC230 Parallel RGB Input
DLPC230 Bit Swap Mux
DLPC230 Internal Data Path
R7
R6
R5
R4
R3
R2
R1
R0
G7
G6
G5
G4
G3
G2
G1
G0
B7
B6
B5
B4
B3
B2
B1
B0
PDATA_23
PDATA_22
PDATA_21
PDATA_20
PDATA_19
PDATA_18
PDATA_17
PDATA_16
PDATA_15
PDATA_14
PDATA_13
PDATA_12
PDATA_11
PDATA_10
PDATA_9
PDATA_8
PDATA_7
PDATA_6
PDATA_5
PDATA_4
PDATA_3
PDATA_2
PDATA_1
PDATA_0
MUX
DATA(23)
DATA(22)
DATA(21)
DATA(20)
DATA(19)
DATA(18)
DATA(17)
DATA(16)
DATA(15)
DATA(14)
DATA(13)
DATA(12)
DATA(11)
DATA(10)
DATA(9)
DATA(8)
DATA(7)
DATA(6)
DATA(5)
DATA(4)
DATA(3)
DATA(2)
DATA(1)
DATA(0)
DLPC230

Figure 16. Example of Typical Parallel Port Bit Mapping

Feature Description (continued)

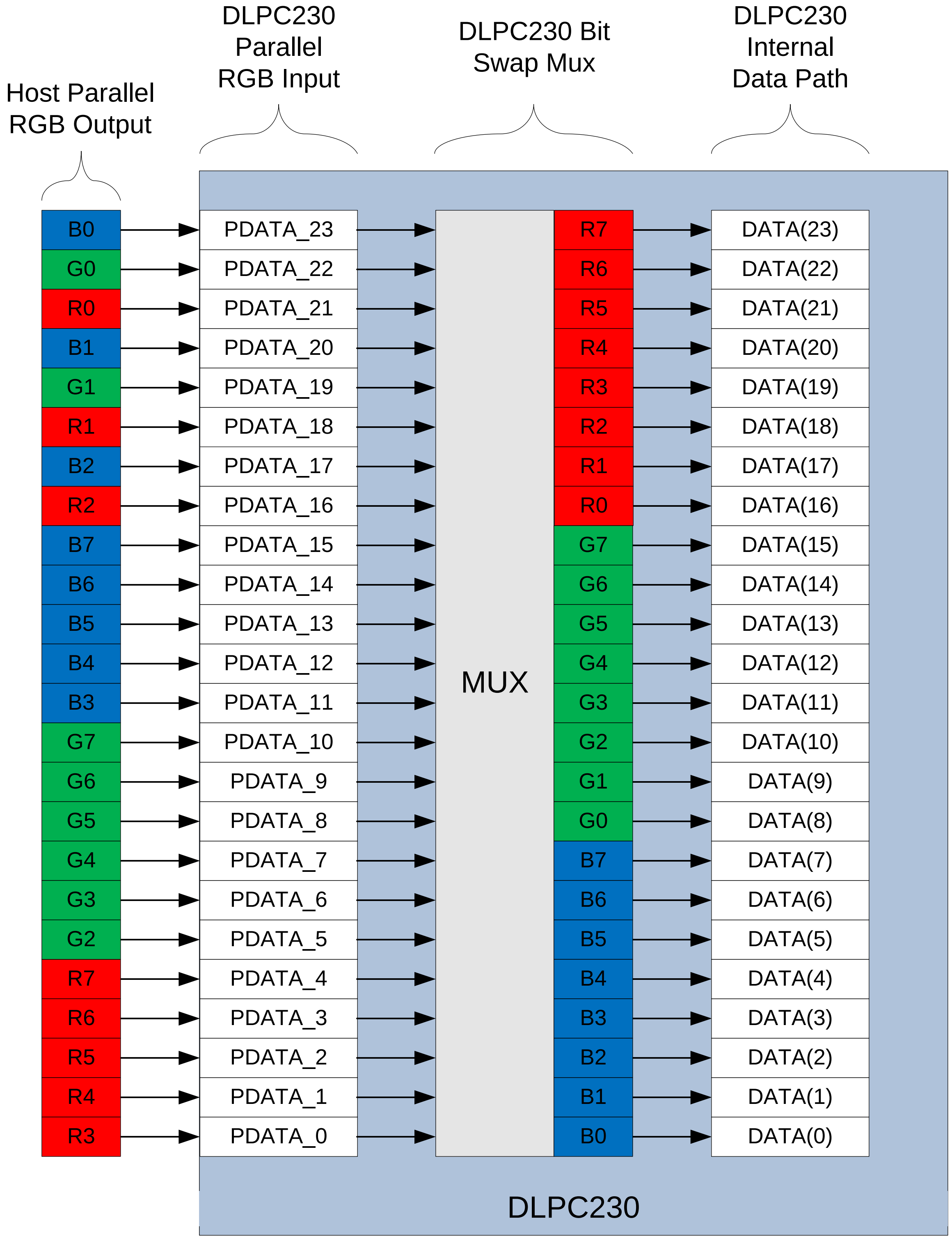

Host Parallel RGB Output
DLPC230 Parallel RGB Input
DLPC230 Bit Swap Mux
DLPC230 Internal Data Path
B0
G0
R0
B1
G1
R1
B2
R2
B7
B6
B5
B4
B3
G7
G6
G5
G4
G3
G2
R7
R6
R5
R4
R3
PDATA_23
PDATA_22
PDATA_21
PDATA_20
PDATA_19
PDATA_18
PDATA_17
PDATA_16
PDATA_15
PDATA_14
PDATA_13
PDATA_12
PDATA_11
PDATA_10
PDATA_9
PDATA_8
PDATA_7
PDATA_6
PDATA_5
PDATA_4
PDATA_3
PDATA_2
PDATA_1
PDATA_0
MUX
R7
R6
R5
R4
R3
R2
R1
R0
G7
G6
G5
G4
G3
G2
G1
G0
B7
B6
B5
B4
B3
B2
B1
B0
DATA(23)
DATA(22)
DATA(21)
DATA(20)
DATA(19)
DATA(18)
DATA(17)
DATA(16)
DATA(15)
DATA(14)
DATA(13)
DATA(12)
DATA(11)
DATA(10)
DATA(9)
DATA(8)
DATA(7)
DATA(6)
DATA(5)
DATA(4)
DATA(3)
DATA(2)
DATA(1)
DATA(0)
DLPC230

Figure 17. Example of Alternate Parallel Port Bit Mapping

Feature Description (continued)

8.3.2 OpenLDI Interface

Each DLPC230-Q1 OpenLDI interface port supports intra-port lane multiplexing (specified in flash) that can help with board layout as needed. The intra-port multiplexing allows the mapping of any Lx_DATA lane pair to any internal data lane pair. When utilizing this feature, each unique lane pair can only be mapped to one unique destination lane pair. The typical lane mapping is shown in Figure 18. An example of an alternate lane mapping is shown in Figure 19.

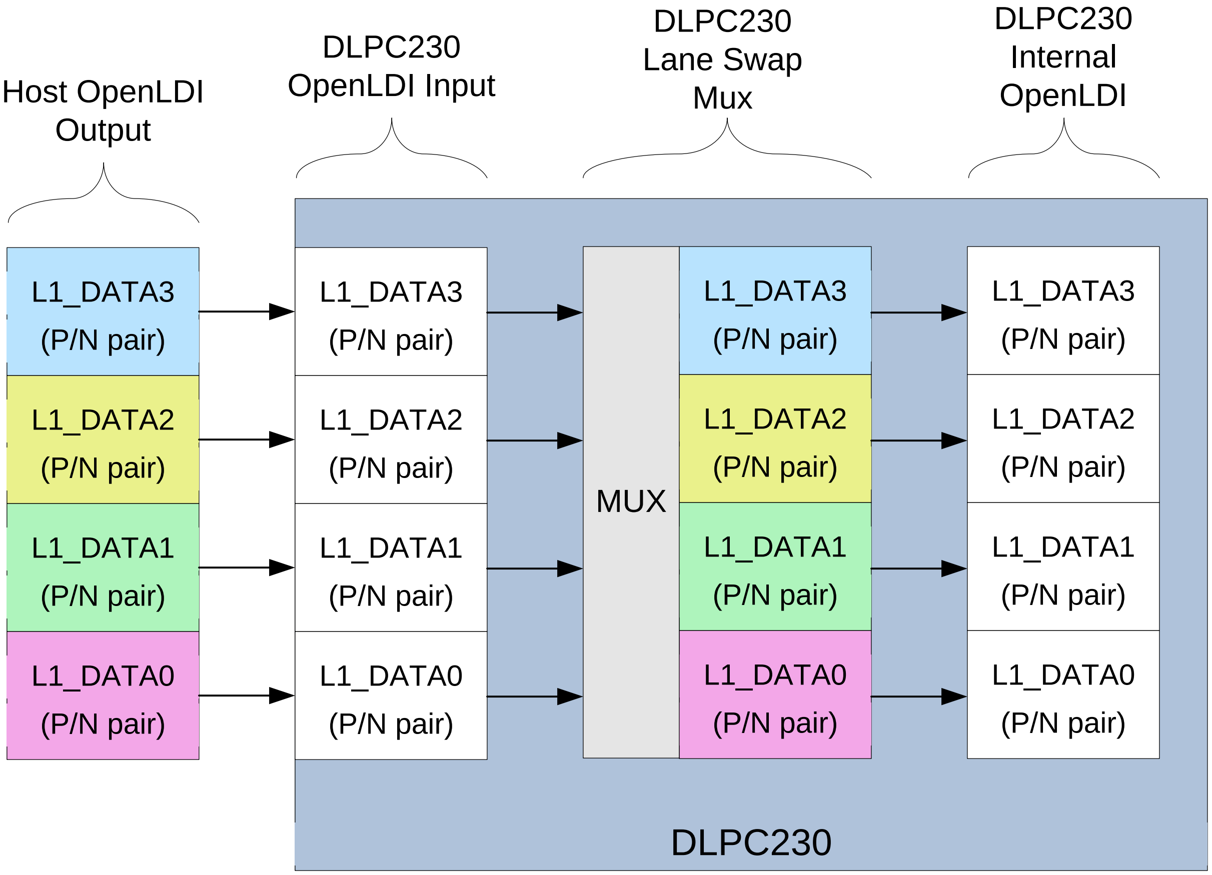

Host OpenLDI Output
DLPC230 OpenLDI Input
DLPC230 Lane Swap Mux
DLPC230 Internal OpenLDI
L1_DATA3 (P/N pair)
L1_DATA2 (P/N pair)
L1_DATA1 (P/N pair)
L1_DATA0 (P/N pair)
L1_DATA3 (P/N pair)
L1_DATA2 (P/N pair)
L1_DATA1 (P/N pair)
L1_DATA0 (P/N pair)
MUX
L1_DATA3 (P/N pair)
L1_DATA2 (P/N pair)
L1_DATA1 (P/N pair)
L1_DATA0 (P/N pair)
L1_DATA3 (P/N pair)
L1_DATA2 (P/N pair)
L1_DATA1 (P/N pair)
L1_DATA0 (P/N pair)
DLPC230

Figure 18. Example of Typical OpenLDI Port Lane Mapping

Feature Description (continued)

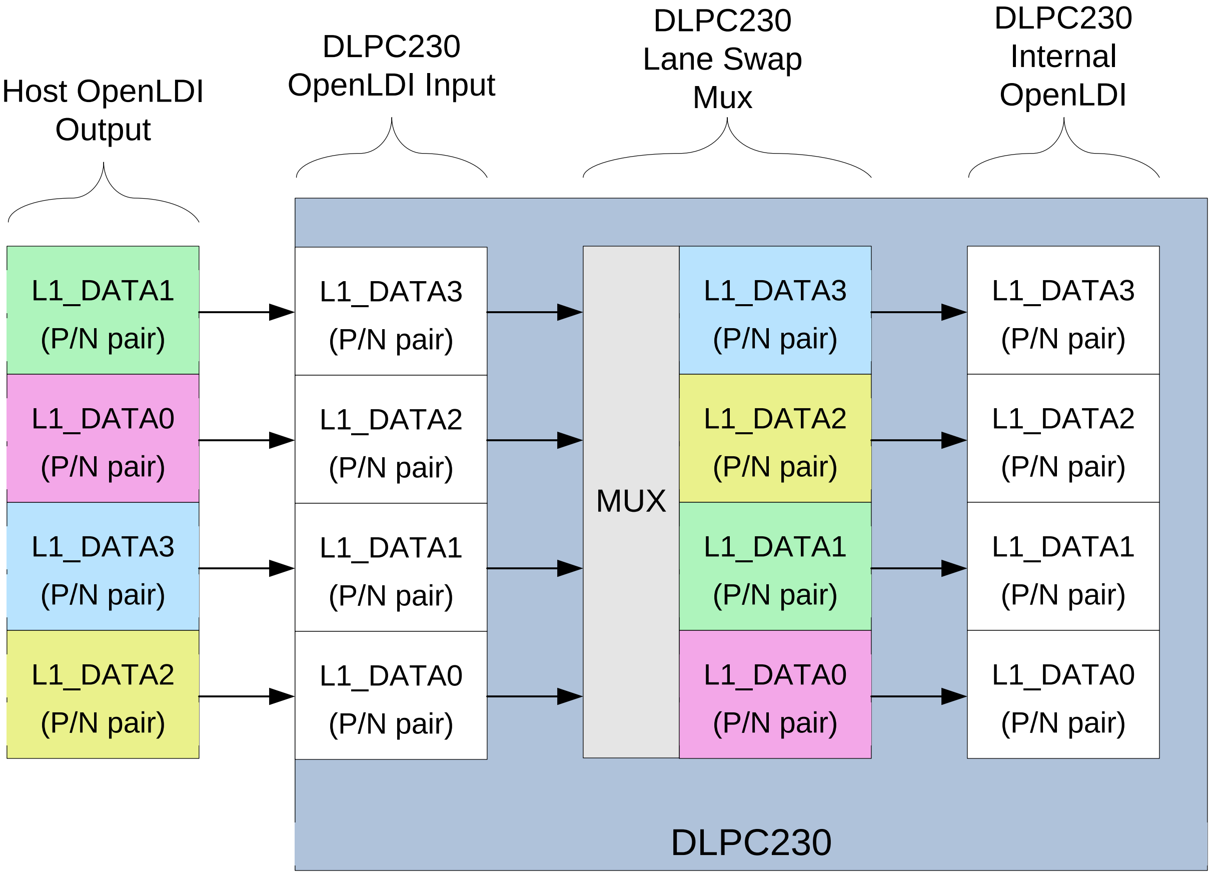

Host OpenLDI Output
DLPC230 OpenLDI Input
DLPC230 Lane Swap Mux
DLPC230 Internal OpenLDI
L1_DATA1 (P/N pair)
L1_DATA0 (P/N pair)
L1_DATA3 (P/N pair)
L1_DATA2 (P/N pair)
L1_DATA3 (P/N pair)
L1_DATA2 (P/N pair)
L1_DATA1 (P/N pair)
L1_DATA0 (P/N pair)
MUX
L1_DATA3 (P/N pair)
L1_DATA2 (P/N pair)
L1_DATA1 (P/N pair)
L1_DATA0 (P/N pair)
L1_DATA3 (P/N pair)
L1_DATA2 (P/N pair)
L1_DATA1 (P/N pair)
L1_DATA0 (P/N pair)
DLPC230

Figure 19. Example of Alternate OpenLDI Port Lane Mapping

Feature Description (continued)

8.3.3 DMD (Sub-LVDS) Interface

The DLPC230-Q1 ASIC DMD interface supports two high-speed sub-LVDS output-only interfaces for data transmission, a single low-speed sub-LVDS output-only interface for command write transactions, as well as a low-speed single-ended input interface used for command read transactions. The DLPC230-Q1 supports a limited number of DMD interface swap configurations (specified in Flash) that can help board layout by remapping specific combinations of DMD interface lines to other DMD interface lines as needed. Table 5 shows some of the options available.

Table 5. ASIC to 8-Lane DMD Pin Mapping Options

DLPC230-Q1 ASIC PIN ROUTING OPTIONS TO DMD PINS				DMD PINS
BASELINE	FULL FLIP HS0/HS1 180	SWAP HS0 PORT WITH HS1 PORT	SWAP HS0 PORT WITH HS1 PORT AND FULL FLIP 180	
HS0_WDATA0_P HS0_WDATA0_N	HS0_WDATA7_P HS0_WDATA7_N	HS1_WDATA0_P HS1_WDATA0_N	HS1_WDATA7_P HS1_WDATA7_N	D_AP(0) D_AN(0)
HS0_WDATA1_P HS0_WDATA1_N	HS0_WDATA6_P HS0_WDATA6_N	HS1_WDATA1_P HS1_WDATA1_N	HS1_WDATA6_P HS1_WDATA6_N	D_AP(1) D_AN(1)
HS0_WDATA2_P HS0_WDATA2_N	HS0_WDATA5_P HS0_WDATA5_N	HS1_WDATA2_P HS1_WDATA2_N	HS1_WDATA5_P HS1_WDATA5_N	D_AP(2) D_AN(2)
HS0_WDATA3_P HS0_WDATA3_N	HS0_WDATA4_P HS0_WDATA4_N	HS1_WDATA3_P HS1_WDATA3_N	HS1_WDATA4_P HS1_WDATA4_N	D_AP(3) D_AN(3)
HS0_WDATA4_P HS0_WDATA4_N	HS0_WDATA3_P HS0_WDATA3_N	HS1_WDATA4_P HS1_WDATA4_N	HS1_WDATA3_P HS1_WDATA3_N	D_AP(4) D_AN(4)
HS0_WDATA5_P HS0_WDATA5_N	HS0_WDATA2_P HS0_WDATA2_N	HS1_WDATA5_P HS1_WDATA5_N	HS1_WDATA2_P HS1_WDATA2_N	D_AP(5) D_AN(5)
HS0_WDATA6_P HS0_WDATA6_N	HS0_WDATA1_P HS0_WDATA1_N	HS1_WDATA6_P HS1_WDATA6_N	HS1_WDATA1_P HS1_WDATA1_N	D_AP(6) D_AN(6)
HS0_WDATA7_P HS0_WDATA7_N	HS0_WDATA0_P HS0_WDATA0_N	HS1_WDATA7_P HS1_WDATA7_N	HS1_WDATA0_P HS1_WDATA0_N	D_AP(7) D_AN(7)
HS1_WDATA0_P HS1_WDATA0_N	HS1_WDATA7_P HS1_WDATA7_N	HS0_WDATA0_P HS0_WDATA0_N	HS0_WDATA7_P HS0_WDATA7_N	D_BP(0) D_BN(0)
HS1_WDATA1_P HS1_WDATA1_N	HS1_WDATA6_P HS1_WDATA6_N	HS0_WDATA1_P HS0_WDATA1_N	HS0_WDATA6_P HS0_WDATA6_N	D_BP(1) D_BN(1)
HS1_WDATA2_P HS1_WDATA2_N	HS1_WDATA5_P HS1_WDATA5_N	HS0_WDATA2_P HS0_WDATA2_N	HS0_WDATA5_P HS0_WDATA5_N	D_BP(2) D_BN(2)
HS1_WDATA3_P HS1_WDATA3_N	HS1_WDATA4_P HS1_WDATA4_N	HS0_WDATA3_P HS0_WDATA3_N	HS0_WDATA4_P HS0_WDATA4_N	D_BP(3) D_BN(3)
HS1_WDATA4_P HS1_WDATA4_N	HS1_WDATA3_P HS1_WDATA3_N	HS0_WDATA4_P HS0_WDATA4_N	HS0_WDATA3_P HS0_WDATA3_N	D_BP(4) D_BN(4)
HS1_WDATA5_P HS1_WDATA5_N	HS1_WDATA2_P HS1_WDATA2_N	HS0_WDATA5_P HS0_WDATA5_N	HS0_WDATA2_P HS0_WDATA2_N	D_BP(5) D_BN(5)
HS1_WDATA6_P HS1_WDATA6_N	HS1_WDATA1_P HS1_WDATA1_N	HS0_WDATA6_P HS0_WDATA6_N	HS0_WDATA1_P HS0_WDATA1_N	D_BP(6) D_BN(6)
HS1_WDATA7_P HS1_WDATA7_N	HS1_WDATA0_P HS1_WDATA0_N	HS0_WDATA7_P HS0_WDATA7_N	HS0_WDATA0_P HS0_WDATA0_N	D_BP(7) D_BN(7)

8.3.4 Serial Flash Interface

The DLPC230-Q1 uses an external SPI serial flash memory device for configuration and operational data. The minimum supported size is 64 Mb. Larger devices may be required based on operation data and splash image size. The maximum supported size is 128 Mb. It should be noted that the system will support 256 Mb and 512 Mb devices, however, only the first 128 Mb of space will be used.

The external serial flash device is supported on a single SPI interface and mostly complies with industry standard SPI flash protocol (See Figure 8). The Host will specify the maximum supported flash interface frequency (which can be based on device limits, system limits, and/or other factors) and the system will program the closest obtainable value less than or equal to this specified maximum.

The DLPC230-Q1 ASIC flash must be connected to the designated SPI flash interface (FLSH_SPI_xxx) to enable support for system initialization, configuration, and operation.

The DLPC230-Q1 should support any flash device that is compatible with the modes of operation, features, and performance as defined in this section.

Table 6. SPI Flash Required Features or Modes of Operation

FEATURE	DLPC230-Q1 REQUIREMENT	COMMENTS
SPI interface width	Single Wire, Two Wire, Four Wire	
SPI protocol	SPI mode 0	
Fast READ addressing	Auto-incrementing	
Programming mode	Page mode	
Page size	256 Bytes	
Sector (or sub-sector) size	4 KB	Required erase granularity
Block structure	Uniform sector / sub-sector	
Block protection bits	0 = Disabled (with Default = 0 = Disabled)	
Status register bit(0)	Write in progress (WIP) {also called flash busy}	
Status register bit(1)	Write enable latch (WEN)	
Status register bits(6:2)	A value of 0 disables programming protection	
Status register bit(7)	Status register write protect (SRWP)	
Status register bits(15:8) (expanded status register), or Secondary Status register	The DLPC230-Q1 supports multi-byte status registers, as well as separate, additional status registers, but only for specific devices/register addresses. The supported registers and addresses are specified in Table 7.	

CAUTION

The selected SPI flash device must block repeated status writes from being written to internal register. The boot application writes to the flash device status register once per 256 bytes during programming. Most flash devices discard status register writes when the status content does not change. Some flash parts, such as the Micron N25Q128A13ESFA0F, do not block status writes when the status data is repeated. This causes the status register to exceed its maximum write limit after several programming cycles, making them incompatible with the DLPC230-Q1. Note that the main application does not write to the status register.

For each write operation, the DLPC230-Q1 boot application executes the following:

1. Write enable command
2. Write status command (to unprotect memory)
3. Read status command to poll the successful execution of the write status (repeated as needed)
4. Write enable command
5. Program or erase command
6. Read status command (repeated as needed) to poll the successful execution of the program or erase operation
7. Write disable command (during programming; this is not performed after erase command.)

For each write operation, the DLPC230-Q1 main application executes the following:

1. Write enable command
2. Program or erase command
3. Read status command (repeated as needed) to poll the successful execution of the program or erase operation
4. Write disable command (during programming; this is not performed after erase command)

The specific instruction op-code and timing compatibility requirements are listed in Table 7 and *Flash Interface Timing Requirements*. Note that DLPC230-Q1 does not read the flash’s full electronic signature ID and thus cannot automatically adapt protocol and clock rates based on the ID.

Table 7. SPI Flash Instruction Op-Code and Access Profile Compatibility Requirements

SPI FLASH COMMAND	FIRST BYTE (OP-CODE)	SECOND BYTE	THIRD BYTE	FOURTH BYTE	FIFTH BYTE	SIXTH BYTE	NO. OF DUMMY CLOCKS	COMMENTS
Fast READ (1/1)	0x0B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0) (1)	8	See Table 8
Dual READ (1/2)	0x3B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0) (1)	8	See Table 8
2X READ (2/2)	0xBB	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0) (1)	4	See Table 8
Quad READ (1/4)	0x6B	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0) (1)	8	See Table 8
4X READ (4/4)	0xEB	ADDRS(0)	ADDRS(1)	ADDRS(2)	dummy	DATA(0) (1)	6	See Table 8
Read status	0x05	n/a	n/a	STATUS(0)	STATUS(1)		0	Status(1) - Winbond only
Write status	0x01	STATUS(0)	STATUS(1)				0	Status(1) - Winbond only
Read Volatile Conf Reg	0x85	Data(0)					0	Micron Only
Write Volatile Conf Reg	0x81	Data(0)					0	Micron Only
Write Enable	0x06						0	
Write Disable	0x04						0	
Page program	0x02	ADDRS(0)	ADDRS(1)	ADDRS(2)	DATA(0) (1)		0	
Sector/Sub-sector Erase (4KB)	0x20	ADDRS(0)	ADDRS(1)	ADDRS(2)			0	
Full Chip Erase	0xC7						0	
Software Reset Enable	0x66							
Software Reset	0x99							
Read Id	0x9F	Data(0)	Data(1)	Data(2)				System will only read 1st three bytes

(1) Only the first data byte is shown, data continues.

More detailed information on the various read operations supported are shown in Table 8.

Table 8. SPI Flash Supported Read Operation Details

READ TYPE (1)	NUMBER OF LINES FOR OP-CODE (2)	NUMBER OF LINES FOR ADDRESS	NUMBER OF LINES FOR DUMMY BYTES	NUMBER OF LINES FOR RETURN DATA
Fast Read (1/1)	1	1	1	1
Dual Read (1/2)	1	1	1	2
2X Read (2/2)	1	2	2	2
Quad Read (1/4)	1	1	1	4
4X Read (4/4)	1	4	4	4

(1) Flash vendors have diverged in naming and controlling their various read capabilities. As such, the Host needs to be very careful to fully understand what is and what is not supported by the DLPC230-Q1. In general, for the supported devices, the DLPC230-Q1 only supports "Extended SPI" or "SPI Mode" (as defined in the various Flash Data Sheets). It does not support "Dual SPI Mode", "Quad SPI Mode", "QPI", "QPI Mode", "Dual QPI", "Quad QPI", "DTR", or "DDR". If uncertain, most devices will support "Fast Reads" in a manner that is consistent with the DLPC230-Q1.

(2) System does not support Read op-codes being spread across more than one data line.

Table 9. DLPC230-Q1 Compatible SPI Flash Device Options[1][2]

DENSITY (M-BITS)	VENDOR	PART NUMBER	PACKAGE SIZE
3.3-V Compatible Devices			
128	Micron[3]	MT25QL128ABA8ESF-OAAT	SO16
128	Macronix	MX25L12835FMR-10G	SO16
128	Macronix	MX25L12845GMR-10G	SO16
128	Macronix	MX25L12839FXDQ-10G	BGA25

(1) For any devices not listed on this table, special care should be taken to insure that the requirements shown in Table 6 and Table 7 are met.

(2) The boot application writes to the flash device status register once per 256 bytes during programming. Most flash devices discard status register writes when the status content does not change. Some flash parts, such as Micron N25Q128A13ESFA0F, do not block status writes when the status data is repeated. This causes the status register to exceed its maximum write limit after several programming cycles, making them incompatible with the DLPC230-Q1. Note that the main application does not write to the status register.

(3) Care should be used when considering Numonyx versions of Micron serial flash devices as they typically do not have the 4KB sector size needed to be DLPC230-Q1 compatible.

While the DLPC230-Q1 supports a variety of clock rates and read operation types, it does have a minimum flash read bandwidth requirement which is shown in Table 10. This minimum read bandwidth can be met in any number of different ways, with the variables being clock rate and read type. The Host is required to select a flash device which can meet this minimum read bandwidth using the DLPC230-Q1 supported interface capabilities. It should be noted that the Host will specify to the system (via flash parameter) the maximum supported clock rate as well as the supported read types for their selected flash device, with which the DLPC230-Q1 SW will automatically select an appropriate combination to maximize this bandwidth (which should at least meet the minimum bandwidth requirement assuming a solution exists per the specified parameters).

Table 10. SPI Flash Interface Bandwidth Requirements

PARAMETER		MIN	MAX	UNIT
$FLSH\_RD_{BW}$	Flash Read Interface Bandwidth	47.00		Mbps

8.3.5 Serial Flash Programming

The serial flash can be programmed through the DLPC230-Q1 using Host commands through the SPI or I^2C command and control interface.

8.3.6 Host Command and Diagnostic Processor Interfaces

The DLPC230-Q1 provides an interface port for Host commands as well as an interface port for a *diagnostic processor*. There are two external communication ports dedicated for this use, one SPI interface and one I^2C interface. The host is allowed to specify (via ASIC input pin) which port will be used for which purpose (for example, Host Command Interface → SPI, therefore "diagnostic processor"→ I^2C - or they can be reversed).

The timing requirements for the SPI interface are shown in *Host/Diagnostic Port SPI Interface Timing Requirements*. The timing requirements for the I^2C interface are shown in *Host/Diagnostic Port I^2C Interface Timing Requirements*. The I^2C slave address pair is 36h/37h.

8.3.7 GPIO Supported Functionality

The DLPC230-Q1 provides 32 general purpose I/O that are available to support a variety of functions for a number of different product configurations. In general, most of these I/O will only support one specific function based on a specific product configuration, although that function may be different for a different product configuration. There are also a few of these I/O that have been reserved for use by the Host for whatever function they might require. In addition, most of these I/O can also be made available for TI test and debug use. Definitions for the HUD and Headlight product configurations are shown in Table 11 and Table 12.

Table 11. GPIO Supported Functionality - HUD Product Configuration

GPIO	SIGNAL NAME	DESCRIPTION [1]
GPIO_00	PMIC_CNTRL_OUT (input)	LED control feedback from the TPS99000-Q1. An external pull-down resistor should be used (connects to TPS99000-Q1 Drive Enable).
GPIO_01	PMIC_SEQ_STRT (output)	Sequence start output from the DLPC230-Q1. This should be connected to the TPS99000-Q1 to time LED related actions and shadow TPS99000-Q1 configuration registers. An external pull-down resistor should be used.
GPIO_02	PMIC_COMP_OUT (input)	LED optical comparison feedback. This is used to count light pulses during each frame. This signal is active-low. An external pull-down resistor should be used.
GPIO_03	PMIC_LED_SEN (output)	LED Shunt Enable - shunts current from LEDs to allow faster LED turn-off. An external pull-down resistor should be used.
GPIO_04	PMIC_LED_DEN (output)	LED FET Drive Enable - enables LED current switching and defines LED pulse length. An external pull-down resistor should be used.
GPIO_05	Reserved for Future Use	An external pull-down resistor should be used
GPIO_06	Host Available	Available for general host use via Host Commands
GPIO_07	Host Available	Available for general host use via Host Commands
GPIO_08	Host Available	Available for general host use via Host Commands
GPIO_09	Reserved for Future Use	An external pull-down resistor should be used
GPIO_10	Reserved for Future Use	An external pull-down resistor should be used
GPIO_11	Reserved for Future Use	An external pull-down resistor should be used
GPIO_12	Reserved for Future Use	An external pull-down resistor should be used
GPIO_13	Reserved for Future Use	An external pull-down resistor should be used
GPIO_14	Reserved for Future Use	An external pull-down resistor should be used
GPIO_15	PMIC_WD1 (output)	Periodic signal that the DLPC230-Q1 processor generates during normal operation. TPS99000-Q1 monitors this signal and reports if this signal stops pulsing. An external pull-down resistor should be used.
GPIO_16	Reserved for Future Use	An external pull-down resistor should be used
GPIO_17	Host Available	Available for general host use via Host Commands
GPIO_18	Reserved for Future Use	An external pull-down resistor should be used
GPIO_19	Reserved for Future Use	An external pull-down resistor should be used
GPIO_20	Reserved for Future Use	An external pull-down resistor should be used
GPIO_21	Reserved for Future Use	An external pull-down resistor should be used
GPIO_22	Reserved for Future Use	An external pull-down resistor should be used
GPIO_23	Reserved for Future Use	An external pull-down resistor should be used
GPIO_24	Reserved for Future Use	An external pull-down resistor should be used
GPIO_25	Reserved for Future Use	An external pull-down resistor should be used
GPIO_26	Host Available	Available for general host use via Host Commands
GPIO_27	Host Available	Available for general host use via Host Commands
GPIO_28	Host Available	Available for general host use via Host Commands
GPIO_29	Host Available	Available for general host use via Host Commands
GPIO_30	Host Available	Available for general host use via Host Commands
GPIO_31	Host Available	Available for general host use via Host Commands

(1) It is recommended that all unused Host Available GPIO be configured as a logic '0' output and be left unconnected in the system. If this is not done, an external pull-down resistor (≤ 10 kΩ) should be used to avoid floating inputs.

Table 12. GPIO Supported Functionality - Headlight Product Configuration

GPIO	SIGNAL NAME	DESCRIPTION (1)
GPIO_00	HL_PWM0 (output)	PWM 0 Output - This can be used for general purposes such as controlling the level of an external light source.
GPIO_01	PMIC_SEQ_STRT (output)	Sequence start output from the DLPC230-Q1. This should be connected to the TPS99000-Q1 to time LED related actions and shadow TPS99000-Q1 configuration registers. An external pull-down resistor should be used.
GPIO_02	HL_PWM1(output)	PWM 1 Output - This can be used for general purposes such as controlling the level of an external light source.
GPIO_03	Reserved for Future Use	An external pull-down resistor should be used
GPIO_04	Reserved for Future Use	An external pull-down resistor should be used
GPIO_05	Reserved for Future Use	An external pull-down resistor should be used
GPIO_06	Host Available	Available for general host use via Host Commands
GPIO_07	Host Available	Available for general host use via Host Commands
GPIO_08	Host Available	Available for general host use via Host Commands
GPIO_09	Reserved for Future Use	An external pull-down resistor should be used
GPIO_10	Reserved for Future Use	An external pull-down resistor should be used
GPIO_11	Reserved for Future Use	An external pull-down resistor should be used
GPIO_12	Reserved for Future Use	An external pull-down resistor should be used
GPIO_13	Reserved for Future Use	An external pull-down resistor should be used
GPIO_14	Reserved for Future Use	An external pull-down resistor should be used
GPIO_15	PMIC_WD1 (output)	Periodic signal that the DLPC230-Q1 processor generates during normal operation. TPS99000-Q1 monitors this signal and reports if this signal stops pulsing. An external pull-down resistor should be used.
GPIO_16	Reserved for Future Use	An external pull-down resistor should be used
GPIO_17	HL_PWM2 (output)	PWM 2 Output - This can be used for general purposes such as controlling the level of an external light source.
GPIO_18	EXT_SMPL	Connects to TPS99000-Q1 EXT_SMPL input. This sequence-aligned signal can be configured to trigger TPS99000-Q1 ADC sampling.
GPIO_19	Reserved for Future Use	An external pull-down resistor should be used
GPIO_20	Reserved for Future Use	An external pull-down resistor should be used
GPIO_21	Reserved for Future Use	An external pull-down resistor should be used
GPIO_22	Reserved for Future Use	An external pull-down resistor should be used
GPIO_23	Reserved for Future Use	An external pull-down resistor should be used
GPIO_24	Reserved for Future Use	An external pull-down resistor should be used
GPIO_25	Reserved for Future Use	An external pull-down resistor should be used
GPIO_26	Host Available	Available for general host use via Host Commands
GPIO_27	Host Available	Available for general host use via Host Commands
GPIO_28	Host Available	Available for general host use via Host Commands
GPIO_29	Host Available	Available for general host use via Host Commands
GPIO_30	Host Available	Available for general host use via Host Commands
GPIO_31	Host Available	Available for general host use via Host Commands

(1) It is recommended that all unused Host Available GPIO be configured as a logic '0' output and be left unconnected in the system. If this is not done, an external pull-down resistor (≤ 10 kΩ) should be used to avoid floating inputs.

8.3.8 Built-In Self Test (BIST)

The DLPC230-Q1 provides a significant amount of BIST support to help ensure the operational integrity of the system. This BIST support is divided into two general BIST types, which are Non-Periodic and Periodic.

Non-Periodic BISTs are tests that are typically run one time, and are run outside of normal operation since their activity will disturb the operation of the system. These tests are specified to be run either by a Flash parameter or by a Host command. The Flash parameter specifies which tests are to be run during system power-up and initialization. The Host command is used to select and specify the running of these tests when the system is in Standby Mode (often just before the system is powered down). Some examples of non-periodic tests are: tests for all of the ASIC memories, tests for the main data processing path, and testing of the DMD memory.

Periodic BISTs are tests that are run on an almost continual basis during normal ASIC operation. These tests are managed (set up, enabled, results gathered and evaluated) automatically by the ASIC embedded software. Some examples of periodic tests are: tuning and verification of the DMD High-Speed Interface, input source monitoring (clock, active pixels, active lines), and external video checksum monitoring.

For more information on BISTs, refer to *DLPC230-Q1 Programmer's Guide (DLPU041 for HUD and DLPU048 for Headlight)*.

8.3.9 EEPROMs

The DLPC230-Q1 may optionally use an external I^{2}C EEPROM memory device for storage of calibration data as an alternative to storing calibration data in the SPI flash memory. The EEPROM must be connected to the designated DLPC230-Q1 master I^{2}C interface (MSTR_XXX).

The DLPC230-Q1 supports the EEPROM devices listed in Table 13.

Table 13. DLPC230-Q1 Supported EEPROMs

MANUFACTURER	PART NUMBER	DENSITY (Kb)	PACKAGE SIZE
STMicro	M24C64A125	64	S08
STMicro	M24C128A125	128	S08
Atmel	A24C64D	64	S08
Atmel	A24C128C	128	S08

8.3.10 Temperature Sensor

The DLPC230-Q1 requires an external temperature sensor (TMP411) to measure the DMD temperature through a remote temperature sense diode residing within the DMD. The DLPC230-Q1 will also read the local temperature reported by the TMP411 device. The TMP411 must be connected to the designated DLPC230-Q1 master I^{2}C interface (MSTR_XXX).

The DLPC230-Q1 uses an averaged DMD temperature reading to manage the thermal environment and/or operation of the DMD. This management occurs over the full range of temperatures supported by the DMD. This temperature reading is used change sequence operation across the temperature range, and park the DMD when it is operated outside of its allowable temperature specification.

8.3.11 Debug Support

The DLPC230-Q1 contains a test point output port, TSTPT_(7:0), which provides the Host with the ability to specify a number of initial system configurations, as well as to provide for ASIC debug support. These test points are tri-stated while reset is applied, are sampled as inputs approximately 1.5 µs after reset is released, and then switch to outputs once the input values have been sampled. The sampled and captured input state for each of these signals is used to configure initial system configurations as specified in the table Pin Functions - Parallel Port Input Data and Control in *Pin Configuration and Functions*.

There are three other signals (JTAGTDO(3:1)) that are sampled as inputs approximately 1.5 µs after reset is released, and then switched to outputs. The sampled and captured state for each of these JTAGTDO signals is used to configure the initial test mode output state of the TSTPT_(7:0) signals. Table 14 defines the test mode selection for a few programmable output states for TSTPT_(7:0) as defined by JTAGTDO(3:1). For normal use (that is, no debug required), the default state of x111 (using weak internal pull-ups) should be used to allow for the normal use of these JTAG TDO signals.

To allow TI to make use of this debug capability, a jumper to an external pull-down is recommended for JTAGTDO(3:1).

Table 14. Test Mode Selection Scenario Defined by JTAGTDO(3:1)(1)

TSTPT_(7:0) OUTPUT	JTAGTDO(3:1) CAPTURED VALUE	
	x111 (DEFAULT) (NO SWITCHING ACTIVITY)	x010 CLOCK DEBUG OUTPUT
TSTPT(0)	HI-Z	60 MHz
TSTPT(1)	HI-Z	30 MHz
TSTPT(2)	HI-Z	7.5 MHz
TSTPT(3)	HI-Z	LOW
TSTPT(4)	HI-Z	15 MHz
TSTPT(5)	HI-Z	60 MHz
TSTPT(6)	HI-Z	LOW
TSTPT(7)	HI-Z	LOW

(1) These are only the default output selections. Software can reprogram the selection at any time.

8.4 Device Functional Modes

The DLPC230-Q1 has three operational modes which are enabled via software command via the Host control interface. These modes are Standby, Display, and Calibration.

8.4.1 Standby Mode

The system will automatically enter Standby mode after power is applied. This is a reduced functional mode that allows Flash update operations and Non-Periodic test operations. The DMD will be parked while the system is operating in this mode and no source may be displayed.

8.4.2 Display Mode

This is the main operational mode of the system. In this mode, normal display activities occur. In this mode the system may display video data and execute periodic BISTs. After system initialization, a host command can be used to transition to this mode from Standby mode. Alternatively, a flash configuration setting can be set to allow the system to automatically transition from standby to display mode after system initialization.

8.4.3 Calibration Mode

This mode is used to calibrate the system's light sources for the desired display properties. For head-up display applications, this includes the ability to adjust individual color light sources to achieve the desired brightness and color point.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DLPC230-Q1 is designed to support projection-based automotive applications such as head-up display (HUD) and high resolution headlight.

This DLP® Products chipset consists of three components—the DLP553X-Q1 Digital Micromirror Device (DMD), the DLPC230-Q1, and the TPS99000-Q1. The DMD is a light modulator consisting of tiny mirrors that are used to form and project images. The DLPC230-Q1 is a controller for the DMD; it formats incoming video sources and controls the timing of the DMD illumination sources and the DMD in order to display the incoming video source. The TPS99000-Q1 is a controller for the illumination sources (LEDs or lasers) and a management IC for the entire chipset. In conjunction, the DLPC230-Q1 and the TPS99000-Q1 can also be used for system-level monitoring, diagnostics, and failure detection features.

9.2 Typical Application

9.2.1 Head-Up Display

Figure 20 shows the system block diagram for a DLP® technology HUD.

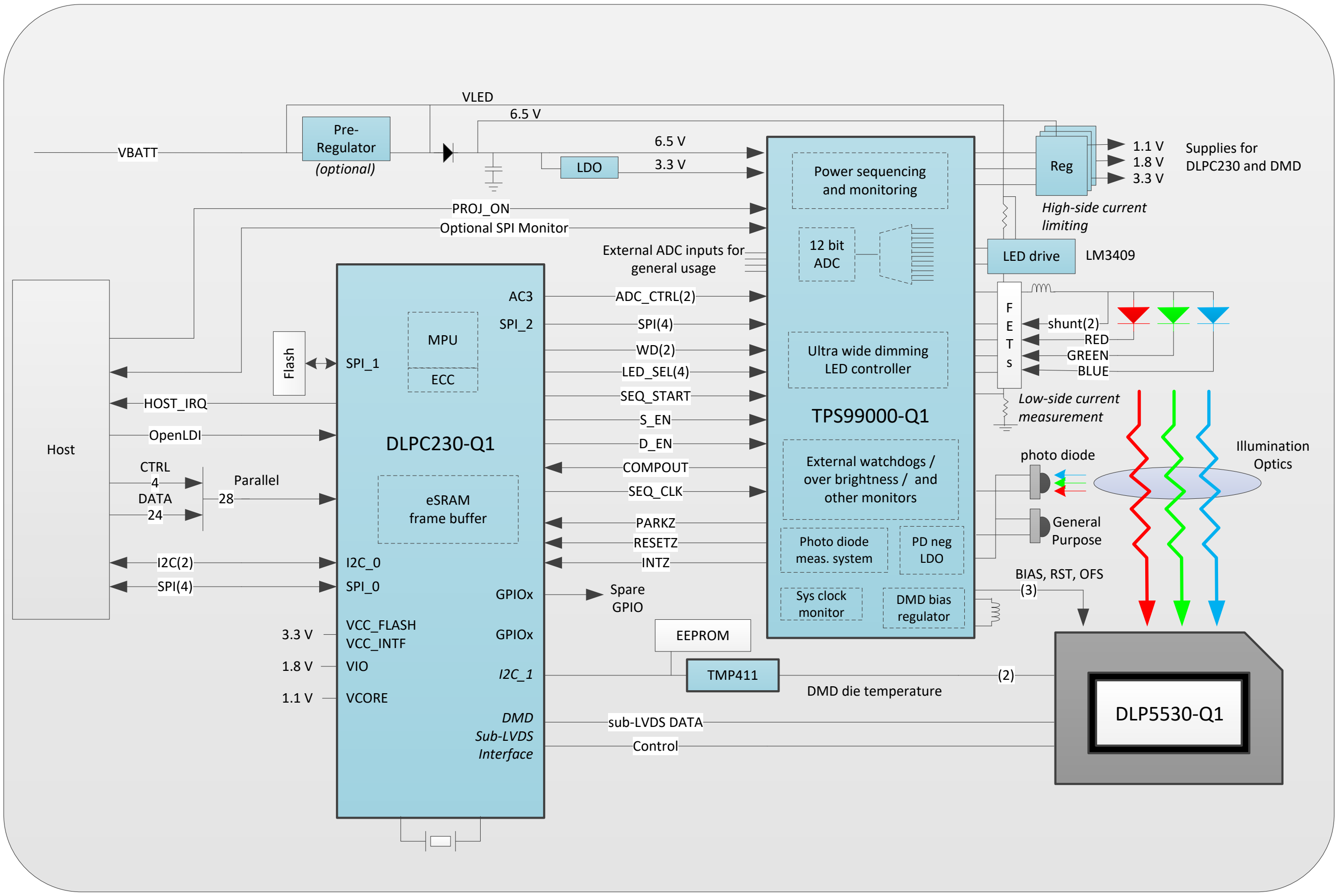

VLED
6.5 V
VBATT
Pre-Regulator
(optional)
6.5 V
LDO
3.3 V
Power sequencing and monitoring
Reg
1.1 V
1.8 V
3.3 V
Supplies for DLPC230 and DMD
High-side current limiting
PROJ_ON
Optional SPI Monitor
12 bit ADC
LED drive
LM3409
External ADC inputs for general usage
Host
Flash
SPI_1
MPU
ECC
AC3
SPI_2
ADC_CTRL(2)
SPI(4)
WD(2)
LED_SEL(4)
SEQ_START
S_EN
D_EN
COMPOUT
SEQ_CLK
PARKZ
RESETZ
INTZ
FETs
shunt(2)
RED
GREEN
BLUE
Ultra wide dimming LED controller
TPS99000-Q1
Low-side current measurement
HOST_IRQ
OpenLDI
DLPC230-Q1
CTRL
4
DATA
24
Parallel
28
eSRAM frame buffer
External watchdogs / over brightness / and other monitors
photo diode
Illumination Optics
General Purpose
Photo diode meas. system
PD neg LDO
I2C(2)
SPI(4)
I2C_0
SPI_0
GPIOx
Spare GPIO
Sys clock monitor
DMD bias regulator
BIAS, RST, OFS
(3)
3.3 V
VCC_FLASH
VCC_INTF
GPIOx
EEPROM
1.8 V
VIO
I2C_1
TMP411
(2)
DMD die temperature
1.1 V
VCORE
DMD Sub-LVDS Interface
sub-LVDS DATA
Control
DLP5530-Q1

Figure 20. HUD System Block Diagram

9.2.1.1 Design Requirements

The DLPC230-Q1 is a controller for the DMD and the timing of the RGB LEDs in the HUD. It requests the proper timing and amplitude from the LEDs to achieve the requested color and brightness from the HUD across the entire operating range. It synchronizes the DMD with these LEDs in order to display full-color video content sent by the host.

The DLPC230-Q1 receives command and input video data from a host processor in the vehicle. Read and write (R/W) commands can be sent using either the I^2C bus or SPI bus. The bus that is not being used for R/W commands can be used as a read-only bus for diagnostic purposes. Input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The SPI flash memory provides the embedded software for the DLPC230-Q1's embedded processor, color calibration data, and default settings. The TPS99000-Q1 provides diagnostic and monitoring information to the DLPC230-Q1 using a SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The DLPC230-Q1 interfaces to a TMP411 via I^2C for temperature information.

Typical Application (continued)

The outputs of the DLPC230-Q1 are LED drive information to the TPS99000-Q1, control signals to the DMD, and monitoring and diagnostics information to the host processor. Based on a host requested brightness and the operating temperature, the DLPC230-Q1 determines the proper timing and amplitudes for the LEDs. It passes this information to the TPS99000-Q1 using a SPI bus and several additional control signals such as D_EN, S_EN, and SEQ_STRT. It controls the DMD mirrors by sending data over a sub-LVDS bus. It can alert the host about any critical errors using a HOST_IRQ signal.

The TPS99000-Q1 is a highly-integrated mixed-signal IC that controls DMD power, the analog response of the LEDs, and provides monitoring and diagnostics information for the HUD system. The power sequencing and monitoring blocks of the TPS99000-Q1 properly power up the DMD, provide accurate DMD voltage rails, as well as monitor the system’s power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The highly accurate photodiode (PD) measurement system and the dimming controller block precisely control the LED response. This enables a DLP technology HUD to achieve a very high dimming range (> 5000:1) with accurate brightness and color across the temperature range of the system. Finally, the TPS99000-Q1 has several general-purpose ADCs that developers can use for system-level monitoring, such as over-brightness detection.

The TPS99000-Q1 receives inputs from the DLPC230-Q1, power rail voltages for monitoring, a photodiode that is used to measure LED response, the host processor, and potentially several other ADC ports. The DLPC230-Q1 sends commands to the TPS99000-Q1 over a SPI port and several other control signals. The TPS99000-Q1 includes watchdogs to monitor the DLPC230-Q1 and ensure that it is operating as expected. The power rails are monitored by the TPS99000-Q1 to detect power failures or glitches and request a proper power down of the DMD in case of an error. The photodiode’s current is measured and amplified using a transimpedance amplifier (TIA) within the TPS99000-Q1. The host processor can read diagnostics information from the TPS99000-Q1 using a dedicated SPI bus, adding an independent monitoring path from the host processor. Additionally the host can request the system to be turned on or off using a PROJ_ON signal. The TPS99000-Q1 has several general-purpose ADCs that can be used to implement other system features such as over-brightness and over-temperature detection.

The outputs of the TPS99000-Q1 are LED drive signals, diagnostic information, and error alerts to the DLPC230-Q1. The TPS99000-Q1 has signals connected to the LM3409 buck controller for high power LEDs and to discrete hardware that control the LEDs. The TPS99000-Q1 can output diagnostic information to the host and the DLPC230-Q1 over two SPI busses. It also has signals such as RESETZ, PARKZ, and INTZ that can be used to trigger power down or reset sequences.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as an input (video data) and produces a mechanical output (mirror position). The electrical interface to the DMD is a sub-LVDS interface driven with the DLPC230-Q1. The mechanical output is the state of more than 1.3 million mirrors in the DMD array that can be tilted ±12°. In a projection system, the mirrors are used as pixels in order to display an image.

Typical Application (continued)

9.2.2 Headlight

Figure 21 shows the system block diagram for a DLP® headlight.

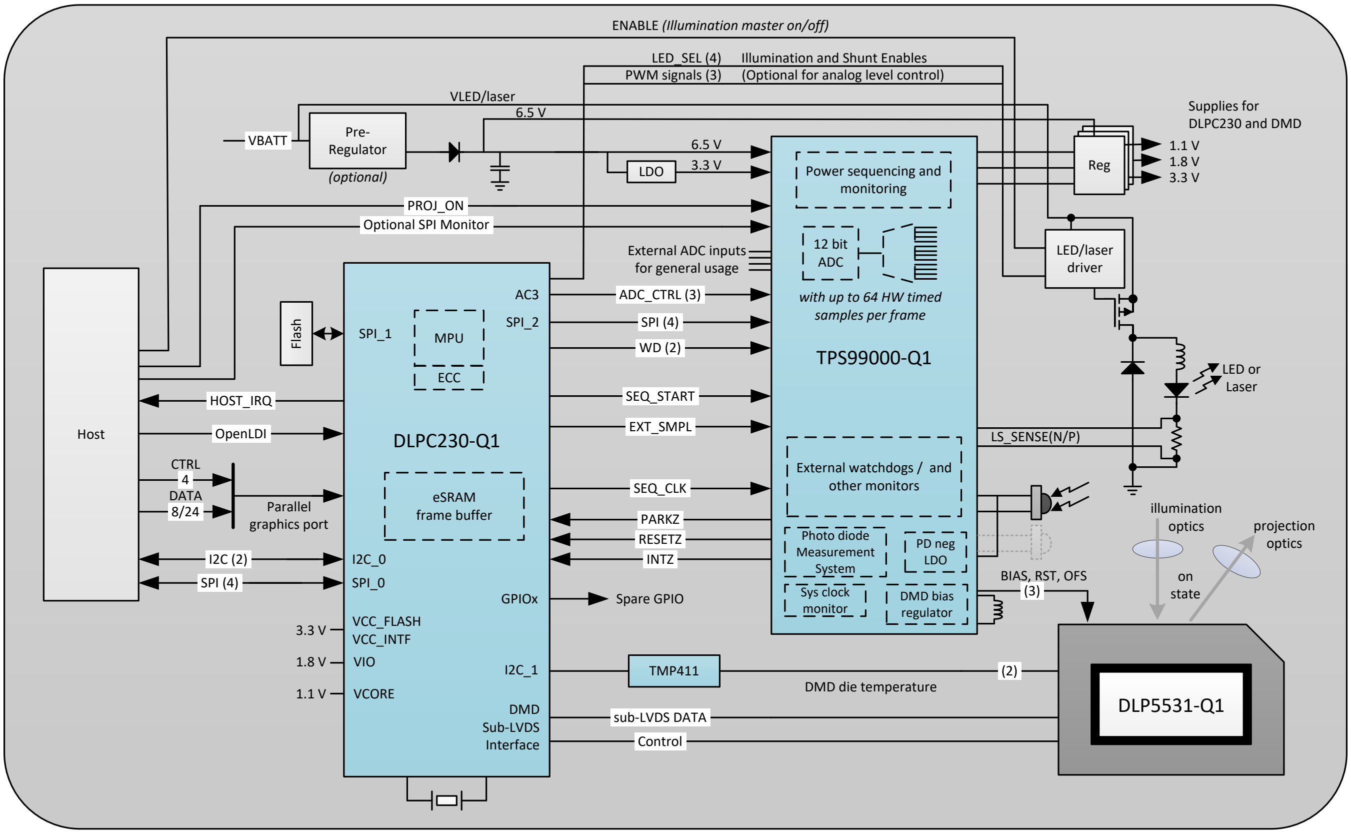

ENABLE (Illumination master on/off)
LED_SEL (4)
PWM signals (3)
Illumination and Shunt Enables
(Optional for analog level control)
VLED/laser
6.5 V
VBATT
Pre-Regulator
(optional)
6.5 V
3.3 V
LDO
Supplies for DLPC230 and DMD
Reg
1.1 V
1.8 V
3.3 V
PROJ_ON
Optional SPI Monitor
Power sequencing and monitoring
External ADC inputs for general usage
12 bit ADC
with up to 64 HW timed samples per frame
LED/laser driver
TPS99000-Q1
Host
Flash
SPI_1
MPU
ECC
AC3
SPI_2
ADC_CTRL (3)
SPI (4)
WD (2)
LED or Laser
HOST_IRQ
OpenLDI
DLPC230-Q1
SEQ_START
EXT_SMPL
LS_SENSE(N/P)
CTRL
4
DATA
8/24
Parallel graphics port
eSRAM frame buffer
SEQ_CLK
External watchdogs / and other monitors
PARKZ
RESETZ
INTZ
illumination optics
projection optics
I2C (2)
SPI (4)
I2C_0
SPI_0
Photo diode Measurement System
PD neg LDO
GPIOx
Spare GPIO
Sys clock monitor
DMD bias regulator
BIAS, RST, OFS
(3)
on state
3.3 V
VCC_FLASH
VCC_INTF
1.8 V
VIO
1.1 V
VCORE
I2C_1
TMP411
(2)
DMD die temperature
DLP5531-Q1
DMD Sub-LVDS Interface
sub-LVDS DATA
Control

Figure 21. Headlight System Block Diagram

9.2.2.1 Design Requirements

The DLPC230-Q1 is a controller for the DMD and the light sources in the DLP technology headlight. It receives input video from the host and synchronizes DMD and light source timing in order to achieve the desired video output. The DLPC230-Q1 formats input video data that is displayed on the DMD. It synchronizes these video segments with light source timing in order to create video with grayscale shading.

The DLPC230-Q1 receives command and input video data from a host processor in the vehicle. R/W commands can be sent using either the I^{2}C bus or SPI bus. The bus that is not being used for R/W commands can be used as a read-only bus for diagnostic purposes. Input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The 24-bit bus can be limited to only 8-bits of data for single light source systems such as headlights. The SPI flash memory provides the embedded software for the DLPC230-Q1's embedded processor and default settings. The TPS99000-Q1 provides diagnostic and monitoring information to the DLPC230-Q1 using a SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The TMP411 uses an I^{2}C interface to provide the DMD array temperature to the DLPC230-Q1.

The outputs of the DLPC230-Q1 are configuration and monitoring commands to the TPS99000-Q1, timing controls to the LED or laser driver, control signals to the DMD, and monitoring and diagnostics information to the host processor. The DLPC230-Q1 communicates with the TPS99000-Q1 over a SPI bus. It uses this to configure the TPS99000-Q1 and to read monitoring and diagnostics information from the TPS99000-Q1. The DLPC230-Q1 sends drive enable signals to the LED or laser driver, and synchronizes this with the DMD mirror timing. The control signals to the DMD are sent using a sub-LVDS interface.

Typical Application (continued)

The TPS99000-Q1 is a highly integrated mixed-signal IC that controls DMD power, the timing of the LEDs or lasers, and provides monitoring and diagnostics information for the DLP technology headlight system. The power sequencing and monitoring blocks of the TPS99000-Q1 properly power up the DMD and provide accurate DMD voltage rails, and then monitor the system's power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The TPS99000-Q1 also has several output signals that can be used to control a variety of LED or laser driver topologies. The TPS99000-Q1 also has several general-purpose ADCs that designers can use for system level monitoring.

The TPS99000-Q1 receives inputs from the DLPC230-Q1, the power rails it monitors, the host processor, and potentially several other ADC ports. The DLPC230-Q1 sends configuration and control commands to the TPS99000-Q1 over a SPI bus and several other control signals. The TPS99000-Q1 includes watchdogs to monitor the DLPC230-Q1 and ensure that it is operating as expected. The power rails are monitored by the TPS99000-Q1 in order to detect power failures or glitches and request a proper power down of the DMD in case of an error. The host processor can read diagnostics information from the TPS99000-Q1 using a dedicated SPI bus. Additionally the host can request the image to be turned on or off using a PROJ_ON signal. Lastly, the TPS99000-Q1 has several general-purpose ADCs that can be used to implement system level monitoring functions.

The outputs of the TPS99000-Q1 are diagnostic information and error alerts to the DLPC230-Q1, and control signals to the LED or laser driver. The TPS99000-Q1 can output diagnostic information to the host and the DLPC230-Q1 over two SPI busses. In case of critical system errors, such as power loss, it outputs signals to the DLPC230-Q1 that trigger power down or reset sequences. It also has output signals that can be used to implement various LED or laser driver topologies.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as an input (video data), and produces a mechanical output (mirror position). The electrical interface to the DMD is a sub-LVDS interface with the DLPC230-Q1. The mechanical output is the state of more than 1.3 million mirrors in the DMD array that can be tilted ±12°. In a projection system the mirrors are used as pixels in order to display an image.

9.2.2.2 Headlight Video Input

The DLPC230-Q1 accepts 8-bit grayscale video data when used in headlight applications.

When using the parallel video port, PDATA_[16-23] are utilized (red input when using a typical RGB888 mapping). PDATA_[0-15] should be tied to ground.

When using the OpenLDI video ports, data bits R0 - R7 are utilized. B0-B7 and G0-G7 are unused.

10 Power Supply Recommendations

10.1 Power Supply Management

The TPS99000-Q1 manages power for the DLPC230-Q1 and DMD. See *Power Supply and Reset Timing Requirements* for all power sequencing and timing requirements.

10.2 Hot Plug Usage

The DLPC230-Q1 does not support Hot Plug use (for itself or for any DMD connected to the system). As such, the system should always be powered down prior to removal of the ASIC or DMD from any system.

10.3 Power Supply Filtering

The following filtering circuits are recommended for the various supply inputs. High frequency 0.1-µF capacitors should be evenly distributed amongst the power balls and placed as close to the power balls as possible.

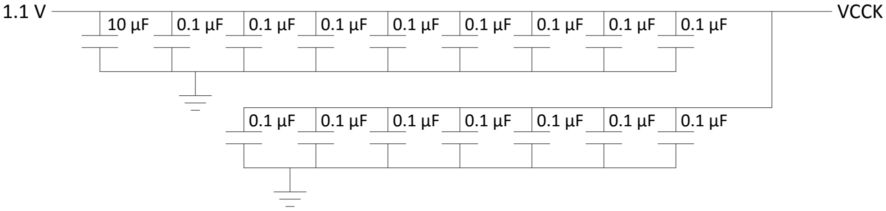

1.1 V
10 µF
0.1 µF
VCCK

Figure 22. VCCK Recommended Filter

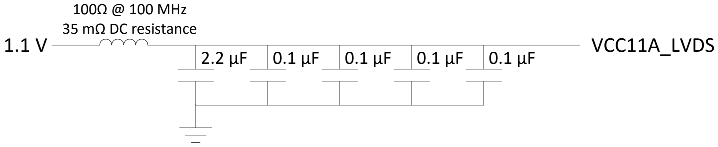

100Ω @ 100 MHz
35 mΩ DC resistance
1.1 V
2.2 µF
0.1 µF
VCC11A_LVDS

Figure 23. VCC11A_LVDS Recommended Filter

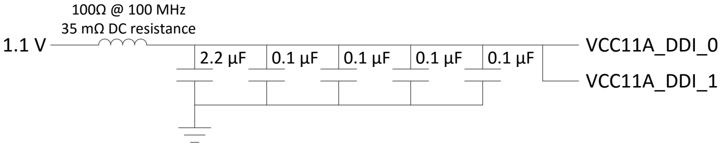

100Ω @ 100 MHz
35 mΩ DC resistance
1.1 V
2.2 µF
0.1 µF
VCC11A_DDI_0
VCC11A_DDI_1

Figure 24. VCC11A_DDI Recommended Filter

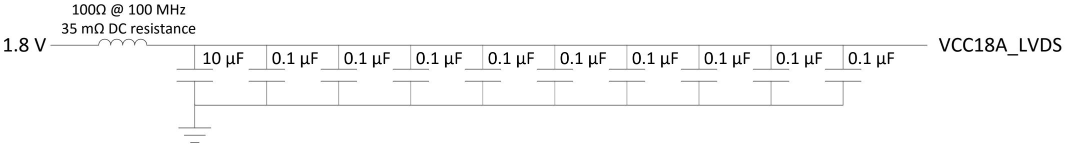

100Ω @ 100 MHz
35 mΩ DC resistance
1.8 V
10 µF
0.1 µF
VCC18A_LVDS

Figure 25. VCC18A_LVDS Recommended Filter

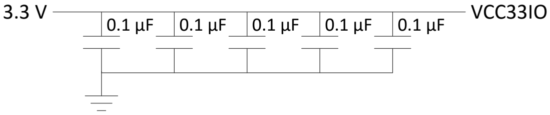

3.3 V
0.1 µF
VCC33IO

Figure 26. VCC33IO Recommended Filter

Power Supply Filtering (continued)

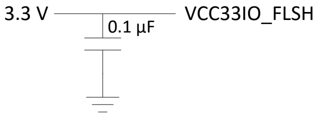


Figure 27. VCC33IO_FLSH Recommended Filter

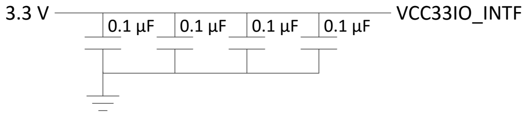


Figure 28. VCC33IO_INTF Recommended Filter

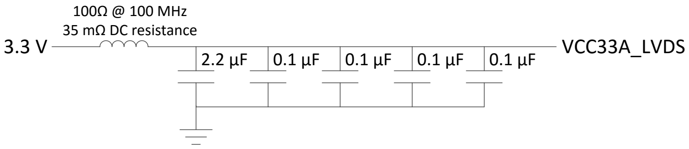


Figure 29. VCC33A_LVDS Recommended Filter

11 Layout

11.1 Layout Guidelines

11.1.1 PCB Layout Guidelines for Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. The DLPC230-Q1 contains two internal PLLs which have dedicated analog supplies (VCC11AD_PLLM, GND11AD_PLLM, VCC11AD_PLLD, GND11AD_PLLD). At a minimum, VCC11AD_PLLx power and GND11AD_PLLx ground pins should be isolated using a simple passive filter consisting of two series Ferrites and two shunt capacitors (to widen the spectrum of noise absorption). Recommended values and layout are shown in Table 15 and Figure 30 respectively.

Table 15. Recommended PLL Filter Components

COMPONENT	PARAMETER	RECOMMENDED VALUE	UNIT
Shunt Capacitor	Capacitance	0.1	µF
Shunt Capacitor	Capacitance	1.0	µF
Series Ferrite	Impedance at 100 MHz	> 100	Ω
	DC Resistance	< 0.40	

Since the PCB layout is critical to PLL performance, it is vital that the quiet ground and power are treated like analog signals. Additional design guidelines are as follows:

- All four components should be placed as close to the ASIC as possible
- It's especially important to keep the leads of the high frequency capacitors as short as possible
- A capacitor of each value should be connected across VCC11AD_PLLM / GND11AD_PLLM and VCC11AD_PLLD / GND11AD_PLLD respectively on the ASIC side of the Ferrites
- VCC11AD_PLLM and VCC11AD_PLLD must be a single trace from the DLPC230-Q1 to both capacitors and then through the series ferrites to the power source
- The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other

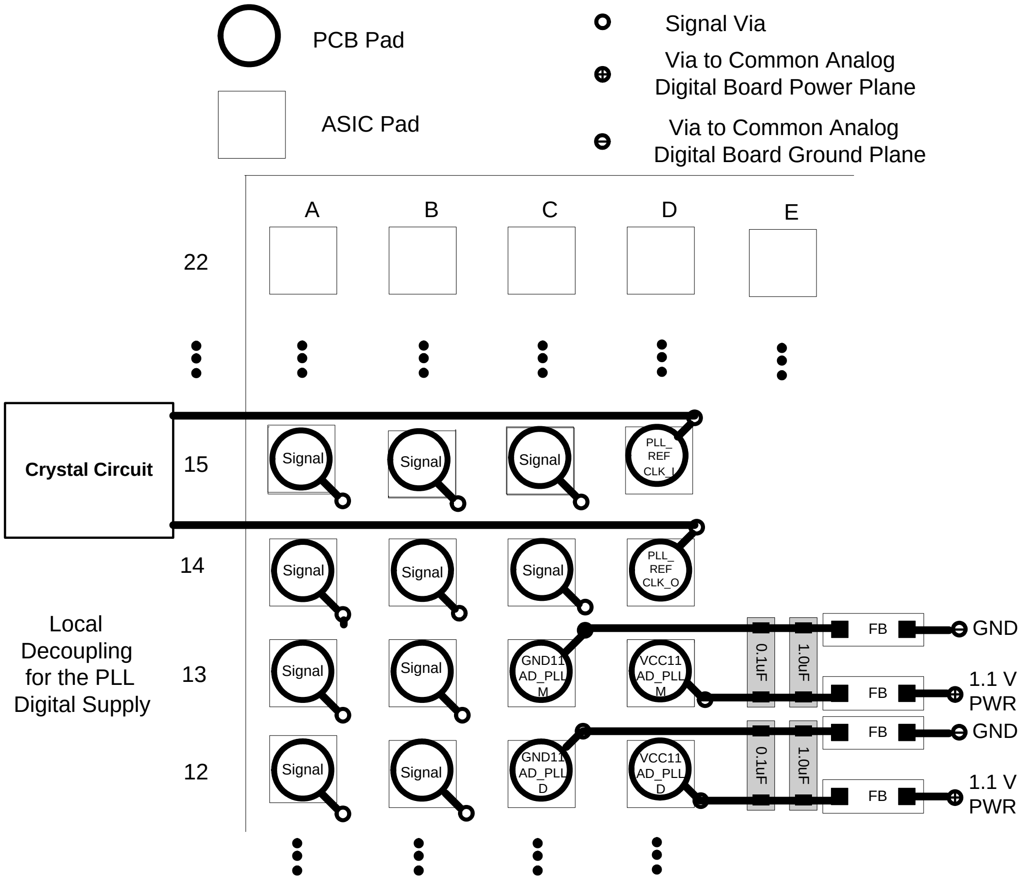
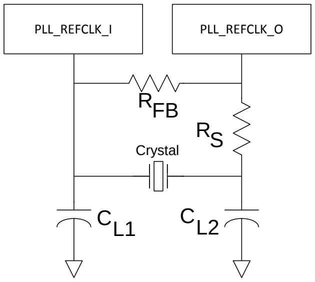

PCB Pad
ASIC Pad
Signal Via
Via to Common Analog Digital Board Power Plane
Via to Common Analog Digital Board Ground Plane
A
B
C
D
E
22
15
14
13
12
Crystal Circuit
Signal
PLL_ REF CLK_I
PLL_ REF CLK_O
GND11 AD_PLL M
VCC11 AD_PLL M
GND11 AD_PLL D
VCC11 AD_PLL D
Local Decoupling for the PLL Digital Supply
0.1uF
1.0uF
FB
GND
1.1 V PWR

Figure 30. PLL Filter Layout

11.1.2 DLPC230-Q1 Reference Clock

The DLPC230-Q1 requires an external reference clock to feed its internal PLL. A crystal or oscillator can supply this reference. The recommended crystal configurations and reference clock frequencies are listed in Table 16, with additional required discrete components shown in Figure 31 and defined in Table 16.



A. C_L = Crystal load capacitance

B. R_{FB} = Feedback Resistor

Figure 31. Discrete Components Required When Using Crystal

11.1.2.1 Recommended Crystal Oscillator Configuration

Table 16. Recommended Crystal Configuration

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	16	MHz
Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity)	±200	PPM
Maximum crystal equivalent series resistance (ESR)	50	Ω
Crystal load capacitance	10	pF
Temperature range	–40°C to +105°C	°C
Drive level (nominal)	100	µW
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor	See equation in (1)	pF
C_{L2} external crystal load capacitor	See equation in (2)	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) CL1 = 2 × (CL – Cstray_pll_refclk_i), where: Cstray_pll_refclk_i = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_i.

(2) CL2 = 2 × (CL – Cstray_pll_refclk_o), where: Cstray_pll_refclk_o = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_o.

The crystal circuit in the DLPC230-Q1 ASIC has dedicated power (VCC3IO_COSC) and ground (GNDIOLA_COSC) pins, with the recommended filtering shown in Figure 32.

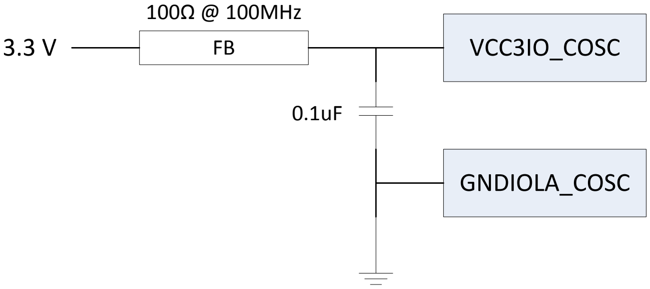


Figure 32. Crystal Power Supply Filtering

Table 17. DLPC230-Q1 Recommended Crystal Parts

MANUFACTURER	PART NUMBER	SPEED	FREQUENCY TOLERANCE, FREQUENCY STABILITY, AGING/YEAR	ESR	LOAD CAPACITANCE	OPERATING TEMPERATURE
TXC	AM16070006[1]	16 MHz	Freq Tolerance: ±10 ppm Freq Stability: ±50 ppm Aging/Year: ±3 ppm	50-Ω max	10 pF	–40°C to +125°C

[1] This device requires a 3-kΩ series resister to limit power.

If an external oscillator is used, the oscillator output must drive the PLL_REFCLK_O pin on the DLPC230-Q1 ASIC, the PLL_REFCLK_I pin should be left unconnected, and the OSC_BYPASS pin must = logic HIGH.

11.1.3 DMD Interface Layout Considerations

The DLPC230-Q1 ASIC sub-LVDS HS/LS differential interface waveform quality and timing is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

DLPC230-Q1 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB design recommendations are provided in Table 18 and Figure 33 as a starting point for the customer.

Table 18. PCB Recommendations for DMD Interface[1] [2]

PARAMETER		MIN	MAX	UNIT
T_W	Trace Width	4		mils
T_S	Intra-lane Trace Spacing	4		mils
T_{SPP}	Inter-lane Trace Spacing	$2 * (T_S + T_W)$		mils
R_{BGR}	Resistor - Bandgap Reference	42.2 (1%)		kΩ

[1] Recommendations to achieve the desired nominal differential impedance as specified by Tx_{load} in *DMD High-Speed Sub-LVDS Electrical Characteristics* and *DMD Low-Speed Sub-LVDS Electrical Characteristics*.

[2] If using the minimum trace width and spacing to escape the ASIC ball field, widening these out after escape would be desirable if practical to achieve the target 100-Ω impedance (e.g. to reduce transmission line losses).

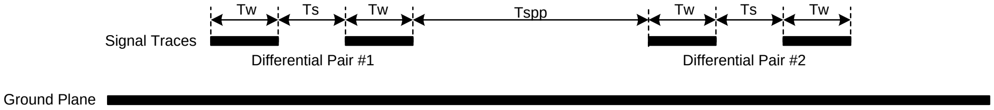


Figure 33. DMD Differential Layout Recommendations

11.1.4 General PCB Recommendations

TI recommends 1-oz copper power planes and 2-oz copper ground planes in the PCB design to achieve the required thermal connectivity, with:

- A minimum of 4 power and ground planes
- A copper plane beneath the thermal ball array containing a via farm with the following attributes
  - Copper plane area (top side of PCB, under package) = 8.0 mm × 8.0 mm
  - Copper plane area (bottom side of PCB, opposite of package) = 6.0 mm × 6.0 mm
  - Thermal via quantity = 7 × 7 array of vias
  - Thermal via size = 0.25 mm (10 mils)
  - Thermal via plating thickness = 0.05-mm (2-mils) wall thickness
- PCB copper coverage per layer
  - Power and Ground layers: 90% minimum coverage
  - Top/Bottom signal layers (ground fill to achieve coverage): 70% minimum coverage with 1.5-oz copper.

11.1.5 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused ASIC input pins be tied through a pull-up resistor to its associated power supply or a pull-down to ground unless specifically noted otherwise in *Pin Configuration and Functions*. For ASIC inputs with an internal pull-up or pull-down resistors, it is unnecessary to add an external pull-up or pull-down unless specifically recommended. Note that internal pull-up and pull-down resistors are weak and should not be expected to drive the external line. When external pull-up or pull-down resistors are needed for pins that have built-in weak pull-ups or pull-downs, use the value specified in Table 2.

Unused output-only pins should never be tied directly to power or ground, but can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or pulled-down) using an appropriate, dedicated resistor.

11.1.6 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 19. Max Pin-to-Pin PCB Interconnect Recommendations - DMD

ASIC INTERFACE	SIGNAL INTERCONNECT TOPOLOGY(1)(2)		UNIT
DMD	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS0_CLK_P DMD_HS0_CLK_N	6.0 (152.4)	See (3)	in (mm)
DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N	6.0 (152.4)	See (3)	in (mm)
DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N			
DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N			
DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N			
DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N			
DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N			
DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N			
DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N			
DMD_HS1_CLK_P DMD_HS1_CLK_N	6.0 (152.4)	See (3)	in (mm)
DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N	6.0 (152.4)	See (3)	in (mm)
DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N			
DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N			
DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N			
DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N			
DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N			
DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N			
DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N			
DMD_LS0_CLK_P DMD_LS0_CLK_N	6.5 (165.1)	See (3)	in (mm)
DMD_LS0_WDATA_P DMD_LS0_WDATA_N	6.5 (165.1)	See (3)	in (mm)
DMD_LS0_RDATA	6.5 (165.1)	See (3)	in (mm)
DMD_LS1_RDATA	6.5 (165.1)	See (3)	in (mm)
DMD_DEN_ARSTZ	N/A	N/A	in (mm)

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the ASIC IBIS models to ensure signal routing lengths do not exceed requirements.

Table 20. Max Pin-to-Pin PCB Interconnect Recommendations - TPS99000-Q1

ASIC INTERFACE	SIGNAL INTERCONNECT TOPOLOGY (1)(2)		UNIT
TPS99000-Q1	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
PMIC_LEDSEL(3)	6.0 (152.4)	See (3)	in (mm)
PMIC_LEDSEL(2)			
PMIC_LEDSEL(1)			
PMIC_LEDSEL(0)			
PMIC_ADC3_CLK			
PMIC_ADC3_MOSI			
PMIC_ADC3_MISO			
PMIC_SEQ_STRT			

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the ASIC IBIS models to ensure signal routing lengths do not exceed requirements.

Table 21. High-Speed PCB Signal Routing Matching Requirements

SIGNAL GROUP LENGTH MATCHING (1)(2)				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD (3)	DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N	DMD_HS0_CLK_P DMD_HS0_CLK_N	±1.0 (±25.4)	in (mm)
	DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N			
	DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N			
	DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N			
	DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N			
	DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N			
	DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N			
	DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N			
DMD (4)	DMD_HS0_x_P	DMD_HS0_x_N	±0.025 (±0.635)	in (mm)

(1) These routing requirements are specific to the PCB routing. Internal package routing mismatches in the DLPC230-Q1 and DMD have already been accounted for in these requirements.
(2) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(3) This is an inter-pair specification (that is, differential pair to differential pair within the group).
(4) This is an intra-pair specification (that is, length mismatch between P and N for the same pair).

Table 21. High-Speed PCB Signal Routing Matching Requirements (continued)

SIGNAL GROUP LENGTH MATCHING [1][2]				
INTERFACE	**SIGNAL GROUP**	**REFERENCE SIGNAL**	**MAX MISMATCH**	**UNIT**
DMD[3]	DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N	DMD_HS1_CLK_P DMD_HS1_CLK_N	±1.0 (±25.4)	in (mm)
	DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N			
	DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N			
	DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N			
	DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N			
	DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N			
	DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N			
	DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N			
DMD[4]	DMD_HS1_x_P	DMD_HS1_x_N	±0.025 (±0.635)	in (mm)
DMD[3]	DMD_LS0_WDATA_P DMD_LS0_WDATA_N	DMD_LS0_CLK_P DMD_LS0_CLK_N	±1.0 (±25.4)	in (mm)
DMD[4]	DMD_LS0_x_P	DMD_LS0_x_N	±0.025 (±0.635)	in (mm)
DMD	DMD_LS0_RDATA DMD_LS1_RDATA	N/A	N/A [5]	in (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	in (mm)
TPS99000-Q1	PMIC_LEDSEL(3)	PMIC_ADC3_CLK	±1.0 (±25.4)	in (mm)
	PMIC_LEDSEL(2)			
	PMIC_LEDSEL(1)			
	PMIC_LEDSEL(0)			
	PMIC_SEQ_STRT			
	PMIC_ADC3_MOSI			

(5) For legacy DMD support, the ASIC provides a single-ended low-speed write interface. The primary low-speed write control interface to the DMD is differential. The low-speed read control interface from the DMD is single-ended, and makes use of the differential write clock. As such, a routing mismatch between these is not applicable.

11.1.7 Number of Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.

11.1.8 Stubs

- Stubs should be avoided.

11.1.9 Terminations

- No external termination resistors are required on the DMD_HS or DMD_LS differential signals.
- The DMD_LS0_RDATA and DMD_LS1_RDATA single-ended signal paths should include a 10-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- DMD_DEN_ARSTZ does not typically require a series resistor, however, for a long trace, one might be needed to reduce undershoot/overshoot.

11.1.10 Routing Vias

- The number of vias on each DMD_HS and DMD_LS signal should be minimized and should not exceed two. If two are required, one should be placed at each end of the line (one at the ASIC and one at the DMD).

11.2 Thermal Considerations

The underlying thermal limitation for the DLPC230-Q1 is that the maximum operating junction temperature (T_J) not be exceeded (this is defined in the *Recommended Operating Conditions*). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC230-Q1, and power dissipation of surrounding components. The DLPC230-Q1's package is designed primarily to extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

TI highly recommends that once the host PCB is designed and built that the thermal performance be measured and validated.

To do this, measure the top center case temperature under the worse case product scenario (max power dissipation, max voltage, max ambient temperature) and validate that the maximum recommended case temperature (T_C) is not exceeded. This specification is based on the measured φ_{JT} for the DLPC230-Q1 package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. The bead and thermocouple wire should contact the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires should be routed closely along the package and the board surface to avoid cooling the bead through the wires.

12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

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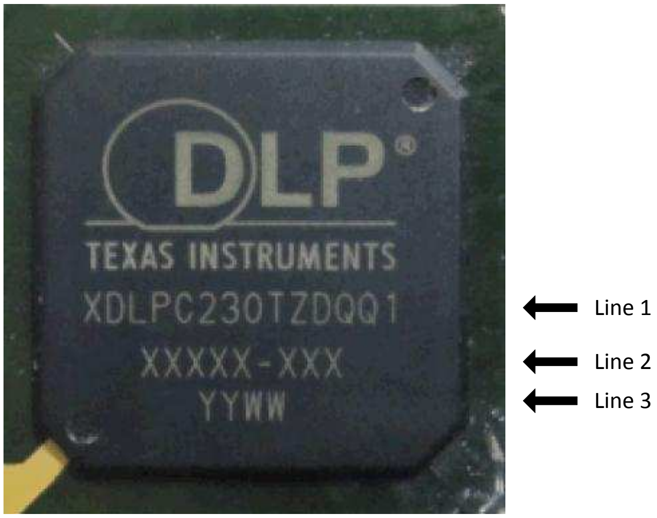
12.1.2 器件命名规则

12.1.2.1 器件标记


DLP
TEXAS INSTRUMENTS
XDLPC230TZDQQ1
XXXXX-XXX
YYWW
Line 1
Line 2
Line 3

标记定义：

第 1 行：	TI 器件型号：工程样片	X = 工程样片 DLPC230 = 器件 ID 空白或 A、B、C ... = 器件修订版本 T = 温度设计器 ZDQ = 封装符号 Q1 = 通过汽车认证
	TI 器件型号：生产	DLPC230 = 器件 ID 空白或 A、B、C ... = 器件修订版本 T = 温度设计器 ZDQ = 封装符号 Q1 = 通过汽车认证
第 2 行：	供应商批次和制造信息	XXXXX = 制造批次编号 -XX = 制造子批次 X（末尾的 X） = 组装子批次 制造编号为 UMC12A。同样，批次编号的首个字符为 K
第 3 行：	供应商年和周代码	YY = 年 WW = 周 示例：1614 - 器件于 2016 年第 14 周制造

12.1.2.2 视频时序参数定义

每帧有效扫描行数 (ALPF) 定义一帧中包含可显示数据的行数：ALPF 是每帧总行数 (TLPF) 的子集。

每行有效像素 (APPL) 定义包含可显示数据的一行中的像素时钟数：APPL 是每行总像素 (TPPL) 的子集。

器件支持 (接下页)

水平后沿 **(HBP)** 消隐 水平同步之后，第一个有效像素之前的消隐像素时钟数量。注意：HBP 时间参考各自同步信号的前缘（有效）边沿。

水平前沿 **(HFP)** 消隐 最后一个有效时钟之后，水平同步之前的消隐像素时钟的数量。

水平同步 **(HS)** 定义水平间隔（行）开始的时序基准点。绝对基准点由 HS 信号的有效边沿定义。有效边沿（源定义的上升沿或下降沿）是测量所有水平消隐参数的基准。

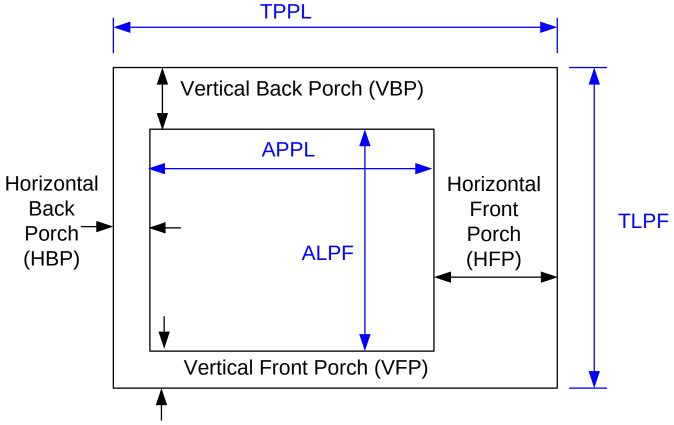
每帧总行数 **(TLPF)** 以行数定义垂直扫描时间（帧时间）：TLPF = 每帧总行数（有效和无效行）。

每行总像素 **(TPPL)** 以像素时钟数定义水平行扫描时间：TPPL = 每行总像素时钟数（有效和无效像素时钟）

垂直同步 **(VS)** 定义垂直间隔（帧）开始的时序基准点。这个绝对基准点由 VS 信号的有效边沿定义。有效边沿（源定义的上升沿或下降沿）是测量所有垂直消隐参数的基准。

垂直后沿 **(VBP)** 消隐 垂直同步后，第一个有效行之前的消隐行的数量。

垂直前沿 **(VFP)** 消隐 在最后一个有效行后，垂直同步前的消隐行数。


TPPL
Vertical Back Porch (VBP)
APPL
Horizontal Back Porch (HBP)
ALPF
Horizontal Front Porch (HFP)
TLPF
Vertical Front Porch (VFP)

12.2 商标

DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 术语表

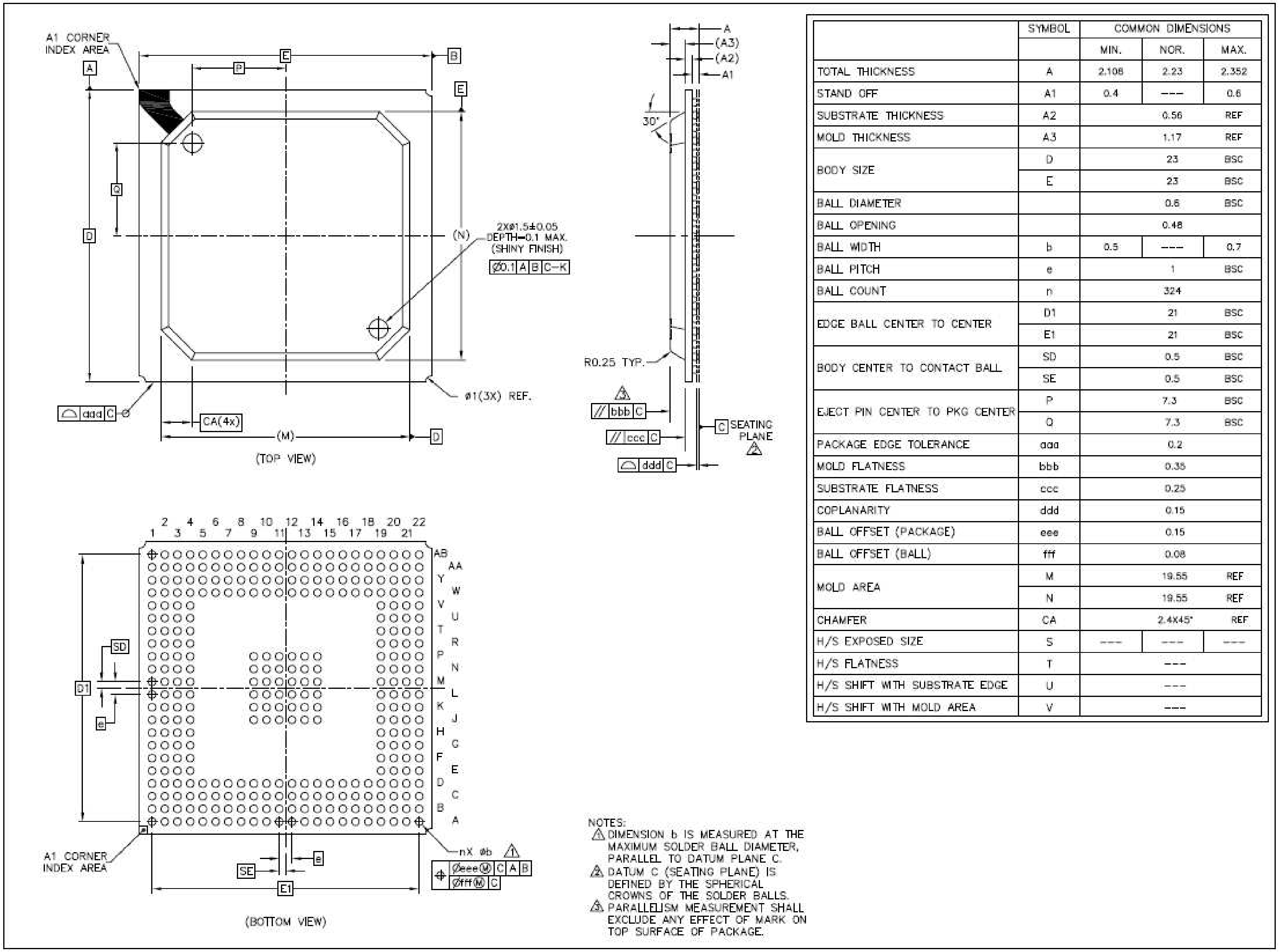
SLYZ022 — *TI* 术语表。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

13.1 DLPC230-Q1 机械数据


A1 CORNER INDEX AREA
A
E
B
P
Q
D
(N)
2XØ1.5±0.05
DEPTH=0.1 MAX.
(SHINY FINISH)
Ø0.1 A B C–K
aaa C
CA(4x)
(M)
Ø1(3X) REF.
(TOP VIEW)
A
(A3)
(A2)
A1
30°
R0.25 TYP.
bbb C
ccc C
ddd C
C SEATING PLANE
2 4 6 8 10 12 14 16 18 20 22
1 3 5 7 9 11 13 15 17 19 21
AB AA Y W V U T R P N M L K J H G F E D C B A
SD
D1
e
SE
E1
nX Øb
Øeee M C A B
Øfff M C
(BOTTOM VIEW)

	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	2.108	2.23	2.352
STAND OFF	A1	0.4	---	0.6
SUBSTRATE THICKNESS	A2		0.56	REF
MOLD THICKNESS	A3		1.17	REF
BODY SIZE	D		23	BSC
	E		23	BSC
BALL DIAMETER			0.6	BSC
BALL OPENING			0.48	
BALL WIDTH	b	0.5	---	0.7
BALL PITCH	e		1	BSC
BALL COUNT	n		324	
EDGE BALL CENTER TO CENTER	D1		21	BSC
	E1		21	BSC
BODY CENTER TO CONTACT BALL	SD		0.5	BSC
	SE		0.5	BSC
EJECT PIN CENTER TO PKG CENTER	P		7.3	BSC
	Q		7.3	BSC
PACKAGE EDGE TOLERANCE	aaa		0.2	
MOLD FLATNESS	bbb		0.35	
SUBSTRATE FLATNESS	ccc		0.25	
COPLANARITY	ddd		0.15	
BALL OFFSET (PACKAGE)	eee		0.15	
BALL OFFSET (BALL)	fff		0.08	
MOLD AREA	M		19.55	REF
	N		19.55	REF
CHAMFER	CA		2.4X45°	REF
H/S EXPOSED SIZE	S	---	---	---
H/S FLATNESS	T		---	
H/S SHIFT WITH SUBSTRATE EDGE	U		---	
H/S SHIFT WITH MOLD AREA	V		---	

NOTES:

1. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE C.
2. DATUM C (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

23mm × 23mm 封装 – 塑料球栅阵列

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC230TZDQQ1	ACTIVE	BGA	ZDQ	324	1	TBD	Call TI	Call TI	-40 to 105		Samples
DLPC230TZDQRQ1	ACTIVE	BGA	ZDQ	324	250	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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